INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

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D4.7 Report on EUROSOI+ Workshop held in Cork, 23-25 January, 2008

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PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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1. Introduction

SOI is no longer a promising technology. It is the necessary technology for the future of the microelectronics and for the smooth transition to the nanoelectronics. The incentive to foster the interactions among SOI material specialists, technologists, device experts, and circuit & system designers was supported by the Information Society of the European Union. As a result, EUROSOI'08 is the Fourth Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits. EUROSOI'08 takes place in Cork, Ireland from Wednesday January 23 to Friday January 25, 2008.

EUROSOI is designed as an international forum for promoting high-level scientific research and exchanges between research groups and industrial partners involved in SOI activities all over the world. Following the lively experience of the previous meetings (Granada, 2005, Grenoble, 2006 and Leuven, 2007), EUROSOI'08 features oral and poster sessions, key-note presentations, a training course as well as room for informal discussions. EUROSOI covers recent progress in SOI, including: (1) Synthesis of advanced SOI wafers (Ge, SiGe and strained layers, SOI heterostructures); (2) Materials evaluation, properties of ultra-thin films and buried oxides; (3) SOI MOSFETs: characterization, modeling and simulations, parameter extraction, reliability issues; (4) High performance CMOS and bipolar devices: low power/voltage and RF circuits, memories, sensors and MEMS; (5) Innovative devices: multiple-gates, tunneling transistors, etc.

A high number of papers have been submitted this year and 55 contributions have been selected for presentation. Many of them originate from strong national and international co-operations. Our special guests are Dr. Sergei Okhonin and Dr. Laurent Clavelier who kindly accepted to deliver outstanding key-note talks. In addition, 6 lectures by international experts are included in the Training Course. A Special Issue of Solid-State Electronics will contain selected full-length papers.

2.- Agenda

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4.- Selection of papers to be published in Solid State Electronics Journal

	Title	Author
1.	INVITED PAPER: Z-RAM Memory Technology	S Okhonin, Innovative Silicon
2.	INVITED PAPER: Review of Advanced Substrate trends	L. Clavelier, LETI
3.	Paper 7.1: Substrate bias effects on the performance of Schottky-barrier SOI nMOSFETs	Jong Tae Park, U Incheon
4.	Paper 2.4: Improved Source-Follower Buffer Implementation by Using Graded-Channel SOI nMOSFETs	M. de Souza, USP
5.	Paper 3.1: Electron Subband Structure and Controlled Valley Splitting in Silicon Thin Body SOI FETs: Two-Band k•p Theory and Beyond	V. Sverdlov, TU Wien
6.	Paper 3.3: Study of Ballisticity in SOI Nano-MOSFETs at Very Low Drain Bias	C. Sampedro, U Granada
7.	Paper 4.1: Silicon-on-SiC hybrid substrate with improved high-frequency and thermal performance	J. Olsson, Uppsala U
8.	Paper 4.2: High-Temperature RF Behavior of Partially-Depleted SOI MOSFET Transistors	M. Emam, UCL
9.	Doping Fluctuation Effects in Trigate SOI MOSFETs	R. Yan, Tyndall
10.	STI-Induced Mechanical Stress-Related Kink Effect of 40nm PD SOI NMOS Devices	J.-B. Kuo, Taipei
11.	Germanium on Sapphire By Wafer Bonding	P. Baine, Queen's U Belfast
12.	Equivalent Oxide Thickness of SOI-GAA devices	F.J. García Ruiz, U Granada
13.	On the switching speed of SOI LEDs	J. Schmitz, MESA, U Twente

14.	New Explicit Compact Charge and Capacitance Model for Undoped Ultra-Thin Body Silicon-on-Insulator (UTB-SOI) MOSFETs	O. Modovan, U Barcelona
15.	Paper 5.3: Evaluation of super-critical thickness strained-Si on insulator (sc-SSOI) substrate	T. Yoshida, Meiji U
16.	Paper 7.2: A Radiation Study of High-Resistivity SOI Substrates for High Energy Physics Applications	S. Ruddell, Queen's U Belfast
17.	Paper 7.4: How Crucial is Gate Misalignment for Low–Voltage Operation in Double Gate SOI MOSFETs?	A .Kranti, Queen's U Belfast
18.	Paper 8.3: Unusual Noise Behavior Versus Temperature in nFinFETs on Silicon on Insulator (SOI) Substrates Processed with Different Strain Techniques	W. Guo, U Caen
19.	Paper 8.4: Co-existence of two-dimensional electron and hole gases in thin double-gate SOI FETs	M. Prunnila, VTT
20.	Paper 2.1: Threshold Voltages of Double and Triple Gate SOI FinFETs	M. Caño de Andrade, USP
21.	Paper 2.3: Ultra-Low-Power Logic Style for Low-Frequency High-Temperature Applications	D. Bol, UCL
22.	Paper 7.3: Comparison Between Analog Performance of Standard and Strained Triple-Gate nFinFETs	M. A. Pavanello, Centro Universitário da FEI
23.	Paper 6.3: Temperature Behavior of Spiral Inductors on High Resistivity Substrate in SOI CMOS Technology	M. El Kaamouchi, UCL
24.	Paper 3.2: Estimations of the Ion-Ioff Performances of Nano nMOSFETs with Alternative Channels Materials	Q. Rafhay, IMEP-LAHC

5.- Minutes of the Management Board Meeting held in Cork, on January 23rd, 2008

EUROSOI Management Board Meeting held in Cork, on 23-01-2008

Attendees:
Prof. Sorin Cristoloveanu, IMEP, Grenoble
Prof. Jean Pierre-Colinge, Tyndall Institute, Cork
Prof. Cor Claeys, IMEC, Leuven
Prof. Denis Flandre, UCL, Louvain la Neuve
Prof. Olof Engstrom, Chalmers, Sweden
Dr. Olivier Faynot, LETI, CEA, Grenoble
Prof. Andrés Godoy, UGR, Granada
Prof. Francisco Gámiz, UGR, Granada (Co-ordinator)

The first management board meeting of EUROSOI+ project (FP7-ICT-2007-216373) was held in Cork, Ireland on January 23rd, 2008, with the following agenda:

1.- Welcome.
2.- Running Guidelines.
3.- Training activities.
4.- Scientific Exchange Program.
5.- Student Grants.
6.- Reports upgrading (SoA and Roadmap).
7.- Technological platform. Working plan.
8.- Questions and suggestions.

1.- Welcome.

Prof. Colinge, organizer and General Chairman of the 4th EUROSOI Workshop welcomed all the attendees for this first MB meeting.

2.- Running Guidelines.

Prof. Gámiz, EUROSOI Co-ordinator, thanked all the attendees for being present at this meeting and emphasized the importance of this new project. He summarized the objectives of the project, and highlighted the tasks which we will have to face along the following months. All the details and description about the work to carry out (DoW) can be found on the Annex I of the Grant

Agreement. This document (DoW) is available to all the contractors, and will be published on the Website (http://www.eurosoi.org) as soon as possible for the consultation of all EUROSOI partners. Prof. Gamiz also mentioned that he would introduce the main objectives, tasks and goals of the project to EUROSOI partners during the Banquet Dinner.

The first task to be organized is the 4th EUROSOI+ Workshop and a Training Course to be held at Cork. Prof. Colinge, Chairman of the Workshop and Leader of WorkPackage 3 (Training activities on Silicon on Insulator Technology) gave the details of the two events.

- With regard to the training event, Prof. Colinge mentioned that it was organized based on a book recently published by Springer and entitled "FinFETs and other multi-gate transistors", edited by Prof.Colinge (ISBN-978-0387-71751-7). The lectures were focused on each one of the chapters, and given by the corresponding authors. Thus, in addition to the viewgraphs of the lectures which were given to the participants before each lecture, the participants would have a reference text for further consultation.

- With regard to the Workshop, Prof. Colinge mentioned that there were 81 participants officially registered (46 at the short course) plus several Tyndall members who did not register. There were 21 students from EU and also participants coming from countries outside the EU such as Switzerland, Japan, South Korea, Taiwan, Brazil, Israel, Ukraine. There were 10 industrial participants (Analog Devices, SOITEC, INTEL, CISSOID, Innovative Silicon, EV group, ST, and Infineon). Regarding the communications we had 55 presentations (32 oral + 23 posters) and 2 invited presentations. As in previous Workshops, a selected number of communications will be published in an special issue of Solid-State Electronics Journal whose guest editors are Prof. Colinge and Prof. Lederer. In the DoW, it is mentioned that a person of each EUROSOI partner will have a reduction of 50% in the Workshop fee. As this workshop was organized before the signature of the contract with the Commission, all the attendees paid for the full fee. However, we agreed that this Workshop will be also supported by EUROSOI+ project. Prof. Colinge announced that after the Workshop he would contact the different partners who attended the Workshop for the reimbursement of half of the fee.

3.- Training activities

In addition to the aforementioned Training Event, we also discussed about other related tasks to carry out:

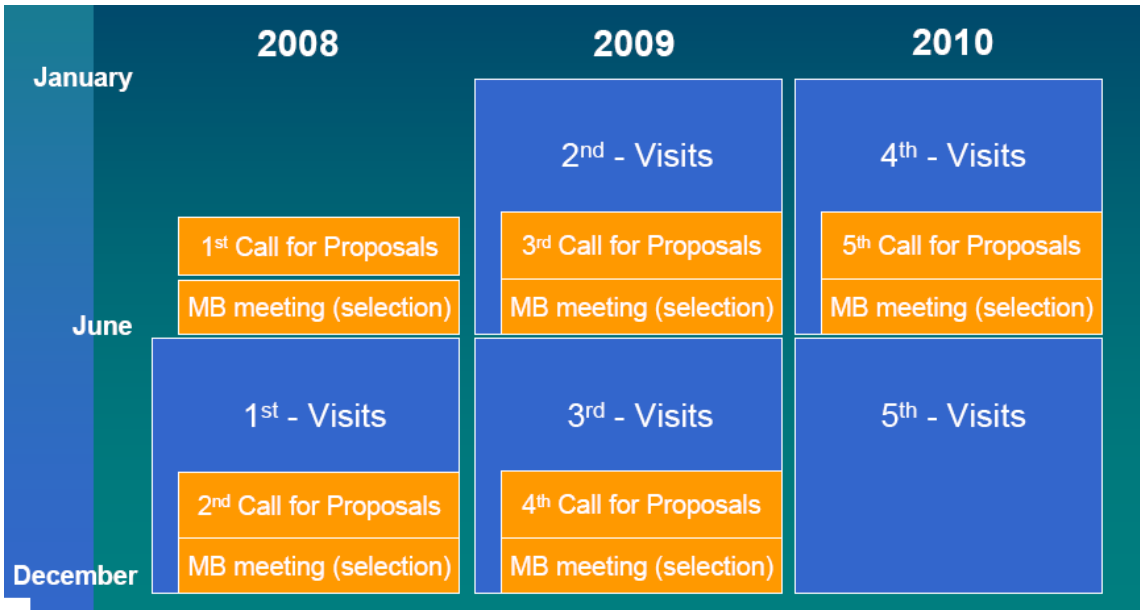
Task3.1. Elaboration of the EUROSOI+ Distinguished Lecturers list.
Prof. Claeys is the responsible for this deliverable (D3.1) to be finished in month 6 (M0+6).

Task3.2. Inventory of the SOI-related training material. Prof. Colinge in close collaboration with Prof. Godoy will design the strategy for the elaboration of this task.

4.- Scientific Exchange Program

We have budgeted 54 weeks (@1400€/week) for scientific visits between partners during the three years. We discussed and agreed the guidelines and application procedure according to the following points developed by Prof. Godoy:

1. Applicants should send a proposal including a short CV + comprehensive description of the visit (purpose, destination, duration, budget, etc) to the Coordinator before the following deadlines:



2. Selection of proposals will be made by the MB in the corresponding meeting of June or December/January. The selection will take into account the following points:

   a. The field should fall within research domains defined by EUROSOI+.
   b. At least one EUROSOI member should be involved in the project research.
   c. Priority will be given to industrial partners.
   d. The visit must be shorter than 4 weeks.
   e. Gender aspects will be considered (promote the participation of women).
   f. No salary costs or expenses generated by research activities will be covered.

3. After the visit (less than one month), the participant should provide a report describing the work developed during the visit.

5.- Student Grants

We have seven student grants (750€/each) to cover travel and registration fees of students who attend and present a paper in EUROSOI Workshops. One month before each Workshop, a call for applications will be launched. For Cork's Workshop, we will do it after the conference. All the students interested in applying for a Grant will submit to the coordinator a letter of support of his/her advisor before February, 15th. The MB will select seven applications among the ones received.

6.- Report Upgrading

Prof. Godoy, Leader of WP2 (Networking activities), reminded that according to our Plan of Activities, Upgraded versions of State-of-the-Art report and EUROSOI Roadmap should be delivered in month 18 (M0+18). In order to be successful it is necessary to start to work on these tasks as soon as possible. He will develop a specific plan of work in the following days. Different partners will be invited to participate in the process. Monothematic meetings are foreseen in the future.

7.- Technological platform

Dr. Olivier Faynot reported about the next steps in this WP5. As leader of WP5 Dr. Faynot will coordinate the characterization of LETI FDSOI devices which will be provided under request to the partners. He also mentioned the organization of specific monothematic working groups meetings to address this issue. The first one will be organized in month 9 (M0+9). FDSOI devices will be available for EUROSOI partners by March 08.
Dr. Olivier Faynot also reported on the organization of visits to different industrial companies to promote the use of FDSOI technology.

8.- Questions and suggestions.

Finally we discussed about the possibility of joint organization of the EUROSOI+ Workshop and IEEE International SOI conference, as it has been suggested by IEEE members. The idea is to reduce the number of international SOI conferences so that their topics will be more focused, more visible and more attended. The joint conference would be organized one year in the USA and, in the following year, in Europe. However the co-ordinator reported that until the end of this project, EUROSOI workshop is a deliverable of the project and therefore it is not possible to organize it outside Europe. However, this is in fact a very interesting proposal, and it means that we are on the right path.

Finally, since there are no more issues to deal with, the co-ordinator thanked the attendants for coming to this meeting, and reminded them that the next MB meeting will be held at UCL, Louvain-la-Neuve, Belgium, in June, 2008.

CONCLUSIONS

The fourth EUROSOI Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits was held in Cork (Ireland) on 23-25 January, 2008 and was focused on recent theoretical, experimental and industrial progress on SOI materials, devices, and circuits. The meeting was attended by more than 80 researchers from labs, universities and industries all over Europe. Fifty five (55) accepted contributions were presented and widely discussed, successfully covering SOI topics, such as: **i) *SOI Materials, Devices and Systems*; ii) *Modelling and characterization;* iii) *Simulation; and* iv) *SOI Circuits and Applications.***

This workshop became the appropriate forum to promote interaction and the exchange of information between research groups and industrial partners working in SOI. The main idea of the meeting was that each participant group should communicate their findings, opinions, experiences and conclusions about SOI questions. In this sense, the main workshop's goal is becoming a first step towards preparing future European task forces in SOI (RTD projects, collaborations, etc.)

We also wanted to have the point of view of different specialists coming from Industrial Centers. We had had two invited talks given by well-known experts in the field of SOI:

- Dr. Sergei Okhonin, Innovative Silicon, Switzerland, "ZRAM memory technology"
- Dr. Laurent Clavelier, CEA-LETI and SOITEC, France, "Review of advanced substrate trends"

We organized this rather informal and lively meeting, whose main objective was to discuss the situation of SOI technology in Europe. We had people from the EU, Switzerland, Japan, South Korea, Taiwan, Brazil, Israel, Ukraine. There were 21 students. There were 10 industrial participants from Analog Devices, SOITEC, INTEL, CISSOID, Innovative Silicon, EV group, ST, and Infineon.

We also organized a panel discussion chaired by Prof. Sorin Cristoloveanu from IMEP, Grenoble and composed by the following five experts:

1. Dr. Damien Bretegnier, SOITEC, France
2. Prof. Denis Flandre, UCL, Louvain-la-Neuve, Belgium
3. Dr. Sergei Okhonin, Innovative Silicon, Switzerland
4. Dr. Olivier Faynot, CEA-LETI, Grenoble France
5. Prof. Jean-Pierre Colinge, Tyndall, Cork, Ireland

Each expert presented his point of view and position on the SOI technology, future applications, and the European situation. After the initial positioning, there was a long live debate among the panellists and the rest of the audience and as a final consequence we can highlight the following three points:

1. There are plenty of “SOI species” which could be potential solutions for 22nm and below (*SOI Zoo and Botanic Garden*) but we need to designate an only SOI candidate among all of them. Otherwise it is impossible to advance our position much more from where we are now: we have excellent devices (LETI FDSOI, IMEC FinFETs, but very few circuit applications).
2. It is becoming urgent to involve/convince design people in next future to work using this only device
3. The announcement of SOITEC about a strong reduction of SOI wafer price and according to SOITEC mainly focused on communication applications: “rather cheap mobile telephone with SOI inside”.

Once more, the main conclusion we can draw from this workshop is the importance that the achievement of EUROSOI+ goals will have for the European Semiconductor Industry. In this respect it was highlighted the lack of prototyping capability in SOI in EUROPE, in spite of the fact that European companies have developed the most advanced SOI devices which are not accessible to many fabless companies or research groups whose designs would be much more competitive.

The final outcome of this meeting is a consequence of the quality of the contributions and the spirit of friendly cooperation shown by all the contributors. We wish to thank all of them for their effort. We would also like to thank all the people who enabled this meeting to take place, in particular Prof. J.P. Colinge, and Tyndall for its support.

A selection of the contributions presented at the Workshop will be published in a special issue of Solid State Electronics Journal devoted to the Fourth Workshop of the Thematic Network of Silicon on Insulator Technology, Devices and Circuits.

EUROSOI 2008

Fourth Workshop of the Thematic Network on
Silicon-On-Insulator
Technology, Devices and Circuits

CONFERENCE PROCEEDINGS

23-25 January 2008
Cork, Ireland

EUROSOI is organized by

Tyndall

Tyndall National Institute

and sponsored by

EUROSOI

Thematic Network on Silicon-On-Insulator Technology, Devices and Circuits

CISSOID

Harsh Environment Electronics Solutions

Welcome – *Fáilte*

SOI holds now a 35% market share of the logic integrated circuit industry. SOI is mainly used for microprocessor, gaming and mobile applications, but SOI has also deeply penetrated other markets, such as memory, power and high-temperature electronics. Multi-core microprocessors built on a 45nm silicon-on-insulator copper process are now an industrial reality and SOI has earned its place on the ITRS roadmap.

The EUROSOI initiative was set up in order to foster strong interactions among SOI material specialists, device experts, and circuit & system designers. The initial EUROSOI Thematic Network, involving 29 partners from 14 countries and supported by the Information Society of the European Union, came to a completion in 2006. The Network was re-conducted in 2008 under the name EUROSOI+.

After the success of the three first EUROSOI Workshops in Granada (2005), Grenoble (2006) and Leuven (2007), it was decided to organize a fourth edition in Cork in 2008.

This year's workshop features a Short Course on Multi-Gate SOI Technology. The importance of Multi-Gate devices is now fully recognized by the ITRS roadmap. The Short Course lectures are given by world-leading experts and focus on the opportunities offered by Multi-Gate FETs and on the challenges they pose in the field of fabrication, device physics and circuit design.

One of the most recent successful offspring of SOI technology is the single-transistor, zero-capacitor memory cell. It was named the number one winning technology by *IEEE Spectrum* Magazine readers in April 2007. EUROSOI has invited Dr. Serguei Okhonin of Innovative Silicon Inc. to present the latest in zero-capacitor SOI memory technology.

Heterogeneous integration techniques require innovations in the field of substrate engineering. Dr. Laurent Clavelier of CEA/LETI has accepted an invitation from EUROSOI to share with us the most recent results in advanced substrate synthesis techniques.

I want to thank all the authors for their contribution and the members of the Steering and Organizing Committees for their help putting together the Workshop. Welcoming the participants coming from all four corners of our little planet, I am looking forward to an exciting conference in the charming city of Cork.

Jean-Pierre Colinge
EUROSOI 2008 Chair

Organizing Committee

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Workshop Program

Wednesday, January 23: Training Course

Conference welcome reception

Thursday, January 24: Technical Program

Session 1: **SOI Memory Devices**

Chair: D. Flandre

Session 2: **Device Modelling and SOI Circuits**

Chair: P. Delatte

Session 3: **Quantum Device Modelling**

Chair: S. Cristoloveanu

Session 4: **Active RF devices**

Chair: D. Lederer

Poster Session

Conference Dinner

Friday, January 25: Technical Program

Session 5: **SOI Material Characterization**

Chair: C. Claeys

Session 6: **Passive RF devices**

Chair: J.-P. Raskin

Discussion panel

Session 7: **SOI Device Physics and Characterization I**

Chair: F. Gámiz

Session 8: **SOI Device Physics and Characterization II**

Chair: J. Alderman

Short Course on Multi-Gate SOI MOSFETs

Wednesday, January 23, 2008

08:30	*REGISTRATION*	
09:15	**Welcome Address**	D. Lederer
09:30	**The SOI MOSFET: from Single Gate to Multi-Gate**	J.-P. Colinge
10:10	*COFFEE BREAK*	
10:30	**Multi-Gate MOSFET Technology**	M. Jurczak
11:20	**Physics of the Multi-Gate MOS System**	B. Majkusiak
12:10	*LUNCH*	
14:00	**Mobility in Multi-Gate MOSFETs**	F. Gámiz
14:50	**Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs**	V. Ferlet-Cavrois
15:40	*COFFEE BREAK*	
16:00-16:50	**Multi-Gate MOSFET Circuit Design**	G. Knoblinger
19:00-21:00	*CONFERENCE WELCOME RECEPTION*	

Technical Program Schedule

Thursday, January 24, 2008

08:30 ***REGISTRATION***

09:00 ***OPENING ADDRESS***
R. Whatmore and J.-P. Colinge, Tyndall National Institute, Cork, Ireland

Session 1. SOI Memory Devices
Chair: D. Flandre, DICE, UCL, Belgium

09:10 **Z-RAM Memory Technology, *Invited*** 19
S. Okhonin, M. Nagoga
Innovative Silicon

09:40 **Influence of Gate-Underlap Design on the Performance of 6T-SRAM Cell with Double Gate SOI MOSFETs** 23
Rashmi, A. Kranti and G.A. Armstrong
NISRC, Queen's University Belfast, UK

10:00 **An In-Depth Study of SRAM Cells in Double-Gate CMOS with Statistical Variation** 25
B. Giraud, A. Vladimirescu and A. Amara
ISEP, Paris, France

10:20 ***COFFEE BREAK***

Session 2. Device Modelling and SOI Circuits
Chair: P. Delatte, CISSOID, Louvain-la-Neuve, Belgium

10:40 **Threshold Voltages of Double and Triple Gate SOI FinFETs** 29
M. G. Caño de Andrade[1] and J. A. Martino[2]
[1]Centro Universitário da FEI, São Bernardo do Campo, Brazil
[2]LSI / PSI / USP, University of São Paulo, São Paulo, Brazil

11:00 **Comparative Analysis of Self-Heating in Different SOI Architectures** 31
M. Braccioli, C. Fiegna and E. Sangiorgi
ARCES-DEIS, University of Bologna, Cesena, Italy

11:20 **Ultra-Low-Power Logic Style for Low-Frequency High-Temperature Applications** 33
D. Bol, D. Flandre and J.-D. Legat
DICE, UCL, Louvain-la-Neuve, BELGIUM

11:40 **Improved Source-Follower Buffer Implementation by Using Graded-Channel SOI nMOSFETs** 35
M. de Souza[1], D. Flandre[2] and M. A. Pavanello[1,3]
[1]LSI/PSI/USP, University of São Paulo, São Paulo, Brazil
[2]DICE, UCL, Louvain-la-Neuve, Belgium
[3]Centro Universitário da FEI, São Bernardo do Campo, Brazil

12:00 **Introduction of Diamond into Advanced FDSOI CMOS** 37
J.-P. Mazellier [1,2], O. Faynot [1], F. Andrieu [1], S. Cristoloveanu [2] and S. Deleonibus [1]
[1] CEA LETI - MINATEC, Grenoble, France
[2] IMEP-INP, MINATEC, Grenoble, France

12:20 ***LUNCH***

Session 3. Quantum Device Modelling

Chair: S. Cristoloveanu, IMEP, Grenoble, France

15:20 ***COFFEE BREAK***

Session 4. Active RF Devices

Chair : D. Lederer, Tyndall National Institute, Cork, Ireland

17:00-19:00	***Poster Session (Ctd)*** *Chair: R. Duane, Tyndall National Institute, Cork, Ireland*	
P22	**New Explicit Compact Charge and Capacitance Model for Undoped Ultra-Thin Body Silicon-on-Insulator (UTB-SOI) MOSFETs** *O. Moldovan[1], F. A. Chaves[2], D. Jiménez[2] and B. Iñiguez[1]* *[1] Dpt d' Eng. Electrònica,Elèctrica i Automàtica, Universitat Rovira i Virgili, Tarragona,Spain* *[2] Dpt d' Eng. Electrònica, Escola Tècnica Superior d' Enginyeria, Universitat Autònoma de Barcelona, Barcelona, Spain*	103
P23	**Ballistic Transport and RF Noise in Ultra-Scaled SOI MOSFETs: a Monte Carlo Study** *M. J. Martín, E. Pascual, T. González and R. Rengel* *Departamento de Física Aplicada, Universidad de Salamanca, Spain*	105

19:30 ***Conference Dinner***

Banquet Speaker: F. Gámiz, Universidad de Granada, Granada, Spain

Technical Program Schedule

Friday, January 25, 2008

Session 5. SOI Material characterization
Chair: C. Claeys, IMEC, Leuven, Belgium

09:00	**Review of Advanced Substrates Trends, *Invited*** *L. Clavelier[1], C Deguet[1], F. Andrieu[1], C. Le Royer[1], Y. Letiec[1], M. Kostrzewa[1], J.P. Mazellier[1], A. Tauzin[1], J.S. Moulet[2], F. Fournel[1], O. Faynot[1], F. Letertre[2], I. Cayrefourcq[2], B. Ghyselen[2], C. Mazure[2]* *[1]CEA-LETI MINATEC, Grenoble, France* *[2]SOITEC, Bernin, FRANCE*	109
09:30	**On the Extraction of Dopant Activation Level for Boron-Doped Thin Germanium-On-Insulator (GeOI)** *L. Hutin, S. Koffel, C. Le Royer, L. Clavelier, P. Scheiblin, V. Mazzocchi and S. Deleonibus* *CEA/LETI MINATEC, Grenoble, France*	111
09:50	**Hydrogen as Source of High-Temperature Charge Instability in the Buried Oxide of SOI Structures and MOSFETs** *A. Nazarov[1], V. Lysenko[1], J.P.Colinge[2] and D. Flandre[3]* *[1] Lashkaryov Institute of Semiconductor Physics, NASU, Kyiv, Ukraine* *[2] Tyndall National Institute, Cork, Ireland* *[3] DICE, UCL, Louvain-la-Neuve, Belgium*	113
10:10	**Evaluation of Super-Critical Thickness Strained-Si On Insulator (sc-SSOI) Substrate** *T. Yoshida[1], D. Kosemura[1], Y. Kakemura[1], M. Takei[1], H. Saito[1], A. Ogura[1], T. Shimura[2], T. Koganesawa[3] and I. Hirosawa[3]* *[1] School of Science and Technology, Meiji University Kawasaki, Kanagawa, Japan* *[2] Graduate School of Engineering, Osaka University, Suita, Osaka, Japan* *[3] Japan Synchrotron Radiation Research Institute, Sayo-cho, Sayo-gun, Hyogo, Japan*	115

10:30 ***COFFEE BREAK***

Session 6. Passive RF Devices
Chair: J.-P. Raskin, EMIC, UCL, Louvain-la-Neuve, Belgium

10:50	**High-Performance Thick Copper Inductors Integrated in Advanced High Resistivity SOI RF CMOS technology** *C. Pastore[1,2], F. Gianesello[1], D. Gloria[1], E. Serret[1], B. Rauber[1] and Ph. Benech[2]* *[1] STMicroelectronics, FTM, Crolles, France* *[2] IMEP, Grenoble, France*	119
11:10	**Temperature and Bias Dependent Performance of Coplanar Waveguide on High Resistivity Silicon Substrate with Passivation Layer** *C. Roda Neve[1], D. Lederer[2] and J.-P. Raskin[1]* *[1] EMIC, UCL, Louvain-la-Neuve, Belgium* *[2] Tyndall National Institute, Lee Maltings, Prospect Row, Cork, Ireland*	121
11:30	**Temperature Behavior of Spiral Inductors on High Resistivity Substrate in SOI CMOS Technology** *M. El Kaamouchi, M. Si Moussa, J.-P. Raskin and D. Vanhoenacker-Janvier* *EMIC, UCL,Louvain-la-Neuve, Belgium*	123

11:50 ***Discussion Panel***
Chair: S. Cristoloveanu, IMEP, Grenoble, France

13:00 ***LUNCH***

Session 7. SOI Device Physics and Characterization I

Chair: F. Gámiz, Universidad de Granada, Spain

15:40 ***COFFEE BREAK***

Session 8. SOI Device Physics and Characterization II

Chair: J. Alderman, Tyndall National Institute, Cork, Ireland

17:40 **Concluding remarks**

J.-P. Colinge, Tyndall National Institute, Cork, Ireland

SESSION 1

SOI Memory Devices

CHAIR
D. Flandre
Université catholique de Louvain

Z-RAM memory technology

S. Okhonin, M. Nagoga

Innovative Silicon, PSE-B, Lausanne, Switzerland
Phone: +41-21-693-8992, Fax: +41-21-693-8990, Email: sokhonin@z-ram.com

1. Abstract

The current status of the single transistor DRAM (Z-RAM) technology is reviewed and the new generation of Z-RAM is described. The new memory is largely based on the bipolar transistor existing in the MOS structure. The memory's main features are high margin, low-power consumption, and scalability.

2. Introduction

Recently introduced Z-RAM memory [1, 2] uses a single transistor (1T) and no capacitor bitcell (hence the "Z" for Zero capacitor RAM), unlike traditional one transistor plus one capacitor (1T/1C) DRAM bitcells. Z-RAM uses a standard SOI logic process - there are no additional processing steps for capacitor fabrication. It offers the simplicity of a single transistor design, and the 'tune-ability' for speed, low-power, or high-density (cost sensitive) applications.

Parameter	Z-RAM	DRAM
Cell Size	Smaller Cell	Larger Cell
Device	Single Transistor	Capacitor Structure
Mfg Process	Minor Changes to SOI Process	Capacitor Structure
Performance	Faster, More Options	Slower, Fewer Options
Power	Equivalent (Depends on Speed-Performance Tuning)	Equivalent

Table. 1 *Z-RAM – DRAM comparison*

Table 1 compares Z-RAM and DRAM. Figure 1 shows a Z-RAM cell in array environment. In this paper we will review the current status of Z-RAM. We will also describe new generation of Z-RAM.

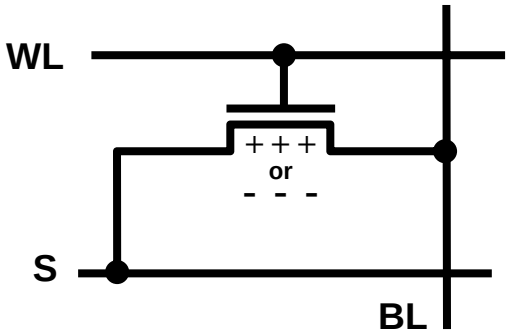

Fig. 1 *Z-RAM cell in array environment*

3. Principle of operation

Figure 2 shows a Z-RAM memory cell. The transistor's Floating Body (FB) acts as a storage node.

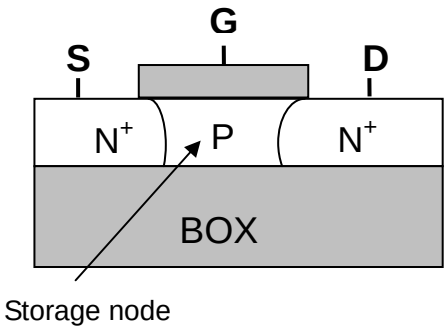

Fig. 2 *Z-RAM memory cell*

The first generation Z-RAM (Gen1) uses the channel impact ionization to create an excess of majority carriers in the FB. The FB charge induces a MOS transistor threshold voltage shift and changes the MOS transistor current (Figure 3).

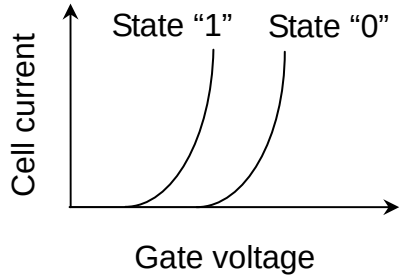

Fig. 3 *I-Vg curves for states “1” and “0” in Gen1 Z-RAM*

While Gen1 Z-RAM uses the MOS transistor, the new Gen2 Z-RAM is largely based on the Bipolar Transistor (BP) present in the MOS structure (Figure 4).

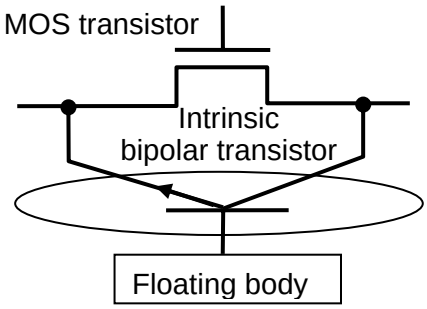

Fig. 4 *Intrinsic bipolar transistor*

In case of an n-channel device the N^+ source, the P-type body and the N^+ drain form the emitter, the base and the collector of an NPN bipolar transistor [3]. In a FB SOI device the body (i.e. the base of the bipolar transistor) is used as a storage node. To write “1”, i.e. to create an excess of majority carriers in the FB, impact ionization is used. These majority carriers are generated by the bipolar transistor current (Figure 5).

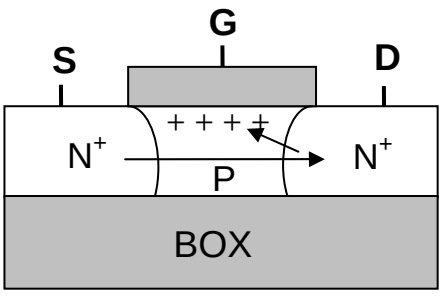

Fig. 5 *Writing “1” in Gen2 Z-RAM*

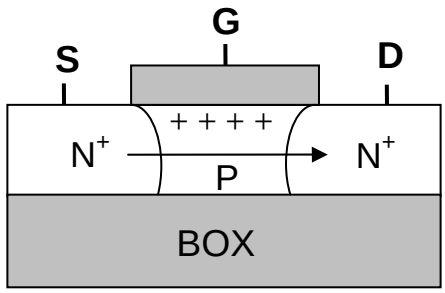

Fig. 6 *Reading “1” in Gen2 Z-RAM*

Reading is performed by sensing the bipolar current in contrast to the Gen1 Z-RAM, where the channel current is used (Figure 6). During read, the bipolar transistor is “on” when the cell state is “1” and it is “off” when the cell state is “0”.

Typically the write “1” current is kept at the same level as the read “1” current and write “0” and read “0” currents are very small (Figure 7).

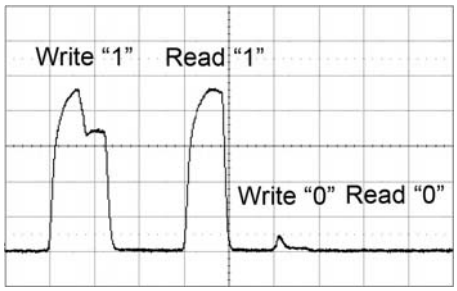

Fig. 7 *Gen2 Z-RAM cell current during operation*

Multiple read operations can be sustained without losing the bitcell data state as shown in Figure 8.

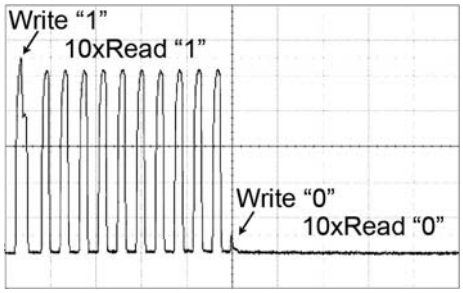

Fig. 8 *Multiple reading in Gen2*

Gen2 Z-RAM naturally provides high margins in comparison to Gen1 (Figure 9). It also improves cell retention time.

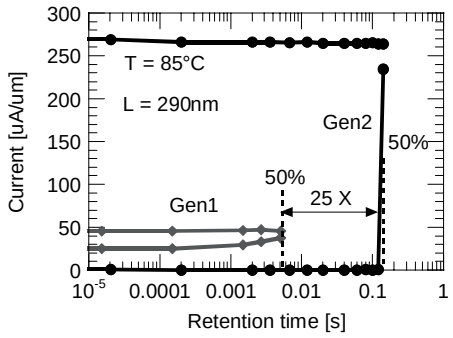

Fig. 9 *Gen1 vs. Gen2 Z-RAM retention and programming window measured on the same transistor*

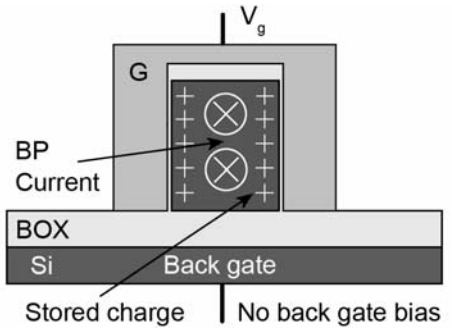

Fig. 14 *Gen2 FinFET cross-section*

To prove the Gen2 concept we successfully built an array using a standard 90nm SOI process. Array data show that Gen2 access time can be as fast as 2ns.

4. Scalability

An important advantage of this innovation is that it expands the Z-RAM applicability to a number of advanced non-planar devices such as FinFET (Figure 12), multi-gate FET, gate-all-around FET, etc [4].

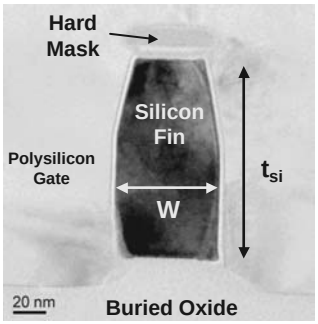

Fig. 12 *Cross-section of the FinFET build by ATDF used in the measurements*

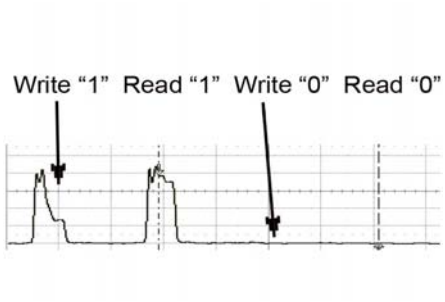

Fig. 13 *FinFET Gen2 cell current during operation*

Figures 12 and 13 show the cross-section of the device used and the current during operation.

Figure 14 shows operational principles of FinFET based Gen2 Z-RAM.

The charge is accumulated under the transistor's gates and the current flows in the middle of fin.

Thus the stored charge provides good control of the bipolar current (Figure 14) in contrast to Gen1 where the charge is stored in the area close to the buried oxide.

In addition Gen2 Z-RAM does not require any back gate bias.

In spite of the small transistor size, state "1" reading current close to 15 µA/fin and programming window of 1V were measured. Even one fin can provide enough current for reliable and fast bitcell state sensing. It opens possibilities of creating very dense memory arrays with one fin per a bit cell.

5. Conclusions

We reviewed the current status of Z-RAM memory. We also presented a new generation of Z-RAM and explained its basic operational principles. New Z-RAM is extremely well scalable and naturally works on different types of advanced devices.

References

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Influence of Gate-Underlap Design on the Performance of 6T-SRAM Cell with Double Gate SOI MOSFETs

Rashmi, A. Kranti and G.A. Armstrong

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1. Abstract

The impact of gate-underlap design on the performance of 6T-SRAM cell, based on 22 nm Double-Gate (DG) SOI MOSFETs, operated at 0.6 V has been analyzed. Optimal design parameters with underlap architecture and trade-offs associated with read/write/standby operations are evaluated for two different configurations of 6T-SRAM cell. Results show that an appropriate spacer-to-straggle ratio in range 2 to 3 can be chosen to match the SOI layer thickness to balance conflicting read/write performance requirements.

2. Introduction

Double-Gate (DG) SOI MOSFETs are promising devices for design of CMOS SRAM cells as they allow excellent channel control and minimize short-channel effects (SCEs) [1]. The use of gate-underlap architecture and high-κ dielectric can further improve device/circuit performance [2]. In the present work, we investigate the impact of underlap design on performance of 6-T SRAM cell realized with undoped, high-κ gate dielectric DG SOI MOSFETs. A variation of SRAM circuit (BG circuit), wherein the two n-type access and the two p-type pull-up transistors operate in back gate (BG) mode [3], is analyzed in addition to the conventional design [4]. BG operation offers dynamic performance tenability which can be utilized to improve trade-offs in SRAM design [5]. The gate-underlap design has been optimized to enhance the read/write performance of the SRAM, evaluated in terms of Static Noise Margin (*SNM*), write-current (I_{wr}) and leakage current (I_{leak}).

3. Results and Discussion

Fig. 1(a) shows the DG MOSFET simulated using ATLAS simulator [6] with high-κ gate dielectric (ε_{hk}) of $15\varepsilon_o$ (ε_o being the permittivity of free space). A mid-gap work-function was used for all transistors. The silicon film thickness, T_{si} was varied from 8.8 nm ($0.4L_g$) to 17.6 nm ($0.8L_g$). The underlap region profile (fig. 1(b)) was modeled as $N_{SD}(x) = (N_{SD})_{peak} \exp(-x^2/\sigma^2)$ [7-9], where spacer width, s was varied from 6 to 60 nm, doping gradient, d is in range 3-5 nm/dec and lateral straggle, σ lies between 5 and 12.5 nm. Fig. 2(a) shows the schematic of the 6-T SRAM cell (BG circuit) employing dynamic feedback on access transistors as well as write-gating of pull-up transistors [3]. The solid lines represent the conventional SRAM cell with modifications for BG circuit marked in dotted lines. The butterfly curves for the two circuit topologies are shown in Fig. 2(b) for comparison.

Fig. 3 shows threshold voltage (V_{th}) dependence on spacer-to-straggle ratio (s/σ), a key design parameter introduced for analog/rf applications [10], for n-MOS DG device. The effective channel length, L_{eff} in weak inversion can be modeled as $L_{eff} = L_g + 2\sigma\left((s/\sigma)-\alpha_{SD}\right)$ for underlap devices, where typical values of α_{SD} $\left(=\sqrt{ln(N_{SD})_{peak}/\xi_{SD}};\ (N_{SD})_{peak}\right.$ is peak source/drain (S/D) doping concentration and ξ_{SD} is S/D doping level at $\left.L_{eff}\right)$ lie in the range 1.5-2.0 for σ values of 5-12.5 nm [2]. An increase in s/σ increases L_{eff} and minimizes SCEs, thus improving gate controllability that translates into an improved SRAM performance. Higher V_{th} results in higher read margin and reduced S/D leakage due to lower off-current [11-13].

Fig. 4(a) shows significant enhancement of *SNM* for BG circuit compared to conventional, irrespective of the choice of d, s/σ and T_{si}/L_g. The *SNM* of BG circuit is virtually double that of conventional circuit and shows a particularly strong rise for thicker silicon up to $s/\sigma = 3$. The optimal range of s/σ would be 2-3 (SNM_{BG} ~200 mV and $SNM_{Conventional}$ ~75 mV), beyond which *SNM* shows no appreciable change. The variation of the ratio of write-current to leakage current with s/σ is shown in Fig. 4(b), for the two SRAM topologies. I_{wr} and I_{leak} both decrease with increase in s/σ, however the ratio shows an impressive value of ~10^5 for thicker silicon at $s/\sigma = 2.3$ for T_{si} of 0.6 L_g. In general if s/σ lies between 2 and 3, I_{wr}/I_{leak} lies in the acceptable range of 10^4-10^7, which corresponds to a maximum I_{leak} of 1 nA and a minimum I_{wr} of 5 μA. The write-current of BG circuit is nearly an order of magnitude lower than for conventional design, whereas I_{leak} is unchanged. Please note however that devices analyzed here show good write-margin of ~ 275 mV (not illustrated here). I_{wr} represents the write-ability of the SRAM cell [3], where I_{wr} (the minimum current during a write cycle) is inversely proportional to write access time. The three performance metrics investigated here – *SNM*, I_{wr} and I_{leak}, need to be balanced. Any factor improving the noise margin of SRAM cell reduces I_{leak}, but also degrades I_{wr}. Using s/σ values in the range of 2-3 for

BG configuration of 6-T SRAM cell seems to provide the best trade-off. Table 1 points out the advantage of using underlap architecture over non-underlap (abrupt S/D doping) design which results in enormous leakage currents for a marginal increase in I_{wr}.

Figs. 5(a)-(c) show the dependence of *SNM*, I_{wr} and I_{leak} on T_{si} for various values of spacer width, for BG 6-T SRAM cell. I_{wr} and I_{leak} increase with increase in T_{si} and decrease in *s*, whereas *SNM* shows the opposite trend. Results show that if T_{si} is varied over the range 11 to 18 nm, a constant *SNM* ~166 mV can be maintained by suitable adjustment of spacer width, without significantly compromising I_{wr} (~10 μA) or I_{leak} (~0.1 nA). By using cell and beta ratios of unity, layout area is minimized, and the proposed 6-T SRAM cell yields promising performance at low V_{dd}, because of high V_{th} and suppressed SCEs offered by gate-underlap architecture in high-κ DG SOI MOSFETs.

5. Conclusions

A 6-T SRAM cell designed with gate-underlap DG MOSFETs operating in back-gate mode at 0.6 V was analysed. Various design compromises using gate underlap with a spacer-to-straggle ratio in the range 2 to 3 illustrate the possible design trade-offs between *SNM*, write-ability and leakage.

Acknowledgement

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC), UK.

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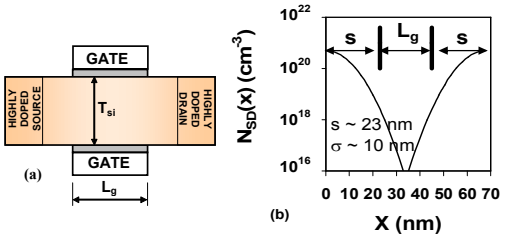

Fig. 1: *(a) Schematic diagram of gate-underlap DG SOI MOSFET. Gate length, L_g=22 nm, width=0.06 μm, T_{HK}=3.5 nm, supply voltage (V_{dd})=0.6 V. (b) Source/Drain doping profile along the channel of DG SOI MOSFET.*

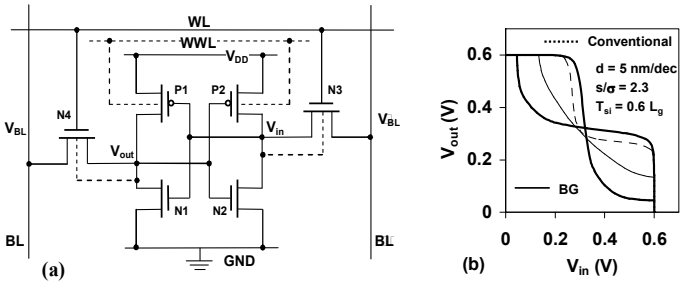

Fig. 2: *(a) Schematic diagram of a 6-T SRAM cell. Solid lines: Conventional circuit, Dotted lines: Back gating in BG circuit. (b) Butterfly curve for BG and conventional circuits at V_{dd}=0.6 V for Lg=22 nm.*

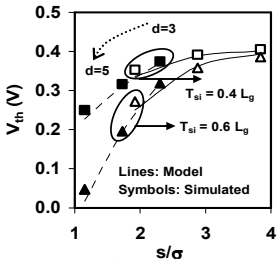

Fig. 3: *Threshold voltage of n-MOS DG device at V_{dd} = 0.6 V. Open symbols: d=3 nm/dec, Solid symbols: d=5 nm/dec. For each d, the lowest and highest V_{th} values correspond to σ of 5 and 10 nm respectively.*

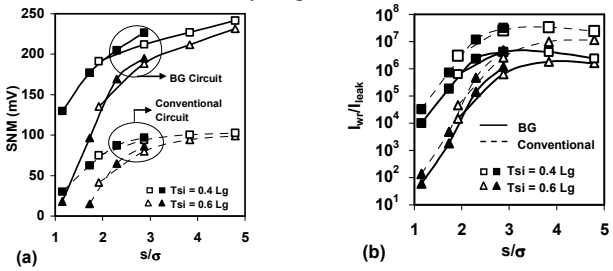

Fig. 4: *Variation of (a) SNM and (b) I_{wr}/I_{leak} of 6-T SRAM cell with s/σ ratio. Open symbols: d=3 nm/dec, Solid symbols: d=5 nm/dec. For each d, σ increases from 5 to 12.5 nm with increase in s/σ.*

SRAM Design				
	BG		Conventional	
	U	*NU*	*U*	*NU*
SNM (mV)	169	110	65	25
I_{wr} (μA)	10.3	14	35	52
I_{leak} (nA)	7.3×10^{-4}	6.1	7.3×10^{-4}	6.4

Table 1: *Comparison of performance metrics for 6-T SRAM cell. U: Underlap design, NU: Non-underlap design. V_{dd}=0.6 V, T_{si}=0.6 L_g d=5 nm/dec, s/σ=2.3 for σ=10 nm.*

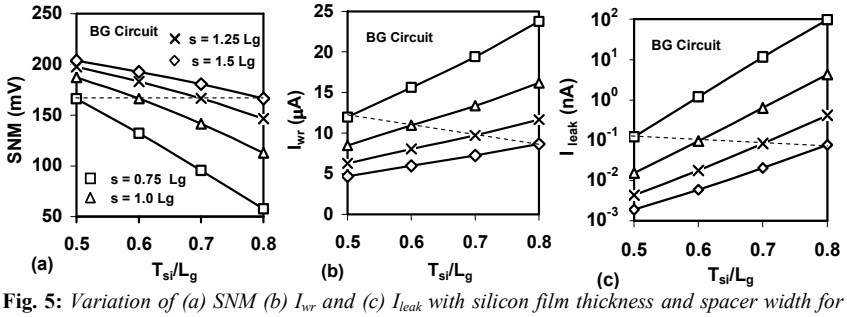

Fig. 5: *Variation of (a) SNM (b) I_{wr} and (c) I_{leak} with silicon film thickness and spacer width for BG configuration of 6-T SRAM cell with d=5 nm/dec. Dashed line represents devices that achieve SNM=166 mV.*

An In-Depth Study of SRAM Cells in Double-Gate CMOS with Statistical Variation

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1. Abstract

This paper presents a comparative study of sub-32 nm CMOS 6T and 4T SRAM cells in fully depleted (FD) double-gate (DG) silicon-on-insulator (SOI) technology with planar independent self-aligned gates. Both independent- and connected-gate operation is analyzed. An improved 4T driverless (DL) SRAM cell is proposed which takes advantage of the back gate to improve stability. Process variability is introduced and statistical characterization results are presented for all cells.

2. Introduction

The DG technology with reduced process variations and better control on leakage current has appeared as a candidate to compete with bulk-CMOS below 32nm. This paper provides an in-depth study of several SRAM cells in DG technology. In conventional transistors, the drain current is controlled by the 'single' gate voltage, whereas in DG structures two independent gates are available to adjust the drain current. This double controllability offers a new degree of freedom leading to novel architectures. 6T and 4T SRAM cell architectures are described in Sec. 4. This work focuses on 4T driverless (DL) cells and proposes a novel DG topology. The Double Gate technology and transistor are briefly described in Sec. 3. The cells are described in Sec. 4. Sec. 5 contains the results of the comparative study and the impact of process variation displayed by the relevant distributions obtained from Monte-Carlo simulations. Conclusions are drawn on design guidelines for robust operation.

3. Overview of the Double-Gate (DG) Transistor

Figure 1 illustrates the simulated drain current as a function of the front-gate voltage for the back gate connected either to 0, V_{DD} or the front gate, with V_{DD}=1.2V. The solid-line curves represent Ids-Vgs for a symmetric transistor with equal Tox. The two gates have exactly the same impact on the drain current. The dashed curves show Ids-Vgs for an asymmetric NMOS. The thickness of the front and back oxide have been set to Tox1=1nm and Tox2=4nm, respectively, resulting in a raised threshold voltage (V_T) for Tox2. As a result the ratio I_{ON}/I_{OFF} increases. When the front and the back gates are at '1' and '0', respectively, the drive current is more than 13 times higher than when the bias is reversed, front gate at '0' and the back gate at V_{DD}. This compares favourably to the symmetric transistor where the drive current is the same for both cases.

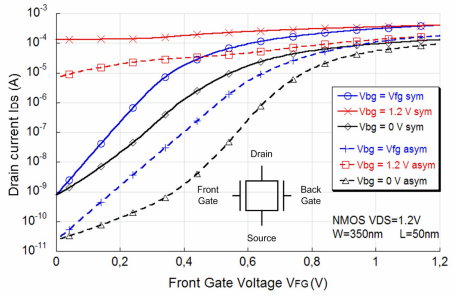

Fig.1: *I_{DS} vs. V_{FGS} for NMOS at VDS = 1.2V and DG NMOS symbol (inset)*

4. Memory Cell Presentation

The cells are generally classified according to the number of transistors. In this paper we consider the two most frequent cell types containing 6T and 4T.

The 6T cell shown in Fig. 2(a) is the most popular SRAM, generally developed in bulk technology. Stability has been our main focus when sizing the cell. This cell has been studied only in read mode since 6T cells present good retention. The method consists in determining the storage node, which presents the highest probability to flip first, in our case the F='0' node when read. The stability condition at this node is

$$I_{G-P} + I_{OFF-P} + I_{ON-A} \leq I_{ON-N} \qquad (1)$$

According to Eq. 1 and by neglecting I_{G-P} and I_{OFF-P}, the stability is proportional to $k_n=W_n/L_n$ and inversely proportional to $k_a=W_a/L_a$. To increase the stability while taking advantage of the second gate, the 6T Hitachi (Fig. 2(b)) was introduced in [1]. The load and access transistors have less influence than the driver as their back gates are connected to low and high potentials, respectively, and so Eq. (1) is better guaranteed.

New cells have been introduced in various technologies to increase the circuit density. Among them are the 4T cells, which can be classified in two types:

• the loadless: 4T LL in Fig. 3(a) inspired from 4T NEC in bulk CMOS and 4T Hitachi (Fig. 3(b)) [1],

• the driverless 4T DL: we propose a new architecture (Fig. 3(d)) inspired from (Fig. 3(c)).

In the 4T Hitachi and 4T DL FB cells, henceforth referred to as 4T FB, the back gates of access transistors are connected to the opposite storage nodes thus forming a feedback loop. In Fig. 3, the dashed arrows represent the currents relative to the critical node during retention and the solid ones during read operation. The cells are sized such that the product of the Static Noise Margins (SNM) in retention and read is maximized. The

stability for retention and read for DL cells is obtained by following the approach used to obtain Eq. (1):

$$I_{G-P} + I_{OFF-P} \leq I_{OFF-A} \quad (2)$$

$$I_{ON-A} \leq I_{G-P} + I_{ON-P} \quad (3)$$

When one gate of a symmetric transistor is at '0' and the other at '1', the resulting current is only 3 times lower than the I_{ONmax} (I_{ONmax} corresponds to the I_{ON} current when both gates are connected to '1'), as shown in Fig. 1. This may lead to loss of data when writing even if the cells are stable during read and retention. This problem affects the cells in Fig. 3(b) and Fig. 3(d) where the front and back-gate of access transistors are not connected. The front gates of access transistor have to impact the drive current much more than the back gates, by unbalancing the transistor as described in Sec. 3, by adjusting T_{ox} and V_T; this leads to a four times larger ratio than for the symmetric case.

5. Results and Discussions

Here are the key criteria for performance characterization, defined in [2]: stability, static power consumption, write-access time, write margin and disturb. TABLE I shows the results of simulations using a compact model. For these measurements the 6T cells have been sized such that the SNM is maximized and the WM is below 1V. The 6T Hitachi displays a read SNM increased by 100mV but a WM degraded by 3X compared to the conventional 6T. The 4T FB cells show improved stability. However, compared to the 4T LL FB, the 4T DL FB displays better characteristics except for a slightly lower read SNM; our 4T DL cell displays read/retention SNM greater than 350 mV, comparable to a 6T, with half the Write Margin, 50% shorter access time and 30% smaller area. Based on these results our proposed cell appears ideal for DG implementation.

Monte-Carlo simulations have been performed to characterize the SNM behaviour under process variations. V_T, gate W and L, and, V_{DD} variations are applied as Gaussian distributions with a 3σ = 10-15%. Fig. 4 shows the histogram of Monte-Carlo simulations for 6T cells in read and 4T in both read and retention.

6. Conclusions

6T and 4T SRAM cells have been characterized in a double gate 32nm CMOS process. The second gate has been used to improve performance. A novel DG-SOI 4T DL cell has been proposed to take advantage of the second gate. The feedback connection through the back gate of the access transistor leads to greatly improved operating characteristics and best overall performance in the presence of process variations.

Acknowledgment

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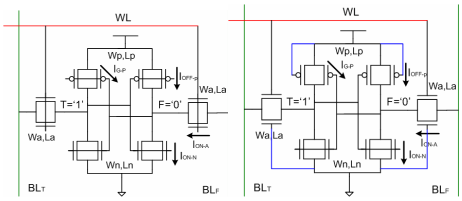
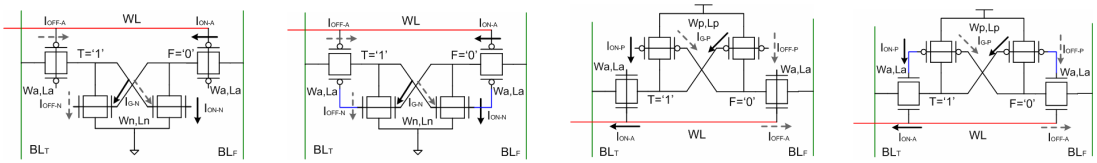
TABLE I: Characterization results

	6T		4T Loadless		4T Driverless	
	6T	6T Hi.	4T LL	4T Hi.	4T DL	4T DL FB
Read Stability (mV)	190	288	213	399	84	377
Retention Stability (mV)	422	400	23	307	46	358
ILEAK (nA)	2.54	2.50	0.58	2.08	1.04	1.42
Write Margin (V)	0.80	1.00	0.35	0.64	0.32	0.50
Write Time (ps)	95	271	22	173	37	111
Write Disturb (µs)	X	X	X	4.08	3.83	6.52



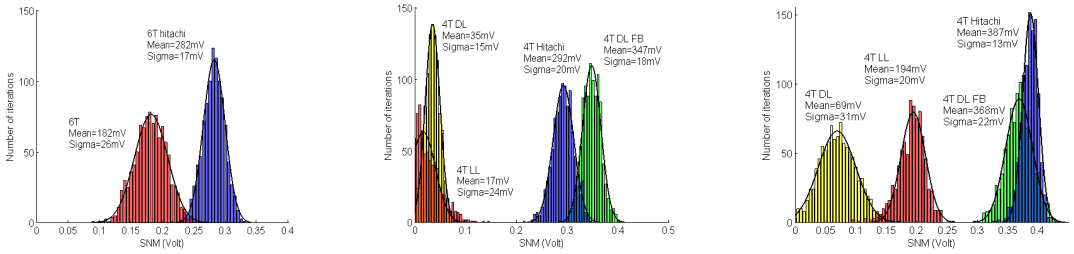
(a) *(b)*

Fig.2: Schematic diagram of 6T SRAM cells



(a) 4T LL *(b) 4T Hitachi* *(c) 4T DL* *(d) 4T DL FB*

Fig.3: *Schematic diagram of studied 4T SRAM cells*



(a) *(b)* *(c)*

Fig.4: *SNM distribution on (a) 6T in reading, (b) 4T cells in retention and (c) in reading*

SESSION 2

Device Modelling and SOI circuits

CHAIR
P. Delatte
CISSOID

Threshold Voltages of Double and Triple Gate SOI FinFETs

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1. Abstract

In this work the behavior of the threshold voltage in double-gate and triple-gate SOI FinFETs transistors with different channel doping concentrations is studied through three-dimensional simulation. The results indicated that for double-gate FinFETs, one or two threshold voltages can be observed, depending on the channel doping concentration. However, in triple-gate it is possible to observe up to four threshold voltages due to the corner effect and the different doping concentration between the up and down sides of the Fin.

2. Introduction

Device FinFETs provide potential advantage, such as: higher integration density, lower short-channel effect and subthreshold slope near ideal [1]. Fig.1 shows the double-gate and triple-gate SOI FinFETs transistors and fig.2 shows the cross sections channel regions.

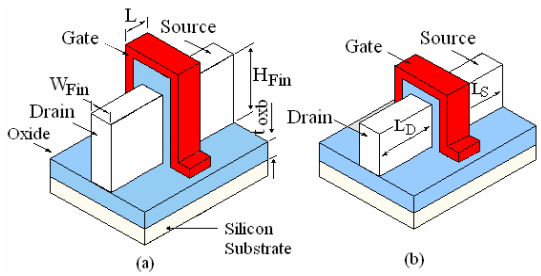


Fig.1: *SOI FinFETs: Double-gate (a); Triple-gate (b).*

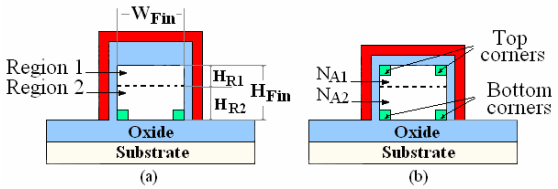


Fig.2: *Cross section view of the FinFETs showing the channel regions and corners: Double-gate (a); Triple-gate (b).*

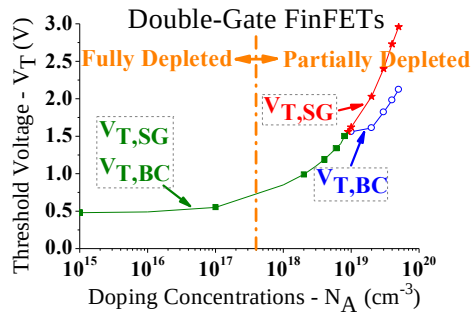
In spite of their exceptional electrostatic control, these architectures FinFETs exhibit corner effects [2]. Due to the corners, up and sidewall side condition of the Fins, and different doping concentrations in channel regions [3], the FinFETs can present from one up to four threshold voltages.

3. Simulation Details

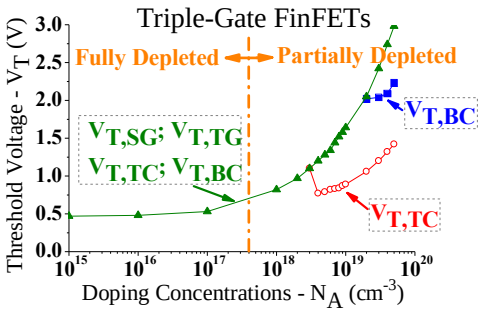
The simulated structures present buried oxide thickness (t_{oxb}) of 145 nm, equivalent gate oxide thickness (EOT) is 2 nm, drain and source length (L_D, L_S) of 100 nm. The width of Fin W_{Fin} is equal to 120 nm; the height of Fin H_{Fin} is 60 nm and the channel length (L) is 1 µm.
The channels of the some devices are divided in two regions, as shown in fig. 2. Region 1 has W_{Fin} = 120 nm and H_{R1} = 5 nm. Region 2 has W_{Fin} is 120 nm and H_{R2} is 55 nm; the interface charge densities of 3 x 10^{10} cm^{-2} is adopted. The simulator used was the Atlas of Silvaco [4] and the threshold voltage is extracted by the maximum transcondutance change method - MTC [5].

4. Results for Single Doped Channels

Fig.3a presents the curve of the threshold voltage versus channel doping concentration (N_A) for double-gate FinFETs.
For higher N_A it is possible to observe two threshold voltages. The lower V_T is related to the inversion of bottom corners ($V_{T,BC}$) due to the substrate coupling (sum of electric field vectors of the substrate and sidewall gate) and the other corresponds to the inversion of the sidewall surfaces controlled by the sidewall gates ($V_{T,SG}$).
For lower N_A, it is possible to see only one threshold voltage (only one peak of the I_D-V_G second derivative curve - MTC) because $V_{T,BC} \cong V_{T,SG}$.
Fig.3b shows the same curves for triple-gate FinFETs. In this case it is possible to obtain up to three threshold voltages for higher N_A. The lower threshold voltage corresponds to the inversion of top corners ($V_{T,TC}$) once these are submitted to the sum of electric field vectors generated by the sidewall and top gates simultaneously. The second one is related to the inversion of bottom corners ($V_{T,BC}$) and the higher one is due to the inversion of the sidewall ($V_{T,SG}$) and top surfaces ($V_{T,TG}$) at the same time.
When the N_A is decreased it is possible to observe two threshold voltages. The lower is the top corners threshold voltage and the other is related to bottom corner, up and sidewall gates simultaneously. For lower N_A it is possible to see just one threshold voltage because $V_{T,TC} \cong V_{T,BC} \cong V_{T,SG} \cong V_{T,TG}$.



(a)



(b)

Fig.3: *V_T x N_A for FinFETs: (a) double-gate; (b) triple-gate.*

5. Results for Double Doped Channels

Fig.4 presents the curve of the threshold voltage versus doping concentration in region 1 (N_{A1}) of the channel for double-gate and triple-gate FinFETs both with N_{A2} = 1 x 10^{16} cm^{-3}. The double-gate FinFETs present just one threshold voltage, independent of the doping concentration difference studied in channel regions. In triple-gate when the difference of doping concentrations in the channel regions increases it is possible to obtain two threshold voltages. These threshold voltages are related to the inversion of the sidewall ($V_{T,SG}$) and the top surfaces ($V_{T,TG}$). The bottom and top corners threshold voltage is not observed in this range studied.

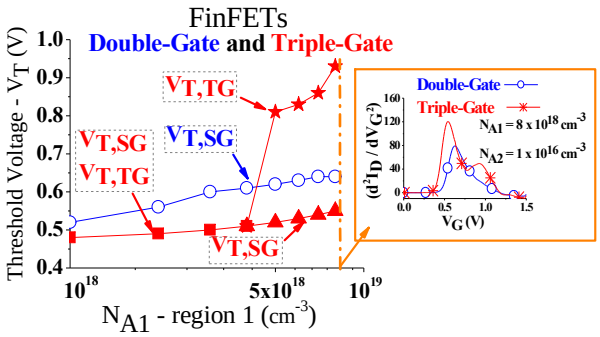


Fig.4: *V_T x N_{A1} and N_{A2} = 1 x 10^{16} cm^{-3} for FinFETs.*

Fig.5 presents the curve of the Threshold voltage versus doping concentration in region 2 (N_{A2}) of the channel for triple-gate FinFETs with N_{A1} = 8 x 10^{18} cm^{-3}. For N_{A2} between 3 to 4 x 10^{18} cm^{-3} it is possible to obtain three threshold voltages.

These threshold voltages are due to the inversion of the top corners ($V_{T,TC}$), sidewall surfaces ($V_{T,SG}$) and the top surface inversion ($V_{T,TG}$) that is controlled by the top gate where the top doping concentration (N_{A1}) is higher than in the remaining of the channel (N_{A2}).

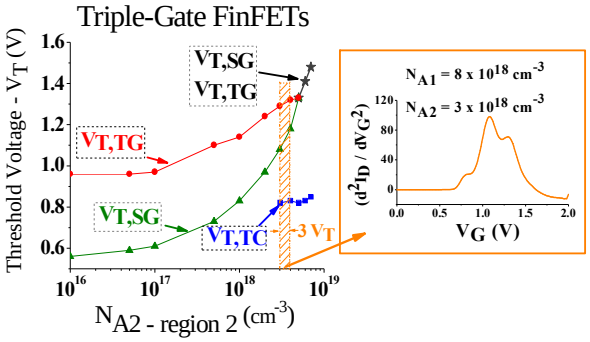


Fig.5: *V_T x N_{A2} and N_{A1} = 8 x 10^{18} cm^{-3} for triple-gate FinFETs.*

Fig.6 presents the curve of the second derivative of the drain current versus gate voltages for triple-gate FinFET with N_{A1} = 6 x 10^{19} cm^{-3} and N_{A2} = 4 x 10^{19} cm^{-3} where it is possible to obtain up to four threshold voltages which are $V_{T,TC}$; $V_{T,BC}$; $V_{T,SG}$ and $V_{T,TG}$.

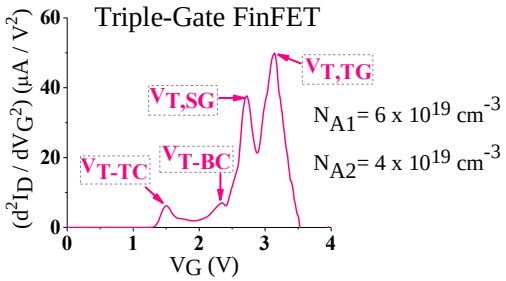


Fig.6: *$d^2 I_D / dV_G^2$ x V_G for triple-gate FinFETs.*

6. Conclusions

When the transistor presents a uniform doping concentration, the double-gate FinFETs can present up to two threshold voltages ($V_{T,BC}$ and $V_{T,SG}$) and the triple-gate FinFETs can present up to three threshold voltages ($V_{T,TC;}$ $V_{T,BC}$ and $V_{T,SG} \cong V_{T,SG}$), both results are observed for higher doping concentration.

When the channel is divided in two regions with different doping it is possible to observe up to four threshold voltages related to the top corners ($V_{T,TC}$), bottom corners ($V_{T,BC}$), sidewall gates ($V_{T,SG}$) and top gate ($V_{T,TG}$).

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Comparative analysis of self-heating in different SOI architectures

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1. Introduction

The aggressive scaling scenario foreseen by the ITRS for the future technological nodes requires to overcome the limitations of the conventional bulk transistor by introducing novel architectures such as planar SOI or FinFETs [1, 2], as well as innovative materials [3].
The adoption of SOI architectures allows to limit detrimental effects such as short channel effects (SCE), gate leakage and sub-threshold currents; on the other hand, the presence of the buried oxide (BOX) layer, featuring a low thermal conductivity, causes severe self-heating effects (SHE) [4, 5]. Furthermore, due to the large dependence of thermal conductivity on the thickness of the front silicon layer [6] further enhancement of SHE is expected in ultra-thin body devices.
In this paper we apply 3D DD E-T simulations to the analysis of SHE in different SOI structures, featuring the same isothermal (I-T) electrical characteristics.

2. Electro-thermal analysis

N-channel Single-Gate SOI (SGSOI), Double-Gate SOI (DGSOI) and FinFETs are compared. Fig. 1 provides a simple sketch of the simulated devices and Tab. 1 reports the values assumed for the most important device parameters. The simulation domain is 14 μm wide in the direction along the channel so that lateral thermal boundary conditions have negligible impact on results. A 1.8 μm thick Si substrate layer is placed beneath the BOX. As we are interested in the impact of self-heating, care has been taken in order to ensure the same I-T electrical characteristics for all the devices. The need to suppress SCE in SGSOI transistors requires an extremely reduced EOT (0.6 nm). Two SGSOI devices are considered: the first one (SGSOI-1) features t_{Si} equal to the FinFET's fin-width (W_{fin}) and a slightly longer gate length in order to control SCE, while the second one (SGSOI-2) features the standard L_G value but much thinner silicon body. While the FinFET's fin width is set to 10 nm, the planar SOI devices feature a channel width $W^{ch} = 5L_G$, a realistic minimum width for planar devices.
3D E-T simulations have been performed using the Sentaurus device simulator [7], with mobility model parameters calibrated in order to reproduce Monte-Carlo calculated $I_{DS}-V_{DS}$ characteristics, according to [8, 9]. Quantum corrections are not considered, in order to reduce the computational burden of the 3D simulations. The Silicon thermal conductivity k_{Si} has been modeled taking into account the large degradation occurring as t_{Si} is scaled down [6, 9]. The substrate electrode is set as an I-T 300 K boundary condition (BC); moreover a lumped thermal resistance $R_{th}=2*10^{-4}$ cm^{2}K/W is connected between the gate and a 300 K BC, in order to take into account the thermal resistance due to the gate dielectric and to the gate-SiO_2 interface [10].

3. Results and discussion

Figs. 2, 3 show the transfer and output characteristics, obtained from I-T and E-T simulations, respectively. The devices features almost the same I-T currents per unit width as is required for a consistent comparison. SHE-related degradation of I_{DS} depends on the device structure.
E-T simulations (Fig. 3) assume gate and S/D contacts as either adiabatic or isothermal 300 K BC.
In both cases the SHE-related degradation of current is maximum for the DGSOI, less critical for the FinFET, and minimum for SGSOI-1. This trend is confirmed even in Fig. 4, where the maximum temperature is plotted as a function of the dissipated power per unit width.
In the case of adiabatic S/D contacts, the differences between SGSOI and the other two structures are related to the wider overlap area between the Si body and the underlaying BOX, through which most of the heat flux occurs. This area is smaller in DGSOI and FinFET (in particular, it is halved in DGSOI, with respect to SGSOI), and this leads to a degraded heat dissipation. Furthermore, the larger SHE of SGSOI-2 compared to SGSOI-1 is due to the degradation of k_{Si} occurring as t_{Si} is scaled down. FinFET presents lower SHE than DGSOI because W_{fin} is much lower than W^{ch} (Tab. 1). In this case, the impact of the heat dissipation occurring in the direction of device width is larger in the FinFET than in the DGSOI, because its relevance increases as the device width decreases. Fig. 5 confirms this behavior: as W_{ch} of the DGSOI is scaled down, the values of I_{ON} and T_{MAX} depart from those obtained from the 2D-DGSOI simulation (corresponding to infinite W_{ch}), and approach the FinFET's ones.
When the S/D contacts are treated as 300 K I-T BC, the differences between the structures become less evident. In this case most of the cooling occurs through the S/D contacts and the cross-sectional area of the S/D access regions become the most relevant parameter, leading to larger SHE in the SGSOI-2 and DGSOI cases, compared to the SGSOI-1 and FinFET.

Acknowledgments Work funded by the Italian MUR (PRIN 2006) and EU (PULLNANO FP6, IST-026828-IP).

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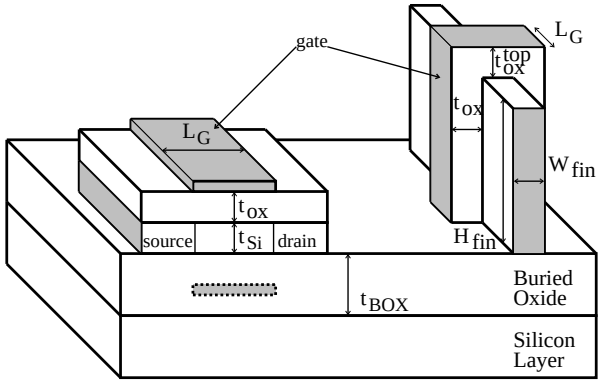


Figure 1: 3D sketch of the simulated SGSOI and DGSOI (left figure) and FinFET (right figure) devices. Figures are not drawn to scale. In the left figure the grey-shadowed dot-contoured region represents the second gate for the DGSOI transistor.

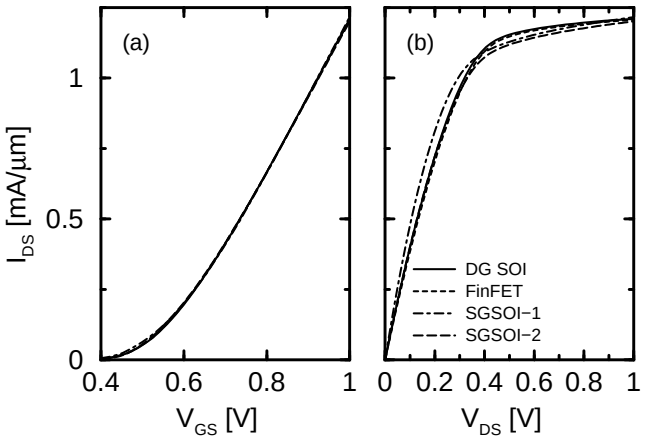
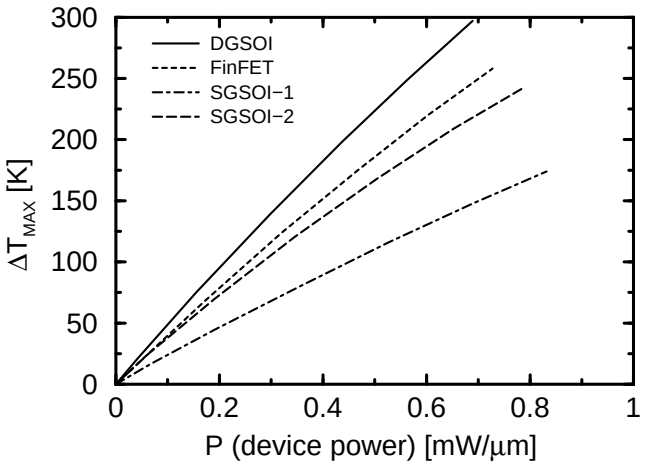


Figure 2: (a) Transfer characteristics (V_{DS}=1.0 V) and (b) output characteristics (V_{GS}=1.0 V), calculated by 3D DD I-T simulations. The figure confirms that the different devices feature similar simulated I−V curves.



	DG SOI	SG SOI	FinFET
R_{TH} (Kμm/mW)	431	209/308	355

Figure 4: ΔT_{MAX} (i.e. T_{MAX}−300 K) as a function of the dissipated power per unit width, for the four considered devices. Consistently to Fig. 3, SGSOI-1 presents the lowest temperature rise and equivalent thermal resistance R_{TH} (i.e. $\Delta T_{MAX}/P$). Table: R_{TH} evaluated for V_{GS}=V_{DS}=V_{DD}.

	DGSOI	SGSOI 1/2	FinFET
Gate Length L_G (nm)	50	64/50	50
Gate Work-func. ϕ_G (eV)	4.6	4.615/4.610	4.6
Gate Ox. Thick. t_{ox} (nm)	0.6	0.6/0.6	0.6
Silicon Thickness t_{Si} (nm)	10	10/5	n.a.
Channel Width W_{ch} (nm)	250	250/250	n.a.
Fin Width W_{fin} (nm)	n.a.	n.a.	10
Fin Height H_{fin} (nm)	n.a.	n.a.	60
Top-gate Ox. Thick. t_{ox}^{top} (nm)	n.a.	n.a.	5
S/D access length (nm)	35	35	35
S/D Doping Conc. (cm^{-3})	1E+20	1E+20	1E+20
Ch. Doping Conc. (cm^{-3})	1E+15	1E+15	1E+15
Buried Ox. Thick. t_{BOX} (nm)	50	50	50
Supply Voltage (V)	1.0	1.0/1.0	1.0

Table 1. Key parameters adopted in simulations. Third column: two different SGSOI architectures, defined to have the same I-T electrical characteristics as DGSOI and FinFET.

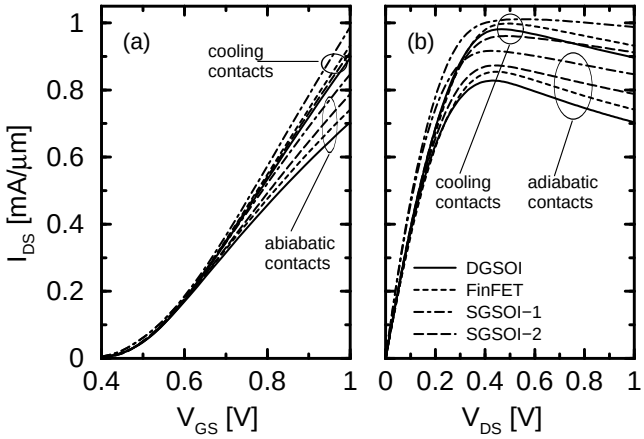


Figure 3: (a) Transfer characteristics (V_{DS}=1.0 V) and (b) output characteristics (V_{GS}=1.0 V), calculated by 3D DD E-T simulations. Two sets of simulations are presented (see the ellipses): in the first one, 300 K isothermal BC are assumed at the S/D contacts; in the second one, the gate and S/D are treated as adiabatic, and the heat flux can occur only through the BOX.

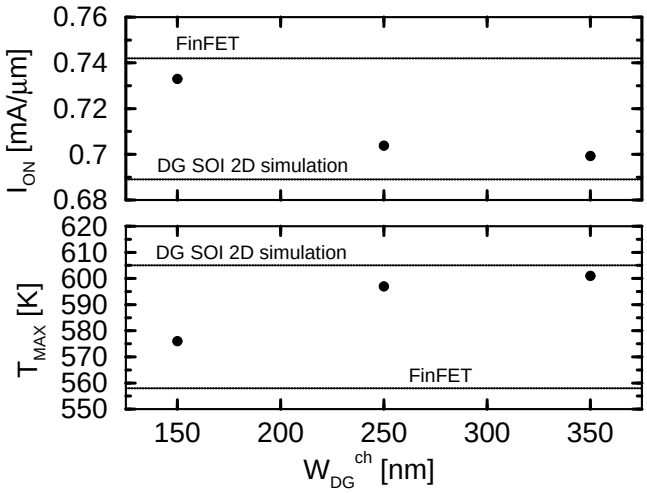


Figure 5: I_{ON} (i.e. I_{DS} for V_{GS}=V_{DS}=V_{DD}) and T_{MAX} vs. DGSOI channel widths (W_{DG}^{ch}). The gate and S/D BC are assumed adiabatic, therefore the heat dissipation can occur only through the BOX. As W_{DG}^{ch} decreases, the values depart from the 2D-DGSOI simulation case (infinite W_{DG}^{ch}), approaching the FinFET case.

Ultra-Low-Power Logic Style for Low-Frequency High-Temperature Applications

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1. Abstract

For ultra-low-power applications as sensor networks, digital integrated circuits may operate at low frequency to reduce dynamic power consumption [1]. At high temperature, the power consumption of such circuits can be dominated by static power dissipation due to leakage current. To avoid prohibitive static power dissipation, designers of high-temperature circuits use very-high-V_T devices on micron-scale SOI technologies [2]. In this contribution, we propose a new logic style, namely Ultra-Low-Power (ULP) logic style, to benefit from the small area and low dynamic power of SOI deep-submicron technologies while keeping ultra-low leakage. In 0.13-µm PD-SOI technology, the static power consumption in active mode is reduced by nearly 3 orders of magnitude at the expense of increased delay.

2. ULP logic style

The structure of ULP logic gates is presented in Fig. 1 [3]. It is based on the equivalent standard CMOS gate with addition of 2 extra devices to gate subthreshold leakage, whose gates are connected to the output node. The header is an NMOS device and the footer is a PMOS device. The connection of the output node to the gate of the header and footer devices acts as a feedback loop by cutting off more the leakage current of the header or the footer device, depending on the output logic level. As shown in Fig. 1 for the ULP inverter, SOI implementation leads to compact layout as the footer (resp. header) can be abutted to the pull-down NMOS (resp. pull-up PMOS).

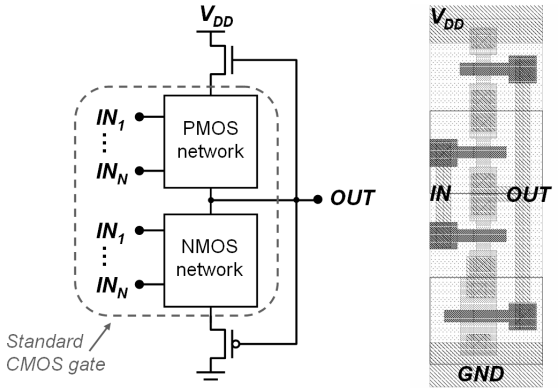

Fig.1: *ULP logic gate schematic and ULP inverter layout*

3. Leakage reduction mechanism

Let us consider I_{OFF} current of the pull-down network (with PMOS footer device included) from the ULP inverter when input voltage is low, as presented in Fig. 2. The leakage reduction mechanism is based on the self-biased negative V_{GS} of the NMOS and PMOS devices inside the pull-down network. V_{GS} values depend on V_A voltage of the internal node A. If devices are symmetrical, V_A is close to $V_{DD}/2$. Devices thus operate with V_{GS} close to $-V_{DD}/2$, leading to ultra-low leakage. Fig. 2 shows measured $I_{OFF,ULP}$ from ULP pull-down network in standard 0.13-µm PD-SOI technology at room and at high temperatures. When V_{DD} increases, the subthreshold current first increases because V_{DS} of the NMOS and PMOS devices increase too. Then, it strongly decreases as V_{GS} of the devices becomes more and more negative. At room temperature, GIDL and gate leakage currents limit the achievable leakage when V_{DD} is higher than 0.7V [4]. At room temperature, $I_{OFF,ULP}$ is reduced by more than 4 orders of magnitudes as compared to $I_{OFF,NMOS}$ of standard NMOS device (V_{DD}=1V). At high temperature, this reduction of I_{OFF} remains larger than 3 orders of magnitude.

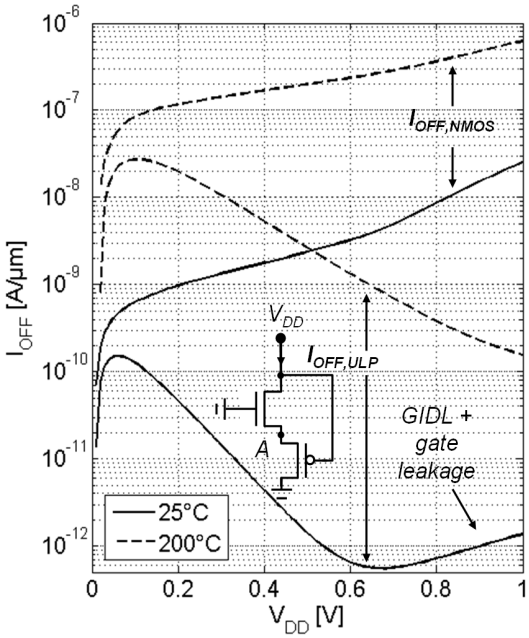

Fig.2*: Measured I_{OFF} vs. V_{DD} (L=0.13 µm)*

4. DC behaviour

In order to assess the correct operation and the robustness of the ULP logic style, let us examine the DC characteristic of the ULP inverter depicted in Fig. 3. Simulation of the voltage transfer curve at 200°C is also presented in Fig. 3. The output levels are close to 0 and V_{DD}. When V_{IN}=0V, V_{GS} of P1 is highly negative and P1 represents a small equivalent impedance. N2 has thus V_{GS}=0 and the I_{ON} pull-up current is the subthreshold current of N2. This I_{ON} current is nearly 3 orders of magnitude higher than I_{OFF} of pull-down network, as shown in Fig. 1. Similar reasoning can be applied to the case V_{IN}=V_{DD}. This leads to very good output logic levels. Moreover, as I_{ON} is only subthreshold current, the slope of the voltage transfer curve from the inverter is very steep, making the design very robust. The drawback is that the delay of the inverter will be high because I_{ON} is a subthreshold current. This is mitigated by the use of low-V_T devices and the high temperature operation.

The curve from Fig. 3 shows hysteresis, the inverter switching voltage is different when the input is rising or falling. This is due to the feedback loop made of the connection of the output node to the header/footer gates [3]. This provides a very high static Noise Margin (NM) for the inverter: NM_L=0.79V and NM_H=0.82V for V_{DD}=1V, which are never achieved with standard CMOS logic style. This unique feature is highly valuable to build robust ultra-low-power SRAM cells.

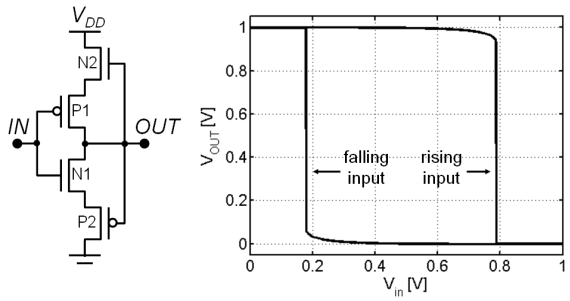

Fig.3: *Simulated voltage transfer curve of ULP inverter ($W/L_{N1,P1,P2}$=0.15/0.13[µm] and W/L_{N2}=0.3/0.13 [µm], V_{DD}=1V, T=200°C)*

5. Performance comparison

In order to assess the efficiency of ULP logic style, performances are compared with standard CMOS logic style at gate level through simulation of an inverter with fan-out of 4. For ultra-low-power applications, delay of the gates is not of uttermost interest. The circuit only has to support low operating frequency in the kHz range. Therefore, we consider the following figures of merit: static current and total power consumption at low operating frequencies (i.e. 1 and 100 kHz), rather than power-delay or energy-delay products. The delay is given for information purpose.

The considered technology is a dual-V_T technology. Low-V_T devices ($V_{T,N}$=0.34V, $V_{T,P}$=-0.33V) are used for ULP logic style to increase drivability of pull-up/down networks and high-V_T devices ($V_{T,N}$=0.43, $V_{T,P}$=-0.42V) are used for standard CMOS logic style to lower static current. Simulation results are summarized in Table 1.

At 1V, ULP inverter provides a static current reduction of nearly 3 orders of magnitude as compared to standard high-V_T CMOS inverter. It leads to very low total power consumption in the pW-range at the expense of longer delay. Notice that the 34-ns delay for FO4 inverter is sufficient to operate circuits at low frequencies such as 100 kHz. The power consumption of high-V_T CMOS inverter at 100 kHz is in the nW-range, being dominated by static current. As shown in Table I, lowering the power supply voltage of high-V_T CMOS logic leads to lower power but it remains in the nW-range.

TABLE I. PERFORMANCE COMPARISON OF INVERTERS AT 200°C

Type	V_{DD} [V]	I_{STAT}	Delay [ns]	Power @ 1 kHz	Power @ 100 kHz
ULP	1	31 pA	34	32 pW	154 pW
High V_T	1	27 **nA**	0.01	27 **nW**	30 **nW**
High V_T	0.5	13 **nA**	0.37	6.8 **nW**	7.7 **nW**

6. Conclusions

We proposed an ULP logic style to benefit from small area and small dynamic power of deep-submicron technologies while keeping ultra-low-leakage at high temperature. ULP logic style is shown to be very robust and to reduce power consumption at low frequency by nearly 3 orders of magnitude. In order for the standard CMOS inverter to achieve the same static current as the ULP inverter, SPICE simulations show that V_T of the devices from the CMOS inverter should be raised by 0.35V. This would lead to a threshold voltage of nearly 0.8V. Such a value is no longer proposed by chip manufacturers in very deep-submicron technologies. ULP logic style is thus a unique technique to design ultra-low-power digital circuits for high-temperature applications, i.e. with neither extra mask nor extra process cost.

Acknowledgment

D. Bol and D. Flandre are with UCL respectively as research fellow and honorary senior research associate of the FNRS of Belgium. The authors would like to thank STMicroelectronics for the device manufacturing.

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Improved Source-Follower Buffer Implementation by Using Graded-Channel SOI nMOSFETs

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1. Abstract

This work studies the performance of source-follower buffers implemented with fully depleted graded-channel (GC) SOI nMOSFETs and compares their performance with those implemented with conventional uniformly doped devices. The analysis is performed by evaluating the buffer voltage gain and linearity with the same mask dimensions. It is shown that by using GC devices, gain very close to the theoretical limit can be achieved, with higher linearity.

2. Introduction and Devices Fabrication

Efficient buffers are of great importance for many analog systems. The classical implementation of a unit-gain buffer is the source-follower [1] (Fig. 1), used, for instance, in integrated APS (active pixel sensor) cells in CMOS imagers [2]. Source-follower buffers are very useful due to their good performance (high input impedance and relatively low output impedance) and low cost, despite presenting less than unity gain and some nonlinearity [1].

The Graded-Channel (GC) SOI nMOSFET is an asymmetric channel device proposed to improve the SOI analog characteristics [3]. Using a simple mask arrangement in the standard SOI CMOS processing, the threshold voltage (V_{th}) implantation is performed at the source side only while the remaining channel is kept with the natural wafer doping concentration. The negative threshold voltage presented by this lightly doped region, can be understood as an extension of the drain region, reducing the effective channel length (L_{eff}=L–L_{LD}, L being the mask channel length and L_{LD} the lightly doped region length). Previous works reported several GC devices advantages over conventional ones for analog applications in common source configuration [3], namely larger transconductance (g_m), reduced drain output conductance (g_D) and appreciable reduction in the harmonic distortion [4]. In this work the impact of the GC channel engineering on the buffer performance will be investigated, focusing on the voltage gain and harmonic distortion. The studied devices have been fabricated according to the process described in [3] and have channel width (W) of 20µm, mask gate length of 2µm and different L_{LD}/L ratios.

3. Measurements results and discussion

Fully depleted conventional and GC SOI nMOSFETs were measured in source-follower configuration, as shown in Fig. 1, and the experimental curves were obtained with an Agilent 4156C Semiconductor Parameter Analyzer. The drain voltage, V_D, has been kept constant at 2.5V and the V_{OUT} *vs* V_{IN} characteristics were obtained by sweeping the gate voltage (hereafter called the input voltage, V_{IN}), and measuring the source voltage, V_{OUT}, for different bias current (I_{bias}) at all inversion regimes. Fig. 2 shows V_{OUT} *vs* V_{IN} curves in weak and strong inversion, with normalized drain bias current ($I_{bias}/(W/L_{eff})$) of 0.1nA and 4µA, respectively. The buffer voltage gain, A_V, defined as the derivative of V_{OUT} with respect of V_{IN}, is also presented in this figure.

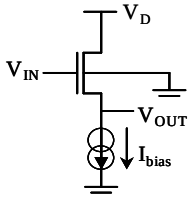

Fig. 1: *Source-follower buffer as measured in this work.*

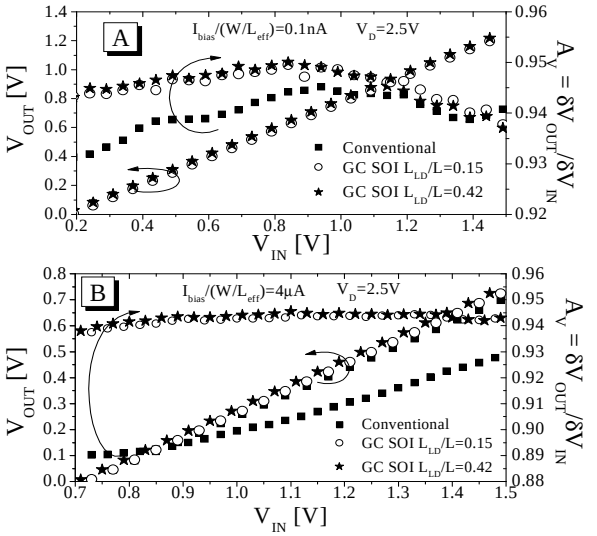

Fig. 2: *Measured voltage gain and output voltage as a funtion of input voltage for devices biased in weak (A) and strong inversion (B).*

From the presented results, one can clearly see the ac gain enhancement provided by GC devices in comparison to the conventional counterpart both in weak and strong inversion whereas the large-signal V_{OUT} *vs* V_{IN} curve are very close due to identical V_{th} and current density.

From the small-signal model, A_V can be expressed as

$$A_v = \frac{g_m}{ng_m + g_D} \qquad (1)$$

Since the body factor, n, is a technology-dependent parameter, one can assume that its variation is the same in conventional and GC devices. Therefore, any gain improvement provided by the GC architecture is related to g_m and g_D. In order to analyze the influence of these parameters on A_V, Fig. 3 presents the g_m and g_D of the devices under study, extracted at V_D=2.5V and V_S=0V. Despite these conditions are not the same presented in Fig. 2, this analysis allows for comparing devices behaviour operating at the same bias condition, aiming to explain the results presented in Fig. 2. The presented results clearly show the expected g_m increase and g_D reduction provided by the GC devices. In addition, it is possible to see that, as V_{IN} decreases, g_D becomes closer to g_m, which causes A_V degradation.

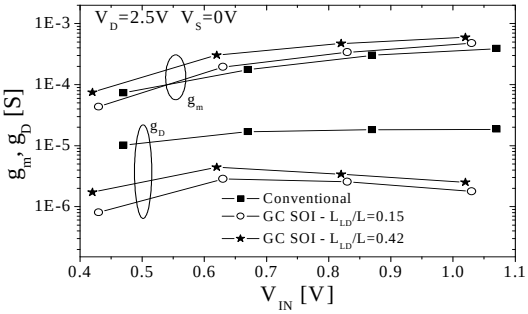

Fig. 3: *Measured transconductance and output conductance as a function of V_{IN}.*

These results justify the better gain and its smaller decrease presented by GC devices as V_{IN} is swept. The reduction of V_{IN} causes V_{DS} increase, worsening g_D for all devices. However, as GC devices present reduced g_D and larger breakdown voltage [3], g_D is kept at lower values for a larger range of V_{DS} than in the conventional device, which is the reason for the virtually constant GC gain while the conventional device presents a significantly reduction, mainly in strong inversion. Also, the larger g_m of GC devices further contribute to the increased gain, as it makes larger g_D increase necessary to degrade A_V.

From I_{DS} *vs* V_{GF} and I_{DS} *vs* V_S curves of all devices under study, g_m and the source transconductance (g_{ms}) were extracted in saturation, and the 1/n factor, which is the theoretical limit of the source-follower gain, when g_D can be neglected, has been obtained as g_m/g_{ms} [5] (Fig. 4). By using these results and the ones presented in Fig. 3, the gain has been calculated through eqn. (1), and is also presented in Fig. 4. As can be noted by the analysis of this figure, the gain of GC devices approaches the theoretical limit whereas, for the conventional device, the difference from this limit at low V_{IN} can reach 11%. These results are in agreement with those presented in Fig. 2.

It is well known that source-followers V_{OUT} *vs* V_{IN} characteristics present some nonlinearity both due to the nonlinear dependence of V_{th} upon V_S and to the g_D dependence on V_{DS} [1]. The total harmonic distortion (THD) has been extracted using the Integral Function Method (IFM) [6], which allows for obtaining distortion properties from DC measurements. IFM considers the input signal as composed by a bias voltage source (which coincides with V_{IN}) associated to a sinusoidal signal with amplitude Va. Fig. 5 presents THD, extracted from the measurements presented in Fig. 2 , with Va=50mV.

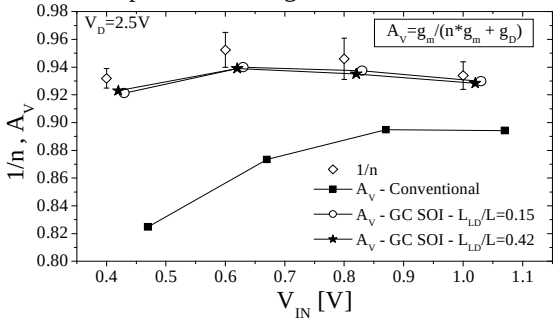

Fig. 4: *Experimental 1/n factor and calculated gain as a function of V_{IN}.*

From the obtained results, one can note that, while in weak inversion, THD/A_V tends to have similar behaviour in all devices (despite the shift of the minima which is related to the V_{IN} for the maximum g_m [6]), as the inversion level moves towards strong inversion, source-followers with GC devices considerably improve the linearity by more than 10 dB, once THD is related to g_D [1] and the inverse of g_m [7].

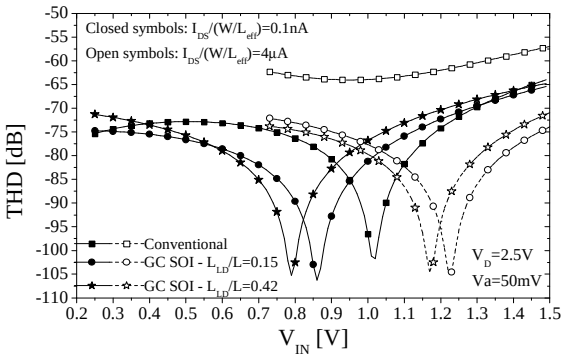

Fig. 5: *THD as a function of V_{IN}, for devices operating at weak and strong inversion, considering Va=50mV.*

4. Conclusions

The performance of source-follower buffers is significantly improved if they are implemented with GC SOI nMOSFETs. It has been demonstrated that the use of GC devices can significantly increase the voltage gain with respect to conventional SOI and also they lead the gain near to the theoretical limit. Additionally, the buffer total harmonic distortion is reduced if GC devices are used.

Acknowledgements

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Introduction of Diamond into advanced FDSOI CMOS

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1. Abstract

The merits of classical Buried OXide (BOX), Ultra Thin BOX (UTBOX) and Diamond BOX for Fully Depleted Silicon-On-Insulator (FDSOI) devices are compared via electro-thermal simulations. Diamond BOX demonstrates reduced parasitic capacitances compared to UTBOX and superior thermal management compared to thick or thin SiO_2 BOX.

2. Introduction

SOI technology is a suitable candidate to fulfill the International Technology Roadmap for Semiconductors requirements in the next years [1]. However, the conventional buried insulator SiO_2, via its poor thermal conductivity, is a barrier to heat evacuation from the device to the substrate ($1.4W.m^{-1}.K^{-1}$ for SiO_2 compared to $148W.m^{-1}.K^{-1}$ for bulk silicon at 300K). Thus, SOI configuration gives rise to self-heating and higher circuit temperature than bulk Si technology [1].

Diamond (noted C*) presents the higher value of thermal conductivity in natural materials and relatively low dielectric permittivity (ε_{C*}=5.5). We choose here to study the implications of replacing SiO_2 by Diamond as thick BOX and compare it to the classical BOX and UTBOX. Both solutions are examined from electrical and thermal points of view in advanced SOI MOSFETs.

3. Simulated structure

Simulated structure is detailed on Fig.1. Substrate is p-type Si doped at $10^{15}cm^{-3}$. Its thickness is fixed at 5µm for electrostatic simulations and 50µm for electro-thermal simulations. Channel doping is $10^{15}cm^{-3}$, and metal gate is mid-gap. Channel length is L_C=25nm and Si thickness (t_{Si}) is 5nm. Thermal contacts are fixed at Source/Drain cap with thermal resistance corresponding to 500nm tungsten plug (typical height of passivation oxide layer). V_{dd} is 1.0V except when redefined.

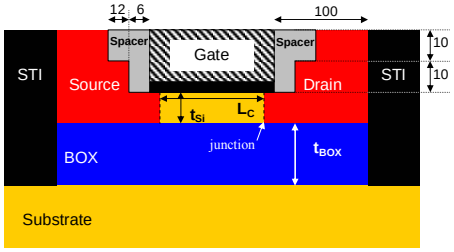

Fig.1: *Schematic representation of the simulated structure. Dimensions are given in nanometers.*

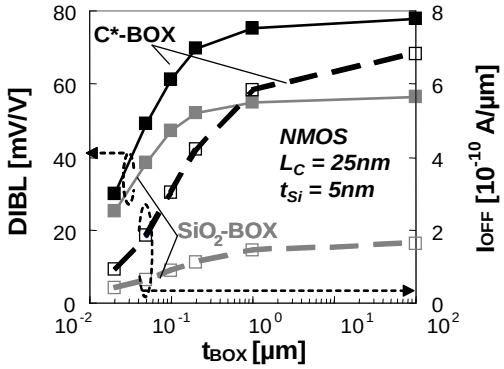

Fig.2: *Comparison of DIBL (closed symbols) and I_{OFF} (open symbols) for C*-BOX and SiO_2-BOX versus t_{BOX}.*

4. Electrical impact

Presence of BOX reduces Short Channel Effects (SCE) and DIBL [1]. BOX thinning improves this ability as can be seen on Fig.2: for a given channel length, DIBL and I_{OFF} are reduced by BOX thinning, considering either SiO_2 or pure Diamond. This has been attributed to the increase of transverse field [2] and reduction of the Drain Induced Virtual Substrate Biasing (DIVSB) [3]. Nevertheless, C*-BOX based devices exhibit higher SCE level, which is due to the higher permittivity of Diamond compared to SiO_2 [4]. With very thick BOX, a saturation behavior is observed, because of a maximum level of DIVSB and minimum vertical electric field (electrical flux is then stopped by the BOX). But the use of a thin BOX leads to a reduced mobility because of the increased electric field between front gate and substrate [2], and to a degraded long channel subthreshold swing [1].

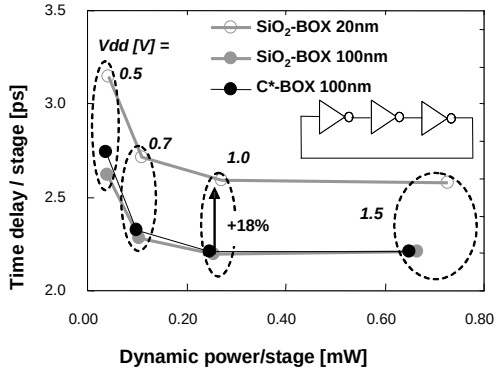

Fig.3: *Time delay versus stage dynamic power of 3-stages ring oscillator. W=1µm. Substrate is modeled as an electrode with a 5.0eV workfunction ($10^{15}cm^{-3}$ p-doped Si). V_{dd} varies between 0.5 and 1.5V.*

Furthermore, parasitic capacitances between source/drain and substrate are also increased with thin BOX. The resulting picture is a 18% increase of the delay/stage of a 3-stages unloaded ring oscillator (see simulations of Fig.3) with the use of a 20nm thin BOX, compared to thick 100nm SiO_2-BOX and C*-BOX, both exhibiting nearly same behavior. Every structures have been optimized to get the same off-state current (10^{-10} A/µm) and presented results are in agreement with [5].

4. Thermal enhancement

For sub-10µm thick diamond layers, great attention must be paid to Diamond Thermal Conductivity (TC). Inset of Fig.4 shows experimental TC dependence on thickness [6-11]. A strong TC degradation is observed, presumably due to the grain morphology (size, grain boundary, defects) and interfaces. SiO_2 shows same behavior but for smaller dimensions due to its amorphous nature: TC of 0.8W.m^{-1}.K^{-1} has been reported for 32nm SiO_2 layer [12], instead of 1.4 W.m^{-1}.K^{-1} for bulk oxide.

Considering these dependences, we have investigated the impact of the BOX thickness on ΔT_{Drain}, defined as device temperature increase at drain junction (hotter part of the device). Results are presented on Fig. 4. ΔT_{Drain} is reduced by 39K (-36%), when the SiO_2-BOX thickness is reduced from 100nm down to 20nm, this last configuration still exhibiting a rise of 109K.

SiO_2-BOX thermal resistance is reduced with thickness whereas Diamond exhibits inverse behavior: TC reduction counterbalances the thinning effect. Nevertheless, C*-BOX shows superior thermal management capabilities than its SiO_2 counterpart, whatever the BOX thickness. In particular, 100nm C*-BOX allows a 77K reduction of ΔT_{Drain} compared with 100nm SiO_2-BOX: 71K versus 148K (-52%). If we assume further technology optimization enabling Diamond TC to be independent of thickness below 300nm (dashed line of Fig.4, for k_{C*}=23 W.m^{-1}.K^{-1}), a significant 99K reduction of ΔT_{Drain} is observed: 49K versus 148K (-66%). The gain in mobility can be estimated at a factor of 2.0 using the $T^{-1.75}$ law of the phonon-limited mobility.

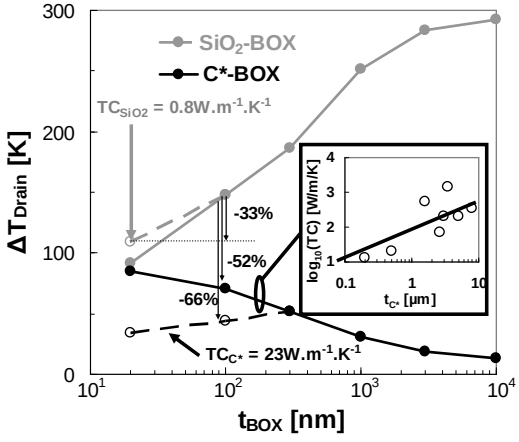

Fig.4: *ΔT_{Drain} vs BOX thickness for 1mW/µm power dissipated. For SiO_2, continuous and dashed line stand for k=1.4 and 0.8 W.m^{-1}.K^{-1} [12]. For Diamond, continuous line stands for fitted TC (see inset: evolution of the thermal conductivity of sub-10µm thick diamond layers from [6-11]) and dashed line stands for TC at 23 W.m^{-1}.K^{-1} (corresponding to 300nm thick diamond).*

Not only a gain in mobility but also in leakage current can be obtained by heating reduction: we have plotted on Fig.5. I_{OFF} current of C*-BOX and SiO_2-BOX based devices as a function of the transistor temperature. At the same temperature, C*-BOX devices suffer higher leakage current, as previously seen. On the other hand, if C*-BOX allows at least a reduction of 25K of the circuit temperature elevation (compared to SiO_2-BOX), C*-BOX based devices can exhibit same leakage level as their oxide counterparts (hotter due to the poor thermal conductivity of SiO_2).

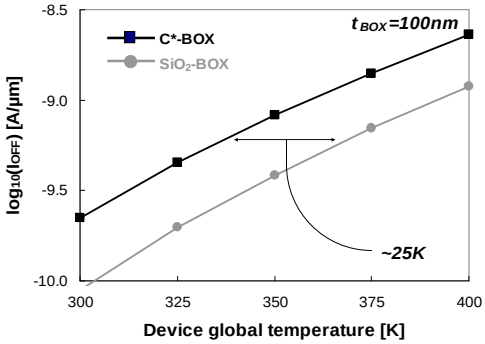

Fig.5: *C* and SiO_2-BOX based I_{OFF} versus temperature in NMOSFETs.*

6. Conclusions

For thermal management issues in future technology nodes of FDSOI-MOSFETs we have compared two approaches: shrinking SiO_2-BOX and introducing C*-BOX. The first way shows improvement in electrostatic control and better thermal management. But it leads to lower operating frequency. 100nm thick C*-BOX is the compromise between improving the speed/power consumption trade-off and still leading to much better thermal management, compared to current BOX or UTBOX. Furthermore, the temperature reduction could allow C*-BOX based devices to exhibit same (or even lower) leakage current as SiO_2-BOX based ones.

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SESSION 3

Quantum device modelling

CHAIR
S. Cristoloveanu
IMEP

Electron Subband Structure and Controlled Valley Splitting in Silicon Thin Body SOI FETs: Two-Band k·p Theory and Beyond

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1. Introduction

For analytical subband structure calculations in silicon (Si) it is commonly assumed that the energy dispersion of the conduction band valleys is well described by a parabolic approximation with the transversal mass m_t and the longitudinal mass m_l. However, in presence of shear strain a more general description based on the two-band **k·p** Hamiltonian is necessary [1-3]. Within the two-band **k·p** model the subband structure for an infinite square well potential can be found analytically. Due to the valley degeneracy, the unprimed subbands remain two-times degenerate within the **k·p** approach. Recently, a valley splitting larger than the spin splitting was reported [4]. Lifting degeneracy reduces scattering and improves the coherence time in spin qubits, which makes silicon-based quantum devises promising for future applications in quantum computing. In this work we propose an alternative mechanism to create and control the valley splitting by applying shear strain.

2. Method and Results

Within the two-band **k·p** model the dispersion relation of a [001] valley is of the form [1-3]

$$E = k_z^2 + \left(k_x^2 + k_y^2\right)m_l / m_t - 2\sqrt{k_z^2 + \delta^2}\,, \qquad (1)$$

where all the wave vectors are normalized by $k_0 = 0.15\times 2\pi / a$, the position of the minimum relative to the X point. Energies are in units of $\hbar^2 k_0^2/(2m_l)$, $\delta^2 = (\eta - m_l k_x k_y / M)^2$, $\eta = m_l D\varepsilon_{xy}/k_0^2$ is dimension-less shear strain, $M^{-1} \approx m_t^{-1} - m_0^{-1}$, ε_{xy} denotes the shear strain component, and D=14 eV is the shear strain deformation potential [1,4]. Excellent agreement between the two-band **k·p** model (1) and the results of empirical pseudo-potential (EPM) band structure calculations with the parameters from [2,5] is demonstrated in Fig.1. Tensile stress in [110] and compressive stress in [-110] direction is assumed. For this setup only shear strain component ε_{xy} is nonzero. The shear strain ε_{xy} substantially modifies the energy dispersion in the [001] valleys. The k_z dispersion is shown in Fig.2 for several values of shear strain. The valley minimum moves both in energy and position, approaching the X-point of the Brillouin zone for larger strain $\eta \to 1$.

The subband energies can be found analytically for an infinite square well potential, which is a good model for an ultra-thin Si film. The dispersion of the unprimed subbands in a [001] thin Si film of thickness t is

$$E_n = p_n^2 + \left(k_x^2 + k_y^2\right)m_l / m_t - 1 - \delta^2/(1 - p_n^2)\,, \qquad (2)$$

where $p_n = (\pi n)/(tk_0)$. For zero strain $\eta = 0$. The denominator of the last term in (2) describes the dependence of the non-parabolicity parameter on the film thickness [5] for the unprimed subbands as shown in Fig.3. This increase of the non-parabolicity parameter with t leads to a decrease of low-field mobility as compared to the mobility computed with the bulk value α=0.5 eV^{-1}. The relative correction is about 7% for t= 3 nm and 15% for t=2.5 nm (Fig.4).

The **k·p** theory predicts the same dispersion (2) for both [001] valleys and cannot describe the valley splitting. To go beyond the **k·p** theory, we introduce an auxiliary tight-binding model defined on a lattice of sites each containing two localized orbitals $\alpha(\mathbf{r})$ and $\beta(\mathbf{r})$ in such a way that it mimics the two-band bulk k_z dispersion [6]. In a finite array of 2N sites the two Bloch functions are:

$$\psi_{\pm}(\mathbf{r}, E) = \sum_{i=1,2}\sum_{n=-N}^{N} C_i \exp(ik_i na/2)\big(a(k_i)\alpha(\mathbf{r} - na/2) + ib(k_i)\beta(\mathbf{r} - na/2)\big) \pm C.C., \qquad (3)$$

where k_i are defined by $E_n(k_i)=E$, a is the Si lattice constant, $a(k_i)$, $b(k_i)$ are the coefficients in the linear combination of two basis functions and are determined from the two-band **k·p** model, and $C.C.$ is complex conjugate. Proceeding as in [6], the following equation for p_n is readily obtained:

$$\sin(p_n^{\pm} k_0 t) = \pm \frac{\delta p_n^{\pm} \sin\left(\dfrac{1 - \delta^2 - p_n^{\pm 2}}{1 - p_n^{\pm 2}} k_0 t\right)}{\sqrt{(1 - p_n^{\pm 2})(1 - \delta^2 - p_n^{\pm 2})}}. \qquad (4)$$

It follows from (4) that for $\delta = 0$, when the dispersion is purely parabolic, the valley splitting is exactly zero. Since δ depends strongly on shear strain, applying uniaxial [110] stress to [001] ultra-thin Si film generates valley splitting proportional to strain. Uniaxial stress is currently used to enhance performance of modern MOSFETs, where it is introduced in a controllable way. For small δ (4) gives

$$\Delta E_v = 2\frac{k_0^2}{m_l}\left(\frac{\pi n}{k_0 t}\right)^2 \frac{\delta}{k_0 t}\sin(k_o t) \qquad (5)$$

for the valley splitting, so that the splitting is engineered by adjusting strain and t.

3. Conclusion

In conclusion, an alternative way to induce controllable valley splitting in ultra-thin Si films by applying uniaxial stress is proposed. For small stress values the splitting is shown to depend linearly on shear strain. Valley splitting rapidly increases with decreasing Si thickness and can be larger than the spin splitting.

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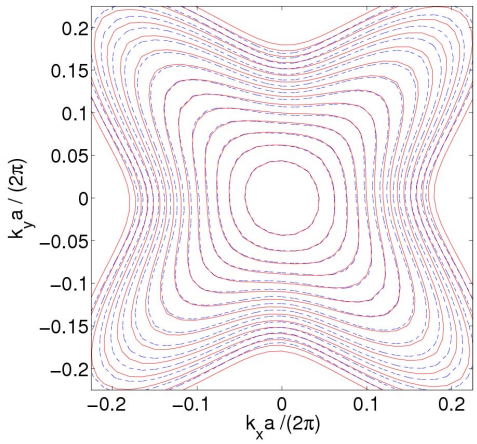

Fig.1: *Comparison between Eq.(1) (dashed lines) and the results of EPM calculations (solid lines). The contour lines are spaced at 50 meV. Tensile stress along [110] and compressive stress along [-110] of 150 MPa in each direction is applied.*

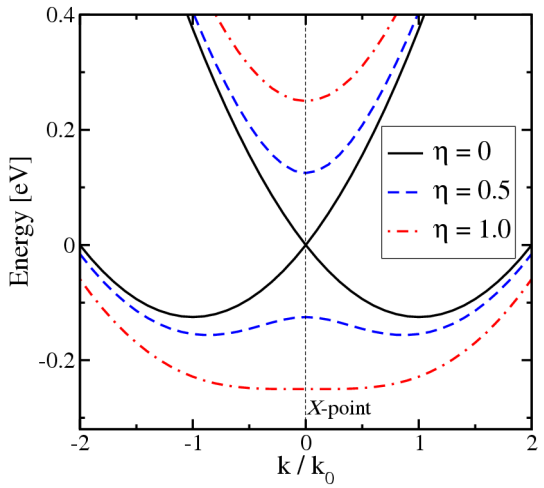

Fig.2: *Conduction band (1) for different shear strain values.*

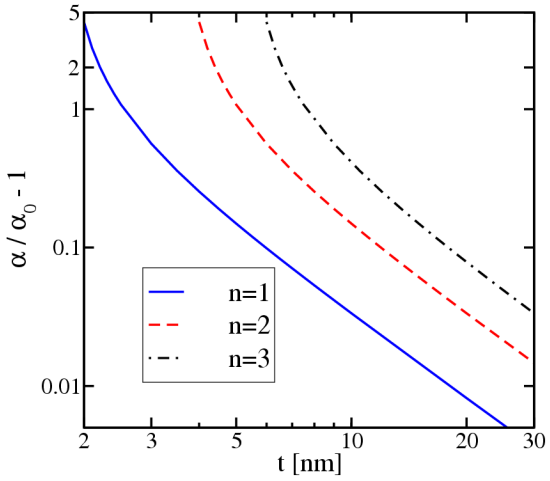

Fig.3: *Dependence of the non-parabolicity parameter on film thickness t.*

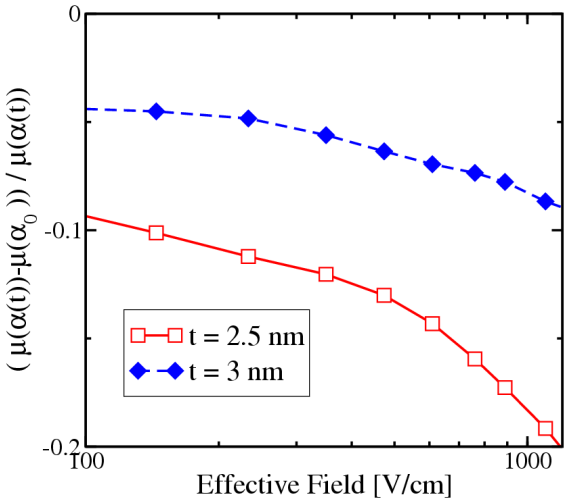

Fig.4: *Relative mobility correction due to thickness dependence of the non-parabolicity parameter as a function of effective field, for two Si film thicknesses. The correction is negative and reaches 20% for t=2.4 nm.*

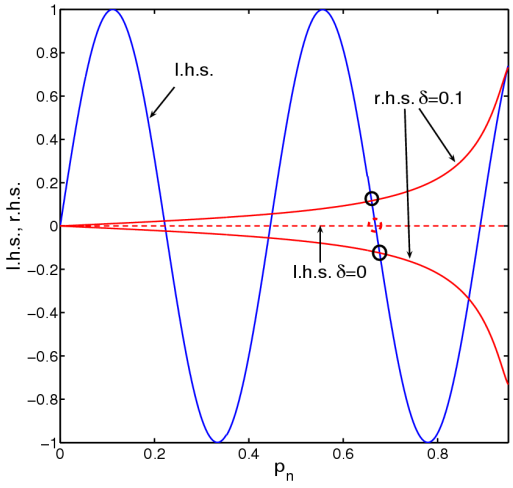

Fig.5: *The left-hand side (l.h.s) and the right-hand side (r.h.s) of (4) as function of p_n, without shear strain (dotted line) and for a nonzero shear strain. Intersections of l.h.s and r.h.s. reflect graphical solutions of (4). Splitting between roots $p_n^{\pm}$ results in valley splitting controlled by shear strain.*

Estimations of the I_{on}-I_{off} Performances of Nano nMOSFETs with Alternative Channels Materials

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1. Abstract

In this work, the impact of light conduction band effective masses on I_{on}-I_{off} performances of Nano nMOSFET has been re-investigated by the mean of simple analytical models. Contrary to previous studies, because of the enhancement of Source to Drain Tunneling (SDT) and the degradation of quantum capacitance in light effective masses materials (like GaAs and Ge), Si based devices turn out to offer an acceptable I_{on}-I_{off} trade off for the last node of the roadmap.

2. Introduction

The introduction of alternative channel material appears to be a possible solution to meet the ITRS expectations for the 22 and 16nm nodes. Indeed, the higher mobility and the smaller effective masses of these materials (such as Ge, GaAs, InGaAs …) induce respectively a larger mean free path and an increased injection velocity, resulting in larger quasi-ballistic drive current [1,2]. Performances of such structures have been analyzed by many authors, both experimentally [3,4] and theoretically [5-8]. It appears that in many cases, the introduction of these channel materials also results in a increased Short Channel Effect (SCE), a degraded quantum capacitance and an enhanced leakage currents.

In this work, to qualitatively estimate the impact of these different effects, a simple analytical model has been developed, and applied to a generic semi-conductor material, allowing an efficient computation of both I_{on} and I_{off} versus effective masses. The first section describes the model derivation, while results are discussed in the second section.

3. Model derivation

For sake of simplicity, following [7], devices are assumed to operate in the quantum limit (one degenerated subband), with a fully ballistic transport along the channel. The on state current has been modeled using in the Natori approach [9], accounting for quantum capacitance degradation, leading to the fully analytical formula Eq. (1). The validity of the quantum limit approximation is investigated in Fig. 1 and 2. A good agreement with numerical Poisson Schrodinger simulation is obtained in extremely thin body (1nm) device. As expected, the agreement between model and simulation is degraded when thicker body (5nm) are considered.

The modeling of leakage currents first requires the computation of the channel energy potential barrier between source and drain (see [10] and Fig. 3), and then the calculation of its transparency, both in tunneling and thermionic (conventional leakage, including SCE) regime. To achieve an analytical expression of this transparency, the barrier has been assumed of parabolic shape. Coefficients of this parabolic energy barrier have been calculated to match the boundary conditions and barriers height of the real barrier, modeled as in ref [10]. The barrier transparency is then solved using the WKB approach (Fig 4. and equ. (6)). Finally, the subthreshold current is obtained using an improved Esaki integral over the energy [11], accounting for quantization (fig. 5 and equ. (5)). This integral can be further simplified by making the appropriate approximations on the Fermi function for the different range of energy.

Both transparency and current computed using the parabolic approximation has been found in good agreement with more accurate numerical calculation performed on the "real" barrier of ref. [10] for a large range of effective masses (0.01 m_0 to 1 m_0) and channel length (6 nm to 50 nm).

4. Results and discussion

To investigate the impact of the effective mass reduction in high mobility channel material like III-V material (0.063m_0 for the Γ valley of GaAs, 0.023m_0 for the InAs one), the on and off current have been calculated versus effective masses. For a fair comparison, the gate work function for each effective mass has been systematically adjusted, as illustrated by fig 6, to match an constant off current of 0.11µA/µm (the ITRS specification for the HP 22 and 16nm node). Fig. 7 shows the subthreshold drain current for various effective masses, after the adjustment procedure. It can be seen that the reduction of the effective masse induces a significant degradation of the subthreshold slope.

The resulting I_{on} current of double gates nMOSFETs (designed according to the 22 and 16nm node of the ITRS) has been plotted as function of the effective mass, including or not quantum capacitance (Fig. 8a and 8b). All the curves exhibits an maximum, featuring an ideal effective mass trade off. When quantum capacitance is properly accounted, the value of these ideal effective masses has been found close to 0.2 m_0 for the smaller device (L = 6 nm), corresponding to the Si value of masses. In other word, the increase of SDT and the degradation of quantum capacitance in light effective mass materials counterbalances the increase of injection velocity when less than 10 nm channel length device are considered.

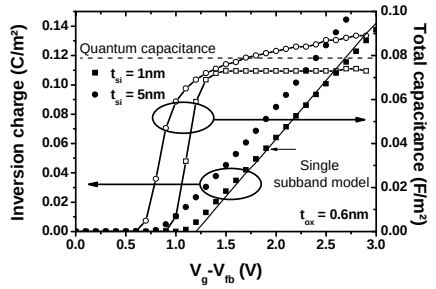

Fig.1: *Inversion charge and total capacitance as a function of the gate voltage, obtained by Poisson-Schrödinger 1D (PS1D) simulation and single subband model. Agreement is acceptable only for extremely thin silicon thicknesses*

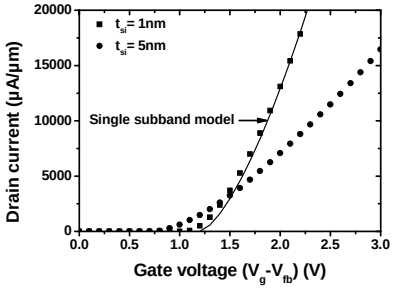

Fig.2: *Ballistic drain current as a function of the gate voltage obtained by PS1D calculation, compared with the model (see also Fig. 1).*

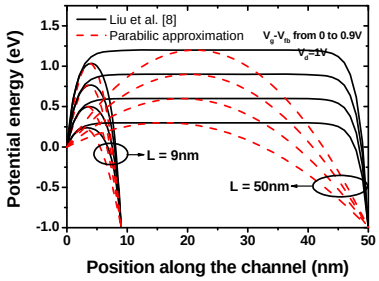

Fig.3: *Potential energy barrier along the source-drain direction for a short and a long channel with a t_{si} of 3nm, obtained by the Liu model [8] and by the parabolic approximation used in this work.*

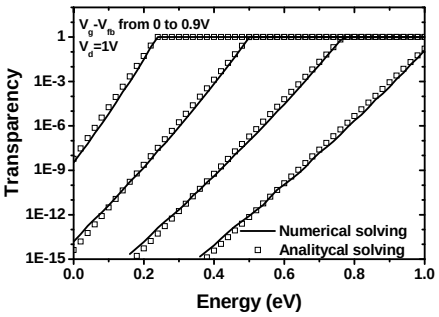

Fig.4: *Transparency versus energy, calculated by the WKB approximation on the barrier obtained with the Liu model, compared with the fully-analytical model in the parabolic approximation*

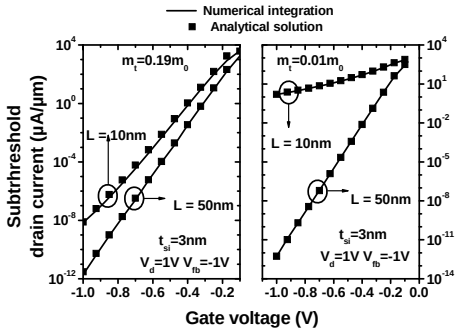

Fig.5: *Subthreshold drain current versus gate voltage obtained by the semi-analytical model and the fully-analytical model, for different channel length and effective masses.*

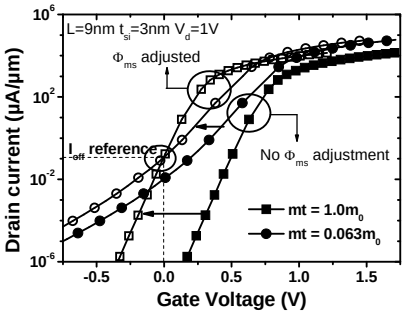

Fig.6: *Drain current versus gate voltage, for two different effective masses, with and without gate work function adjustment. After adjustment, all curve have an I_{off}=0.11µA/µm at V_g=0*

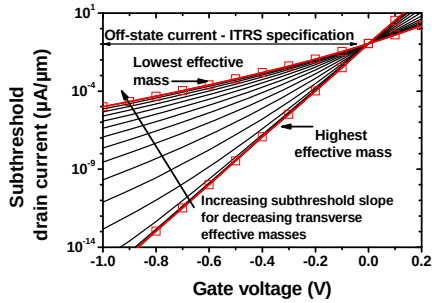

Fig.7: *Subthreshold drain current versus gate voltage for various effective masses (from 0.063m_0 to 1.063m_0) after gate work function adjustment (constant I_{off})*

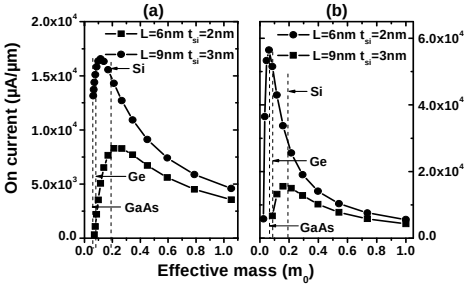

Fig.8: *On state drain current versus effective mass for two double gate FETs designed according to the 22 and 16nm node of the ITRS at same I_{off} (a) with quantum capacitance degration, (b) without. The dashed line represent the transverse effective mass of Si, Ge and GaAs*

On state current equations :

$$I_{on} = \frac{16\,q^{\frac{5}{2}}\sqrt{m_t}}{3\pi^2\hbar^2}\left(\frac{Q_{inv}}{C_q}\right)^{\frac{3}{2}} \quad (1)$$

with

$$Q_{inv} = 2\frac{C_{ox}\cdot C_q}{C_q + 2C_{ox}}\left(V_g - V_t\right) \quad (2)$$

and $$C_q = \frac{2q^2 m_t}{\pi\hbar^2} \quad (3)$$

Off state current equations:

$$I_{off} = q\frac{4\sqrt{2m_t k_b T\cdot q}}{h^2}\int_0^{\infty} T(E)\,F_{-1/2}(E)\,dE \quad (4)$$

with $$F_{-1/2}(u) = \int_0^{\infty}\frac{2dy}{1+\exp\left(y^2-u\right)} \quad (5)$$

and $$T(E) = \exp\left(-\frac{2}{\hbar}\int_a^b\sqrt{2\,m_x\left(Ep(x)-E\right)}\,dx\right) \quad (6)$$

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Acknowledgments:
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Study of Ballisticity in SOI Nano-MOSFETs at Very Low Drain Bias

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1. Abstract

This work presents a thorough study of quasi-ballistic transport at very low and moderate drain-to-source bias in single gate (SG) and double gate (DG) SOI MOSFETs. The simulations performed with a Quantum corrected Ensemble Monte Carlo simulator (Q-EMC) show opposite trends in the nanoballisticity at moderate and low lateral field. For each regime, the mechanisms governing the quasi-ballistic transport are analyzed. The ratio between transit time and relaxation time explains why the proportion of ballistic carriers increases with drain bias until a value which also depends on the inversion charge.

2. Introduction

With the 45nm technological node in mass production since November 2007, the ultimate physical limits from the scaling point of view appear in the technology line of sight. Following this trend, channel lengths are aggressively shrunk towards the sub-10nm dimensions. In such conditions, the carrier transport becomes less diffusive and approaches to the quasi-ballistic operation. In this scenario, the study of this transition becomes very relevant since state-of-the-art and next generations transistors will operate in these conditions approaching to the ultimate limit for MOSFETs represented by the ballistic transistor. Previous works have been devoted to quasi-ballistic transport at moderate and high drain bias [1, 2]. This paper is focused on the study of electron transport in advanced SOI devices at very low bias conditions (V_{DS} < 100 mV). Both single gate (SG) and double gate (DG) nanotransistors with 15nm channel length and different silicon thickness have been considered. A Quantum corrected Ensemble Monte Carlo (Q-EMC) simulator including phonon and surface roughness scattering is employed to perform the simulations. This tool allows us to take into account the effect of both ballistic and non-ballistic carriers in the behaviour of the device. The role of each scattering mechanism can be also revealed. To include quantum effects, the Multi-Valley Effective Conduction Band Edge (MV-ECBE) method has been used. This approximation, specially developed to be implemented in EMC tools, takes into account the effects of an arbitrary effective mass tensor describing the characteristics of the silicon conduction band valleys and the confinement directions [3].

3. Simulation Results and Discussion

It has been observed that the quasi-ballistic regime does not depend exclusively on the channel length and other geometrical issues. It is possible to obtain the same degree of nanoballisticity for different channel lengths by tuning the applied bias (i.e. V_G and V_{DS}) [2]. Effective ballisticity (defined as the ratio between drain currents for pure ballistic and diffusive devices) tends to the ballistic limit when the lateral field is increased for a given gate voltage. As the kinetic energy of the carriers increases, the total scattering rate is also higher (mainly due to the contribution of phonon scattering) [4]. It is observed then a reduction in the intrinsic ballisticity, B_{int} (i.e. ratio of electrons injected in the source contact that reach the end of the channel without being scattered). However the source-to-drain transit time is also reduced. Therefore, the amount of scattering events is not large enough to modify significantly the carrier velocity. Note that the transport is not purely ballistic but quasi-ballistic. At very low drain bias conditions, the situation is quite different as suggested earlier [5]. The scattering probability is drastically reduced due to the small lateral field applied. Therefore, it would be possible to enhance the intrinsic ballisticity if the carrier transit time is not too long compared to the relaxation time. When the drain voltage is increased, B_{int} also grown as shown in Fig. 1 for 6nm thick and 15nm length DG and SG devices. This means that the transit time decreases faster than the increase of the scattering rate. In other words, the mean number of scattering events decreases (Fig. 2), leading to enhanced B_{int}. This behavior stands until the carrier energy becomes large enough to trigger additional scattering events. This point coincides with the maximum of Fig. 1 and the plateau in Fig. 2 (15-20mV). From this point, the transport regime corresponds to the afore mentioned standard case of moderate lateral fields [2]. This ballisticity peak, which

reflects the balance between transit time and relaxation time, depends on the inversion charge as shown in Fig. 1. It can be observed how this peak is shifted to higher V_{DS} as the inversion charge is reduced and its position coincides for DG and SG structures when the same inversion charge is considered. The differences on B_{int} for DG and SG with the same inversion charge can be attributed to coupling effects between channels (volume inversion). As the silicon thickness is increased, Fig. 3, DGSOI tends to behave as two parallel SGSOI transistors and therefore, B_{int} approaches for both structures at identical gate bias. Further simulations will show the effects of channel length and surface roughness scattering in intrinsic ballisticity.

4. Conclusions

This work presents an interesting facet of nanoballisticity in advanced SOI MOSFETs at very low drain bias conditions. Quantum-corrected Monte Carlo simulations clearly show that the intrinsic nanoballisticity increases with the drain-to-source voltage for very low bias conditions. For higher values, the typical behavior for moderate lateral field is recovered and the scattering becomes more important decreasing the ratio of pure ballistic electrons. It has been observed how the ballisticity peak depends on the inversion charge and channel coupling, recovering the SG behavior when parallel channels are decoupled in DGSOI devices. These results infer that experimental evidence for ballistic transport may be obtained more easily at low drain bias.

5. Acknowledgements

This work has been supported by the EU in the frame of EUROSOI+ network, by the Spanish Government project FIS-2005-6832 and Junta de Andalucía Project TIC-00831.

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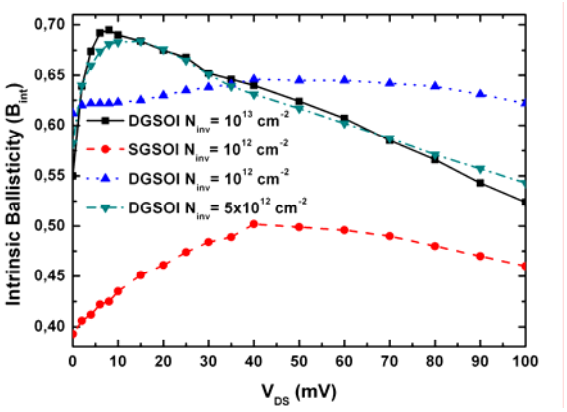

Fig.1: *Intrinsic ballisticity for 15nm channel length SG and DG devices for different values of inversion charge. Note how the ballisticity peak appears for the same drain voltage in SG and DG devices when the inversion charge fits.*

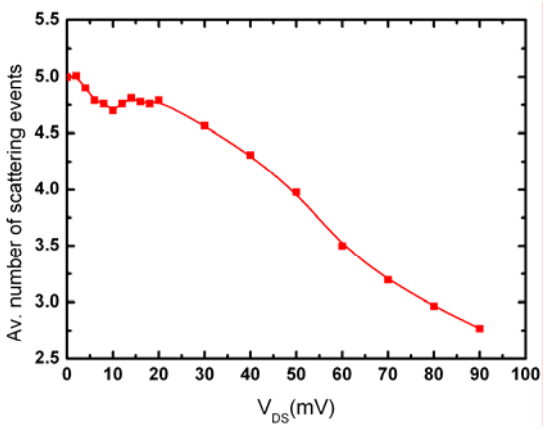

Fig.2: *Average number of scattering events at the end of the DGSOI channel. A decrease of this value means a quasi-ballistic behavior for moderate bias conditions.*

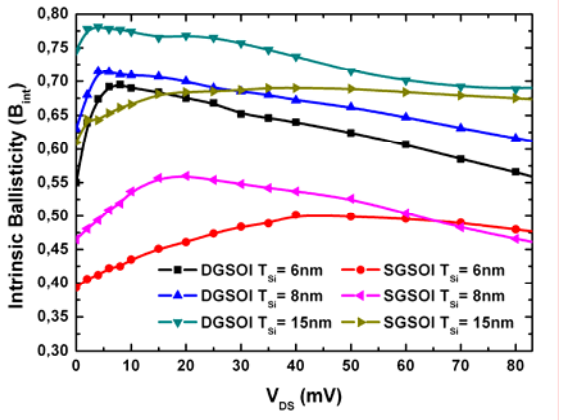

Fig.3: *Intrinsic Ballisticity for 15nm channel length DG and SG devices and silicon thicknesses varying from 6 to 15 nm.*

Ultra Scaled MultiGate SOI MOSFETs: Accumulation-Mode *vs.* Inversion-Mode

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Tyndall National Institute,Lee Maltings, Prospect Row, Cork, Ireland

1. Abstract

The performances of accumulation-mode and inversion-mode Multigate FETs in ultra scaled devices are compared through device simulations. We show that for sub 10nm cross dimensions, device performances (subthreshold slope, threshold voltage…) depend mainly on cross section size and bias voltage and very little on channel doping.

2. Introduction

In a continuous effort to increase current drive and better control short-channel effects, device dimensions are shrunk. As well, silicon-on-insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multigate structure. Like with classical single-gate SOI MOSFETs, it is possible to fabricate accumulation-mode (AM) and inversion-mode (IM) Multigate FETs. Here, we study through device simulations the impact of channel doping and geometry on the properties and performances of both types of devices in ultra small SOI devices.

3. Device Modelling

We have developed a 3D ballistic quantum simulator based on the non-equilibrium Green functions using the Comsol Multiphysics software and on an implementation of the fast uncoupled mode space (FUMS) approach [1]. The main loop of the program self-consistently computes the electrostatic potential in the device, V_1, by solving Poisson equation and the electron concentration, n_1, using the non-equilibrium Green functions (NEGF) [2]. As we use a mode space approach, the coordinates *y* and *z* of the cross section perpendicular to the transport direction, *x*, of the device are replaced by the mode energies $E_m(x)$ of the electronics subband in the devices. This drastically reduces the computational budget as in practice only the first few subbands are occupied by electrons and need to be calculated [1]. If *M* is the number of subband occupied, we then only have to solve *M* times a 1D NEGF problem along the x-direction instead of a full 3D problem, which is much faster. We have, however, to provide the subband energy profile $E_m(x)$ and the related wave functions $\Psi_m(x,y,z)$. This is done by solving a 2D Schrödinger problem in the cross section of the device. The computation algorithm is summarized in Fig.1.

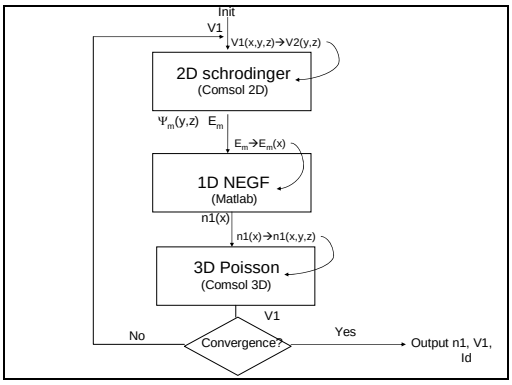

Fig. 1: *Computation algorithm for device simulation.*

4. Simulation Results

With this simulator, we can design and study the performances of both AM and IM Multigate SOI MOSFETs. In Fig. 2, 3 and 4, we clearly see the influence of the cross section size on the channel shape and location in the body of triple gate (trigate) devices. For cross sections smaller than 5x5 nm^2, there is mainly one single central channel in the device as the quantum confinement effect prevails and most of the electrons are in the first energy subband. When the cross section is increased, the quantum confinement effect is balanced by the electrostatic attraction of the gates, which tends to create two channels at the top near the corners. This effect is more pronounced above threshold as the gate voltage is increased (Fig. 3). In that case, the maximum of the first wavefunction is no longer located in the center but more near the top corners. Moreover, the electrons also occupy higher order subbands. This is related to the fact that the subbands are closer in energy from each other due to the increased cross section size.

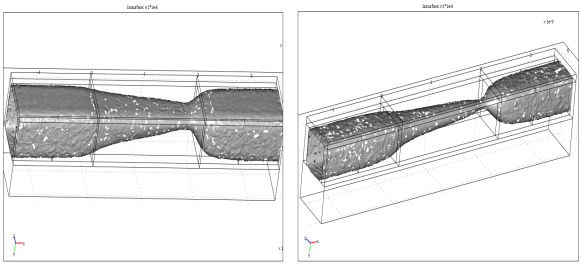

Fig 2: *Electron concentration, n, isocontours at threshold ($n=5x10^{18}cm^{-3}$) in n-channel AM trigate FETs with $t_{si}=W_{si}=7nm$ (Left) and $t_{si}=W_{si}=5nm$ (Right).*

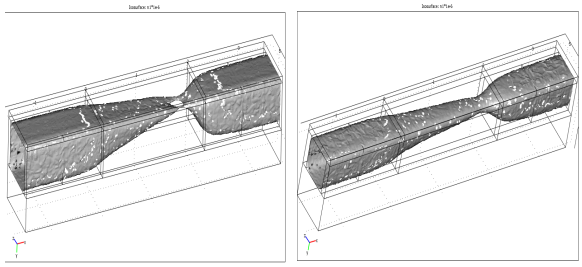

Fig 3: *n isocontours 0.2V above threshold in n-channel AM trigate FETs with $t_{si}=W_{si}=7nm$ ($n=1x10^{19}cm^{-3}$) (Left) and $t_{si}=W_{si}=5nm$ ($n=7.5x10^{18}cm^{-3}$) (Right).*

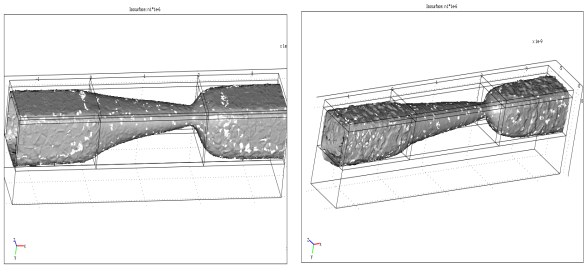

Fig 4: *n isocontours at 0.2V below threshold in n-channel AM trigate FETs with $t_{si}=W_{si}=7nm$ ($n=2x10^{18}cm^{-3}$) (Left) and $t_{si}=W_{si}=5nm$ ($n=1x10^{18}cm^{-3}$) (Right)*

I_D-V_G curves for different channel doping and operation modes are shown in Fig. 5 for $t_{si}=W_{si}=5nm$ and $t_{si}=W_{si}=7nm$. The figure shows that the doping (type and level) does not have a major impact on the IV characteristics, at least in the ballistic regime. For very small channel dimensions, the electrostatics control from the surrounding gate seems much higher than the one from the doping impurities. The shape of the electron channel and the subthreshold slope show very little dependence on the channel doping and the doping type. On the contrary, the electron distribution is influenced by the cross-section size and the backgate voltage. The simulated subthreshold slopes are 92 and 96 mV/decade for the 5x5 and 7x7nm^2 nanowires respectively, independently of the doping. These high values could be due to short-channel effects (L=20nm). The threshold voltage does not change from its intrinsic value up to a doping of $10^{18}cm^{-3}$ whatever the mode is. Then it experiences a symmetrical shift, positive for AM and negative for IM that is reduced for smaller cross section. For a backgate voltage of -2.5V and a buried oxide thickness of 5nm, the intrinsic threshold voltage for the 5x5 nm cross section nanowires is around 0.4V. The shift at $10^{19}cm^{-3}$ is equal to 65mV. For the 7x7 nm cross section nanowires, the intrinsic threshold voltage is around 0.1V. The shift at $10^{19}cm^{-3}$ is equal to 100mV.

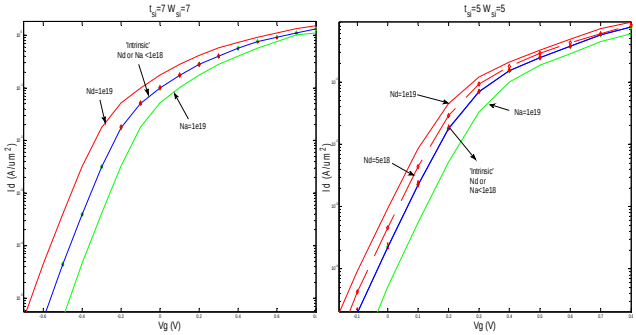

Fig 5: *Simulated I_D-V_G curves vs. channel doping (cm^{-3}) in AM and IM trigate NFETs with $t_{si}=W_{si}=7nm$ (Left) and $t_{si}=W_{si}=5nm$ (Right).*

4. Conclusions

We have developed an accurate but time efficient 3D ballistic quantum simulator that is based on the non-equilibrium Green functions using the Comsol Multiphysics software. This has allowed us to investigate and compare the performances of accumulation-mode and inversion-mode Multigate FETs in ultra scaled devices through device simulations. We have shown that in ultra scaled devices, device performance factors such as subthreshold slope and threshold voltage mainly rely on cross-section size and bias voltage and very little on channel doping. This is true for both AM and IM transistors. Non-intentionally doped AM devices, with doping resulting from the diffusion of dopants from source and drain are then a very interesting candidate for future digital applications, as controlling the doping in IM device could be an issue due to the small dimension and number of doping atoms to implant.

Acknowledgements

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SESSION 4

Active RF Devices

CHAIR
D. Lederer
Tyndall National Institute

Silicon-on-SiC hybrid substrate with improved high-frequency and thermal performance

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1. Abstract

A novel SOI hybrid substrate consisting of silicon-on-silicon carbide is presented. The substrate opens up new possibilities for silicon-based RF and power devices, as well as for heterogeneous integration, such as silicon and SiC devices combined on the same chip. The semi-insulating properties and the high thermal conductivity of the SiC-substrate enable SOI technology with low substrate RF-losses and reduced device self-heating. MOS transistors manufactured on the hybrid substrate show very good electrical performance and no self-heating compared to ordinary SOI-material. Furthermore, RF-measurements up to 30 GHz show more than a factor of ten lower substrate losses.

2. Introduction

A new Si-on-SiC hybrid substrate for high performance SOI was recently presented by our group [1]. The feasibility of the concept was demonstrated by manufacturing of MOSFET devices on the material. That was the first ever demonstration of this technology. In this paper further characterization results of the substrate are presented, such as high frequency measurements and thermal data.

The direct bonded hybrid substrate uses polysilicon as an intermediate layer, thereby eluding the thermally unfavourable SiO_2 [2]. The MOSFET characteristics as well as the absence of self-heating effects are shown and are benchmarked against devices on commercially available epitaxial and SOI wafers, as well as Si-on-poly-SiC (SoPSiC, PicoGiga). Previous efforts to improve the SOI thermal properties by replacing the SiO_2 insulator have included diamond [3], AlN [4], and Al_2O_3 [5].

3. Experimental

A 2" 4H-SiC wafer (SiCrystal) was used as substrate wafer. In order to improve the quality of the bond, 200 nm of amorphous silicon (α-Si) was deposited with LPCVD. The Si device layer (330 nm) was obtained from a commercial 4" SOI wafer (Soitec). This layer was patterned with a grid mask, thus creating square Si islands separated by channels which provide escape paths for water. These two wafers were rendered hydrophilic, put on top of each other (Fig. 1) and thermally annealed at 1000°C in N_2 to create a strong bond. The SOI handle wafer was removed with TMAH etchant, and the buried oxide with an HF solution. The new hybrid wafer had a surface roughness of 2 nm rms, as measured with AFM.

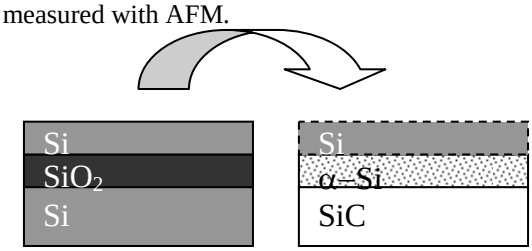


Fig.1: *Bonding process of the BaSiC hybrid wafer.*

This hybrid wafer is referred to as BaSiC. NMOS devices were processed using standard MOS process (B & P implants), with a substrate doping of 10^{17} cm^{-3} and 120 Å of gate oxide. Dopants were activated with a 900 °C thermal reoxidation and device isolation was attained with TEOS, with a final FGA at 400ºC (N_2/H_2). Gate lengths ranged from 1-20 μm. Reference devices (4" epi-Si (100), SOI (100), and SoPSiC (111)) were also manufactured with an identical process flow. Furthermore, thermal test structures were also manufactured on the substrates. The final BaSiC wafer is shown in Fig. 2.

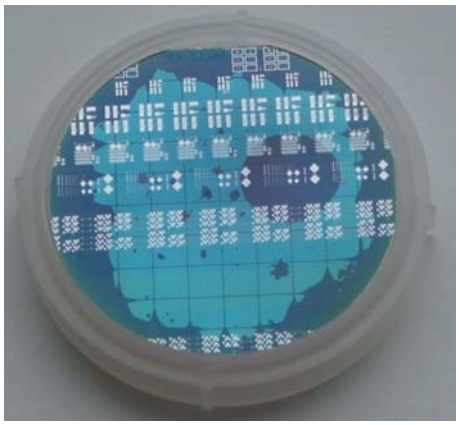
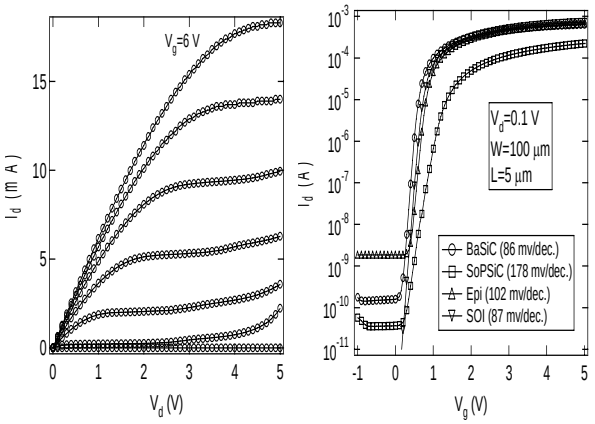


Fig.2: *BaSiC wafer with MOS transistors and test structures.*

4. Results

The I_d-V_d characteristics of a typical BaSiC device are shown in Fig. 3a, illustrating excellent current drive (the same as for the SOI and epi reference wafers). The sub-threshold slopes, measured in the linear region at V_{ds}=0.1 V are shown in Fig. 3b. Very little difference between SOI and BaSiC is seen, with values around 80-100 mV/dec.



a) b)

Fig.3: *a)I_d-V_d curve traces from long-channel (5 µm) BaSiC device in V_g increments of 1 V. b) I_d-V_g curves measured in the linear region (V_d=0.1 V). Note similar I_{off} for BaSiC/SOI.*

The thermal advantage of the BaSiC is demonstrated when the dissipated power is increased in the MOS transistors, see Fig. 4. As expected, self-heating does occur for the SOI reference but not for the BaSiC. Furthermore, the effective thermal resistance of the different substrates was estimated using heating resistors. The temperature increase as a function of power density is seen in Fig. 5 for the BaSiC and the SOI reference. A factor of two difference in effective thermal resistance is observed, which is in good agreement to results on similar structures [2].

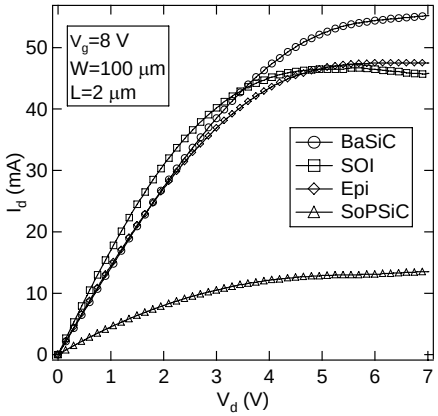


Fig.4: *I_d-V_d at high voltages. $I_{d,sat}$ (SOI) drops due to self-heating effects.*

In terms of RF performance, Fig. 6 describes the relative resistive substrate losses. The equivalent parallel resistance is significantly higher for BaSiC compared to SOI and SoPSiC, measured on an open-pad structure for a wide frequency range up to 30 GHz. In fact the resistance measured on the BaSiC is the conduction in the surface silicon film, since the SiC substrate behaves semi-insulating, as expected. Interestingly, low substrate loss has also been shown for poly-SiC [6].

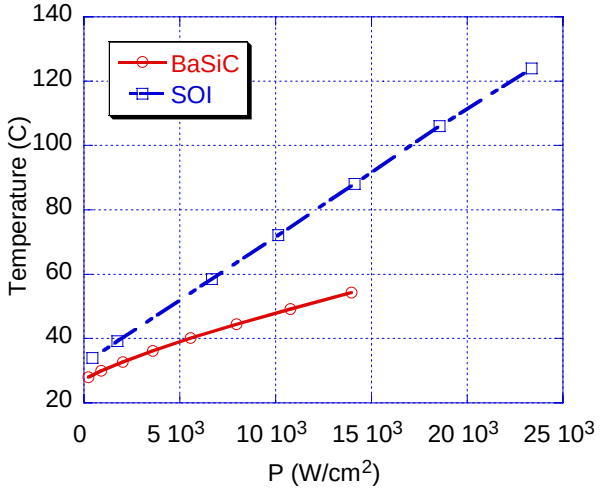


Fig.5: *Measured temperature as a function of applied power density for BaSiC and SOI substrates.*

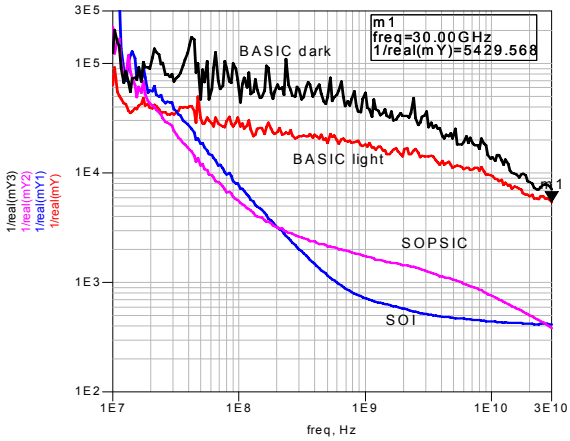


Fig.6: *Network vector analyzer measurements of the hybrid substrate in light*

5. Conclusions

A new Si-on-SiC hybrid substrate has been demonstrated. MOS transistors were manufactured in the substrate and showed very good electrical performance. The low thermal conductivity of SiC results in an effective thermal resistance a factor of two lower than the SOI reference. Due to the semi-insulating properties of the SiC, the BaSiC hybrid substrate has very low losses at high frequency as compared to the SOI and SoPSiC reference substrates.

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High-Temperature RF Behavior of Partially-Depleted SOI MOSFET Transistors

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1. Abstract

This work presents the high temperature DC and RF behaviors of Partially-Depleted SOI MOSFETs. Standard equivalent circuit and extraction methodologies are used to show an interesting stability of performance with temperatures as high as 250°C.

2. Introduction

High temperature is a large value market that has been difficult to serve until now. Automotive electronics, on-engine and on-transmission applications require maximum temperatures of up to 200°C, with the wheel-mounted applications going even higher. In previous published works [1], high temperature DC behavior has been considered. In this work, RF behavior at high temperatures, up to 250°C is presented for two Partially-Depleted SOI structures, which are Floating-body (FB) transistors; where the body is not connected and body-tied (BT) transistors; where body and source are shorted together by a silicided contact. In addition, parameters extraction of a small-signal equivalent circuit is presented for temperatures ranging from 25 to 250°C and frequencies ranging from 40 MHz to 40 GHz. Measured transistors feature 30 gate fingers of 2 µm wide each connected in parallel, on a 130 nm High-Resistivity SOI CMOS technology.

3. High-Temperature DC Behavior

Figure 1 shows the degradation of threshold voltage V_{th} and subthreshold slope S with temperature. A 43% decrease with temperature in threshold voltage is noticed for both FB and BT transistors with a severe degradation of subthreshold slope nearly doubling its value at 250°C compared to room temperature. This is very critical for digital circuit designers. On the other hand, the BT transistor shows much higher ON to OFF current ratio than FB transistor, but it also degrades faster with temperature as shown in Fig. 2. This is related to a higher degradation scheme of OFF current of BT transistor. A very interesting advantage of BT transistor over FB transistor is shown in Fig. 3 and 4 where the ZTC points are noticed at higher V_{GS} for BT transistor for both drain current and transconductance measured at V_{DS} = 1.2 V. This ensures an operation of transistors in ON mode at the ZTC point, at higher overdrive voltage and then giving higher drive current which is quite important for designing analog circuits working under high temperature environments. On the other hand, a suppression of the kink effect at higher temperatures shown in Fig. 5, promotes FB transistors to work at harsh environments without problems arising from floating body effects.

4. High-Temperature RF Behavior

As the temperature increases, the cut-off frequency f_T of both transistors decreases as shown in Fig. 6, with a slightly different slope, reaching about 75% of its maximum value at room temperature for FB transistor and about 79% for BT transistor. The extraction of the extrinsic resistances R_{ge}, R_{de} and R_{se} is done using the cold FET method proposed by Bracale *et al.* in [2] and applying the $\omega^2 Re(Z_{ij})$ versus ω^2 method proposed by G. Crupi *et al.* in [3] to minimize the frequency dependence of $Re(Z_{ij})$ associated to an incomplete capacitance de-embedding and/or intrinsic capacitive effects. Fig. 7 shows the extraction results and it is worth notice that there is nearly no change in R_{de} and R_{se} and a slight increase of R_{ge} with temperature. The intrinsic elements are extracted using the equivalent circuit (Fig. 8) and the direct extraction method in saturation region introduced by Raskin *et al.* in [4]. Results, shown in Fig. 9 and 10, show nearly constant behavior with temperature for all intrinsic capacitances and for output conductance. FB transistor shows lower C_{gs} thus higher f_T than BT transistor. Also FB shows lower C_{ds} than BT due to the shorted body-source in the case of BT transistor. Knowing that $f_T = G_m/2\pi(C_{gs}+C_{gd})$, the slight difference in f_T degradation vs. temperature between both devices comes from mainly the different decrease of intrinsic transconductance as shown in Fig. 10, where BT transistor degrades slightly faster than FB transistor.

5. Conclusion

This work presents RF behavior of PD SOI MOSFETs in high-temperature environment up to 250°C. Although severe degradation in most of DC performance figures of merit are shown, besides a noticeable degradation of cut-off frequency, still the extraction of the equivalent circuit and extrinsic resistances shows quite a stable RF performance with temperature giving an important advantage for RF circuit designers with some tradeoffs between FB and BT transistors.

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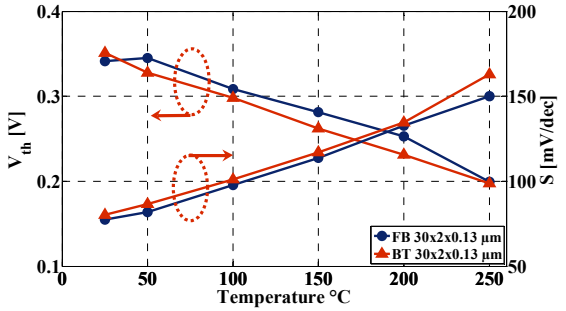

Fig. 1: *Variation V_{th} and S with temperature.*

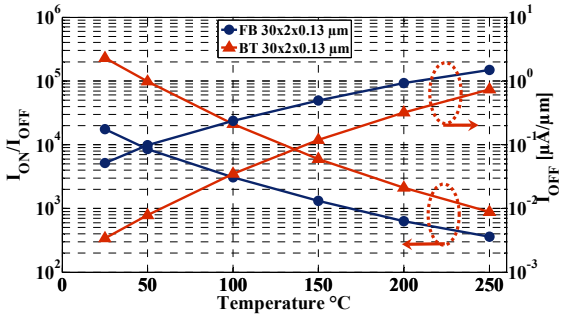

Fig. 2: *Variation of I_{ON} – to – I_{OFF} ratio with temperature.*

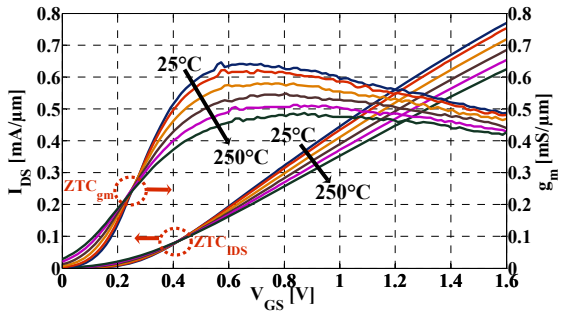

Fig. 3: *I_{DS}, g_m and ZTC points for FB transistor in saturation.*

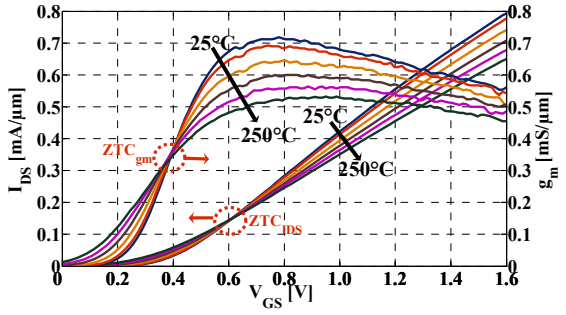

Fig. 4: *I_{DS}, g_m and ZTC point for BT transistor in saturation.*

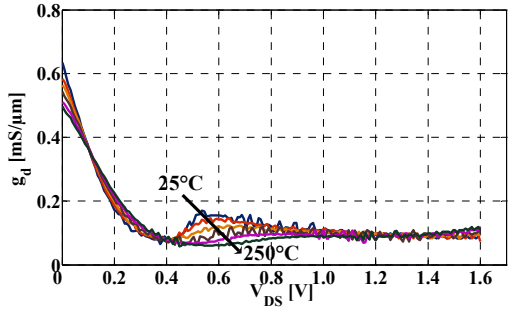

Fig. 5: *Variation of g_d with temperature for FB transistor.*

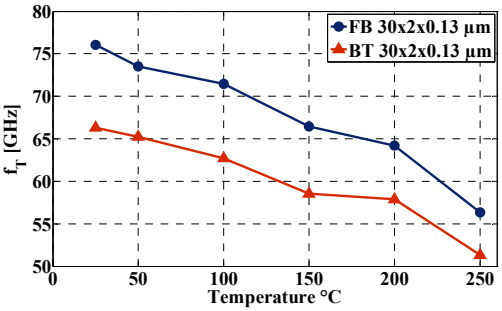

Fig. 6: *Variation of cut-off frequency with temperature.*

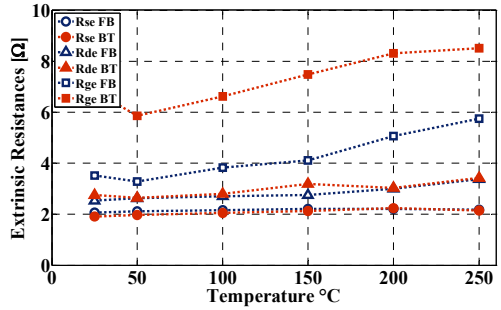

Fig. 7: *Variation of extrinsic resistances with temperature.*

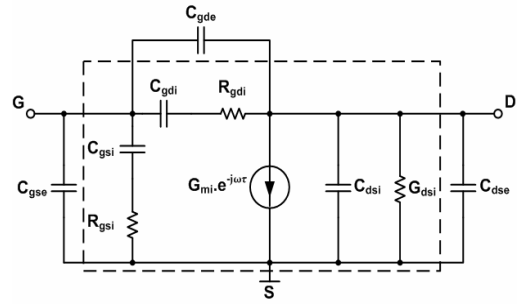

Fig. 8: *Small Signal equivalent circuit.*

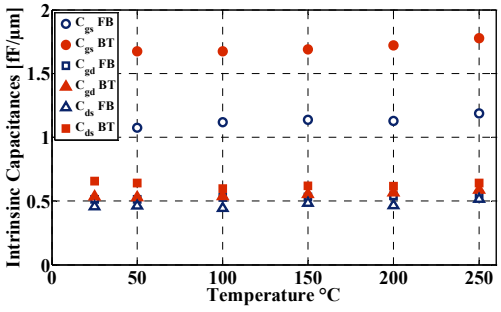

Fig. 9: *Variation of intrinsic capacitances with temperature, $C_{gs} = C_{gsi}+C_{gse}$, $C_{gd} = C_{gdi}+C_{gde}$, $C_{ds} = C_{dsi}+C_{dse}$.*

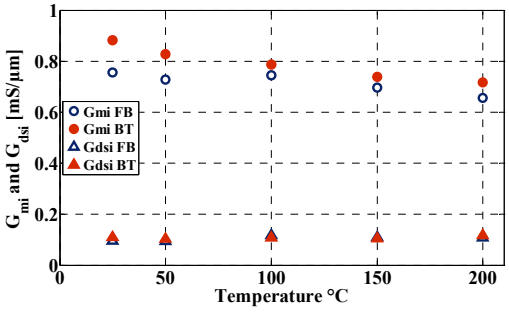

Fig. 10: *Variation of G_{mi} and G_{dsi} with temperature.*

RF Behavior of Strained Fully Depleted SOI MOSFETs

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1. Abstract

Using a Four-Point bending setup the DC and RF characteristics of Fully Depleted SOI MOSFET transistors are analyzed under different stress conditions. We show that the change in the transistors' characteristics is mainly due to the variation of mobility which increases with stress and entails a change in the channel resistance. This effect is visible in DC as a change in the drain current or in RF as a change in the cut-off frequency of the transistor. As far as we know four-point bending has never been coupled to RF characterization.

2. Introduction

The effects of stress on the behavior of semiconductors have been known since a long time now, and have been used as electromechanical transducers in many sensor applications [1] and to enhance the transport properties in advanced sub-micron MOSFETs these last years [2]. The main effect of stress (or strain) is the change of carrier's mobility, through the change in the effective mass and sub-band splitting [2]; this can be readily understood as a piezo-resistive effect where the total resistivity of a semiconductor changes under stress.

Strained MOSFETs have been used to improve the performance of VLSI circuits by subjecting nFETs to tensile longitudinal stress and the pFETs to compressive longitudinal stress; this is usually done by a stressing SiGe epitaxial layer for tension and by a SiN capping layer for compression [2].

The effect of strain in MOSFETs has been rarely characterized in the RF regime [3], and as far as we know there is no publication related to the use of a four-point bending setup to characterize the RF behavior of MOSFETs under mechanical stress. Here, we use such measurement setup to study the DC as well as the RF properties of strained MOSFETs. Based on a small-signal equivalent circuit the variation of the gate transconductance (G_m), the total gate capacitance (C_{gg}) and the cut-off frequency (f_T) of a Fully Depleted pMOSFET are extracted as a function of strain.

3. Experimental setup

On-wafer four-point bending setups have been used to thoroughly study the DC behavior of MOSFETs [4].

The interest here is the ability to apply exactly the desired amount of stress whether tension or compression and to observe directly the variation of the DC and RF transistor's properties.

Our tested transistors are Fully Depleted SOI pFET with 12 gate fingers of 6.6 µm width and a channel length of 0.25 µm. The body thickness is 30 nm and the contacts are made of nickel silicide.

The four-point bending applies a bending moment to a sample or wafer as shown in Fig. 1, depending on the design it is possible to achieve either tension or compression. In our case the setup was used to apply transversal tensile stress (perpendicular to the Source-Drain current). Due to the present limitations of the setup the stress was kept below 30 MPa. The stress in a four-point bending setup is quantified by the following relation [4]:

$$\sigma = \frac{3.E.d.t}{2.a^2} \qquad (1)$$

Where σ is the stress measured in Pa, E is the sample's Young's Modulus, d is the maximum displacement due to stress, t the sample thickness, and $2.a$ is the distance between the internal contact points. Displacement was measured to micrometer precision with a displacement detector, still d measurement is probably the biggest single contributor of error in stress estimation.

RF Measurements were done using a Vector Network Analyzer (VNA) from 40 MHz up to 40 GHz.

4. Results and Discussion

The DC effects are summarized by a change in the channel resistance; this will be seen as a change in I_{DS} current (ΔI_{DS}) but also as a change in the channel transconductance G_m. The change in current is linearly proportional to the applied stress, however the change for a certain drain voltage V_{DS} increases as the gate voltage V_{GS} approaches the threshold voltage V_{th} as shown in Fig. 2. This sudden increase of the ΔI_{DS} close to the V_{th} could be related to a slight change of V_{th} with stress or also linked to an inaccuracy of a few mV on the V_{th} extraction. Also the change in the channel resistance can be seen as a change in the DC transconductance G_m, this is plotted versus stress values in Fig. 3.

The transistor's RF properties also vary with stress since the cut-off frequency f_T is dependent on mobility through G_m and is approximated by $f_T = G_m/2\pi C_{gg}$. Using the small signal equivalent circuit shown in Fig. 4 the RF intrinsic values of transconductance (G_{mi}) have been extracted using Bracale's method as detailed in

[5], these are shown in Fig. 5. The relatively low cut-off frequency enabled the direct measurement of f_T without need for extrapolation. The variation of f_T with stress is shown in Fig. 6. The observed variation in f_T (1.4%) is lower than that in G_m (2%), the explanation would be a variation in C_{gg}. In Fig. 7, an increase of C_{gg} is indeed extracted with the applied stress. However, Singh *et al.* [3] reported a constant behavior of C_{gs} as a function of stress. The variation of C_{gg} shown in Fig. 7 could be related to a real change in channel capacitance caused by a change in the charge distribution in the transistor channel or to an error induced by the setup itself or for instance the re-probing. The low applied stress values imply a small change in the transistor's parameters, and then could lead to a higher sensitivity to measurement inaccuracy. Currently measurements at much higher stress values are under consideration.

5. Conclusion

Using a four-point bending setup a pFET under different stress conditions was measured, DC and RF characterizations were performed. We showed that there indeed is a change in the RF behavior of the transistor that can be due to the increase in the channel transconductance G_m, but we also observed a change in C_{gg}. Detailed measurements are currently under way on FD-SOI and other devices (Partially Depleted, Bulk, FinFETs, etc) in order to analyze the reative impact of mechanical strain on several MOS technologies.

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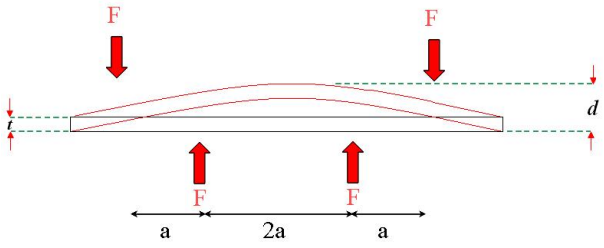

Fig. 1: *Representation of a four-point bending setup.*

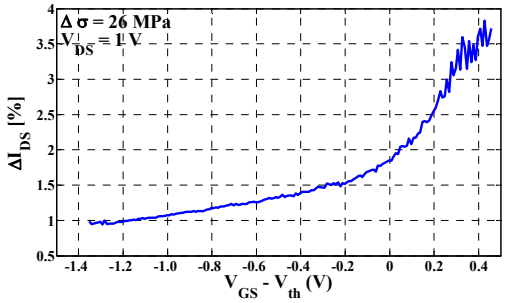

Fig. 2: I_{DS} *variation due to the application of 26 MPa as a function of gate overdrive.*

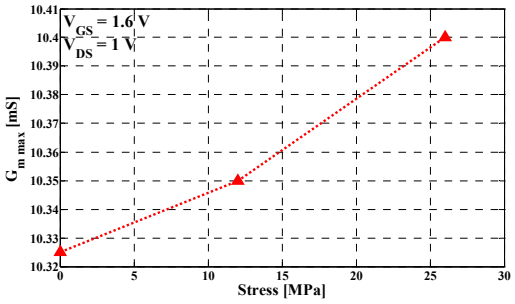

Fig. 3: *Change in DC transconductance G_m as a function of stress.*

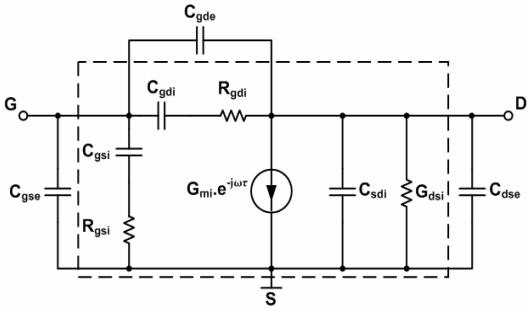

Fig. 4: *Small signal equivalent circuit for a MOSFET Cgs = Cgsi+Cgse, Cgd = Cgdi+Cgde, Cds = Cdsi+Cdse.*

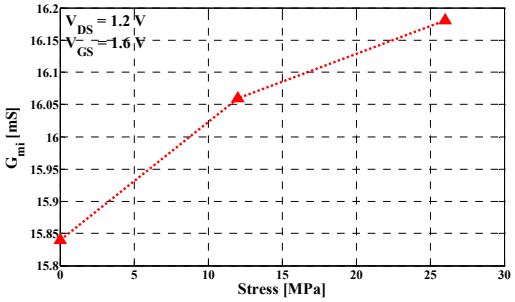

Fig. 5: *Change in extracted RF intrinsic transconductance G_{mi} as a function of stress.*

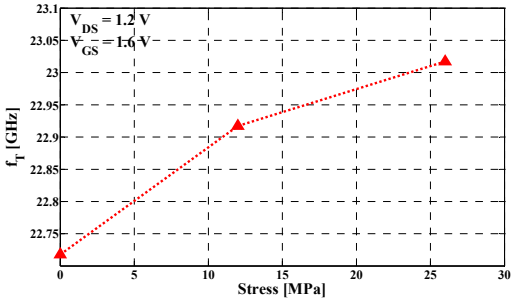

Fig. 6: *Change in cut-off frequency f_T as a function of stress.*

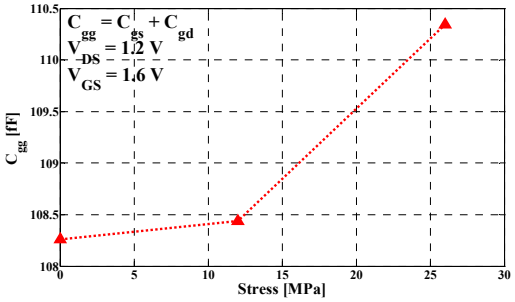

Fig. 7: *Change in C_{gg} capacitance as a function of stress.*

DC and RF characteristics of FinFET over a wide temperature range

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1. Abstract

DC and RF characteristics of n-type FinFET transistor over a wide temperature range, from 77 to 473K, are presented for the first time. We experimentally demonstrate that the impact of temperature on the main analog and RF factors of merit of FinFETs is similar to what it can be observed for classical deep submicron single gate MOSFETs.

2. Introduction

In recent years, FinFET transistors have received much interest thanks to the better immunity to short-cannel effects [1]. DC characteristics of FinFETs at high temperature were recently reported in [2]. RF characteristics of Bulk Si MOSFETs measured at low temperature (77K) have been presented in a few papers [3]-[4]. To the knowledge of the authors, the DC and RF characteristics, over a wide temperature range, of advanced MOSFETs such as FinFETs have not been reported in the literature yet. This is the aim of the present paper.

3. Device Description

Triple gate multifingered, 60-nm channel length, n-type FinFET, with 50 gate fingers and 9 fins per finger, is characterized. The fin width and height are of 32 and 60 nm, respectively. The device is fabricated on top of a 145 nm buried oxide. The gate stack includes 2 nm CET (Capacitance Equivalent Thickness) SiON, 5 nm MOCVD TiN metal gate and 100 nm-thick polysilicon. The channel is left undoped and HALOs are not implanted. Two measurement setups are used to perform the DC and RF characterization of the device under test: a cryogenic probe station for temperatures ranging from 70-300K and a high temperature chuck mounted with a classical RF probe station for the measurements of DC and high frequency parameters from 300-473K range.

4. DC and RF Characterization

Fig. 1 shows the threshold voltage (V_T) and the DC gate transconductance G_m as a function of temperature for a 60-nm n-type FinFET. As the temperature increases, the intrinsic concentration of mobile carriers (n_i) in the transistor channel increases leading to a reduction in the gate voltage needed to reach the strong inversion regime and then causing a linear reduction of V_T as observed in Fig. 1. For the transconductance G_m, its reduction with the temperature increase is mainly due to the mobility degradation. For bulk Si MOSFETs V_T^{77K}/V_T^{300K} ratios of 1.3 and 1.2 for 0.18 µm and 65 nm channel length, respectively, were observed in [3]-[4]. For 60 nm FinFET the ratio is of 1.4 for the temperature range (77/300K) and 2.4 for the temperature range 77-473K. Furthermore, the peak G_m^{77K}/G_m^{300K} ratio, in saturation was about 1.5 for both Si bulk transistors in [3]-[4] while it is 1.56 for FinFET in the same temperature range, and 2 for 77-473K range. Fig. 2 shows the subthreshold slope (S) as a function of temperature for a 60 nm FinFET. The measured S^{77K}/S^{473K} ratio is of approximately 0.33. Similar value has been obtained for Si Bulk MOSFET [3]-[4] from measurements made at low temperature.

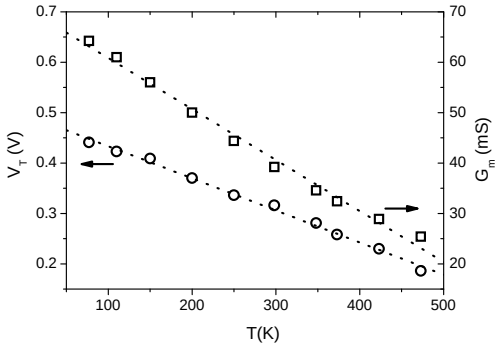

Fig. 1: *V_T and G_m as a function of temperature. G_m is measured at V_{DS}=1.1 V and V_{GS}-V_T=0.2 V.*

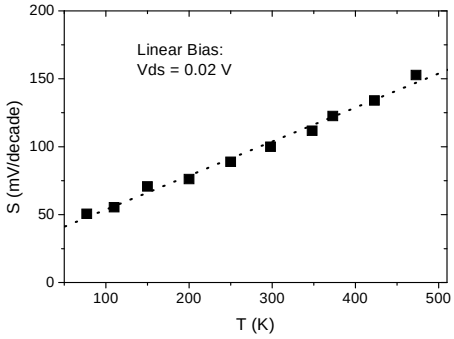

Fig. 2: *Subthreshold slope as a function of temperature.*

For the RF characterization, S-parameters are measured from 40 MHz to 65 GHz at various temperature conditions, from 77K to 473K. The coplanar pads and feed lines are withdrawn using on-wafer de-embedding

structures including an open test structure. Based on the small-signal equivalent circuit presented in Fig. 3 and specific extraction techniques [5]-[6], the intrinsic and extrinsic parameters are extracted for various temperatures. The extrinsic resistances were obtained in strong inversion (V_{DS}=0 V and various $V_{GS} > V_T$), by linear regression of Z-parameters vs. $1/(V_{GS}-V_T)$ [6]. Fig. 4 shows the extracted resistances as a function of temperature. R_d and R_s slightly increase with the temperature. As temperature increases the mobility is degraded, incrementing resistivity of the implanted and LDD regions. On the contrary, R_g is reduced as temperature increases, which could be related to a carrier mobility increment in the poly-Si region [7], or metal/Poly-Si interface effects, or even to an artefact of the extraction technique itself. Further investigations are needed to clarify this behaviour. After withdrawing the extrinsic resistances, the intrinsic parameters are extracted [5] in saturation (V_{DS}=1.1 V and V_{GS}=0.62 V). Figs. 5 and 6 show the extracted intrinsic transconductance (G_{mi}), output conductance (G_{dsi}) and capacitances, respectively. Fig. 7 shows the unit gain current frequency (f_t). It is worth noting that the intrinsic capacitances (C_{gsi} and C_{gdi}) in Fig. 5 are almost constant over the whole temperature range.

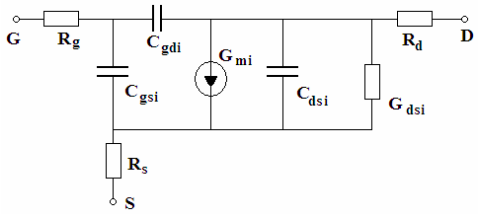

Fig. 3: *Equivalent circuit used for the parameters extraction. R_g, R_d and R_s represent the extrinsic series resistances.*

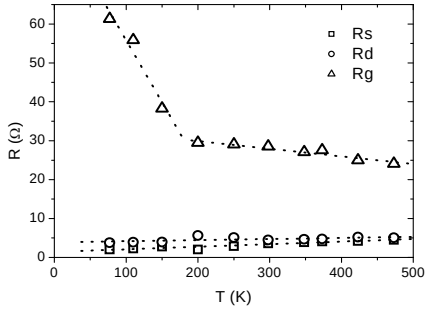

Fig. 4: *Extrinsic series resistances vs. temperature.*

Fig. 6 indicates the decrease of G_{dsi} and G_{mi} with temperature increase. The conductance reduction is related to mobility degradation. From Fig. 6, $G_{mi}^{77K}/G_{mi}^{300K}$ ratio is 1.5 and 1.9 for 77-473K range. For comparison purpose, $G_{mi}^{77K}/G_{mi}^{300K}$ ratios of 1.4 and 1.3 for 0.18 µm and 65 nm bulk transistors, respectively, are given in [4]-[5]. Finally, in Fig. 7 a 77/300K ratio of 1.3 on f_t is observed, which corresponds to an increment of 33%. Similar f_t enhancement has been reported in [3] for 65-nm Si Bulk MOSFET. At high temperature, the 300/473K f_t ratio of 60-nm FinFET shows the same value of 1.3, corresponding to a decrement of 23%. Recently, a cutoff frequency reduction of 21% has been measured for 130 nm Partially-Depleted SOI transistors [8]. f_t is directly related to G_{mi} variation versus temperature.

5. Conclusions

DC and RF parameters of a 60-nm FinFET are presented for a wide temperature range. The DC parameters show a strong thermal dependence, whereas for RF parameters, the intrinsic capacitances are nearly constant, and G_{dsi} and G_{mi} are temperature dependent. f_t shows an increment of 33% from 300 to 77K and a reduction of ~23% from 300 to 473K. The overall results show that FinFETs have a similar thermal behavior respectively to bulk and SOI technologies.

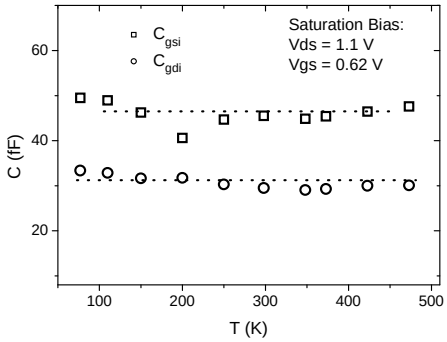

Fig. 5: *Intrinsic capacitances vs. temperature.*

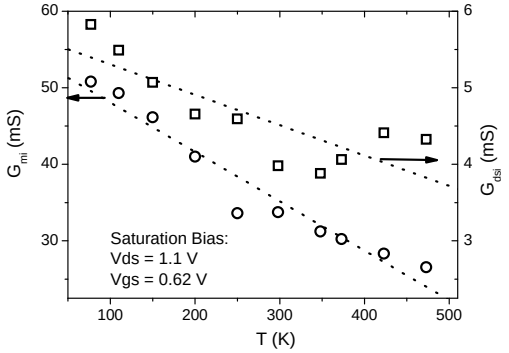

Fig. 6: *Intrinsic G_{mi} and G_{dsi} vs. temperature.*

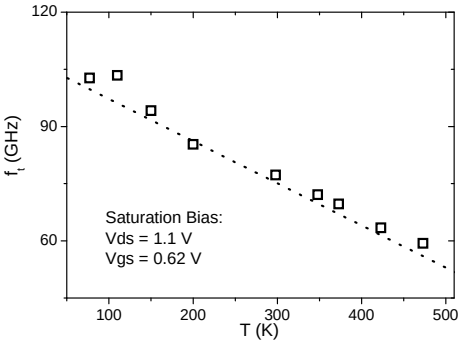

Fig. 7: *f_t vs. temperature.*

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POSTER SESSION

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Influence of Carrier Confinement on the Subthreshold Swing of Multigate SOI MOSFETs

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1. Abstract

The minimum energy of the first conduction subband varies with gate voltage in trigate SOI MOSFETs in subthreshold operation. In an inversion-mode device, the energy level of the lowest subband increases when the electron concentration increases, while it decreases under the same conditions in some accumulation-mode devices. As a result of this quantum effect, the subthreshold swing of accumulation-mode trigate FETs is smaller than predicted by classical theory, while that of inversion-mode devices is higher. This effect is not observed in FinFETs and GAA MOSFETs and can be amplified by modifying the device cross section.

2. Introduction

It has been previously shown that the minimum of the energy subbands increases in trigate FETs when the section of the device is reduced. Furthermore, in inversion-mode devices, the minimum energy of the energy subbands increases when the electron concentration is increased, which dynamically increases the threshold voltage as the inversion charge builds up. This effect reduces the current drive of the device and is not predicted by classical simulators. It also increases the value of the subthreshold swing, expressed in millivolts per decade, as the energy of the first subband increases with carrier concentration in subthreshold operation.[1] In this paper, we analyze this phenomenon in different type of multigate devices operating either in inversion or accumulation mode.

3. Device simulation

Two-dimensional simulations of FinFETs, trigate and GAA FETs have been carried out by solving the Poisson equation and the Schrödinger equation self-consistently.[1] Both inversion-mode and accumulation-mode N-channel devices were simulated. The gate oxide thickness, t_{ox}, is 2 nm and the buried oxide thickness, t_{BOX}, is 10 nm. The fin height, or silicon film thickness, t_{si}, is equal to the device width, W_{si}, in the trigate and GAA devices, and it is equal to $3\times W_{si}$ in the FinFET. There is no hard mask at the top of the FinFET, which is basically a trigate FET with a 3:1 height to width aspect ratio. The inversion-mode (IM) devices have a P-type doping concentration of 5×10^{18}cm^{-3} and the accumulation-mode (AM) devices an N-type doping concentration of 2×10^{19}cm^{-3}. Devices with a larger section (10nm×10nm for GAA and trigate devices and 10nm×30nm for the FinFET) were simulated as well and present the same characteristics as the 5nm×5nm and 5nm×15nm devices. The subthreshold curve, defined as $dV_G/d(log(I_D))$ plotted *vs.* V_G is shown in Figure 1 for the different devices, as a function of the average electron concentration.

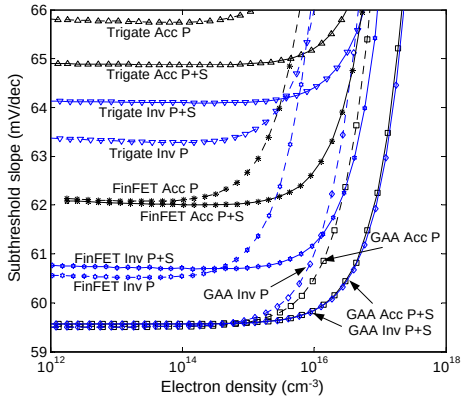

Fig.1: *Subthreshold swing in inversion-mode (Inv.) and accumulation-mode (Acc.) trigate FETs calculated using the Poisson equation (P) or a Poisson/Schrödinger solver (P+S).*

The subthreshold swing is defined as the value of S when the curves plateau, typically for electron concentrations below 10^{14} cm^{-3}. In the GAA device, the subthreshold swing reaches the theoretical limit of 59.6 mV/decade at T=300K. This is because there is no body effect in this device. In the FinFET, similar classical (P) and quantum (P+S) subthreshold swings are obtained. The subthreshold swing value is a little bit higher than in the GAA device because there is a non-zero body effect. The swing in the accumulation-mode device is larger than that in the inversion-mode device because the charge centroid of the AM device is in the centre of the devices (at a distance $W_{si}/2$ from the lateral Si/SiO_2 interfaces), while the charge centroids in the IM device are located at a smaller distance from the interfaces.[2] In the trigate device, the subthreshold swing is larger than in the two other devices because of a larger body effect.[3,4] More remarkably, the classical simulation overestimates the subthreshold swing in the accumulation-mode device, while it underestimates it in the inversion-mode device.

4. Discussion

Figure 2 helps understanding the discrepancy between the classical and quantum calculations in trigate devices. In the GAA device, where there is no back gate and, therefore, no body effect, the shape of the potential distribution within the silicon remains unchanged as long as the device is in subthreshold operation, *i.e.* when the electron concentration is low. As a result, the minimum of the first energy subband stays constant as long as the electron concentration is below 10^{17} cm^{-3}.

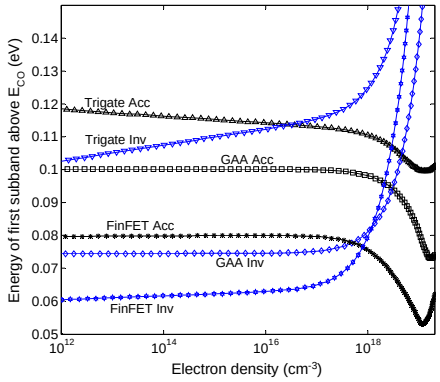

Fig.2: *Minimum energy of first subband vs. average electron concentration in inversion-mode (Inv.) and accumulation-mode (Acc.) trigate FETs calculated using the Poisson equation (P) or a Poisson/Schrödinger solver (P+S).*

The increase or decrease of the energy level is related to the "compression" or "decompression" of the electron gas, represented by the $-\frac{\hbar^2}{2m}\nabla^2\Psi$ term in Schrödinger's equation. To illustrate this we simulate a special structure with an electron "reservoir" below the silicon fin (Figure 3).

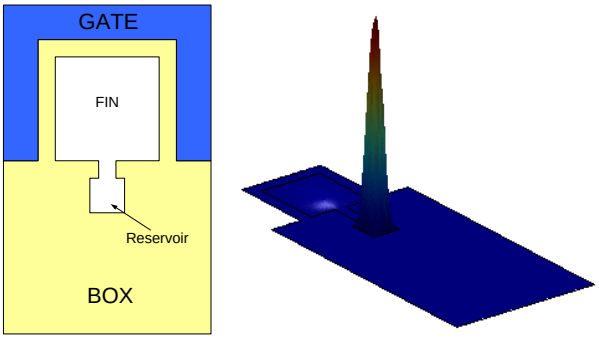

Fig.3: *Accumulation-mode MuGFET with an electron "reservoir" below the Fin (right). Electron concentration at V_G=-0.5V (left).*

At low gate voltage the electron wavefunctions are compressed in the small volume of the reservoir, which creates relatively high subband energy levels. As the gate voltage is increased, the wavefunction "move" towards the fin, where they are "decompressed", and the energy values decrease (Figure 4). At very high gate voltage, the wavefunctions are again "compressed" in two peaks near the top of the fin, and the energy increases again.

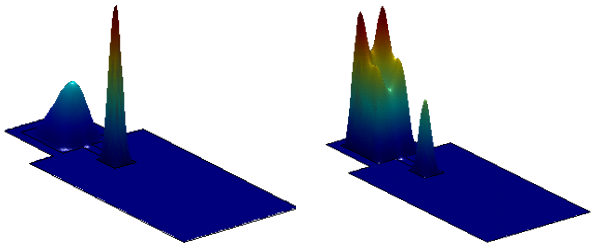

Fig.4: *Electron concentration at V_G=0.0V (left) and +0.9V (right).*

The energy of the first subband is shown in Figure 5 in the accumulation-mode device with a "reservoir", as a function of electron density. It decreases when the electron gas is "decompressed" and increases when it is "compressed". The effect on this energy reduction on the subthreshold slope curve can be seen in Figure 6, where the classical and quantum simulations are compared.

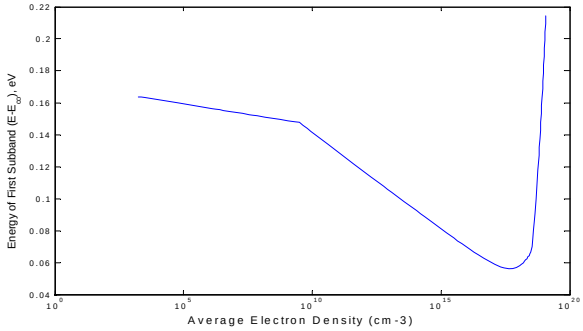

Fig.5: *Energy of first subband vs. electron concentration.*

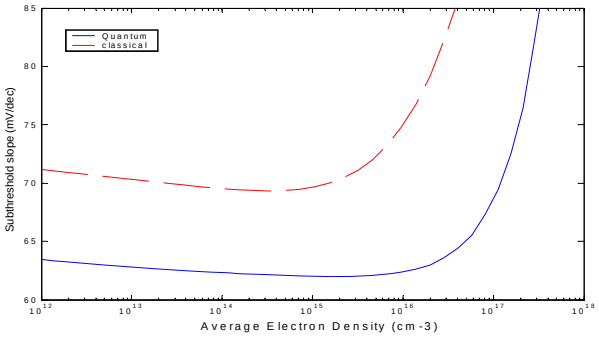

Fig.6: *Subthreshold curve vs. electron concentration.*

5. Conclusions

Electron wavefunction "compression/decompression" is shown to worsen/improve the subthreshold slope of MuGFETs, respectively.

Acknowledgements
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Triode-like Non-Saturation Characteristics of SOI-MOSFETs under Reverse Drain Bias

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1. Abstract

New operation mode of SOI-MOSFETs is proposed for better input-output linearity and analog signal transmission. When the drain electrode is negatively-biased under the source grounded for an n-channel SOI-MOSFET, the channel pinch-off never occurs due to positive feed back of the reverse drain bias. Triode-like non-saturation characteristics are demonstrated with the experimental 0.1 μm channel SOI-MOSFET suggesting new additional advantages of SOI technology.

2. Introduction

SOI-MOSFETs are becoming more and more important for fabricating high performance system on a chip. Various 3-dimensional structures of SOI transistors have been proposed and developed as well as the conventional planar SOI devices. Current-voltage characteristics of those transistors are fundamentally the same as the conventional silicon bulk ones although various advantages are provided with SOI structures especially in deeply-scaled technology-nodes.

This paper reports on a new operation mode and its advantages of SOI-MOSFETs. The SOI-MOSFETs operate in a triode-like non-saturation mode which is favorable for various analog applications.

3. Device Operation

Figure 1 shows a schematic cross-section of the experimental n-channel SOI-MOSFET. The device is a partially-depleted thin SOI device. The special feature is the difference in channel formation; pinch-off free.

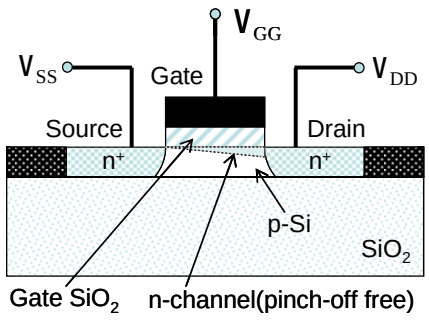

Fig.1: *Schematic cross-section of the experimental n-channel (pinch-off free) SOI-MOSFET*

A positive bias applied to the gate induces electrons at the SOI surface forming a channel while the source electrode is grounded. When the drain electrode is negatively-biased, the channel pinch-off never occurs due to the positive feed-back to channel modulation. The channel resistance decreases with increasing the negative drain bias. This feature is opposite to the conventional MOS transistor operation.

The drain current I_D in the basic gradual channel model is described as the following equation:

$$I_D = \beta\left\{(V_{GS} - V_T)V_{DS} - \frac{1}{2}{V_{DS}}^2\right\} \quad (1)$$

$$V_{GS} = V_{GG} - V_{SS}, \quad V_{DS} = V_{DD} - V_{SS} \quad (2)$$

where β is structure coefficient and V_T is threshold voltage. V_{GG}, V_{SS}, and V_{DD} are gate, source, and drain voltage, respectively. The equation indicates the triode region of the conventional operation behind pinch-off but remains essentially the same under the negatively-applied reverse drain bias conditions as well. This means lower drain resistance over wide drain voltages.

The transconductance g_m is given as,

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = \beta V_{DS}. \quad (3)$$

The g_m increases proportionally with V_{DS} while it is independent to V_{DS} with the conventional operation mode in saturation region.

Because the drain pn junction is positively-biased in this operation, the conventional MOSFET does not work. An SOI structure of which its body is electrically floating or linked to drain potential, however, suppresses the junction forward current. The source pn junction is reversely-biased, which fortunately acts as a leakage current stopper.

4. Device fabrication

The starting material was a p-Si(100) bonded SOI 150nm thick with buried oxide of 400 nm. After the gate oxynitidation with thickness of 2 nm, the poly Si gate was deposited and patterned by EB lithography. The gate length and width were 0.1 μm and 5 μm, respectively. The source and drain regions were ion implanted with arsenic and phosphorus for extension

and deep n^+ regions, respectively. Salicidation process with Co was used to reduce sheet resistances on the source, drain, and gate regions.

Figure 2 shows a cross sectional TEM picture of the fabricated SOI-MOSFET.

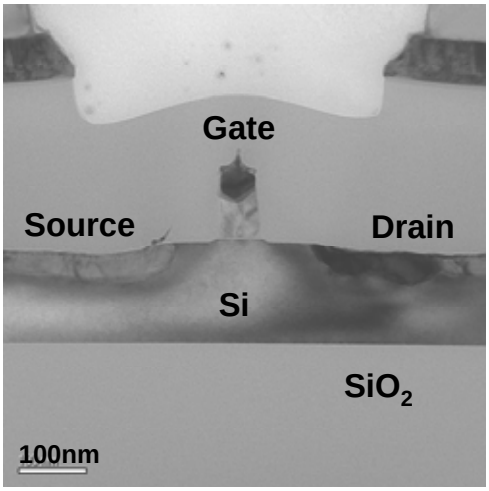

Fig.2: *Cross-sectional TEM picture of the fabricated n-channel SOI-MOSFET* with channel length of 0.1μm

5. Current-voltage characteristics

Figure 3 shows drain current-voltage characteristics in the triode-like operation mode of the n-channel SOI-MOSFET with gate length of 0.1 μm and width of 5 μm. The gate voltages were applied from 0.2 to 1.2 V with 0.2V step. The drain electrode was reversely biased. No current saturation was observed over the wide drain voltages. Under the relatively low gate voltages lower than 0.8 V, the I_D seemed to be represented with eq. (1). Under the higher gate voltages, however, the I_D was slightly getting off the triode curves expected from eq.(1). It was not due to "channel pinch-off" but a different current flow mode; the space-charge-limited-current. Under $V_G < V_T$, $-I_D$ increased with $-V_{DS}$ due to gate-induced barrier-lowering at the source. The feature is compared with the conventional operation mode of the same device as shown in Fig.4.

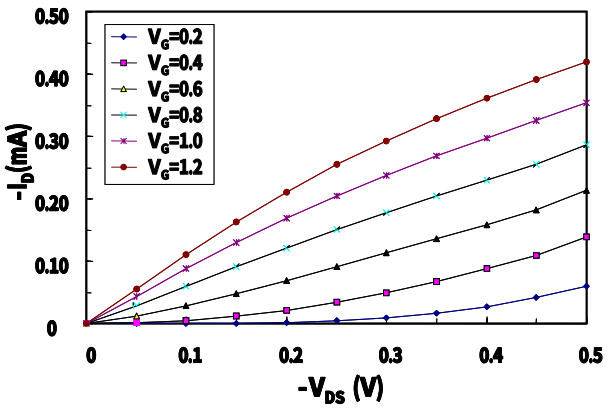

Fig.3: Characteristics of the fabricated SOI-MOSFET in triode-like operation mode under reverse drain bias

The drain currents well saturated even with the short channel of 0.1μm. It is clear that the greater drain current was obtained in the triode operation mode in Fig.3 than the conventional operation mode in Fig.4.

Figure 5 shows the transconductance g_m of the fabricated device. The g_m was larger than that of the conventional operation mode in saturation region and increased proportionally with $-V_{DS}$ as expected from eq.(3). When $-V_{DS}$ was less than 0.2V, it was getting off the linear relation. This is also due to the space-charge-limited current.

6. Conclusions

Triode-like non-current saturation characteristics has been demonstrated by using SOI-MOSFETs. The new operation mode is realized with reverse drain bias featuring larger drive-current and better input-output linearity compared with the conventional mode. The SOI structure fortunately serves to suppress the junction leakage current. This new operation mode may expand SOI applications to analog markets.

Acknowledgement

The authors would like to thank Fujitsu Laboratories Ltd. for sample fabrication.

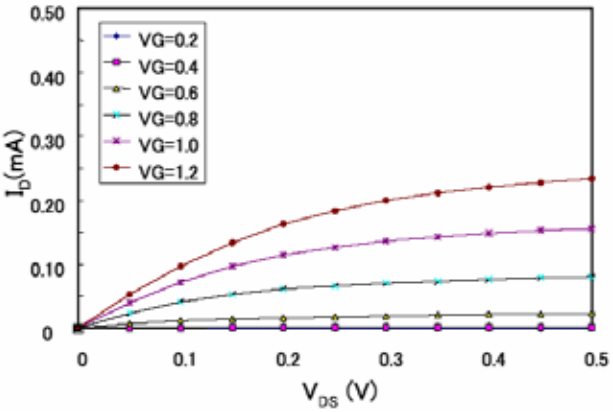

Fig.4: *Characteristics of the same SOI-MOSFET in the conventional pentode-like operation mode under normal drain bias*

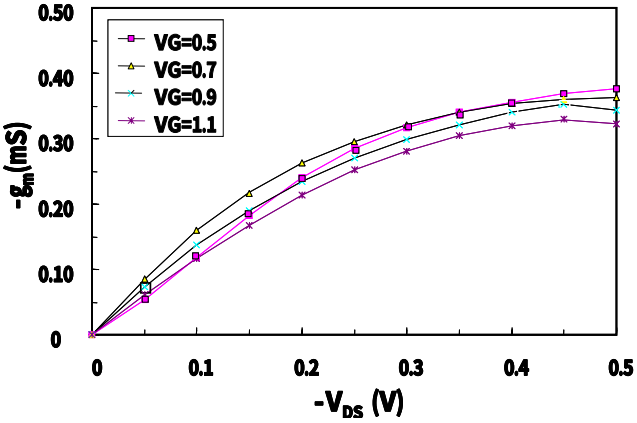

Fig.5: *Transconductance g_m of the fabricated SOI-MOSFET* in triode-like operation mode under reverse drain bias

Doping Fluctuation Effects in Trigate SOI MOSFETs

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Abstract

Random doping fluctuation effects are studied in n-channel Trigate SOI MOSFETs using numerical simulations. The presence of a single positive doping impurity atom increases the threshold voltage. Electrical parameters vary with the polarity and the physical location of the impurity atom.

Introduction

Random doping fluctuation effects are known to cause variations of the electrical parameters of small MOSFETs[1,2,3] and FinFETs.[4] To give an example, a trigate device with a channel length, width and height of 10nm and a doping concentration of 10^{18} cm^{-3} has a single doping atom in its channel, statistically. This means some devices will be undoped, while some will have one or two doping atoms. Even "undoped" devices will contain doping atoms arising from the original SOI film doping, from random contamination effects or from the S/D implantation process.

Device Simulation

Three-dimensional simulation of n-channel trigate FETs were carried out by solving the 3D Poisson, Drift-Diffusion and Continuity equations numerically using Comsol Multiphysics™.[5] The gate oxide thickness is 2 nm and the silicon in the channel is nominally intrinsic. A single P-type doping atom is represented by a small sphere with a diameter of 0.5nm containing an equivalent doping concentration $N_A=1/V$, where V is the volume of the sphere. The doping atom can be moved around and placed at any location in the silicon. A midgap gate material is used. Figure 1 shows the electron concentration distribution of a trigate FET with $t_{si}=W_{si}=5$nm for different doping situations: (a) undoped device; (b) a single acceptor doping atom located at the top left corner and (c) a single donor atom at the same location. A single doping atom was moved to 125 different positions in five slices located between the source and the drain junctions of the transistor (figure 2). The $I_D(V_G)$ curves were computed to extract the value of $V_{TH.}$ in each case. The undoped structure was taken as a reference. As a general observation, ΔV_{TH} increases when a positive doping impurity is placed in the transistor.

ΔV_{TH} is higher when the doping atom is located near the centre of the device. Near the four corners, the impact of the doping atom is very limited.

For a donor (N-type) doping atom, as expected, this atom renders V_{TH} more negative. The FET is now an accumulation-mode device. A donor atom slightly increases the electron concentration and, thus, reduces the threshold voltage, but its influence does not "radiate out" like the P-type impurity atom, so the magnitude of the threshold shift is significantly less than when an acceptor atom is introduced. Figure 3 shows the average variation of V_{TH} for each slice in the entire trigate device. For both N-type and P-type doping impurities, the greatest shifts of V_{TH} occurs when the doping atom is placed in the centre of the channel. The variation tends to be zero when the impurity moves close to the source or drain. Table 1 shows the maximum and minimum ΔV_{TH} for both N-type and P-type doping atom in each slice. Generally, the maximum was found in the centre of the slice and the minimum was near the corners.

Conclusion

Random doping fluctuation effects were modeled by introducing a single doping atom in a trigate FET. The typical variation of V_{TH} per doping atom is a few tens of mV. The threshold shift depends on the position and the polarity of the atom. The variation is greater for an inversion-mode (IM) than an accumulation-mode (AM) device and is greatest when the doping atom is near the center of the channel region.

Acknowledgments

This material is based upon works supported by Science Foundation Ireland under Grant 05/IN/I888.

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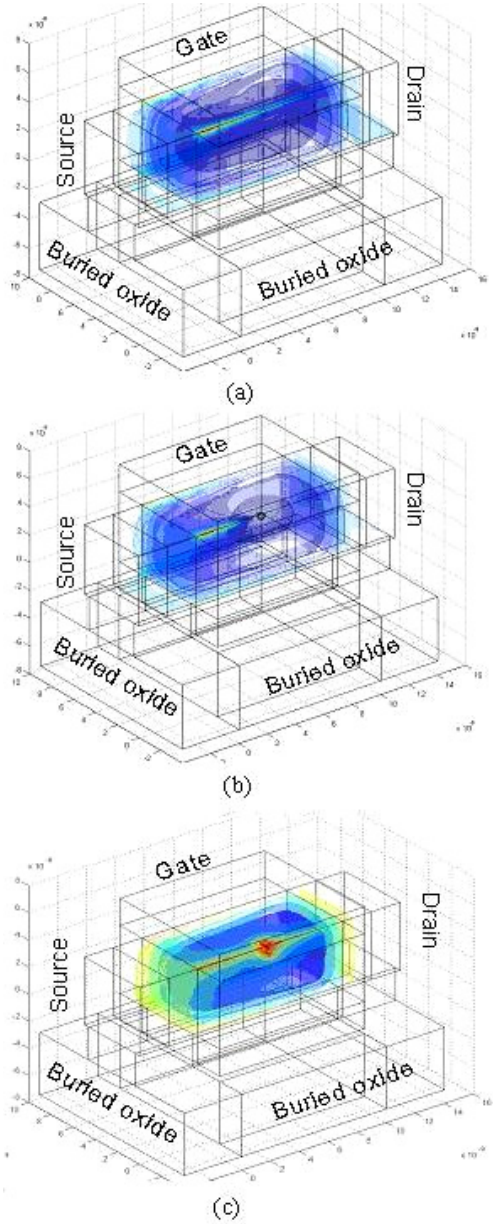

Figure 1: Electron concentration in a trigate FET. V_G=0.3V, V_D=0.2V. $L/2=W_{si}=t_{si}$=5nm. (a) undoped MOSFET, (b) MOSFET with a single acceptor doping atom and (c) MOSFET with a single donor doping atom.

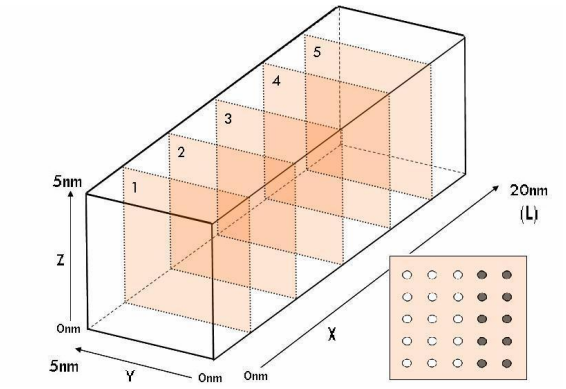

Figure 2 A single doping atom was placed in one of five slices along the silicon channel. For each slice, 15 positions (white dots) were simulated. Because of the transistor bilateral symmetry, 25 data points (black and white dots) were therefore obtained in each slice.

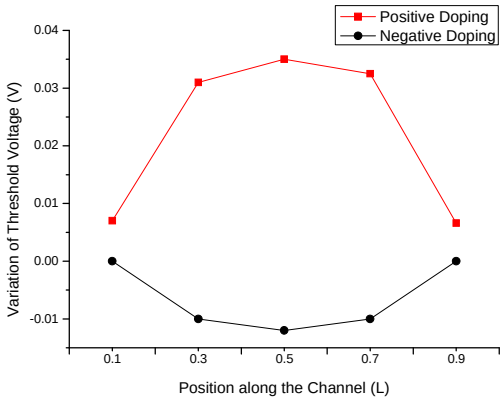

Figure 3 Average variations of threshold voltage in the entire 5nm x 5nm x 20nm trigate device.

Position in the Channel		Max(ΔV_{TH})	Min(ΔV_{TH})
Undoped(reference)		0	0
Acceptor doping atom	0.1 x L	10 mV	0 mV
	0.3 x L	40 mV	20 mV
	0.5 x L	50 mV	30 mV
	0.7 x L	50 mV	20 mV
	0.9 x L	10 mV	0 mV
Donor doping atom	0.1 x L	0 mV	0 mV
	0.3 x L	-10 mV	-10 mV
	0.5 x L	-40 mV	0 mV
	0.7 x L	-10 mV	-10 mV
	0.9 x L	0 mV	0 mV

Table 1: Maximum and minimum threshold voltage shift in different positions for a single *acceptor* doping atom or a single *donor* doping atom.

Impact of the top surface density of states on the characteristics of ultrathin SOI pseudo-MOSFETs

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Abstract

The pseudo-MOS transistor (Ψ-MOSFET) is a quick and reliable technique for the characterization of silicon-on-insulator (SOI) wafers. Numerical simulations clarify the influence of the free surface quality on the Ψ-MOSFET characteristics, shedding light on the dramatic threshold voltage shift experimentally observed when the SOI layer thickness is reduced below 50 nm. An empirical model is proposed.

1. Introduction

Ultra-thin silicon-on-insulator (SOI) MOSFET has been studied intensively and proposed as one of the best candidates for the so called *end of the roadmap*. The pseudo-MOSFET technique [1,2] is a unique method allowing the wafer characterization before any CMOS device processing. The Ψ-MOSFET is basically an upside-down wafer-scale experiment. The schematic set-up is shown in Fig. 1: source and drain electrodes are formed by two point-contact tungsten carbide probes. The substrate behaves as the gate electrode, the buried oxide (BOX) as the gate oxide and the SOI layer is the transistor body.

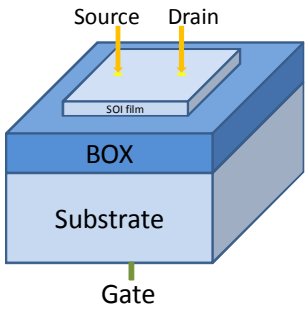

Fig.1: *Schematic configuration of the Ψ-MOSFET.*

An electron inversion channel is formed by positively biasing the substrate. The low-field carrier mobility, threshold voltage, flat band voltage, density of interface defects can be obtained combining this configuration with usual extraction procedures [1,3]. In this paper, we investigate and explain the outstanding increase in threshold voltage that was experimentally observed in SOI films thinner than 50 nm (Fig. 2) [4].

2. Pseudo-MOSFET simulation

The in-depth 1-D numerical solution of Poisson equation was calculated by considering that the gate voltage drops exclusively in the BOX and SOI film. Both buried interface (film-BOX) density of traps, D_{it1}, and top interface (free surface) density of traps, D_{it2}, were considered. Then the threshold voltage was extracted from the inversion charge versus gate voltage characteristic.

Figure 2 shows the simulation-extracted threshold voltage versus the silicon layer thickness for different values of free surface density of states, D_{it2}. It is clear that the top surface charge is responsible for the threshold voltage shift with film thickness. For $D_{it2}=2x10^{13}cm^{-2}eV^{-1}$, the simulation reproduces the experimental curve for non-passivated wafers, and this density of traps is in good agreement with suggested values [5].

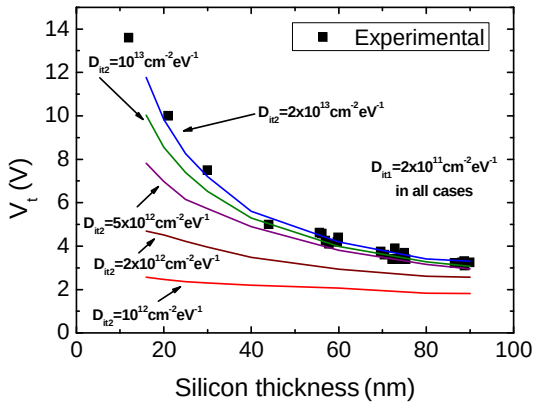

Fig.2: *Simulated threshold voltage vs. silicon film thickness for various top density of states. For $D_{it2}=2x10^{13}cm^{-2}eV^{-1}$ the simulation fits the experimental data. $t_{BOX}=145nm$.*

The effect of the buried density of states (not shown) is just a vertical shift of the curves ($\sim qD_{it1}/C_{ox}$ as in the usual MOSFET transistor).

3. Potential profile

Figure 3 explains the reason for this behavior. The simulations reveal that the potential profile is severely dominated by the top interface density when the trap density is high ($D_{it2}=2x10^{13}cm^{-2}eV^{-1}$, Fig. 3a) and the film is ultrathin. This invalidates the usual thick-film Ψ-MOSFET model which assumes zero top-charges (Fig. 3b). It follows that the inversion condition (quasi-fixed BOX interface potential) requires a higher gate voltage than for zero surface charge.

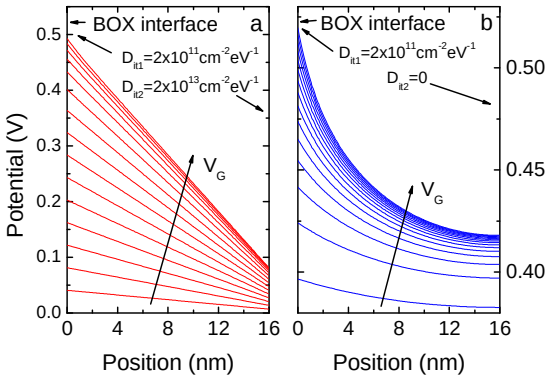

Fig.3: *Potential profiles from BOX interface to free surface for a 16nm thick MOSFET with (a) high and (b) low density of states at the top surface. V_G increases from 1V (depletion) by 1V steps.*

As a consequence of the aggressive silicon thickness reduction, the potential is floating at the top interface: the condition of zero potential at the free surface is no longer valid in ultrathin films. Therefore the gate voltage must support an additional term accounting for the band shift. In ultrathin devices, the curvature of the band at inversion cannot be considered as a $2\varphi_F=2kT/qln(N_{film}/n_i)$. This stands as a source of errors in the extraction of the film parameters.

4. Model for the threshold voltage

We proposed an empirical model for the threshold voltage. Three parameters are used depending on the technology.

$$V_t(t_{Si}) = V_{t0}\left(1+\frac{V_q}{V_{t0}}e^{-Rt_{Si}}\right) \qquad (1)$$

where V_{to} is the conventional thick-film Ψ-MOSFET threshold voltage, and V_q and R are thin film parameters depending on the density of states D_{it2}. The proper selection of the fitting parameters will be discussed. A good agreement with the numerical solution is observed in the whole charge range (Figure 4).

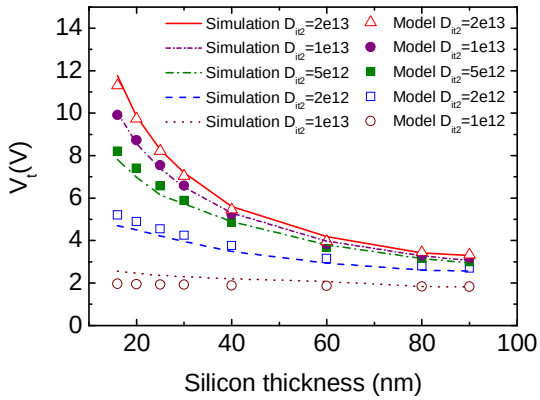

Fig.4: *Comparison between the empirical model (symbols) presented in Eq. (1) and the simulations results (lines). In all cases $D_{it1}=2x10^{11}cm^{-2}eV^{-1}$, $t_{BOX}=145nm$.*

5. Conclusions

The threshold voltage in the pseudo-MOSFET depends on the density of states at the free surface, which can be passivated or not. Poisson equation shows that in ultrathin devices the potential is strongly controlled by the quality of the top surface. For unpassivated wafers, the threshold voltage increase in thinner films is exacerbated. Our simulations clarify previous experimental results and confirm the usefulness of the pseudo-MOSFET characterization technique even for ultrathin SOI wafers.

Acknowledgements

The authors would like to thanks our colleagues N.Bresson and F.Allibert from SOITEC for support, measurement data and illuminating suggestions. This work was partially carried out within the framework of Research Project TEC-2005-01948 supported by the Spanish Government and the Marie Curie Project EDITH N°504195.

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Gate Oxide Integrity on SOI

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Analog Devices BV, Raheen Business Park, Co. Limerick, Ireland

Overview

This paper will address one of the challenges involved in combining high performance bipolars with low geometry CMOS on a single process. Dielectric isolation of bipolars to substrate is essential for optimising their high frequency performance, and is achieved by using SOI wafers. Use of SOI wafers shifts the sensitivites of a CMOS process to background metallic levels, making reliable, manufacturable gate oxides more difficult to achieve. This paper will show how this challenge is being met on a new process platform currently under development at ADI.

Background

ADI's new process platform will offer foundry compatible 0.35um CMOS with ADI's high voltage CMOS (16V and 30V) and high performance double poly bipolars at various voltage ratings. Unlike previous generation processes, bipolar isolation to substrate is provided by use of trench and bonded wafers. This migration to SOI for improved bipolar performance has consequences for the processing of CMOS on the flow. When a gate oxide module is processed on SOI rather than bulk wafers, the sensitivity of the quality of the gate oxide to background metallic contamination is adversely affected. For SOI wafers, very low levels of metallics introduced to the wafer during processing are confined to the shallow device wafer due to their reduced diffusivities through the buried oxide of the wafer. This prevents normal gettering strategies from being relied upon for the process [1][2], and can lead to an increase in the matallic concentration in the device wafer during processing making their incorporation into gate oxides more likely.

Gettering Strategy on Bulk Material

In any CMOS process flow a gettering strategy is employed to ensure high quality gate oxides. A strategy that's typically employed to ensure yielding, reliable gate oxides are achieved on bulk wafers, is to carefully control the oxygen concentration of starting wafers to ensure oxygen precipitate induced stacking faults are created within the bulk of the wafer during processing. These oxygen precipitate induced stacking faults act as low energy locations which getter excess metallics introduced during processing. This mechanism is illustrated in figure 1 below; in the bulk of the wafer the stacking faults are clearly visible, but in the denuded zone near to the surface of the wafer where devices will be processed no stacking faults are present. This gettering strategy performs very successfully for ADI's CMOS flows running on bulk material.

Fig 1: *Defect etched bulk wafer illustrating oxygen precipitate induced stacking faults in wafer bulk.*

Gettering on SOI: Heavy Implantation

In order to realise high quality gate oxides on SOI a number of strategies were investigated in ADI during the last year. The first stratgey investigated was to rely on heavy implantation to create areas of stress away from intrinsic devices at an appropriate stage in the process to ensure the intrinsic device regions were clean during gate oxide growth. The use of heavy implantation to offer additional gettering on SOI is a long established strategy [3][4], and in the implementation described below yielded very promising results for certain process options with heavy implants appropriately located in the process flow.

Implants that are normally used exclusively to provide low resistance contacts to bipolar buried layers on high voltage process options were placed on a testchip at various distances from large, flat, gate-oxide capacitors. These implants are ideally located in the process flow to provide gettering by implantation damage with only a single significant thermal cycle between them and gate oxide growth. The results for these capacitors' catastrophic breakdowns on wafers that received these implants versus those that did not are shown in figure 2 below. Without those heavy implants we see a midfield distribution constituting approximately 3% of measurements for the gate oxide breakdown characteristic. The experimental result shown below has since been repeated with similar results. High quality gate oxide has repeatedly been achieved using this

heavy implantation gettering technique leading to confidence in this mechanism to deliver high quality reliable gate oxides for this process option going forward.

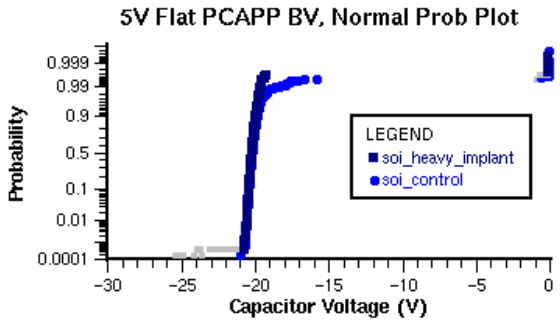

Fig.2: *Effect of Heavy Implantation on Midfield Breakdown Distribution*

SOI Intrinsic Gettering

With cycle time pressures and sensitivities to the order of implantations and thermal cycles it is not possible to execute the above solution for every process option on SOI. A universal solution that can work for any process flow is desirable. Such a solution may lie in choice of starting materials.

Several SOI starting materials with intrinsic, layout independent gettering mechanisms have been investigated at ADI recently. The results from these experiments have shown the effectiveness of these intrinsic gettering mechanisms in cleaning up gate oxides and the affect, if any, on the performance of the core devices on the process. The plot below (figure 3) shows results from one such experiment. Breakdown of a large 70A gate oxide capacitor is plotted for several different wafer types using a low voltage BICMOS process. The intrinsic distribution of catastrophic breakdown is as low as 30% for some SOI types, but ranges right up to 95% for another. This result illustrates that it is possible to improve the gettering effectiveness of SOI wafers to the point where they deliver gate oxide quality comparable to that achieved on bulk material, all other things equal. This gettering strategy leads to a layout independent gate oxide quality assurance.

Typically, intrinsic gettering strategies rely on engineering of the buried oxide to device wafer interface, a region where certain devices are active. Investigations so far have shown that normal device characteristics can be degraded by these intrinsic gettering techniques. Further, wafer costs are increased and from an engineering point of view control of the effectiveness of the gettering strategy is out of the hands of the foundry, while from a manufacturability point of view such material can only be single sourced due to IP control of the strategies such mechanisms are usually under.

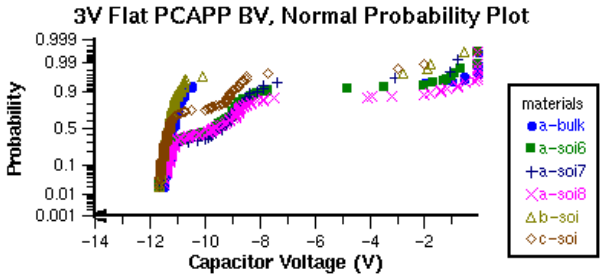

Fig 3: *Gate Oxide Quality on Various SOI Substrates with Intrinsic Gettering*

Conclusions

One of the risks inherent in the development of the next generation process platform at ADI was identified at the outset of the process development: gate oxide quality on SOI material due to reduced gettering. The various options available for overcoming this challenge have or are being investigated. This work will ensure that reliable gate oxides can be achieved on all process options of ADI's new process platform as they are released for production during the coming year.

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Theoretical considerations on lifetime of electrons in quasi-bound states and the tunnel current from the MOS/SOI quantum wells

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1. Abstract

Lifetime of electrons in quasi-bound states in silicon body of the MOS/SOI structures is modeled basing on the half width of the resonant tunneling peak and the quantum well round-trip time approaches. The tunnel current in the double gate MOS structure is simulated and considered in dependence on the body thickness.

2. Introduction

According to the last ITRS forecast, the ultrathin-body fully-depleted SOI and double gate MOS/SOI structures will be essential transistor devices beyond 2012. Due to the energy quantization in the silicon body layer its thickness should affect not only the drain current but also the tunnel leakage current. This effect has been experimentally observed leading to the conclusions that the reduction of the silicon layer results in a decrease of the tunnel current at the same surface density of electrons [1] as well as at the same gate voltage [2]. In contradiction to [2], the theoretical consideration [3] suggests an increase of the tunnel current at the same gate voltage. The model used in [3] was based on the quasi-classical model of the lifetime of electrons in the quasi-bound state of the quantum well. The aim of this work is to reconsider the silicon thickness dependence of the electron tunnel current using more rigorous model based on the half-width of the resonant tunneling peak and in a wider range of the semiconductor thicknesses.

3. Theory

The electron energy in the ultrathin silicon body is quantized creating two ladders of the levels E_{ij}. The tunnel leakage current from the silicon body to the gate electrodes can be expressed as a sum of contributions from the quasi-bound states, determined by the ratio of the density of electrons on the ij-th level N_{ij} and the lifetime τ_{ij} of electrons in the ij-th quasi-bound state:

$$J_e = q\sum_{ij}\frac{N_{ij}}{\tau_{ij}} \tag{1}$$

Basing on the Heisenberg uncertainty principle, the lifetime of electrons can be expressed as:

$$\tau_{ij} = \frac{\hbar}{\Gamma_{ij}} \tag{2}$$

where Γ_{ij} is the half width of the resonant tunneling probability peak [4]. Another, quasi-classical approach [5] expresses the lifetime τ_{ij} by the round-trip time within the quantum well t_{Tij} and the tunneling probability P doubled to include tunneling to two gates:

$$\tau_{ij} = \frac{t_{Tij}}{2P_{ij}} \tag{3}$$

In order to assure accuracy of simulation, the tunneling probability P and the resonant tunneling probability P_r needed to determine Γ were calculated with the use of the transfer matrix method, while the electrostatics problem for the double gate MOS structure was solved including both Poisson's and Schrödinger's equations.

4. Results

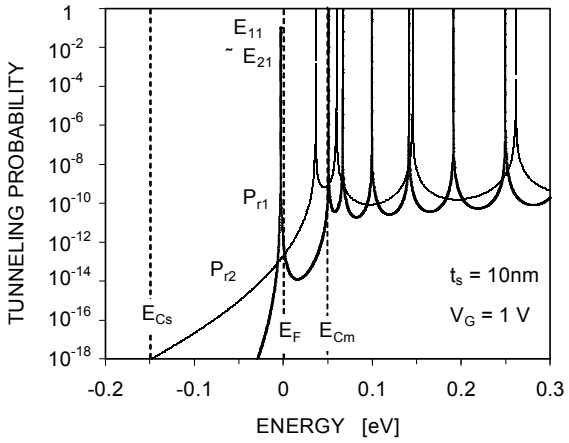

Fig.1: *The gate-to-gate tunneling probability vs. the energy.*

Fig. 1 shows the exemplary energy dependence of the probability of tunneling P_r between the gates of the symmetrical double gate MOS structure of the body thickness 10 nm, the oxide thickness 1nm, doping level 10^{17} cm^{-3}, and the midgap metal work function 4.6 eV. Sharp peaks correspond to the quasi-bound states in the silicon body quantum well. The lifetime of electrons resulting from the half width of these peaks is shown in Fig. 2 and is compared with the lifetime obtained with the use of the quasi-classical model. Both approaches QM (2) and Q-CL (3) give nearly the same results, in agreement with [6], with some numerical discrepancies

near the maximum of the potential energy in the middle of the semiconductor E_{Cm}. It is interesting noticing that the round-trip time in the Q-CL approach for E < E_{cm} has to be expressed simply as the sum of times for two surface sub-wells without including tunneling through the middle potential barrier, as in [3].

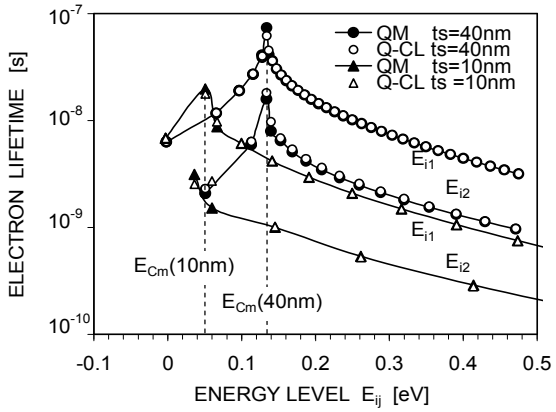

Fig.2: *The lifetime of electrons according to two approaches.*

Fig. 3 and Fig. 4 show the tunnel current according to the QM model (2) in dependence on the gate voltage and the surface density of electrons, respectively.

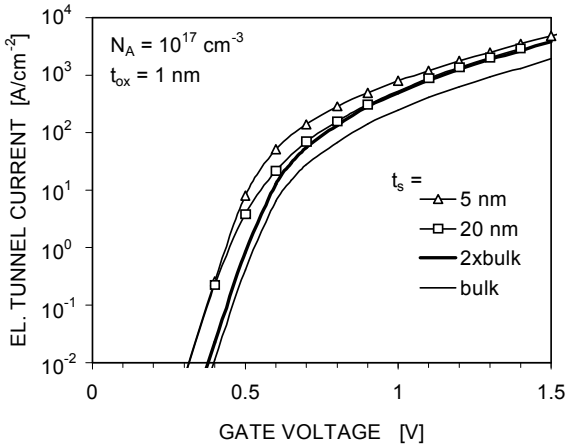

Fig.3: *The tunnel current in dependence on the gate voltage.*

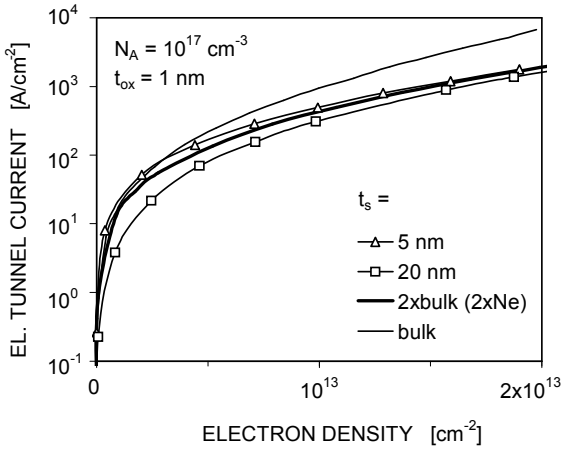

Fig.4: *The tunnel current versus the electron surface density.*

If the thickness of the silicon layer is reduced, the tunnel current increases at the same gate voltage, which is in disagreement with [2]. However, if the tunnel current is compared for the same density of electrons in the semiconductor, a reduction of the body thickness results first in a decrease of the tunnel current for t_s > 20nm and in an increase of this current for t_s < 20nm. It is worth noticing that the tunnel current for the bulk transistor is always the highest, even in comparison to the case 2xbulk. In order to ensure the same doubled value of the density of electrons, the electric field in the bulk substrate has to be stronger, which in turn results in much higher probability of tunneling. Since the effect of the semiconductor thickness on the tunnel current can depend on doping level, Fig. 5 shows the electron tunnel current for the undoped substrate. Similarly as in Fig. 3, a reduction of the silicon thickness at the same gate bias results in a larger tunnel current .

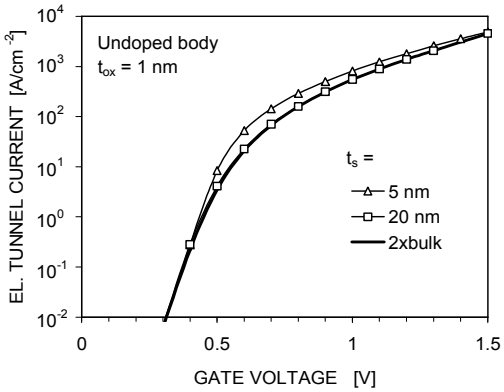

Fig.5: *The gate tunnel current for the undoped silicon body.*

4. Conclusions

According to the model of tunneling based on the lifetime of the electron quasi-bound states expressed as the half-width of the resonant tunneling peak, a reduction of the silicon thickness in the double gate SOI structure should result in an increase of the tunnel leakage current at the same gate voltage and in a decrease of this current at the same density of electrons in the silicon body for t_s > 20nm. The first conclusions is in contradiction to the experimental observation [2] and further experimental and theoretical investigation should be performed with a careful examination of all effects affecting the tunnel current.

Acknowledgments

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Cross-Sensitivities of Ring Oscillators on Thin Dielectric Membrane for Pressure Sensing Applications

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1. Introduction

SOI technology has appeared as a key enabler in the fabrication of active pressure sensors on very thin dielectric membranes. Recently, first electrical characterization of devices and ring oscillators on dielectric membranes were presented. The effect of a pressure applied on a membrane was discussed. In the present work, we report a first analysis of the sensitivity of such system to cross-parameters: the temperature and the supply voltage.

2. Fabrication

The wafers followed a standard SOI CMOS process supplemented by two main steps. The first one is a nitride layer deposition and patterning for the membrane formation, while the second one is the TMAH back-etching with addition of APS and silicon powder allowing using an aluminum layer as a mask (Fig. 1(a)). The membrane is a multilayered film and has the following structure: SOI wafer buried oxide, LPCVD silicon nitride, PECVD oxide and APCVD passivation oxide. The residual tensile stress is estimated at 172 MPa. It is square shaped of 800 µm side and 1.5 µm thickness. The ring oscillators (RO) are made of seven CMOS inverters, with W = L = 12 µm devices. They are located off membrane and at the middle of the edge of the membrane, where the stress with applied pressure is maximized [1] (Fig. 1(b)). Two different RO's orientations were implemented: inverters with nMOS and pMOS channel, respectively, parallel and perpendicular to the stress (Oscillator //), and the opposite configuration (Oscillator ⊥).

3. Electrical Results

All measured oscillators present a Zero Temperature Coefficient voltage (V_{ZTC}), as illustrated in Figs. 2 and 3 for on and off membrane oscillators. At such an operating point, the output frequency is insensitive to the temperature. It originates from the mutual compensation of the threshold voltage and the carriers mobility dependencies with temperature [2], which modify the channel resistivity and hence the output frequency.

From Figs. 2 and 3, oscillation frequencies differ whether the circuit is implemented on or off a membrane: this frequency is 13% higher for the oscillator ⊥ than one out off membrane, at room temperature and 2 V supply. This variation is mainly attributed to the substrate's contribution to the parasitic capacitances. Besides, the residual membrane's stress is assumed being responsible of a 12% frequency difference between oscillator // and oscillator ⊥, under the same conditions (Fig. 4).

From Fig. 4, operating a couple of oscillators at one V_{ZTC} does not provide a temperature independent output because of a slight V_{ZTC} mismatch. As suggested in [3], by considering the output frequency dependency with the membrane's stress and the temperature, we have for both orientations oscillators:

$$F_{//} \approx F_0(1+\pi_{//}\sigma)(1+\alpha T)$$
$$F_{\perp} \approx F_0(1+\pi_{\perp}\sigma)(1+\alpha T),$$

where $\pi_{//}$ and $\pi_{\perp}$ are the piezoresistive coefficients, σ is the stress, α is the temperature coefficient and T is the temperature. Neglecting the second order terms, the frequency ratio between both oscillators can be expressed as:

$$F_{//}/F_{\perp} \approx 1+(\pi_{//}-\pi_{\perp})\sigma,$$

a temperature independent expression. In practice, this statement was verified only at higher supply voltages (i.e. 2 V). In this latter case a steady output frequency ratio of 1.13 is observed with only 1.4% variation between 25 °C and 200°C.

Stress sensitivity experiments were conducted at room and high temperature as a function of the supply voltage (V_{dd} - V_{ss}) and lead to, respectively, an increase of the output frequency of 5% and 8% for oscillator // (-1% and +1% for oscillator ⊥). The output frequency increase is weakly dependent on the supply voltage at room temperature while it increases with the voltage at 200°C.

4. Conclusions

The supply voltage plays a determinant role in terms of sensitivity to the temperature. Nevertheless, the use of oscillator frequencies ratio provides a stable sensor

output for sufficient supply voltages (from 2 V). Finally, these first cross-sensitivities experiments let us figure out the applicability of this system in high temperature environments. Hence, a possible self-heating due to the high thermal insulation character of the membranes does not appear being detrimental to the sensitivity of the sensor.

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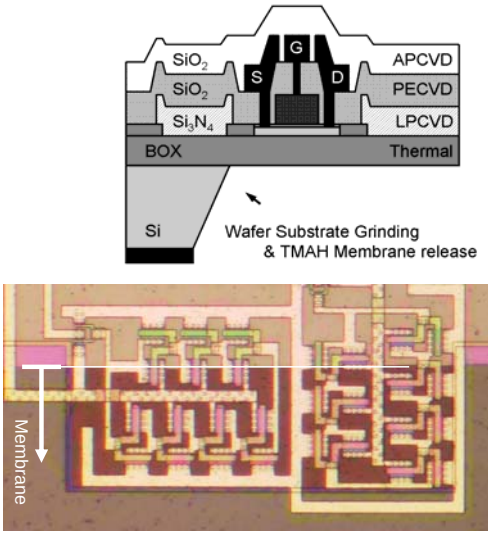

Fig. 1: *(a) SOI wafer's cross-section view with devices and circuits on thin multilayered dielectric membrane, (b) microphotograph of ring oscillators implemented at the border of such a membrane (oscillators⊥ on left, // on right).*

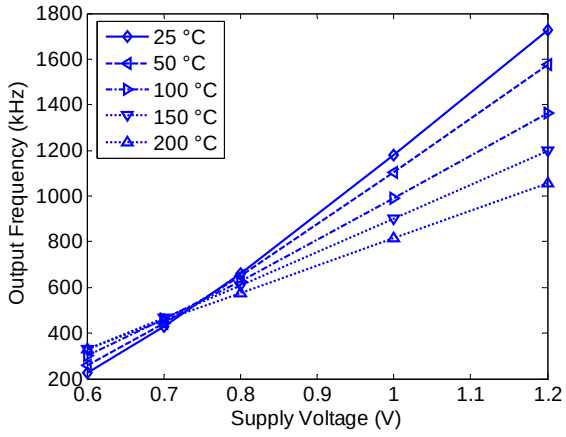

Fig. 2: *Typical output frequency of an off-membrane ring oscillator as a function of the supply voltage for various temperature values.*

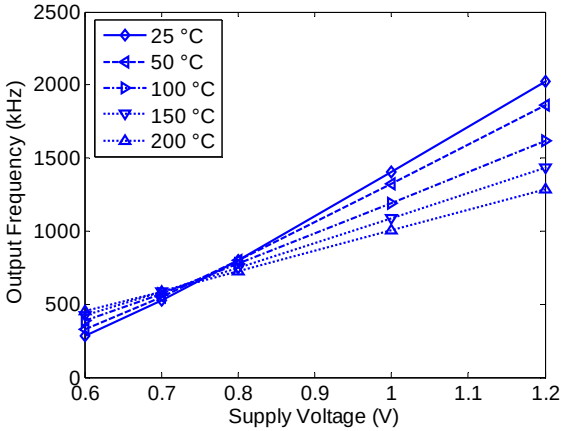

Fig. 3: *Typical output frequency of an on-membrane ring oscillator as a function of the supply voltage for various operating temperature values.*

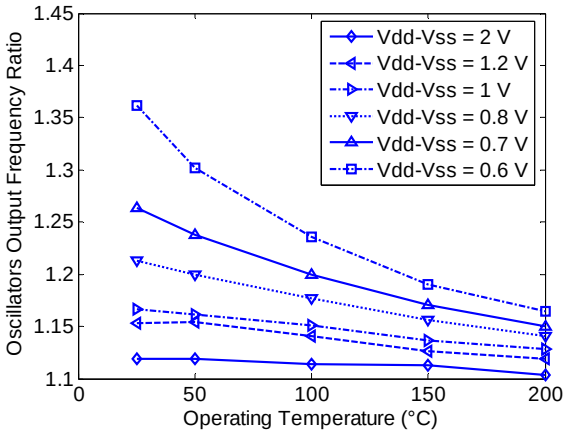

Fig. 4: *Output frequency ratio of two on-membrane ring oscillators (one // and one ⊥) as a function of the temperature for various supply voltages.*

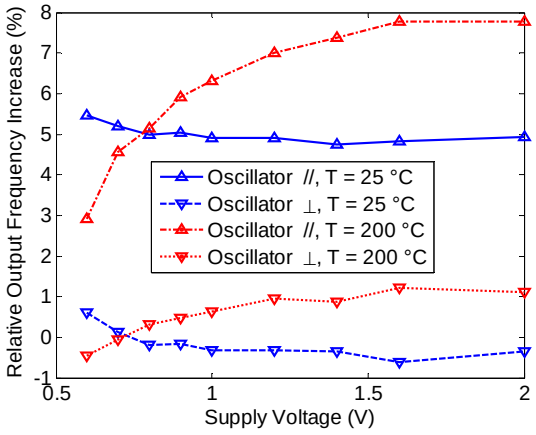

Fig. 5: *Output frequency sensitivity of two on-membrane ring oscillators (differing in their orientation), as a function of the supply voltage at 25 °C and 200 °C. The stress applied at both temperatures is not supposed being the same.*

3-D capacitive MEMS sensors co-integrated with SOI CMOS circuits

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1. Abstract

A SOI CMOS compatible process, guaranteed by use of classical CMOS materials and fabrication techniques and demonstrated with fabrication of a complete functional circuit, is presented. From our Fully Depleted (FD) SOI CMOS process, addition of only one mask (3 lithographic steps) is needed to obtain a flow sense MEMS-based circuit.

2. Introduction

In agreement with CMOS trends, our work concerns the fabrication of MEMS with thin film SOI, to obtain structures presenting an out-of-plane (3-D) movable part. To build such 3-D MEMS, several techniques have been proposed in the literature: projection micro-stereolithography [1], plastic deformation under magnetic field [2], reflow of solder hinges [3], multi-stack silicon-direct wafer bonding [4] or even slide a probe tip under the released structures [5]. These techniques add extra and tricky fabrication steps to the classical CMOS process and are therefore often hardly suitable to an easy co-integration with CMOS.
Our MEMS-CMOS process, only requiring well-qualified cleanrooms steps following by a transistor-respectful release, does not suffer for such difficulties and allows a simple co-integration.

3. Three-dimensional MEMS fabrication

For our microsystems, a SOI wafer is basically considered as the starting material. It consists in a 100 nm-thick monocristalline silicon film on top of a 400 nm buried oxide (BOX) lying on a thick silicon handling substrate. Our goal is to use a layer of SOI stack as sacrificial layer.
In self-assembling 3-D microsystems, use can be made of intrinsic stresses to generate a desired geometry. Mainly originating from thermal expansion mismatch between layers, important stresses can be induced in multilayered structures and controlled a posteriori by monitoring the stack thickness. A significant stress increase can be achieved in a plastic layer, like aluminum, by annealing at sufficiently high temperature [6].
For the 3-D sensors reported in this paper, LPCVD silicon nitride deposited at 800°C over the thin silicon layer generates large gradient of stress and aluminum is used as the metallic contacting layer. A thermal treatment is applied to Al for increasing its residual stress to values higher than 100 MPa thanks to its plastic flow behavior. The bending moment is then large enough to curve our single-side anchored beams and overcome all stiction energies allowing the release of the structures and very large deflections.

4. SOI MEMS-MOS co-integration

In the purpose of co-integrating MOS circuits and MEMS sensors, the most critical steps for our chosen process are the thermal annealing and the release of MEMS without degrading CMOS circuits. For building the microstructures, smart use of the stack constituted by the thin top Si layer and the BOX allows a simple co-integration. Fig. 1 presents the process flow for the co-integration of CMOS circuits and MEMS. A particular chemistry occurs when a thin silicon layer is etched by SF_6 plasma (25 W, 30 min): the first phase is a classical anisotropic dry etch with vertical side walls of the Si layer whereas a second phase occurs, when the whole Si thickness is etched and then BOX is reached, with very selective but isotropic silicon etch. With simply photoresist masking of integrated circuits, cantilevers release can be achieved. Afterwards, the annealing to assemble microstructures also helps to improve the metal (poly)silicon contacts and reduce the gate oxide interface traps. No modification of the thermal budget of our CMOS process is then needed.
Figure 2 shows the good electrical behavior of the SOI MOS transistors of various geometries located close to the released 3-D MEMS.

5. Integrated 3-D sensors

In such a case, co-integration of our microsystems with a CMOS-SOI process requires only one mask and 3 extra lithographic steps, mainly to protect the MEMS areas when processing the IC part (implantations, etchings, etc.) and protect the IC part when processing only the MEMS devices (dry etching and release). Fig. 3 shows a SEM picture of a complete co-integrated CMOS-MEMS circuits. The 3-D capacitive cantilevers are connected at the internal nodes of CMOS ring oscillators made of 5 inverters in order to perform a capacitance to frequency conversion.
These sensors consume extremely low power, present high sensitivity and large sensing range as well as occupy low chip area. Measurements under air flow are presented in Fig. 4. The flow bends downwards the cantilevers, increases their capacitance and, therefore,

lowers the oscillating frequency.

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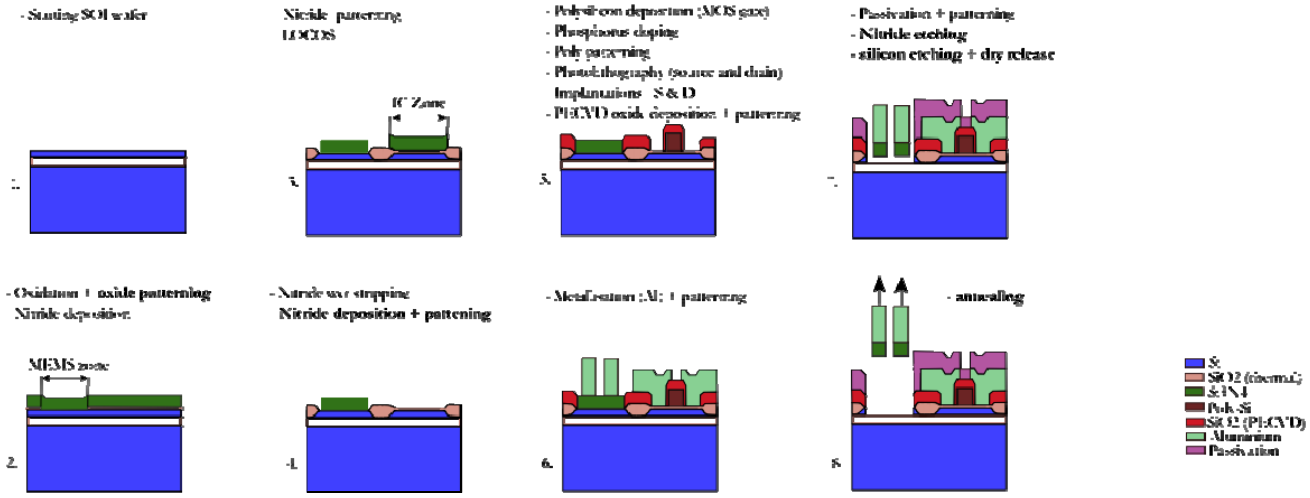
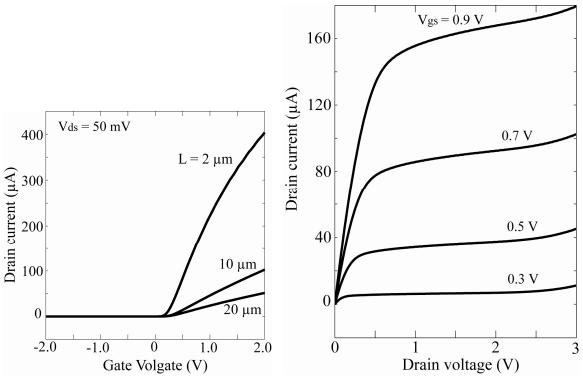


Fig. 1: *SOI MOS-MEMS co-integration process flow.*



(a) *(b)*

Fig. 2: *Fully Depleted SOI nMOSFETs of 20 µm-wide: (a) I_{ds}-V_{gs} at V_{ds} = 50 mV for various channel lengths (2, 10 and 20 µm), (b) I_{ds}-V_{ds} versus V_{gs} for a transistor with a channel length of 2 µm.*

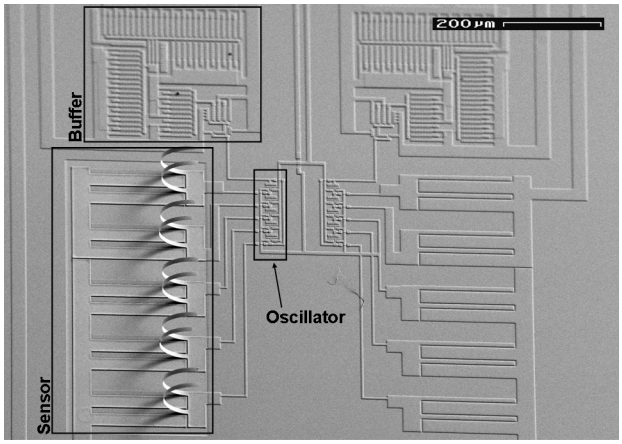


Fig. 3: *SEM picture of a co-integrated 3-D MEMS capacitive sensor with its associated SOI CMOS circuit, a ring oscillator with an output buffer.*

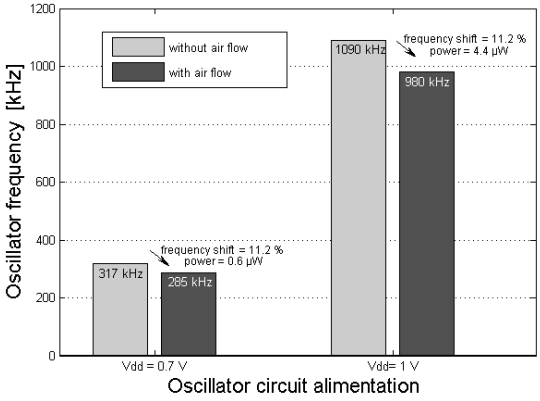


Fig. 4: *Frequency response of the 3-D capacitive MEMS oscillator with and without applied air flow.*

Analog Operation of Uniaxially and Biaxially Strained FD SOI nMOSFETs at Cryogenic Temperatures

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1. Abstract

This work studies the analog performance of uniaxially and biaxially strained fully depeleted SOI nMOSFETs operating at cryogenic temperatures. The analysis is performed focusing on some important analog figures of merit such as transconductance, transconductance-to-drain current ratio, output conductance and intrinsic gain. It is shown that the use of any kind of strain promotes the improvement of most analog parameters, resulting in better or at least not worst gain than its unstrained counterpart.

2. Introduction and Devices Fabrication

Tensile strain is an effective way of increasing the mobility, and hence drive current, in deep-submicrometer nMOSFETs, contributing to the continuous device downscaling [1]. In addition to these benefits, the operation of MOS devices at low temperatures is known to improve their performance beyond scaling of device dimensions [2].

In this work the impact of the temperature reduction on the analog performance of uniaxially and biaxially strained FD SOI devices will be investigated by evaluating some important parameters namely the maximum transconductance ($g_{m,max}$), the transconductance-to-drain current ratio (g_m/I_{DS}), the output conductance (g_D) and the intrinsic gain (A_v).

The studied devices are from a 65 nm planar single-gate technology with mesa isolation [3]. The gate stack is formed by an 1.5 nm-thick thermal silicon oxynitride and polysilicon with thickness of 100 nm. The final silicon film and buried oxide thicknesses are 15 nm and 150 nm, respectively. Raised source and drain regions elevated with 25 nm and Ni silicidation are used to reduce the series resistance. Uniaxial tensile strain (intrinsic stress of 800 MPa) has been obtained by depositing a 100 nm tensile nitride contact etch-stop layer (sCESL). Biaxial strain has been obtained using strained SOI (sSOI) wafers with a $Si_{0.8}Ge_{0.2}$ strain relaxed buffer and a similar device process flow as for standard SOI.

3. Results and discussion

Fully depleted SOI nMOSFETs with L=160 nm and W=1 µm have been cooled by using the Variable Temperature Micro Probe System K20 from MMR Technologies and the experimental curves were obtained with a Keithley 4200 Semiconductor Characterization System.

Figure 1 presents the maximum transconductance ($g_{m,max}$) as a function of the temperature for devices under different strain conditions, both in linear and saturation regions.

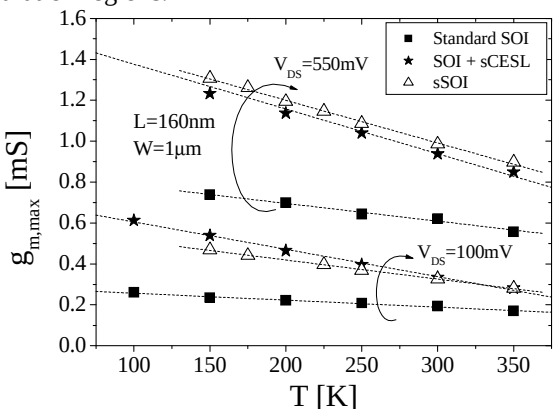

Fig.1: *Maximum transconductance as a funtion of temperature extracted at V_{DS}=100mV and 550mV for 160 nm-long devices under different strain conditions.*

From these curves one can note that the use of strain improves the transconductance at any temperature. In addition, the higher $g_{m,max}$ variation with temperature indicates that the transconductance gain tends to increase with temperature reduction. In the case where sCESL is applied, this transconductance enhancement is due to the larger thermal expansion coefficient presented by the nitride layer in comparison to the silicon film, increasing the tensile effect as temperature is reduced. When biaxial tensile strain is used, the larger $g_{m,max}$ increase with temperature lowering can be related to the reduced surface roughness of strained silicon in comparison to its

unstrained counterpart [4]. While in linear regime $g_{m,max}$ tends to be larger for the device with sCESL, for larger V_{DS} the maximum transconductance tends to be slightly larger for the biaxially strained device than for the uniaxially strained one. This inversion of behavior could be attributed to the presence of neutral defects in the material, which promotes the increase of scattering of electrons in the device with sCESL [5].

The g_m/I_{DS} as a function of normalized drain current in strong inversion is presented in Figure 2. As expected, the temperature reduction increases the g_m/I_{DS} [6] for all unstrained and strained devices. The larger g_m/I_{DS} presented by the strained devices is caused by the enhanced mobility. Among the strained transistors, the biaxially strained option offers the largest $I_{DS}/(W/L_{eff})$ also due to the larger mobility. In addition, one can note that for a given g_m/I_{DS}, the strained devices provide larger normalized drain current than the standard SOI one.

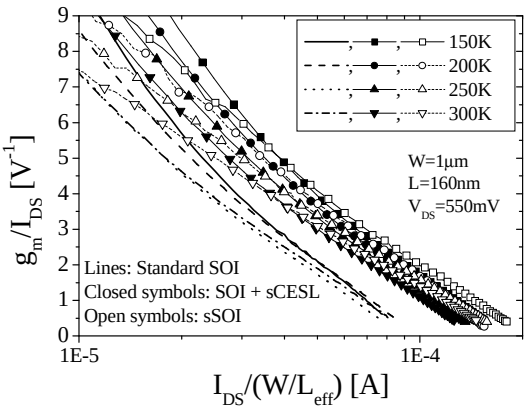

Fig.2: *Measured g_m/I_{DS} curves as a funtion of normalized drain current for L=160nm strained and standard devices at different temperatures.*

From I_{DS} *vs.* V_{DS} curves measured with gate voltage overdrive ($V_{GT}=V_{GF}-V_T$, V_{GF} is the gate voltage and V_T the threshold voltage) of 400 mV, the output conductance (g_D) has been extracted and is shown in Figure 3.

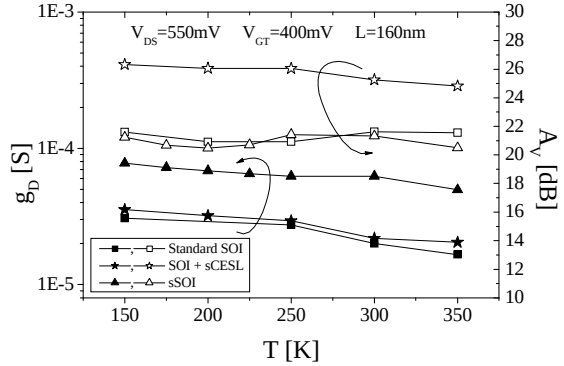

Fig.3: *Output conductance and intrinsic voltage gain as a funtion of temperature, extracted at V_{DS}=550mV and V_{GT}=400mV for devices under different strain conditions.*

The temperature reduction degrades g_D in standard and both strained devices. Besides, the presented results show that the use of sCESL promotes a slight degradation on g_D with respect to standard devices, while the use of sSOI tends to increase this degradation. This effect can be related to the increased DIBL in strained devices [3]. Table I presents the extracted values of DIBL, which has been obtained by extracting the threshold voltage at constant current level of $I_{DS} = 10^{-7} * (W/L)$ [A] with V_{DS}=0.1 V and V_{DS}=1 V. As demonstrated in this table, the use of any kind of strain promotes the increase of the DIBL effect, although it reduces with temperature lowering in all cases. Also, the presented results indicate that, among the devices under study, the biaxially strained ones are more susceptible to the ocurrence of short-channel effects, which is in agreement with data reported in [3].

Table I – *DIBL extracted with V_{DS}=100mV and 1V for all devices under study for different temperatures.*

Device	DIBL [mV/V]		
	T=150K	T=200K	T=300K
Standard SOI	20.55	31.11	39.28
SOI + sCESL	40.44	46.00	56.97
sSOI	109.33	123.33	145.57

Figure 3 also presents the device intrinsic voltage gain ($A_v=g_m/g_D$) as a function of temperature, extracted at V_{DS}=0.55V and V_{GT}=400mV. From the presented results one can note that the temperature reduction tends to slightly increase the gain. For the device with sCESL, the small g_D increase is not enough to reduce the gain in comparison to the standard device. On the other hand, for the sSOI device, the g_m enhancement is compensated by the g_D degradation, leading to A_V values similar to those presented by the standard device in all temperature range.

4. Conclusions

In this work an evaluation of the analog performance of uniaxially and biaxially strained SOI nMOSFETs at low temperatures has been reported. It has been verified that both applied strain techniques provide transconductance gain, which also increases with temperature reduction. It is shown that despite the transconductance enhancement provided by the use of strain, the uniaxially one can achieve larger gain than the biaxially counterpart, for all temperatures, since the later has shown to be more susceptible to the occurrence of DIBL, worsening its output conductance.

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Width effects in 50nm narrow strained SOI: electrical characterizations of FDSOI nMOSFETs and Grazing Incidence X-Ray Diffraction measurements

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1. Abstract

We studied the width effects in 50nm narrow and 10nm thin strained SOI (sSOI) by fine electrical characterisation of Fully Depleted (FD) SOI nMOSFETs and Grazing Incidence X-Ray Diffraction (GIXRD) measurements. We demonstrate that the mobility is increased by about 110% by sSOI down to 50nm narrow channel. This is mainly explained by the strain that is measured to be maintained in the channel length direction.

2. Introduction

It was already demonstrated that the channel width influences the sSOI-induced nMOSFETs performance [1,2,3]. To explain this dependence, we accurately extracted the threshold voltage and the effective mobility down to 50nm narrow channel (with a proper correction of the parasitic capacitances) and measured directly the strain by GIXRD in narrow test structures.

3. Impact of channel width on the electrical properties of FD sSOI nMOSFETs

Studied devices consist on FDSOI nMOSFETs with a TiN/HfO_2 gate stack and a <110>-oriented channel on either a 0.8% strained SOI (fabricated with a $Si_{0.8}Ge_{0.2}$ layer) or an unstrained SOI substrate. The thickness of the silicon active layer is 10nm. The gate length (L) is 10µm and gate width (W) varies from 10µm down to 30nm. The mobility is extracted with the split-CV method [4] taking into account the parasitic capacitances correction [5,6], so that the intrinsic gate to channel capacitance (C_{GC}) was approximated to

$$C_{GC}(W,V_G) = C_{GC}(W_{wide}, V_G - V_{Twide} + V_T).\frac{C_{inv}(W)}{C_{inv}(W_{wide})}$$ with

W_{wide} the gate width and V_{Twide} the threshold voltage of a wide nMOSFET. Note that without any correction of the capacitance, the effective mobility is strongly underestimated (Fig.1). The evolution of the effective mobility as a function of the gate width W is drawn in Fig.2 with the parasitic capacitance correction. The sSOI-induced mobility enhancement only slightly decreases from 120% for W=10µm down to 110% for W=50nm.

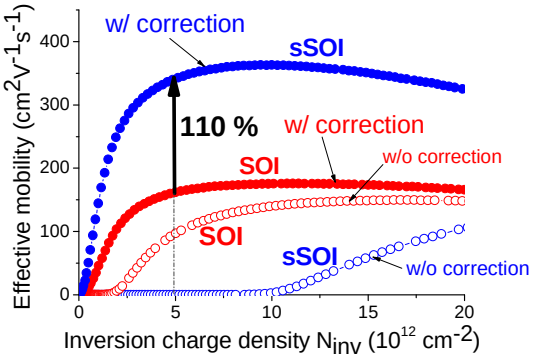

Fig.1: *Effective mobility of a 50nm narrow nMOSFET as a function of the inversion charge density with and without capacitance correction.*

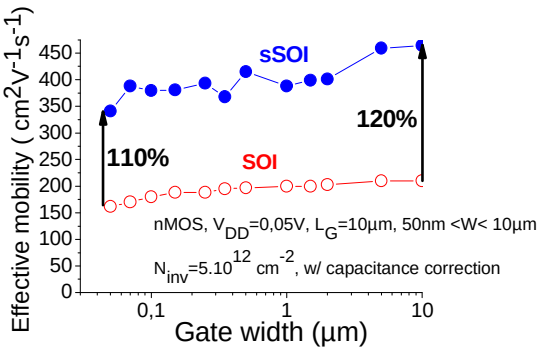

Fig.2: *Effective mobility of nMOS structures on SOI and sSOI versus gate width. Measurements are performed at $N_{inv}=5.10^{12}$ cm^{-2} and corrected from parasitic capacitances.*

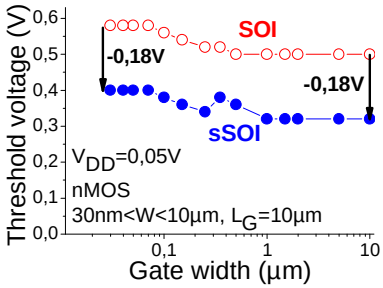

Fig.3: *Threshold voltage of nMOS structures on SOI and sSOI versus gate width.*

The threshold voltage V_T (see Fig.3) is extracted at a constant drain current (equal to 10^{-7} W/L Ampere).

The sSOI-relative V_{Ts} are lower than the unstrained SOI ones due to the general strain effects: conduction band degeneracy lift and lowering of the unprimed Δ2 valleys. This V_T-shift between sSOI and SOI is quite independent of the gate width as shown in Fig.3. This is consistent with the mobility enhancement behaviour vs. channel width (Fig.2). To understand these dependences, the strain was measured by Grazing Incidence X-Ray Diffraction (GIXRD) in 50nm tests structures.

4. Strain analysis by Grazing Incidence X-Ray Diffraction (GIXRD)

The test samples geometry is described in the inset of Fig.6. It consists on 4mm long and W=50, 100, 200 nm wide sSOI lines. The strain measurements were performed at the European Synchrotron Radiation Facililty (ESRF) in Grenoble. The X-Ray beam intensity enables the analysis of 10nm-thin sSOI lines. Note that the thickness of the sSOI lines is the same as the electrical devices. The energy of X-rays used is 12 keV. The main advantage of measuring the strain by GIXRD, compared for example to the Raman technique, comes from the possibility to extract the lattice parameter (and strain) along different directions with a high accuracy. The (220) and (2-20) crystallographic planes perpendicular to the (001) surface are considered (see insets of Figs.4 and 5). They allow getting the longitudinal strain along the sSOI lines and the transverse strain perpendicular to the lines direction. These two directions correspond respectively to the ones along and perpendicular to the electronic transport in the MOSFETs. The substrate Bragg peak can be measured separately from the strained silicon layer peak by changing the X-ray incidence angle. The strain of the sSOI layer can be measured "independently" of the wavelength thanks to the relationship $\varepsilon = \frac{\sin(\psi_{Si}/2)}{\sin(\psi_{sSi}/2)} - 1$, with ψ the detector angular position. The diffracted intensities along the (220) and (2-20) reflections are shown in Figs.4 and 5. This type of scan (similar to the standard θ/2θ geometry) measures the lattice parameter of the Si substrate, the sSOI unpatterned 2D layers, or the 50nm-width lines.

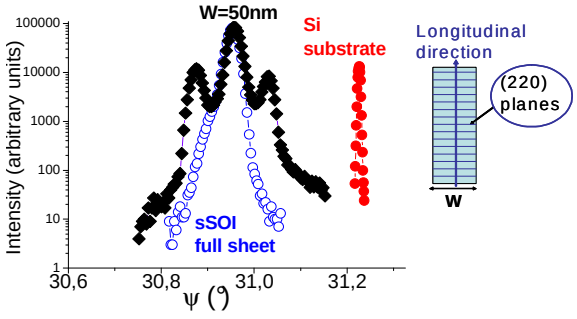

Fig.4: (220) *Bragg peaks of 50nm-width sSOI lines, non-patterned sSOI reference and unstrained Si substrate.* **Inset:** *Schematics of the (220) planes.*

In the longitudinal direction, the Bragg peak of the 50nm narrow sSOI lines is at the same position as the unpatterned sSOI one (see Fig.4), indicating that the strain longitudinal to the lines is independent of the line width (see also Fig.6). In the transverse direction, the Bragg peak of the narrow sSOI lines shifts to the Bragg peak of the Si substrate (see Fig.5). This means that the strain in the line width direction decreases when the line width decreases (see also Fig.6), down to 0.3% for W=50nm.

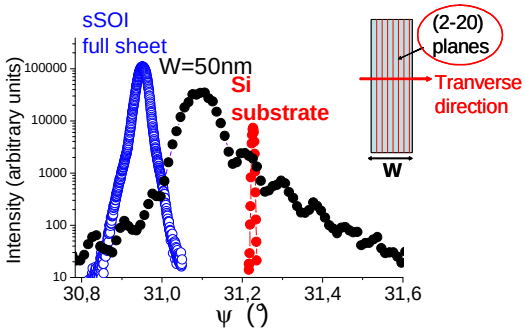

Fig.5: (2-20) *Bragg peaks of 50nm-width sSOI lines, non-patterned sSOI reference and unstrained Si substrate.* **Inset:** *Schematics of the (2-20) planes.*

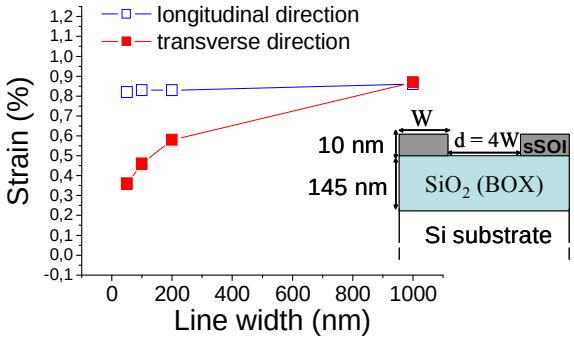

Fig.6: *Strain versus sSOI line-width W in the direction parallel (blue open symbols) and perpendicular (red full symbols) to the lines.* **Inset:** *Schematics of studied samples obtained by e-beam lithography and Si etching.*

5. Conclusions

GIXRD measurements demonstrate that for long and narrow active areas, the strain in the sSOI is kept constant along the longer direction. We speculate that this is the main reason why we obtained a 110% mobility enhancement in 10µm long FD sSOI nMOSFETs down to 50nm narrow channel.

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STI-Induced Mechanical Stress-Related Kink Effect of 40nm PD SOI NMOS Devices

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Abstract

This paper reports the STI-induced mechanical stress-related kink effect behaviors of the 40nm PD SOI NMOS device. As verified by the experimentally measured data and the 2D simulation results, the kink effect behaviors occur at a higher V_D for the 40nm PD device with a smaller S/D length of 0.17 μ m as compared to the one with the S/D length of 1.7 μ m due to the higher body-source bandgap narrowing effect on the parasitic bipolar device from the higher STI-induced mechanical stress, offset by the enhanced impact ionization coming from the bandgap narrowing in the surface high electric field region..

Introduction

Mechanical stress induced by STI may affect the performance of MOS devices [1][2]. Until now, no paper reports the STI-induced mechanical stress effect on the kink behaviors of PD SOI CMOS devices. For nanometer PD SOI CMOS devices, the S/D region may be very small- the influence of the STI-induced mechanical stress cannot be overlooked. In this paper, STI-induced mechanical stress-related kink effect behaviors of the 40nm PD SOI NMOS device are reported.

STI - Induced Kink Effect

The 40nm PD SOI NMOS test device fabricated in the industry with its cross section as shown in Fig.1 has a 70nm thin film doped with a p-type density of $3x10^{18}cm^{-3}$ above a buried oxide of 145nm and a gate oxide of 1.5nm. Two cases with the S/D length of 1.7 μ m and 0.17 μ m have been designed for the study. Experimental measurement of the test device and 2D simulation considering mechanical stress effects have been used to carry out the study.

Fig.2 shows the hydrostatic pressure and the associated bandgap narrowing distribution in the lateral direction of the 40nm PD SOI NMOS device with S/D length of 0.17 μ m and 1.7 μ m. As induced by STI, the mechanical stress in terms of hydrostatic pressure is large in the S/D region near STI and decreases away from it. The corresponding bandgap narrowing, which is correlated to the mechanical stress, has a dramatic

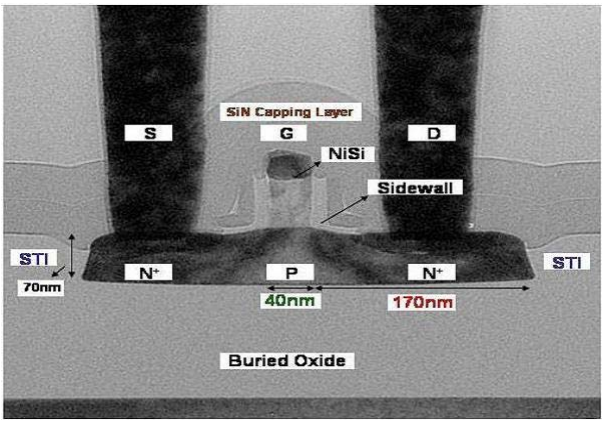

Fig.1: TEM cross section of the 40nm PD SOI NMOS device.

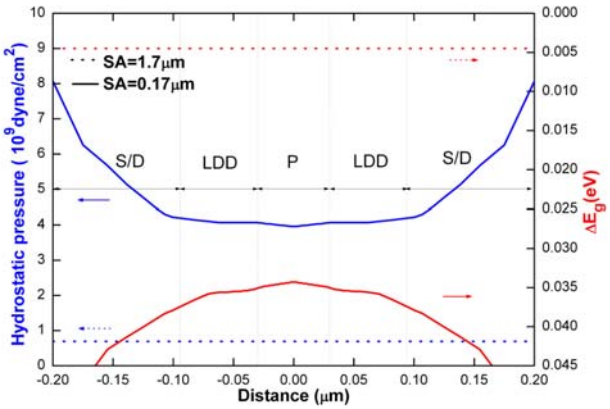

Fig.2: Mechanical stress and bandgap narrowing distribution in the lateral direction of the PD SOI NMOS device

impact on the kink effect of the 40nm PD NMOS device. Fig.3 shows I_D versus V_D of the 40nm PD NMOS device with the S/D length of 1.7 μ m and 0.17 μ m, biased with its body floating, based on the measured data and 2D device simulation results. In order to discriminate the bandgap narrowing effect in the parasitic bipolar device from that in the high electric-field impact ionization region, simulations based on the impact ionization model considering bandgap narrowing and without have been done. As shown in the figure, with a smaller S/D length of 0.17 μ m, the kink effect behavior occurs at a larger V_D as compared to the case

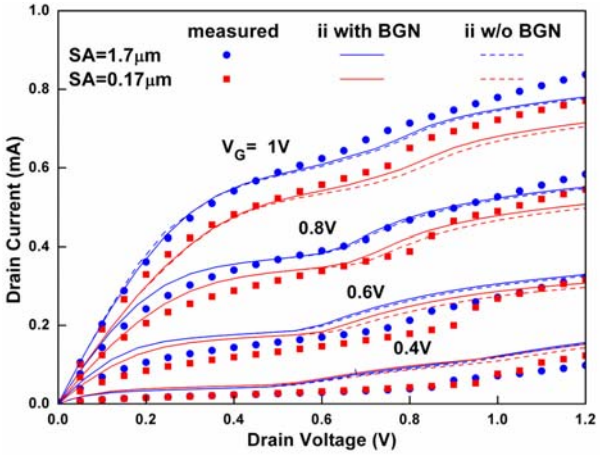

Fig.3: I_D vs V_D of the 40nm PD SOI NMOS device with the S/D length of 1.7μm and 0.17μm.

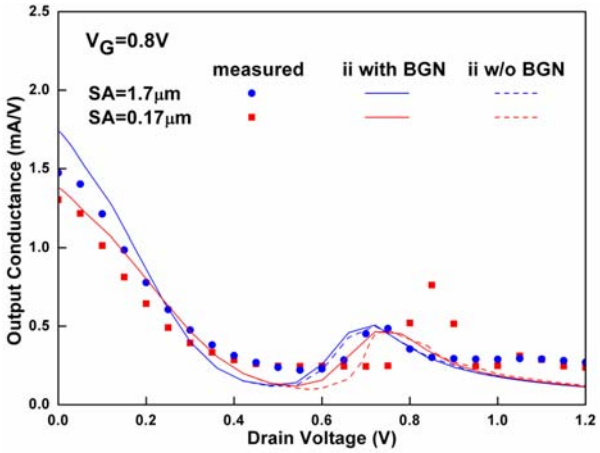

Fig. 4: Output conductance vs V_D of the 40nm PD SOI NMOS device biased at V_G=0.8V.

with the S/D length of 1.7 μ m. Considering the bandgap narrowing in the impact ionization model for simulation, the kink effect occurs at a reduced V_D. Fig.4 shows the related output conductance versus V_D characteristics of the PD device biased at V_G=0.8V. With the shorter S/D length of 0.17 μ m, the kink effect behavior indeed occurs at a larger V_D due to the higher bandgap narrowing effect on the function of the parasitic bipolar device from the larger mechanical stress, which is confirmed by the body-source voltage-the V_{BE} of the parasitic bipolar device in the thin film as shown in Fig.5. With a smaller S/D length of 0.17 μ m, the body-source voltage rises at a larger V_D, which indicates the later turn-on the parasitic bipolar device. The kink effect is also determined by the impact ionization in high electric field region of the surface channel [4]. Bandgap narrowing in the high e-field region may help impact ionization. As shown in the figure, with a smaller S/D length of 0.17 μ m, considering the bandgap narrowing in impact ionization model for simulation, the difference in V_{BE} between the 0.17 μ m and the 1.7 μ m cases becomes smaller. The trends predicted by the simulation are correlated to the

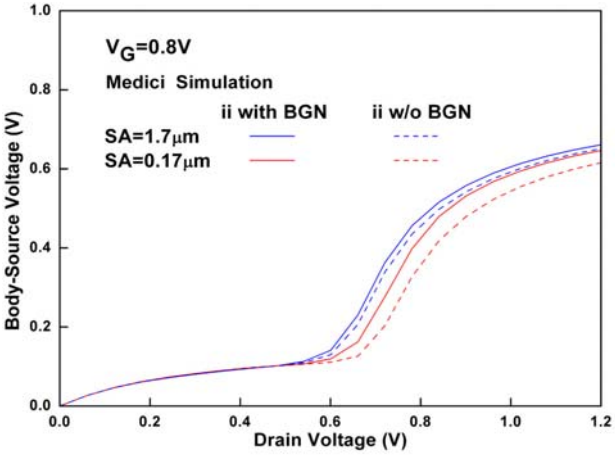

Fig.5: V_{BE} vs V_D of the 40nm PD SOI NMOS device.

experimentally data as shown in the figures.

Discussion

The higher V_D at the onset of the kink effect behavior of the 40nm PD SOI NMOS device with the smaller S/D length of 0.17 μ m could be reasoned by considering the function of the parasitic bipolar device in the thin film. At the onset of the kink effect behavior, the parasitic bipolar device is triggered to turn on with its current gain as a function of the difference in the bandgap narrowing between the base and the emitter: $\beta \alpha \exp(\Delta E_{gb} - \Delta E_{ge}/kT)$ [3]. Due to the higher mechanical stress from STI, the bandgap narrowing in the emitter/source ΔE_{ge} is larger than that in the base/channel region ΔE_{gb}. Therefore, the function of the parasitic bipolar device in the thin film of the device with the shorter S/D length of 0.17 μ m becomes weaker as indicated by the smaller current gain. As a result, the kink effect behavior occurs at a higher V_D. The bandgap narrowing induced effect on the parasitic bipolar device is offset by the enhanced impact ionization due to the bandgap narrowing in the surface high electric field region. Considering the bandgap narrowing in the impact ionization model for simulation, the bandgap narrowing-related parasitic bipolar device effect on the kink effect is reduced.

Conclusions

In this paper, the STI-induced mechanical stress-related kink effect behaviors of the 40nm PD SOI NMOS device has been reported. The kink effect behaviors occur at a higher V_D for the 40nm PD device with a smaller S/D length of 0.17 μ m to the higher body-source bandgap narrowing effect on the parasitic bipolar device coming from the higher STI-induced mechanical stress, offset by the enhanced impact ionization from the bandgap narrowing in the surface high electric field region.

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Variation-Tolerant Design by Selective Body-Biasing Control on PD-SOI for Yield Improvement

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1. Abstract

Mitigating the impact of process variation derived from aggressive technology scaling has been becoming one of agonizing challenges no longer among only device engineers. In order for circuit designers to suppress the fluctuations in circuit performance, a variation-tolerant design methodology is strongly expected. We propose a body-biasing control on PD-SOI devices which satisfies both timing and leakage power constraints based on the leakage monitor circuit. Simulation results have shown improvement in the design yield up to 91%.

2. Introduction

In recent years, increase in process variations with aggressive technology scaling significantly degrades circuit performance and chip yield [1]. Although predominant factors in variability included lot-to-lot / wafer-to-wafer / die-to-die variations in the past, within-die (intra-die) variations have been becoming a major concern in recent technologies [2]. An adaptive body-biasing control [3], widely known as post-silicon compensation, basically employs a delay monitor and mitigates the impact of process variation. However, the body-bias for an entire chip unfortunately causes exponential increase in leakage power due to the throughout lowered threshold voltage. Therefore, we propose a selective body-biasing control on PD-SOI, where the body of each transistor can be individually controlled [4], in order to satisfy the constraints on not only the delay but also the leakage power.

3. Selective body-biasing control considering delay and leakage power

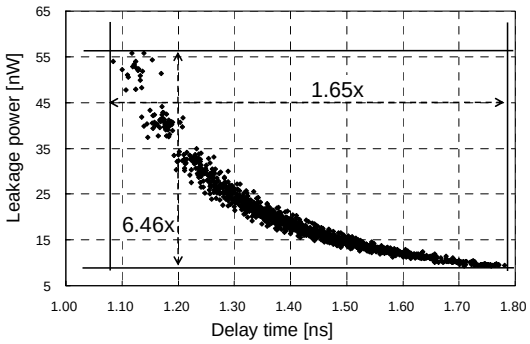

Fig.1: *Correlation between the delay and leakage power due to inter/intra-die variation in V_{th}*

The impact of inter / intra-die variation on delay time and leakage power with the benchmark circuit *cm85a* [5] has been analyzed by a 1,650-point monte-carlo simulation as summarized in Fig. 1. Since there is a correlation between the delay time and the leakage power, the use of leakage monitor circuits [6] shown in Fig. 2 compensates the delay time fluctuation by providing a body-bias properly. However, a body-bias for the entire chip in turn sacrifices a design yield in terms of leakage power constraint.

Then, we propose a fine-grained body-biasing control with SOI devices to suppress the increase in leakage power. The variation compensation block shown in Fig. 3 consists of a leakage current monitor, a control circuit, and a 16:1 multiplexer (MUX) selecting a body-bias voltage. Based on the leakage monitor output (V_{sen}), the magnitude of body-bias is determined by the control circuit, and the proper forward body-bias voltages ($V_{body\text{-}n}$, $V_{body\text{-}p}$) up to 600 mV are provided for logic circuits and the leakage current monitor as a feedback control. Here, a forward body-bias is provided only to the cells on the several critical paths with possibility of

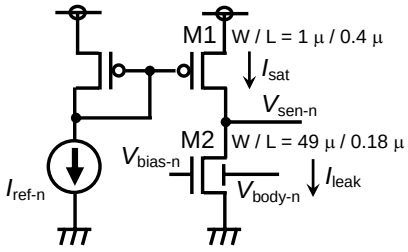

Fig.2: *Schematic of leakage current monitor [6]*

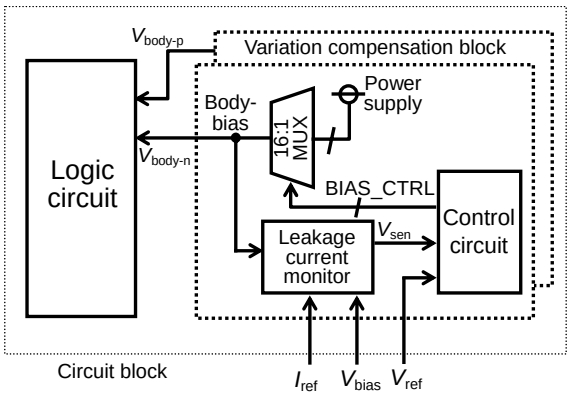

Fig.3: *Block diagram of variation compensation circuit*

timing violation due to variability. For the remaining cells satisfying the timing constraint, the zero body-bias is assigned. Here, the design overhead in wire length due to the selective body-bias is 11 % compared with the conventional body-tied (zero body-bias) structure.

4. Simulation results

In order to evaluate the proposed scheme, we have performed SPICE simulation with MCNC benchmark circuits [5] based on 0.18 μm PD-SOI process when V_{DD} = 1.0 V and $V_{th\text{-}n}$ / $V_{th\text{-}p}$ = 0.22 / – 0.36 V. We have calculated the fluctuations of delay time and leakage power when assuming inter / intra-die variations in the gate length (L) as a Gaussian distribution where 3σ corresponds to 15 % in L, and estimated the total design yield in terms of both timing and leakage constraints. In the variation compensation circuit, the current sources ($I_{ref\text{-}n}$, $I_{ref\text{-}p}$) are set to 100 μA, the reference voltages are determined to $V_{ref\text{-}n}$ / $V_{ref\text{-}p}$ = 0.62 V / 0.77 V, and the voltage sources are fixed to $V_{bias\text{-}n}$ / $V_{bias\text{-}p}$ = 0.2 V / 0.7 V. These current and voltage sources are supplied as external inputs.

With respect to the distribution of critical path delay in *cm85a* illustrated in Fig. 4, both the body-bias for entire circuit and the proposed selective body-bias not only shorten the delay time but also mitigate the delay variation. The standard deviation σ is reduced by 50 %, and the coefficient of variation (CV: σ/μ) is improved by 4.7 point.

In terms of the leakage power which is susceptible to the variation in V_{th}, it results in the σ/μ of 43 % for the no body-bias in *cm85a* as summarized in Fig. 5. The use of body-bias for the entire circuit reduces the σ/μ down to 8.9 %. On the other hand, although the σ/μ stays in 11 % in the proposed scheme, the mean of leakage power is reduced by 23 %. Thus, the proposed scheme suppresses the increase in the mean of leakage power due to the body-bias from 2.6x down to 2.0x compared with the no body-bias.

Finally, we discuss the total design yield in terms of both timing and leakage constraints. Fig. 6 indicates the distribution of delay time and leakage power with their constraints. Here, even though the body-bias for the entire circuit achieves a delay yield of 97 %, 87 % of the circuits violate the leakage constraint due to the throughout lowered threshold voltage. However, the proposed scheme realizes a total design yield of 91 % since the leakage power is reduced owing to the locally lowered threshold voltage in the selective body-biasing control.

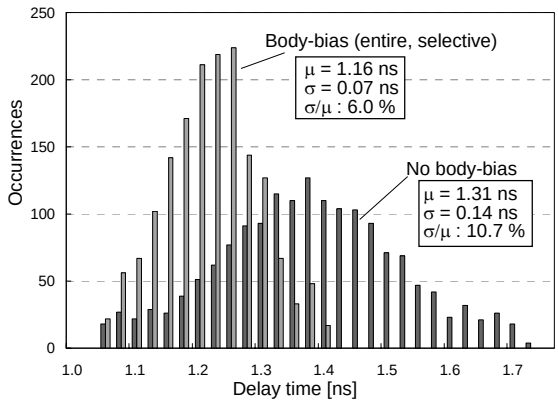

Fig.4: *Distribution of critical path delay in cm85a*

5. Conclusion

In this paper, we have proposed a variation-tolerant design methodology which not only mitigates the delay variation but also reduces the leakage power derived from the body-biasing control. The proposed selective body-biasing control on PD-SOI devices, where the threshold voltage of each transistor can be individually controlled, provides the body-bias within the limitation on the leakage power. As a result, the proposed scheme shortens the delay time and mitigates the delay variation such like the body-bias for the entire circuit. Moreover, the total design yield in terms of both delay and leakage power constraints is expanded to 91 %.

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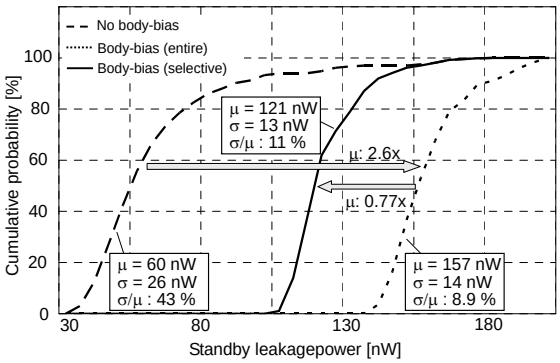

Fig.5: *Cumulative probability of leakage power*

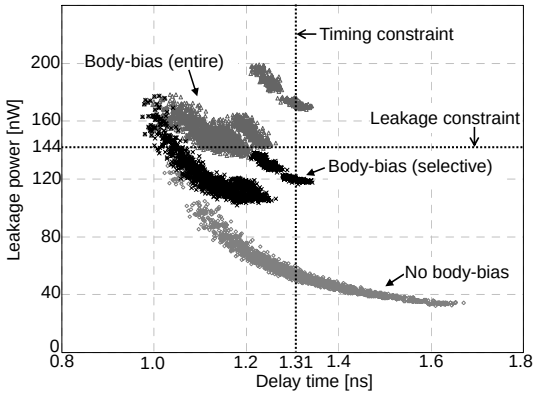

Fig.6: *Total design yield in terms of delay and leakage power constraints*

SOI-based 2D- and Si-based 3D photonic crystals

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1. Abstract

We present a study of a generic approach to integrate 2D photonic components embedded in 3D PhCs and couple them to single- and multi-mode ridge waveguides. 3D photonic crystals are fabricated by spatially selective self-assembly of silica and PMMA beads into an fcc-type lattice on a patterned SOI substrate. 2D defect layers are fabricated in 3D PMMA opals by controlled removal of determined beads by electron beam lithography. Simulations of mode matching and coupling efficiencies are presented, which provide guidelines for the fabrication of experimental structures on inverted silicon opals. This is an example of SOI-based nanophotonics illustrating the relevant issues of heterogeneous integration in this field.

2. Introduction

The advantages of photonic crystals (PhCs) over classical optical materials hold the promise of ultra-compact optical components to, for example, guide light or control the spontaneous emission.

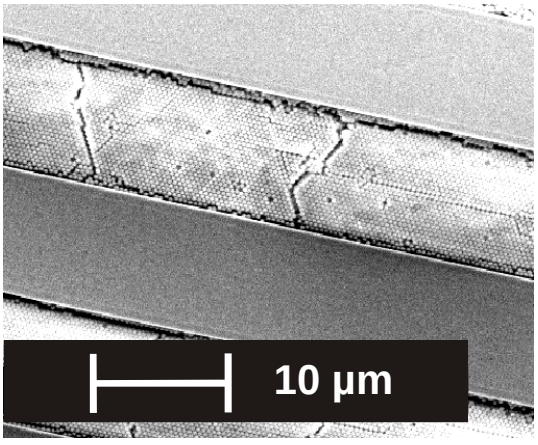

Fig.1: *PMMA opal sedimented with high spatial selectivity; bead size 370 nm.*

There are, however, multiple challenges on the way to the realization of PhC based photonic components and their integration onto a chip. To fabricate silicon based integrated components and eventually an all-optical microchip, one needs a thorough knowledge and control of various physical principles including mode matching, waveguiding and coupling processes. The necessary feasible technological concept for spatial selectivity and fabrication methods were developed for this purpose. The growth method is highly selective and fast as well as compatible with the state-of-the art silicon technology as described below.

3. Proposed Structures

An approach proposed by Chutinan et.al. [1] offers particular interesting possibilities for the fabrication of all-optical devices with 2D PhC layers based on dielectric pillars sandwiched between two 3D PhCs. The main component (waveguides or splittersg or cavities,, among others) will be incorporated in the 2D layer and is achieved with specific patterning using electron beam lithography [2]. The 3D PhC on top and bottom provides field confinement in the vertical direction. For a successful integration of these two structures, mode matching between the 2D and 3D PhC components must be provided, i.e., the eigenmodes of the 2D PhC layer have to match the ones at the interface of the 3D PhC.

We present the results of our integration study of 2D photonic components embedded in 3D PhCs and coupling to single-mode or multi- ridge waveguides. The 3D PhC “base” is fabricated by a variation of the vertical deposition technique (VDT) [4] with an acoustic field applied to increase the crystalline quality. The resulting structures show an impressive fcc arrangement free of distortion throughout the whole sample in all 3 dimensions [5, 6, 7]. (Fig.1).

The 2D defect layer is inscribed by electron beam (e-beam) lithography either onto the top layer of the

polymer opal (Fig 3) or on a layer of resist deposited on top of the silica opal to form a template for passive or active devices [2,3]. After processing the defect layer, a second 3D PhC is assembled on top and the whole structure can be subsequently inversed to achieve a full photonic bandgap. (Fig.4)

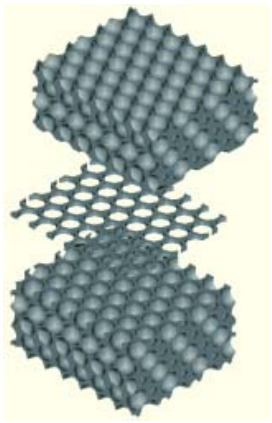

Fig.2: *Exploded view of proposed structure. The main functionality is incorporated in the 2D PhC layer.*

Matched with an incoming waveguide, these structures will enable us to control emission and/or propagation directionality. We present simulations on mode matching and coupling efficiencies as well as optical characterisations of buried 2D defect layers in PMMA opals (Fig. 2, 3). Silica opals have been selectively grown on patterned SOI substrates. Simulation results showed that in an as-grown inverted silicon opal, the maximum transmission is around 7 % due to reflected light which subsequently couples into the silica walls and substrate. Light then propagates in these media and some part of it reaches the output ridge waveguide. This effect is expected to be reduced with the enlargement of the hexagonal well size. However, the fabrication of actual structures that enable a good control of mode matching and losses is still a major challenge.

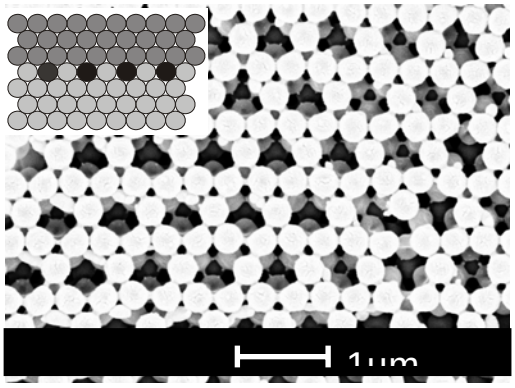

Fig. 3. 2D defect layer inscribed into an PMMA opal with bead size 370 nm by e-beam lithography. The inset indicates the means of fabricating a buried defect layer by this method.

4. Conclusion

Opals with a high crystalline quality have been fabricated. Pre-patterned SOI substrates lead to. The used growth method exhibits a high spatial selectivity. 2D defect layers and buried defect layers have been fabricated on 3D PMMA opals by e-beam lithography. FDTD simulations are used to understand and determine mode structures for emitters imbedded in 3D PhCs and to find a design template most useful to light emitter structures and coupling light to mode-matched rib waveguides. The simulation results are in good agreement with first experimental results. This approach is promising, yet requires a lot of future work. It would, however, open the door to compact silicon-based photonic circuits.

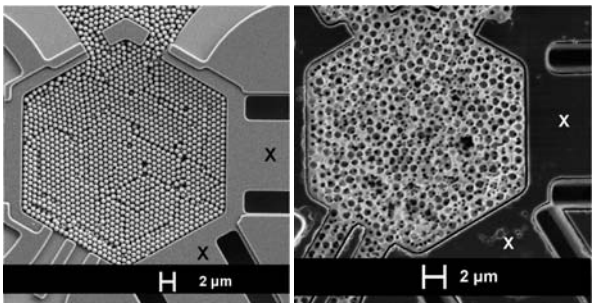

Fig.4. *Example for silica opal template (bead size 810 nm) connected to ridge waveguide (marked with "x") (left) and inverted structure (right).*

5. Acknowledgements

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Study of the Gate Direct Tunneling Current in Symetric DG MOSFET Based on an Analytic Potential Model

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1. Abstract

The double-gate (DG) MOSFET has been considered as the most promising device structure to extend CMOS scaling into the nanometer regime [1] (see Fig. 1). However, gate direct tunnelling currents associated with the ultrathin gate oxides are a physical limiting factor. In this study we propose an extension of an analytical classical potential model for symmetric DG MOSFET [2] to take into account quantum effects and so compute the gate current. Our results are compared with those computed with SCHRED tool simulator [3].

2. Analytic Potential Model for SDG MOSFETs

In a SDG MOSFET the same voltage is applied to the two gates having the same work function and the thin silicon is lightly doped and the depletion charge is negligible. Since there is no contact to the silicon body, the energy levels are referenced to the conduction band of the n^+ source-drain. So that one can write Poisson's equations for the silicon region as [2]:

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon_{si}} n_i e^{q\varphi/kT}$$

where q is the electronic charge, ε_{si} the permittivity of silicon and n_i intrinsic carrier density. Integrating twice the potential as a function of *x* can be obtained:

$$\varphi = \varphi_0 - \frac{2kT}{q} ln\left[cos\left(\frac{q^2 n_i}{2\varepsilon_{si} kT} e^{q\varphi_0/2kT} x \right) \right],$$

where φ_0 is the potential at the center of the silicon film.

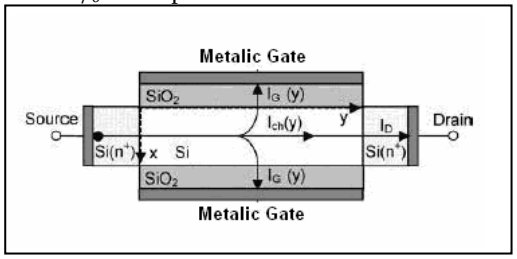

Fig.1: *Sketch of the geometry of the DG MOSFET structure and illustration of the gate tunneling current flowing into the front and back gates..*

Fig. 2 shows the band diagram of a DG MOSFET along the vertical direction.

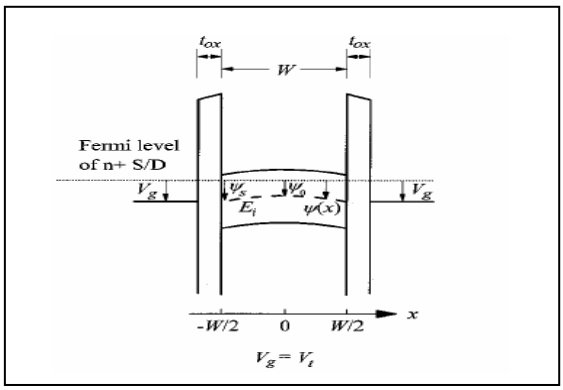

Fig.2: *Schematic band diagrams of a symmetric DG nMOSFET along the x direction.*

3. Direct Tunneling Current Model

Once the classical model of the potential as a function of *x* is modified to take into account quantum effects, the Schrödinger's equation is solved to obtain the inversion charge density N_{ij} of the *ith* valley and *jth* subband using the 2D electron density and Fermi-Dirac statistics. On the other hand we have chosen a modified WKB method to calculate the electron transmission probability, and within the electron effective mass approximation, it can be written in the form of [4]:

$$T = T_R \cdot T_{WKB},$$

where T_{WKB} is the usual WKB approximation of the transmission probability and T_R is the correction factor taking into account the reflections from oxide boundaries. Combining the results from the quantum mechanical calculation, one can readily obtain the total direct tunnelling current

$$J = \sum_{ij} J_{ij} = q \sum_{ij} N_{ij} T_{ij} f_{ij} \ ,$$

where f_{ij} is the impact frequency of electrons hitting the appropriate oxide barrier plane.

4. Calculation of Direct Tunneling Current with Schred

Using Schred tool of nanohub which solves in a self-consistent manner Schrodinger and Poisson's equations, we have obtained the profile of the conduction band from the SDG MOSFET structure allowing us to calculate N_{ij}, T_{ij} and f_{ij} . It has been done for several gate voltage and different thicknesses for silicon body and the results of direct tunnelling are showed in figure 3.

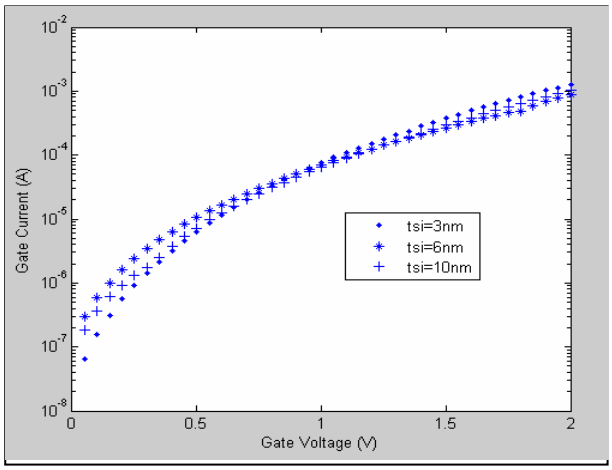

Fig.3: *Gate voltage dependence of the gate tunnel current in quantum calculations for 3,6 and 10 nm of body thickness with Schred tool.*

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Germanium on Sapphire By Wafer Bonding

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1. Abstract

Similar thermal coefficients of expansion between germanium and sapphire make the bonding of germanium to sapphire a reality. Germanium directly bonded to sapphire results in microvoid generation during post bond annealing. Deposition of a silicon dioxide layer by Plasma Enhanced Chemical Vapour Deposition (PECVD), prior to bonding, results in a microvoid free bond interface after annealing. Grinding and polishing of the subsequent germanium layer has been achieved leaving a 7µm thick GeOS substrate. Sub micron GeOS layers have also been achieved with hydrogen/helium implantation and layer transfer.

2. Introduction

Germanium provides advantages such as, higher carrier mobility and compatibility with emerging high-k dielectrics. For optimized performance of SOI devices, in terms of mobility, the ITRS road map points to strained SiGe layers and germanium layers on insulator (GeOI). These materials require high k gate dielectrics. In these circumstances Ge becomes an attractive material for MOSFET technology.
Silicon on sapphire technology (SOS) has been employed for many years [1], offering the same advantages as SOI. Sapphire substrates are often preferred in rf and MMIC applications as they have excellent dielectric properties, which make it an excellent substrate for passive elements. Sapphire's high resistivity also ensures low crosstalk through the substrate between noisy digital and sensitive analogue components. Sapphire will also provide reduced self-heating effects due to its higher thermal conductivity compared with that of silicon dioxide. Combining the two substrates, i.e., Germanium on Sapphire (GeOS), provides a unique platform for system on a chip (SOC) technology.
The GeOS platform provides good heat removal, low rf losses and low crosstalk for high frequency circuits, a lattice matched substrate for the growth of GaAs and matched coefficient of thermal expansion. This work describes the realization of such a platform.

3. Experimental

Wafer bonding was carried out between 100mm diameter electronic grade P type germanium substrates, 160µm thick and 100mm diameter C plane sapphire substrates, 500µm thick. Initial bonding was carried out at room temperature between the germanium and the sapphire with no interface oxide. Following on from this a PECVD silicon dioxide layer was utilised at the bond interface. This layer was deposited, prior to bonding, on the sapphire substrate. Subsequent bond annealing was carried out at temperatures ranging from room temperature to 600^{o}C in a N2 ambient. Prior to bonding, the sapphire substrates received a standard silicon based cleaning schedule consisting of SPM and modified agitated SC1 solution. The germanium substrates received an alcohol based clean followed by NH4OH activation [2]. Two different thinning techniques were investigated. Grinding and polishing was employed for > 1µm GeOS and co-implant layer transfer for <1µm GeOS.

4. Results

As the sapphire substrates are transparent from the sapphire side, visual inspection of the bond interface can be easily achieved. Figure 1 shows the bond interface of a germanium substrate directly bonded to a sapphire substrate at room temperature.

Fig.1: *Germanium to sapphire room temperature bond interface.*

Voids present are due to particulates or defects on the germanium surface which have not be removed by the non optimised germanium cleaning schedule. Subsequent annealing at temperatures above 200C results in micovoid formation at the interface. Figure 2 shows the bond interface after annealing at 500^{o}C. In the case of silicon bonded to sapphire with no interfacial

oxide, microvoids are present on annealing. This is thought to be due to the two single crystal surfaces not being able to absorb moisture during annealing[3]. Water can also form GeO, which is known to be volatile, leading to micovoid generation.

Fig. 2: *Germanium/sapphire bond interface after anneal at 500°C.*

This would be similar in the case of germanium bonded to sapphire, hence the microvoids shown in figure 2. Also in the silicon on sapphire case, silicon bonded directly to sapphire would not be able to withstand annealing above 250°C. The silicon would fracture as a result of the difference in expansion coefficients. In this case the germanium and sapphire have similar coefficients of expansion resulting in a no fracturing of the germanium even after annealing at 500°C as shown here. In order to avoid microvoid formation during annealing a PECVD silicon dioxide layer was deposited at 300°C onto the sapphire substrate. After densification and polishing treatments the oxide-coated sapphire was bonded to a germanium substrate. Figure 3 shows the bond interface both after room temperature bonding and after annealing at 500°C.

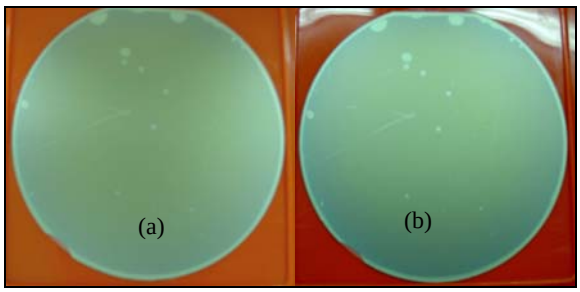

Fig.3: *Germanium/oxide coated sapphire bond interface a) Roon temperature, b)after 500°C anneal*

As can be seen from figure 3 no microvoids are present after annealing at 500°C. In this case the silicon dioxide layer has absorbed any of the annealing by-products[4].
Thinning of the germanium layer was attempted using both grinding and polishing technology and layer transfer technology. Grinding was performed on the germanium/oxide coated sapphire bonded pair using a Shibiyama precision grind system. This allowed the samples to receive a coarse grind followed by a fine grind leaving a GeOS thickness of less than 10µm. Subsequent specialized polishing of the germanium layer removes grind damage leaving 7µm thick germanium layers on oxide coated sapphire. The final polished layer is shown in Figure 4.
In order to realise sub micron single crystal layers on sapphire, germanium substrates were co-implanted with Hydrogen and Helium Through a PECVD oxide layer. Once bonded, the PECVD oxide coated sapphire samples were given a bond strength enhancement anneal at 150°C for 72hrs followed by a layer splitting anneal at 300°C. Under these transfer conditions a 0.2µm GeOS layer was produced.

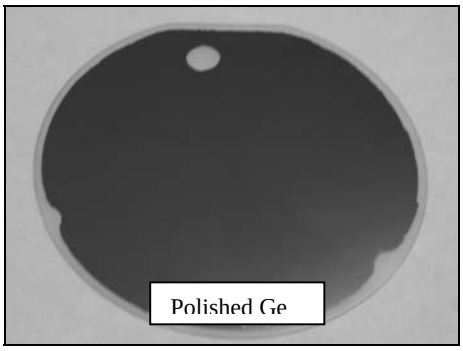

Fig. 4 : *7µm polished single crystal germanium layer on oxide coated sapphire.*

5. Conclusions

Germanium on sapphire by wafer bonding can be achieved. Annealing without an interfacial oxide results in microvoid formation above 200°C. Depositing a PECVD silicon dioxide layer prior to bonding enables absorbs by-products during bond annealing stopping microvoid generation. Thinning by grinding and polishing establishes a >1 micron platform while layer transfer provides a sub micron platform.

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Equivalent Oxide Thickness of SOI-GAA devices

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1. Abstract

In this work, the behavior of the gate capacitance of Gate-All-Around (GAA) devices with square cross section has been studied. It is shown that the Equivalent Oxide Thickness (EOT) used for planar devices is not valid anymore, and a new expression is obtained by using an approximate model of Metal-Insulator-Metal capacitors.

2. Introduction

Multiple Gate (MuG) Silicon-On-Insulator SOI MOSFETs have been presented in the literature as a good option for device scaling, as they allow a better electrostatic control of the channel and therefore a reduction of the Short Channel Effects (SCEs) [1]. Furthermore, the use of MuG MOSFETs combined with high-κ insulators can be an interesting option [2]. However, some key features referring to gate capacitance of this kind of devices are still lacking. Actually, previous works have demonstrated that the Equivalent Oxide Thickness (EOT) used in the literature is not valid for this kind of devices and a new expression has recently been presented for the case of cylindrical Surrounding Gate Transistors (SGTs) [3]. In this work we have considered a GAA with square cross section, and its capacitance will be studied as a function of different parameters.

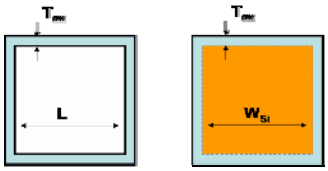

Fig.1: *MIM capacitor (left) and GAA device (right).*

3. Results

When non planar devices are considered, the insulator capacitance becomes a function of the device geometry, and in most cases it becomes quite involved to obtain an analytical expression. This is the case for the device under study. As a first approximation, we have used a Finite Element Method to solve the Laplace equation for the Metal-Insulator-Metal (MIM) capacitor shown in Fig. 1 (*left*). In this case the capacitance only depends on the ratio T_{ox}/L, where T_{ox} is the physical thickness of the insulator and L the side of the inner square of the capacitor; Fig. 2 shows the results along with two different analytic approximations. The first one corresponds to the normalized capacitance obtained for planar devices with the same overall gate length (that has been used in other works to model the EOT of this kind of devices [4]). The second one is an expression obtained from curve-fitting:

$$C_{ox} = \frac{5\varepsilon_{ox}}{\ln\left(1+\frac{5}{4}\frac{T_{ox}}{L}\right)} \qquad (1)$$

It is interesting to note that according to the results shown in Fig. 2, for very small T_{ox}/L ratios the behavior of the square capacitor is quite similar to a planar capacitor with the same overall gate-insulator length. On the other hand, for greater T_{ox}/L ratios, the difference between the capacitance of this square device and the corresponding to a similar planar device grows. This is of particular importance when high-κ materials are used as gate insulators. In this case, usual T_{ox} considered are in the range of a few nanometers. For small devices (around or bellow 10nm of Silicon thickness) the ratio T_{ox}/L is not small enough to consider the planar capacitance expression as a good approximation.

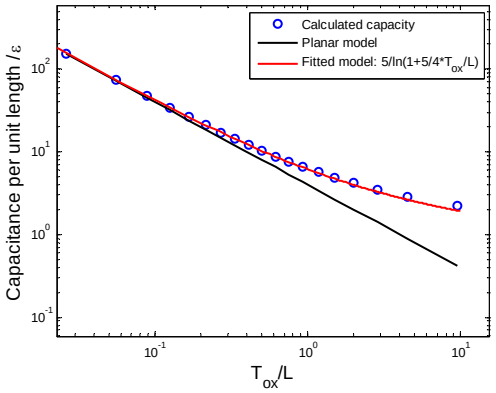

Fig.2: *Capacitance of a square MIM capacitor.*

Our next step has been to study the validity of Eq. (1) in order to find an EOT expression that can be used for SOI-GAA. To do so, the capacitance (1) must be equated when two different gate dielectrics are

employed, replacing L by W_{Si}. SiO_2 will be the first material (ε_{ox1}, T_{ox1}), and the second one is the high-κ insulator(ε_{ox2}, T_{ox2}). Hence, a new expression can be found for the equivalent oxide thickness of the high-κ material:

$$T_{ox2} = \frac{4}{5} W_{Si} \left[\left(1 + \frac{5}{4} \frac{T_{ox1}}{W_{Si}} \right)^{\varepsilon_{ox2}/\varepsilon_{ox1}} - 1 \right] \qquad (2)$$

In order to study the suitability of the previous equation, we have calculated the QED as a function of the gate voltage for three devices with $W_{Si}=H_{Si}=10nm$, $N_A=10^{12}cm^{-3}$ and a midgap metal gate with work function $\Phi_m = 4.61eV$ [5]. The insulator of the first of them was SiO_2 with $T_{ox} = 1nm$ while for the other two devices HfO_2 was used with two different values: *6.41nm*, corresponding to the EOT of a planar capacitance, and *9nm*, obtained from (2). Fig. 3 shows the results obtained. It can be seen that the use of the new expression for the EOT produces much more accurate results than the typical one used for planar devices. It has been observed that the QED obtained for the devices with 1nm thickness SiO_2 and 9nm thickness HfO_2 is very similar. Therefore, the use of Eq. (2) not only permits similar total charge values, but it also to get the same gate control on the channel.

Figures 4 and 5 show the charge density per unit length as a function of the EOT when the device dimensions are modified. Two approaches for the EOT have been used: Eq. (2) and planar capacitance expression. In Fig. 4, the silicon width and height are kept constant but the oxide thickness is modified, thereby changing the T_{ox}/W_{Si} ratio. Fig. 5 shows the result obtained when the same T_{ox}/W_{Si} relation is kept constant but the silicon thickness is scaled. In both cases excellent agreement is achieved only when Eq. (2) is used for the EOT.

4. Conclusions

The gate capacitance of GAA devices, and its dependence with the oxide thickness, has been studied. A new expression has been obtained for the EOT from a Metal-Insulator-Metal capacitor with same geometry and dimensions than the GAA. The new expression has been used when SiO_2 is substituted by HfO_2, and an excellent agreement has been obtained for devices with different dimensions. As a conclusion, the EOT expression based in the gate capacitance of planar devices, should not be used anymore for MuG devices.

Acknowledgments

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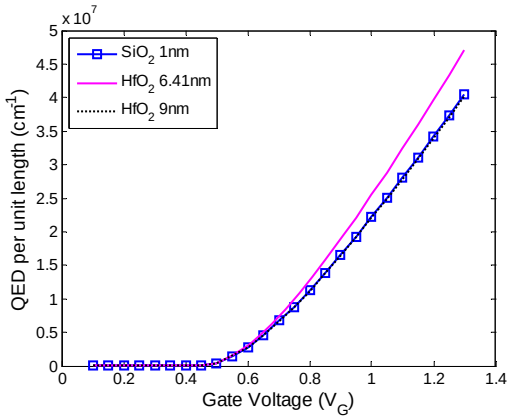

Fig.3: *QED per unit length as a function of V_G for three devices with $W_{Si}=H_{Si}=10nm$, $N_A=10^{12}cm^{-3}$ and different gate insulators: 1nm thickness SiO_2 and HfO_2 with 6.41nm and 9nm thickness.*

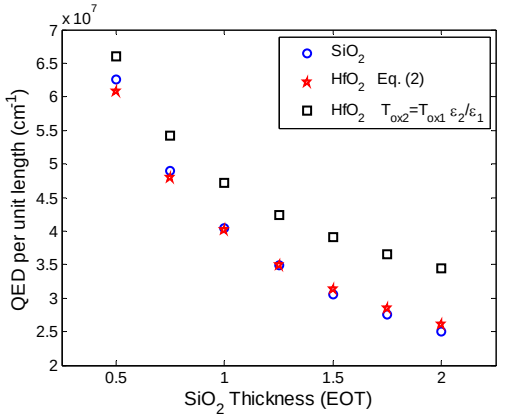

Fig.4: *QED per unit length as a function of the EOT for devices with $W_{Si}=H_{Si}=10nm$ and two different gate insulator materials: SiO_2 and HfO_2. Two approaches have been considered for HfO_2 thickness: the planar one and Eq. (2).*

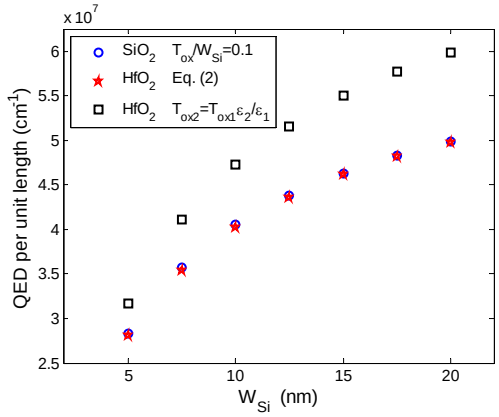

Fig.5: *QED per unit length as a function of W_{Si} for devices with T_{ox}/W_{Si} =0.1 and two different gate insulator materials: SiO_2 and HfO_2. Two approaches have been considered for HfO_2 thickness: the planar one and Eq. (2).*

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Current-voltage model for Schottky-barrier graphene based transistors

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1. Abstract

A low complexity computational model of the current-voltage characteristics for graphene nano-ribbon (GNR) field effect transistors (FET), able to simulate a hundred of points in few seconds using a PC, is presented. For quantum capacitance controlled devices, self-consistent calculations of the electrostatic potential can be skipped. Instead, analytical closed-form electrostatic potential from Laplace's equation yields accurate results compared with that obtained by self-consistent Non-Equilibrium Green's Functions (NEGF) method.

2. Introduction

Graphene has recently emerged as a potential candidate material for nanoelectronics due to its electronic properties[1]. Geometrically is a monolayer of carbon atoms tightly packed into a 2D honeycomb lattice known to be a zero-gap material that could be fabricated using mechanical exfoliation[2] and epitaxial growth[3]. Interestingly, graphene could be patterned in nano-ribbons, using planar technologies as electron beam lithography and etching[3-4], having properties theoretically predicted to range from metallic to semiconducting depending on their width and edges[5]. This band-gap tuning capability and the possibility of large-scale integration using planar technologies open a route towards an all-graphene electronic nanodevices and circuits. Notably, recent studies[2] reported mobilities for electrons and holes in graphene of the order of 10^4 $cm^2/V{\cdot}s$. However, mobility for GNRs is expected to have smaller values than graphene, with an inverse dependence with the band gap[6], but conclusive experimental studies still lack. At this early state of development of GNR technology it seems timely to develop models of building blocks helping to conduct experiments in the same line as previously reported for carbon nanotube based devices[7-8]. This work presents an easy to implement model for analyze or design the current-voltage (I-V) characteristics of GNR-FETs in connection with physical parameters, such as GNR width (W) and gate insulator thickness (t_{ins}), and electrical parameters, such as SB height (φ_{SB}). The proposed approach prevents the computational burden that self-consistency implies by using a closed-form electrostatic potential from Laplace's equation. This simplification yields accurate results compared with self-consistent results from NEGF method[9] in the relevant limit dominated by the GNR quantum capacitance (C_{GNR}). Note that it appears to be the interesting case for advanced applications because the ability of the gate to control the potential in the channel is maximized.

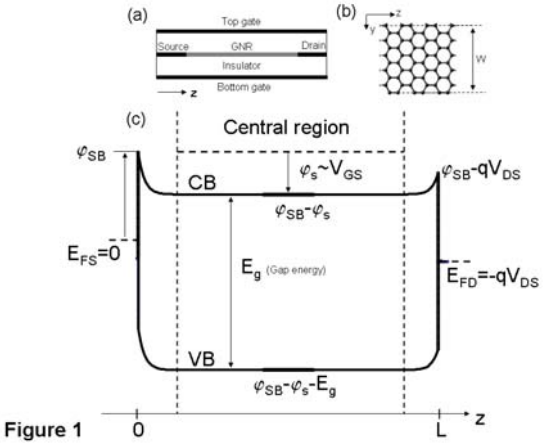

Fig.1: *Geometry and band diagram of the GNR-FET: (a) cross-section, (b) top view of the armchair shaped edge GNR forming the channel, and (c) sketch of the spatial band diagram along the transport direction.*

3. Model

Let us consider a semiconducting GNR contacted with metal electrodes acting as source/drain (S/D) reservoirs [Figs. 1(a)-(b)]. The resulting spatial band diagram along the transport direction is sketched in Fig. 1(c). For a long-channel transistor the potential energy at the central region is exclusively controlled by the gate electrode and I further assume that: (i) C_{GNR} dominates respect the total gate capacitance, and (ii) $C_{GNR} \approx 0$. The validity of the latter assumption depends on the quantum confinement strength. In the quantum capacitance limit the problem can be highly simplified because the electrostatic is governed by the Laplace's equation, instead of the more involved Poisson's equation, having two important consequences affecting the band diagram: (i) the central region shifts following the gate voltage on a 1:1 ratio; and (ii) the band edge

near the contact region has a simple analytical closed-form. The current through the structure is calculated by means of the Landauer formula. The current carried by each subband is splitted into tunneling and thermionic components for carriers injected through and above the barrier respectively. Assuming phase-incoherent transport, transmission probabilities are computed through the S/D regions by WKB method separately and then combined incoherently for obtaining the global transmission entering Landauer's formula.

4. Model assessment

To assess the model I have simulated an armchair edge GNR channel with a ribbon index N=12, presenting a width W≈1.35 nm. The simulations were done at room temperature and the GNR bandgap assumed to be 0.83 eV. A gate insulator thickness t_{ins}=2 nm is assumed. The metal S/D is directly attached to the GNR channel, and the SB height for both electrons and holes between the S/D and the channel is half of the GNR bandgap $\varphi_{SB}=E_g/2$. The flatband voltage is zero. A power supply of V_{DS}=0.5 V is used. The nominal device parameters are varied to explore different scaling issues. The transfer characteristic exhibit two branches at the left and right from the minimum off-state current (Fig. 2). This minimum occurs at $V_{GS}=V_{DS}/2$ for a half-gap SB height being the spatial band diagram symmetric for electrons and holes and the respective currents are identical. This bias point is named the ambipolar conduction point. When V_{GS} is greater (smaller) than $V_{DS}/2$, the SB width for electrons (holes) is reduced, producing a dominating electron (hole) tunneling current. The effect of power supply up-scaling is to further reduce the SB width at the drain side making it more transparent and allowing more turn-on current to pass. The output characteristics of the SB GNR-FET are shown in the inset of Fig. 2. The dominant current for the nominal device is electron tunneling and exhibit linear and saturation regimes. Increasing V_{GS} produces a larger saturation current and voltage due to further transparency of SB and the expansion of the energy window for carrier injection from the source into the channel. Besides, downsizing W increases the gap and hence φ_{SB} in the simulation (assumed to be $E_g/2$) further reducing the current due to a less populated higher energy levels [Fig. 3(a)], but the resulting on-off current ratio, a figure-of-merit for digital circuits, is largely improved. Reducing the SB heigth respect to the half-gap case favors electron transport and results in a parallel shift of the ambipolar conduction point towards smaller gate voltages and asymmetries between the left and right branches of the transfer characteristic [Fig. 3(b)]. Also note that for low φ_{SB} and V_{GS}, the thermionic electron current exceeds the tunneling electron current and should be taken into account for computing the off-state current.

In conclusion, a simple model for the I-V characteristics of Schottky-barrier graphene field effect transistors which captures the main physical effects governing the operation of this device has been presented. Typical simulation of a I-V characteristic with 100 points takes no more than few seconds on a PC. The results obtained applying this model to prototype devices are in close agreement with a more rigorous treatment based on the NEGF approach, thus validating the approximations made. The presented model is intended to assist at the design stage as well as for quantitative understanding of experiments involving GNR-FETs.

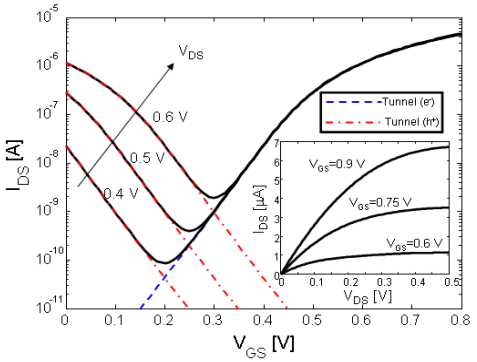

Fig.2: *Transfer and output characteristics (inset) for the nominal GNR-FET. Decomposition of the total current in electron and hole tunneling contributions are shown.*

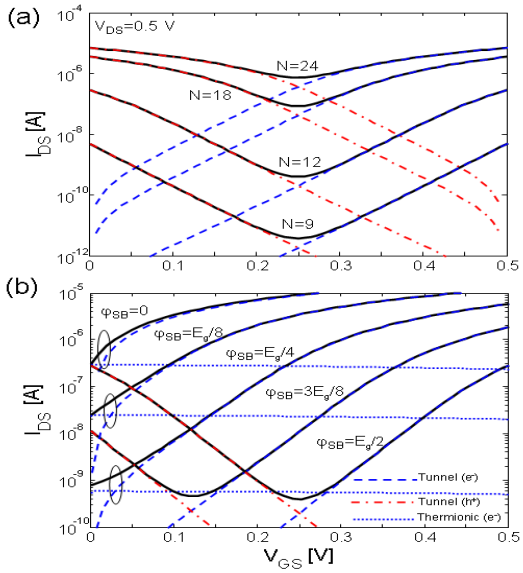

Fig.3: *Influence of the GNR width (a) and SB height (b) in the transfer characteristics.*

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Oxide free wafer bonding of silicon-on-silicon carbide substrates

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1. Abstract

The manufacturing of a novel high thermal conductive Si-on-SiC substrate is demonstrated. The silicon is connected to semi-insulating silicon carbide directly, without any intermediate silicon oxide, which may increase thermal dissipation. Previously, bonding without oxide has been troubled with bubble formation during thermal heat treatment. By using ventilation grids within the surface, the problem is circumvented. By using an intermediate layer of amorphous silicon, the grid can be omitted.

2. Introduction

Recently, our group presented MOSFET devices on Si-on-SiC for the first time [1]. In this work, the manufacturing of the hybrid substrate is presented.

Wafer bonding is extensively used in SOI manufacturing, both as bond and etch-back, and in combination with SmartCut. In these cases the insulator is the silicon dioxide thermally grown on one or both wafers prior to bonding. The buried oxide exhibit favourable electrical properties, but its use is hampered by the oxide's poor thermal conductivity. In order to improve the thermal properties, efforts have been made to replace the oxide with for example diamond [2], AlN [3], and sapphire [4].

Besides low surface roughness and cleanliness, the secret for success of bonding full wafers lies in the oxide's high solubility of low molecular species present at the bond [5]. When the oxide is omitted, all desorbed species from water or hydrocarbons have to diffuse to the edge of the wafers in order to escape. During this journey they are likely trapped. The trapped molecules then form nucleation centres where more molecules gathers and eventually form bubbles. This is the problem to be solved.

3. Experimental

Two inch silicon carbide wafers (SiCrystal), 100 mm Unibond SOI (Soitec), and 100 mm standard bulk wafers (Topsil) were used in the experiments.

SiC and SOI wafers were rendered hydrophilic in HNO_3, 69wt.-%, at 70°C for ten minutes. The wafers were rinsed, spun dry, and then placed in surface contact. The wafers formed a bond immediately upon contact, but pressing with the tweezers could further increase the bond area. After inspection, the bond was strengthen by a thermal anneal at 1000°C in N_2 for an hour.

In later experiments, a grid was formed in SOI wafer device layer using lithography and dry etching prior to bonding. Also, the SiC was deposited with 200 nm Si using low-pressure chemical vapour deposition (LPCVD) at 560°C with SiH_4 as precursor. Bonding between gridded SOI and SiC was carried out as above. The SOI handle wafer was removed with tetra methyl ammonium hydroxide, 25 wt.-% at 90 °C, and the buried oxide with HF, 10 wt.-%.

In an additional experiment, silicon wafers were deposited with around 200 nm LPCVD Si at increasing temperatures from 555°C to 620°C. These wafers were analysed with atomic force microscopy and by x-ray diffraction (XRD), some of them after a thermal anneal. Pairs from each temperature, either with one of the wafers deposited, or with both wafers deposited, were bonded to each other and annealed as above.

Transmission electron microscopy (TEM) was conducted on the Si to LPCVD Si bond interface.

3. Results and discussion

The initial direct bond rapidly covered all area after room temperature contacting (excluding a bubble in the centre). After annealing bubbles appeared all over the surface, Fig. 1.

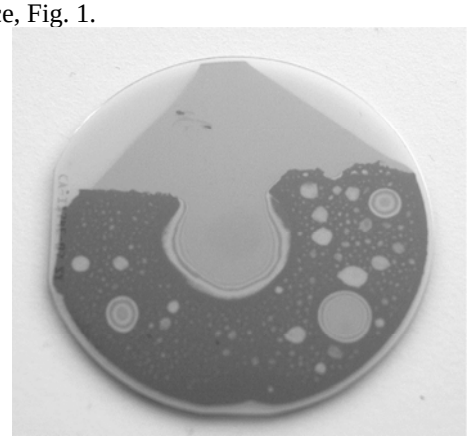


Fig.1: *Direct bonded SiC to Si. Numerous bubbles appear after 1000°C annealing*

This misbehaviour is blamed on desorbed water that cannot be resolved in the silicon or the silicon carbide.

By introducing a grid of ventilating channels prior to bonding the water finds escape routs at closer distances, creating bubble free square Si islands, see Fig.2. After etch-back of the handle wafer and buried oxide, large areas remained for further processing [1].

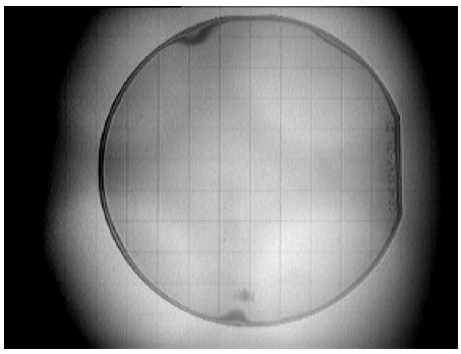
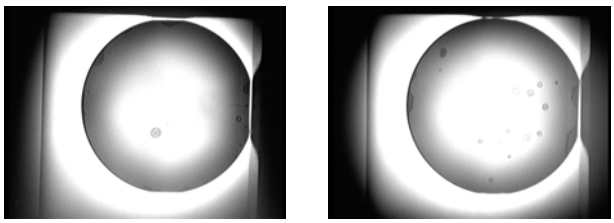


Fig.2: *Silicon carbide wafer bonded to SOI. The grid ventilates desorbed water during annealing. No bubbles are formed.*

Varying the deposition temperature from 555 to 620 °C gave increasing surface roughness. A sudden rise in roughness was observed between 570 and 575°C; the films obtained at 570 °C and lower were 0.1 to 0.3 nm rms and bonded well. Pairs with both wafers deposited showed no bubble formation after bonding and annealing, Fig. 3a. Wafer pairs bonded in the same manner, but with just one of the wafers deposited showed on the other hand evidentially more bubbles, Fig. 3b. The results indicate that one layer of deposited Si reduce bubble formation, and that two layers are even more efficient.



a b

Fig.3: *Direct bonded silicon wafers after annealing at 1000 °C. Both bonding surfaces deposited with amorphous silicon (a), and the same type of bond with just one wafer deposited (b). In the latter case, more bubbles are formed.*

Wafers deposited at 575 °C and higher had an roughness of 1 to 3 nm and could not be bonded. The XRD measurements revealed that a sudden rise in crystallinity above 570 °C. Thus, the films obtained at lower temperatures are to be concerned as amorphous, while the films become more polycrystalline at higher temperatures. XRD spectra of as deposited and annealed silicon reveals that some recrystallization takes place already at 450°C, Fig. 4. It is therefore expected that the initially amorphous silicon film at the bond will get more polycrystalline in character after the bond anneal.

The TEM analysis discloses a dense bond, see Fig. 5.

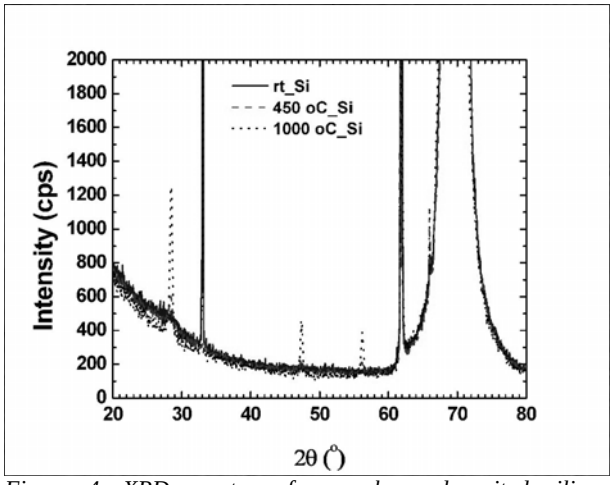


Figure 4. XRD spectra of amorphous deposited silicon annealed at different temperatures. Already at 450°C some recrystallization takes place.

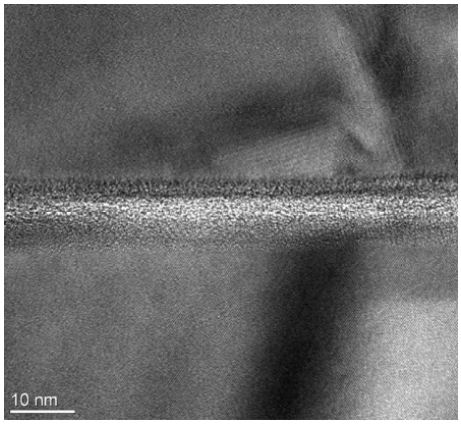


Figure 5. High resolution TEM of a bond interface between crystalline and amorphous silicon.

4. Conclusions

New Si-on-SiC hybrid substrate without intermediate oxide has been manufactured. A void-free bonding result if a ventilation grid is introduced prior to bonding. The void-free bonding of amorphous Si to amorphous Si shows that the grid then can be omitted, as will be implemented on Si to SiC bonding.

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Improved Thermal Characteristics in SOI using a Buried Aluminium Nitride Insulator

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1. Abstract

New silicon-on-insulator (SOI) structures have been formed using hydrophilic wafer bonding. These devices demonstrate an improvement in thermal characteristics of SOI via fabrication of a hybrid substrate consisting of Si on a buried AlN insulator. Use of AlN would bring about reduced device self heating compared to ordinary SOI material and enable integration of IC and electroacoustic technology.

2. Introduction

The low thermal conductivity of SiO_2 in SOI materials produces high self heating effects for applications requiring high power dissipation. Various materials have been investigated previously to improve on SOI thermal properties by replacing the thermally unfavourable SiO_2 [1]. Various materials investigated include diamond [2] AlN [3,4], Al_2O_3 [5] and SiC [6]. In this work sputter deposited AlN is thermally characterised and compared to current SOI substrates utilising SiO_2. This material has a comparable thermal conductivity to silicon, two orders of magnitude higher than alternative materials such as alumina and is a current thin film technology used in acoustic resonators and sensors.

3. Film synthesis and bonding

After cleaning the n-type (100) Si epi-layered substrate, 200 nm thick AlN film is deposited by reactive sputtering using a Von Ardenne reactive balanced magnetron sputter deposition system operated in a pulsed direct current (DC) mode. The AlN film is sputter deposited, at room temperature [7]. The surface roughness of such a film is around 0.7 nm RMS, which is improved further via deposition of an amorphous Si layer. The 200 nm α-Si layer is sputter deposited in the same chamber directly after AlN deposition creating a very smooth surface for bonding, 0.3 nm RMS. High quality, device layer silicon is fabricated on this surface via hydrophilic bonding of Simgui SIMOX SOI wafers. Escape paths for water were created naturally through the roughness of the SIMOX Si device layer, having an RMS of 1.3 nm. The roughness here is on the limit of this type of bonding and is somewhat compensated in this case by the high smoothness of the prepared wafer surface. The bonding of the SOI wafer to the amorphous Si surface is spontaneous after initial pressure although the bond front has to be chased. The bonded wafers are annealed for one hour at 500 °C in a N_2 ambient. The SOI handle wafer is subsequently etched back via Deep Reactive Ion Etching (DRIE) in two steps. Back etching is stopped on the oxide layer, which is removed via wet etching in HF. The silicon device layer is now transferred to the surface of the new SOI wafer containing the AlN insulator.

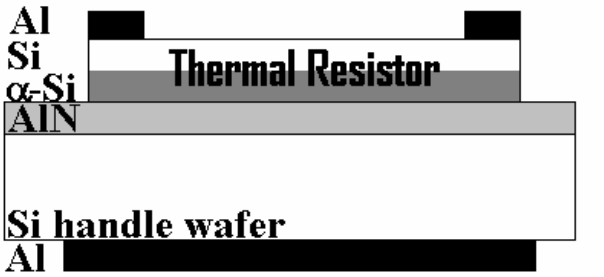

Fig.1: *Cross-section of test structures for thermal characterization.*

Thermal test structures are then processed in this Si device layer via standard MOS processes. The cross section of a thermal test structure is shown in Fig. 1.

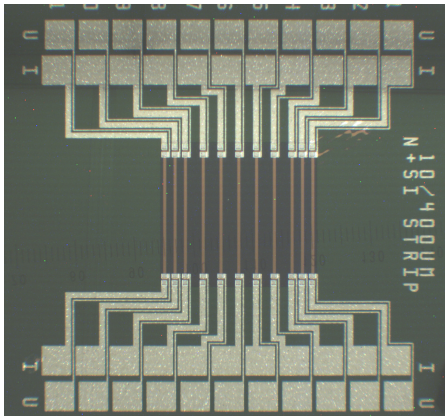

Fig.2: *Test structures for thermal characterization*

Doping of the active Si layer is performed by implantation dose of $3x10^{15}$ cm^{-2} phosphorous at 40 KeV. The dopants were activated with a 900°C thermal reoxidation and device isolation was attained with TEOS and a final FGA at 400°C in forming gas. Reference devices were also fabricated simultaneously on ordinary SOI wafers. Fabricated thermal test

structures with 10 μm width and a length of 400 μm can be seen in Fig. 2. Capacitive structures are also simultaneously fabricated on to the same substrates.

4. Thermal Characterisation

Typical high quality AlN films deposited in this system have a full width half maximum (FWHM) of the (0 0 2) rocking curve below 2 degrees, as seen in Fig. 3. The quality of the films deposited can also be seen in the TEM image of Fig. 4 which shows good columnar growth.

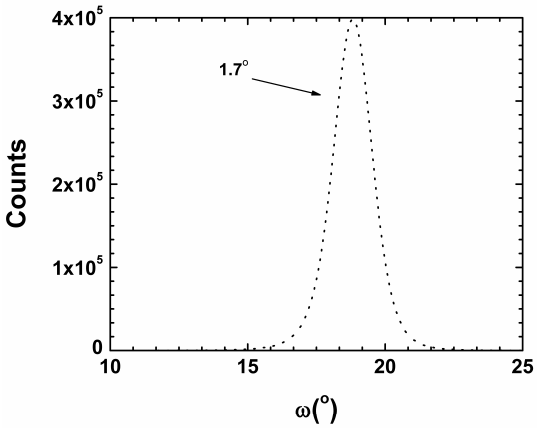

Fig.3: *Typical FWHM of the (0 0 2) rocking curve, for AlN deposited directly on Si wafers.*

The dielectric quality of the AlN films can be seen by using the simple parallel plate capacitor equation, the capacitance at accumulation and assuming AlN has a dielectric constant of 8.9 we obtain a dielectric thickness of 200 nm, thus confirming film quality and dielectric constant.

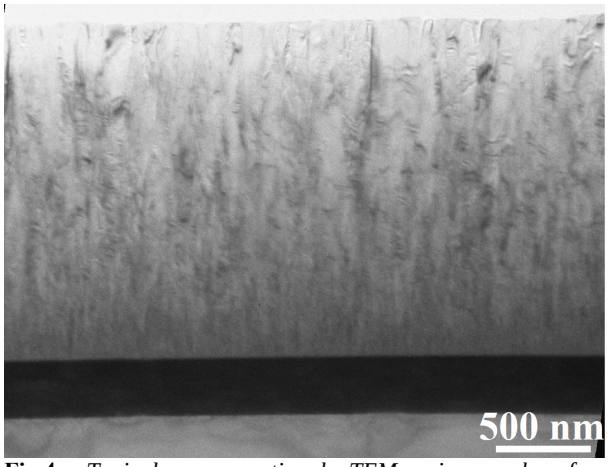

Fig.4: *Typical cross-sectional TEM micrograph of a reactively sputter deposited AlN film.*

Thermal response of the buried oxide (box) is calibrated via measuring the resistance, at low power density, of the thermal resistors whilst heating on a hot chuck. The characteristics of both AlN and SOI box can be seen in Fig. 5. It can already be seen that to cover the resistive region of interest, when high power density is used, the SOI substrate needs to be calibrated to a higher temperature range, thus indicating a better thermal characteristics from the AlN box.

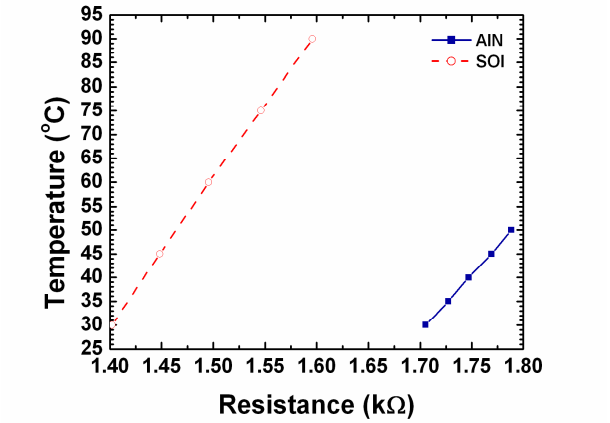

Fig.5: *Resistance-temperature calibration of AlN buried insulator and SOI substrates.*

The temperature increase as a function of power density is seen in Fig. 6. It can be seen that there is a factor of two difference in effective thermal resistance indicating reduced self heating effects in the improved AlN box when compared to ordinary SOI.

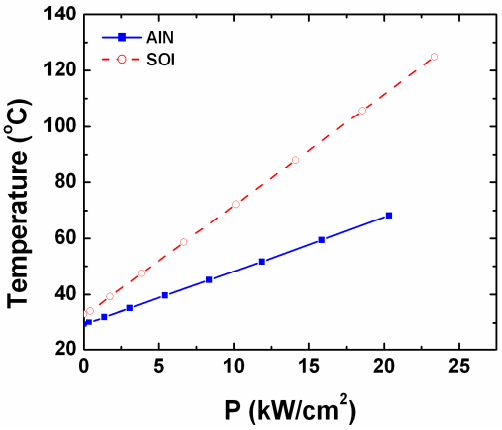

Fig.6: *Measured temperature as a function of applied power density for AlN buried insulator and SOI substrates.*

4. Conclusions

The use of wafer bonding has enabled the use of high quality materials to be investigated for improvement in thermal properties of SOI. Due to its low thermal conductivity a new Si on AlN box has been demonstrated here to have a factor of two lower thermal resistance than a SOI reference.

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In-depth characterization of quantum effects in SOI MOSFETs for modeling purposes

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1. Abstract

A detailed quantitative study of the inversion charge obtained by means of classical and quantum simulation tools has been performed in order to analyze the need of the inclusion of quantum mechanical effects (QME) in compact models of different SOI transistors.
The differences obtained between the classical and quantum charge distributions are higher in (Surrounding Gate Transistors) SGTs than in DGMOSFETs (Double Gate MOSFETs) due to the higher confinement of the inversion charge in SGTs.

2. Introduction

The reduction of MOSFET dimensions connected with the continuous increase in integrated circuits performance has pushed the conventional bulk MOSFET technology to their physical limits.
SOI technology is currently considered one of the most serious alternatives to keep up the pace of advance described in Moore's law [1]. The use of SOI substrates makes feasible the fabrication of new devices such as DGMOSFETs, SGT, FinFETs, etc. These new devices show promising features in comparison to the conventional bulk counterparts which face important limitations in the sub-50-nm gate length regime (short channel effects, threshold voltage roll-off, sub-threshold slope degradation, increase of the off-state leakage current, fluctuation of device characteristics with random channel dopant, etc.).
Here, we deal with an in-depth quantitative characterization of QME in the inversion charge calculation, from the modelling point of view, in two of the most interesting SOI MOSFET structures: DGMOSFETs and SGTs.

3. Simulator description

Conventional bulk and double gate MOSFETs
These devices were simulated with a one dimensional self-consistent Poisson-Schrödinger solver making use of a non-uniform adaptive mesh and an iterative-Newton numerical scheme. A non-parabolic band model was used [2].

Surrounding gate transistors (SGTs)
The SGT simulator calculates the charge distribution in a structure with a gate that surrounds a cylindrical silicon channel where conduction takes place. The simulator self-consistently solves the 2D Poisson and Schrödinger equations [3].

4. Results and discussion

We have studied the inversion charge in different conventional and SOI MOSFETs. The most representative technological parameters were swept to compare the charge distributions obtained by means of classical and quantum calculations. To do so, we have calculated and plotted the Q factor defined as follows:

$$Q = \frac{Q_{Iclassical} - Q_{Iquantum}}{Q_{Iclassical}} \qquad (1)$$

where $Q_{Iclassical}$ ($Q_{Iquantum}$) represents the inversion charge obtained classically (accounting for QME). This factor clearly depicts the need to include QME in the compact models that will be used in circuit simulators.

Conventional bulk MOSFETs
In order to compare SOI devices with conventional bulk MOSFETs, we have plotted in Fig. 1 the Q factor for bulk MOSFETs with the following technological parameters: midgap metal gate, $N_A=10^{14}$ cm^{-3}, T_{ox} =0.9, 1.5, 3, 6nm. The use of such a low doping concentration along with oxide thicknesses corresponding to ultimate devices is justified as follows: since thin silicon layer SOI devices are left undoped because they are not affected by short channel effects, we have used the same doping concentration for all the devices studied in this manuscript, including bulk MOSFETs, in order to make the comparison coherent.

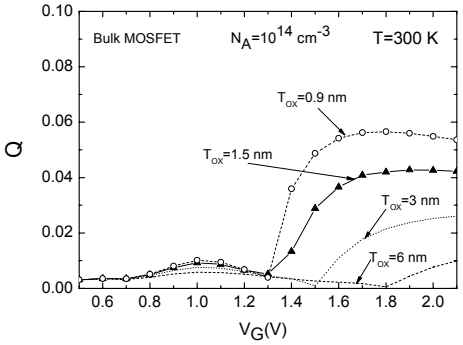

Fig.1: Bulk MOSFET Q factor. Midgap metal gate, $N_A=10^{14}$ cm^{-3}. T_{ox} =6nm (dashed lines), T_{ox} =3nm (dotted lines), T_{ox}=1.5nm (solid triangles), T_{ox}=0.9nm (hollow circles).

Double gate MOSFETs

Several DGMOSFETs have also been studied. The Q factor has been plotted for devices with different oxide thicknesses: T_{ox}=6, 3, 1.5, 0.9 nm. Different silicon layer thicknesses were used for each oxide thickness.

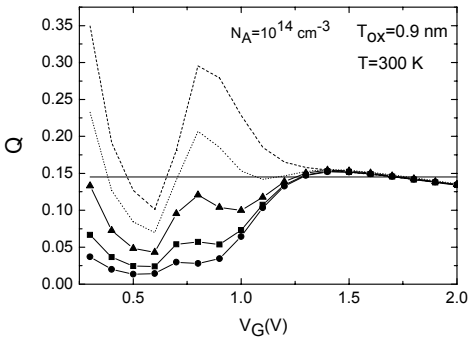

Fig. 2: DGMOSFET Q factor. The technological parameters used are the following: T_{ox}=0.9 nm, midgap metal gate, $N_A=10^{14}$ cm^{-3}, T_{Si}=6nm (dashed lines), T_{Si}=8nm (dotted lines), T_{Si}=12nm (solid triangles), T_{Si}=20nm (solid squares), T_{Si}=30nm (solid circles).

Surrounding gate MOSFETs

The same study has been carried out on SGTs.

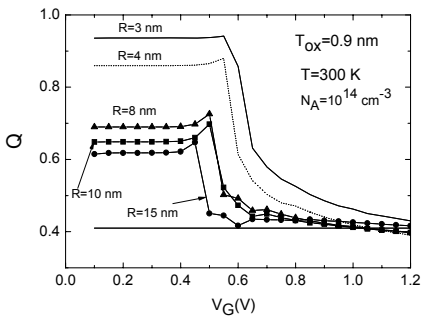

Fig. 3: SGT Q factor. $N_A=10^{14}$ cm^{-3}, midgap metal gate, T_{ox}=0.9 nm. R=3nm (solid lines), R=4nm (dotted lines), R=8nm (solid triangles), R=10nm (solid squares), R=15nm (solid circles).

All the Q factor curves show a similar behaviour at high gate voltages (they reach a constant value, not dependant on the silicon layer thickness, which has been highlighted with a solid straight line, see Fig. 2 and 3). We have calculated approximately the Q factor making use of a modified oxide capacitance that accounts for the separation of the inversion charge from the oxide interface described by the charge centroid.

$$C_{oxquantum}^{-1}=\frac{t_{ox}}{\varepsilon_{ox}}+\frac{z_I}{\varepsilon_{Si}} \quad \Rightarrow \quad C_{oxquantum}=\frac{\varepsilon_{ox}}{t_{ox}+\frac{\varepsilon_{ox}}{\varepsilon_{Si}}z_I}$$

$$Q=\frac{Q_{Iclassical}-Q_{Iquantum}}{Q_{Iclassical}}\approx\frac{C_{ox}f_{classical}(V_G)-C_{oxquantum}f_{classical}(V_G)}{C_{ox}f_{classical}(V_G)}\approx \quad (1)$$

$$\frac{C_{ox}-C_{oxquantum}}{C_{ox}}\approx 1-\frac{C_{oxquantum}}{C_{ox}}\approx\frac{\frac{\varepsilon_{ox}}{\varepsilon_{Si}}z_I}{t_{ox}+\frac{\varepsilon_{ox}}{\varepsilon_{Si}}z_I}$$

The Q factor at high gate voltages have been plotted (symbols in Figure 4) for all the devices studied. The analytical Q factor (calculated using Eq. 1) is shown in solid lines. They reproduce the values obtained for bulk and DG MOSFETs. However, the SGT Q factor (much higher due a higher degree of confinement) can not be fitted.

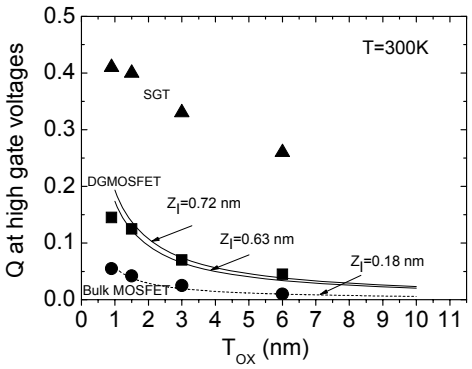

Fig. 4: Q factor at high gate voltages (strong inversion, where all the Q factor curves merge) versus oxide thickness (squares DGMOSFETs, circles bulk MOSFETs, triangles SGTs).

4. Conclusions

A detailed study of the inversion charge obtained by means of classical and quantum simulations has been performed. The Q factor has been modelled easily for bulk and DGMOSFETs. The 2D confinement of the charge in SGTs makes the Q factor much higher.

5. Acknowledgments

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On the switching speed of SOI LEDs

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1. Abstract

Recently, we presented a novel design for a silicon LED in SmartCUT™ SOI wafers. It exhibits a record quantum efficiency for SOI-based silicon LEDs and opens the way to the integration of light emitters in a VLSI process on SOI. In this paper, we present first experimental and modeling results showing that this new design has the potential to switch on and off faster than 1 MHz – sufficiently fast for several commercial applications such as an integrated optocoupler.

2. Introduction

The design of our LED is presented in Figure 1. The light-emitting central region is a lowly p-type doped silicon volume of 5 x 60 x 0.15 μm^3.

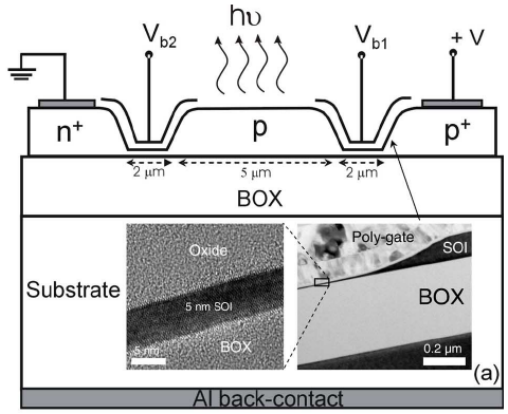

Fig.1: *Schematic cross-section of the SOI LED under study in this work. Reprinted from [1].*

Two highly doped (n+ and p+) regions provide the carriers to be recombined in the lowly doped central region. The highly doped regions are separated from the central region by gated, ultra-thin (down to 5 nm) silicon slabs. These allow the injection of one type of carriers, while they form a barrier for the other type of carrier. As a result, carriers injected in the central region have no other option than to recombine.

Through the use of high-purity silicon with a low doping level, an injection level around 10^{17} cm^{-3}, and well-passivated silicon surfaces (using thermal oxidation), the non-radiative recombination rate in the central volume is not too high, and the probability for radiative recombination becomes significant.

The device exhibits an external quantum efficiency of 1.4 x 10^{-4} at room temperature, for emission around 1150 nm (the silicon B-B peak) – comparable to the best bulk-silicon LEDs when no special surface modifications are made to enhance the outcoupling [2]. This device exhibits a power output up to 0.25 µW [1].

3. Switching speed

For integrated optics, a switching light source has great advantages over a continuous light source that requires an external switching device. Our LED has been designed to be fast-switching (apart from the rather large dimensions of the present prototypes, due to our lab capabilities). However, the LEDs compactness, and its unconventional emission wavelength complicate a direct measurement of the on/off switching behavior of the LED with the instruments at hand. In this section, we present indirect estimates of the switching speed.

On-switching

The on-switching speed is intrinsically determined by the RC-delay occuring in the device, when the diode is switched to forward-bias. (That is, if V in figure 1 is switched from low to high and back to create light modulation; alternatively, the light can be modulated with V_{b1} and/or V_{b2}!) It is not correct to assume that the device will start emitting light as soon as current starts to flow, so electrical measurements are not conclusive to determine the on-switching behaviour. However, we can assume that, once the excess carriers are inside the central region, they will mix almost instantaneously given the device dimensions, the low field in the central region and the thermal velocity.

The total capacitance of the diode sketched in figure 1 consists of three major components: the diffusion capacitance, the gate capacitances, and the capacitance towards the substrate. (The latter is an order of magnitude less than the gate capacitance.)

A rough calculation of the capacitances and resistances involved can give an indication of on-switching speed. When the positive terminal V is switched from 0 to 1 V, charge needs to be supplied to charge up the gate capacitance V_{b1} of 1 pF. The external resistance of the device is approximately 1 kΩ. Then, charge is to be supplied to the central region to raise the carrier density. Assuming that the central region has $np = n_i^2$ in off-state, and $n = p = 5x10^{17}$ cm^{-3} in the on-state, caused by a change of 1 V in the forward bias, the diffusion capacitance is first-order estimated at 7 pF with the device dimensions mentioned in Section 2. Combined with the gate capacitance, this would lead to an on-switching RC-time of 8 ns.

Off-switching

The off-switching can be studied with electrical measurements. As a diode is switched from forward-bias to reverse, a short transient current will be observed originating in the excess carriers flowing out of the depletion region. This so-called reverse recovery current [4,5] of the diode gives a direct indication how long it takes to remove the excess carriers from the central region of our LED. It can be readily assumed that light emission will stop instantly when the pn-product has dropped back to n_i^2 [6]. Therefore, the reverse recovery current indicates the speed of off-switching of our LED. Figure 2 shows the recovery current of our LED, when the forward-voltage of the diode is switched from high to zero volts. The measurement was carried out using a Keithley 4200 with pulsed-IV extension, in oscilloscope mode. The fast decay of the recovery current indicates that the LED will switch off within ~200 ns.

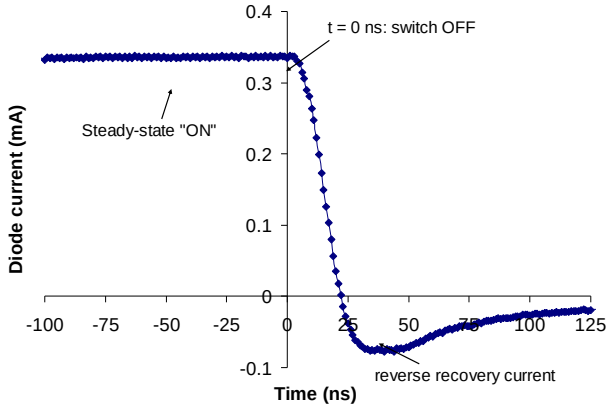

Fig.2: *The off-switching behaviour of an SOI LED.s and $|V_{b1}| = V_{b2} = 1$ V. The diodes are pumped by a voltage pulse: pulse width of 250 ns; pulse decay of 10 ns. The on-state bias was 3.5 V, off-state 0 V.*

4. Device modeling

The switching behaviour can be systematically investigated using a modeling package such as ATLAS [3]. At the time of writing, we can only report the first results of SOI pin-diodes without the gated, thinned-down access regions. The simulator reproduces the dc I-V characteristics of this diode (fig. 3).

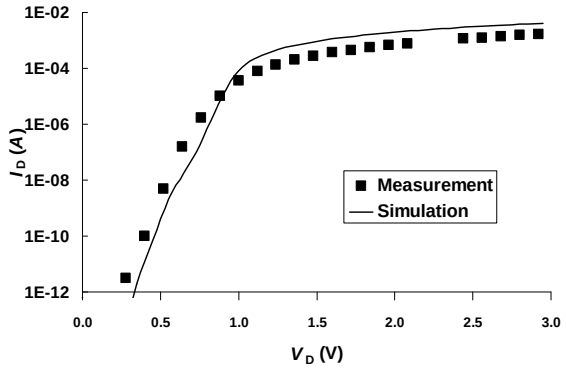

Fig. 3: *Simulated and measured I-V characteristics of a lateral SOI pin diode with 30 µm intrinsic region.*

The overall picture of on- and off-switching of such a device is in line with our findings reported in Section 3 (Fig. 4). In accordance with gated-pin-diodes reported earlier [7] the low voltage regime the current of our SOI diode is determined by Shockley-Read-Hall recombination in the bulk and at the Si/SiO_2 interfaces. The high voltage regime is determined by series resistance of the charge plasma in the intrinsic region.
We expect to report considerable further progress with both simulations and measurements at the workshop.

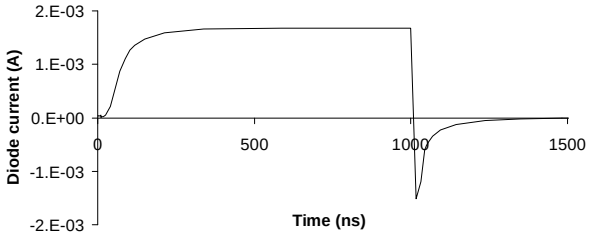

Fig. 4: *Simulated switching behaviour of a lateral SOI pin diode with a 30 µm intrinsic region, showing a 1/e on-switching time of about 90 ns and 1/e off-switching time of 50 ns. The on-state bias is 2.0 V, off-state 0 V.*

5. Conclusions

In this paper we address the switching speed of an SOI-based LED with emission efficiency comparable to bulk Si LEDs. On the basis of calculations, simulations and electrical measurements, we made plausible that the device can reach a switching speed around 1 MHz. Further work will include the direct optical switching measurement, and device improvement (shorter access regions) to further increase the speed.

6. Acknowledgements

We would like to thank Tom Aarnink for assistance with the device manufacturing, Gert 't Hooft, Martin Kittler and Alfred Driessen for fruitful discussions, and Lee Stauffer and coworkers for their assistance with the recovery current measurement. This work is supported by the Dutch Technology Foundation STW (project 6159 HELIOS).

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New Explicit Compact Charge and Capacitance Model for Undoped Ultra-Thin Body Silicon-on-Insulator (UTB-SOI) MOSFETs

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1. Abstract

An analytic, explicit and continuous charge model for undoped Ultra-Thin Body (UTB) SOI MOSFET is presented. This charge model allows obtaining analytical expressions of the total capacitances. Our model is valid from below to well above threshold, showing a smooth transition between the regimes. The drain current, charge and capacitances are written as continuous explicit functions of the applied bias. We obtain a very good agreement with 2-D numerical simulations for two different silicon film thicknesses.

2. Introduction

As the traditional CMOS is fast approaching the limit of the bulk technology scaling, non-classical CMOS devices such as ultra-thin body silicon-on-insulator (UTB-SOI), double-gate devices and surrounding-gate (SRG) structures provide a path to scale CMOS to the end of the Roadmap using new transistor structural designs and new materials [1]. In order to benchmark the circuit performance and optimize the layout of UTB-SOI devices, there is a strong demand for a physics-based compact model that can be implemented into the existing circuit simulators. In this paper, based on a previous work done by A.S. Roy et.al [2] where a channel current model, written in terms of the charge densities at the source and drain ends, was developed for an asymmetric undoped double-gate (DG) MOSFET, we present analytical and explicit charge and capacitance models obtained from a unified-charge-control-model derived by [2] from the 1-D Poisson equation in the direction perpendicular to the channel, for the case when only one interface is in strong inversion, which actually corresponds to the practical regime of operation of an UTB SOI MOSFET. This case will be simulated by a symmetric DG, having a grounded back-gate and a variable front-gate voltage. This functioning is identical with the one of an UTB SOI MOSFET. In this work, we have assumed, as in [2], that both oxides have the same thickness, although an extension to the case for two different oxide thicknesses can be done using a similar procedure. The charge and capacitance expressions are written in terms of explicit and infinitely continuous expressions of the applied bias. It is shown that this analytic model covers very well all regions of MOSFET operation: from linear to saturation and from sub-threshold to strong inversion without the need of empirical parameters. The capacitance characteristics have been validated by 2-D numerical simulations (DESSIS-ISE). In addition, to demonstrate the accuracy of our model, we present results for two different silicon film thicknesses.

3. Model

An analytical expression of the total channel charge is obtained by integrating the mobile charge sheet density over the channel length (Q_{Tot}=-Q_G):

$$Q_{Tot} = -W^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{C_{ox}(1+\alpha)} + \frac{kT}{q}\left(Q + \frac{2Q^2}{2Q+Q_0} \right) \right) dQ \quad (1)$$

where $\alpha = \frac{C_{Si}}{C_{Si}+C_{ox}}$. Following Ward's channel charge partitioning scheme, we also obtain analytical expressions for the total drain (Q_D) and source (Q_S) charges, after integrating:

$$Q_D = W \int_0^L \frac{x}{L} Q dx = -\frac{W^3 \mu^2}{L (I_{DS})^2} \int_{Q_s}^{Q_d} Q^2 \left(\left(\frac{Q^2 - Q_s^2}{2C_{ox}(1+\alpha)} \right) + \right. \quad (2)$$

$$\left. + \frac{kT}{q}\left(2(Q-Q_s) - \frac{1}{2} Q_0 \log\left[\frac{2Q+Q_0}{2Q_s+Q_0} \right] \right) \right) \cdot$$

$$\cdot \left(\frac{1}{C_{ox}(1+\alpha)} + \frac{kT}{q}\left(\frac{1}{Q} + \frac{2}{2Q+Q_0} \right) \right) dQ$$

$$Q_S = Q_{Tot} - Q_D \quad (3)$$

However, due to the fact that we have only the front interface in strong inversion, the total gate charge will be just the front gate charge. From [2] we have:

$$Q_F = \frac{Q_G}{1+\alpha} + \frac{W}{1+\alpha} 2\alpha \cdot V_{GS} L \quad (4)$$

So, the intrinsic capacitances, C_{gd} and C_{gs}, are obtained as:

$$C_{gi} = -\frac{dQ_F}{dVi} = -\frac{1}{(1+\alpha)} \frac{dQ_G}{dVi} \quad (5)$$

where *i=d,s* and the other capacitances, C_{dg} and C_{sg} are obtained by differentiating the total charges (Q_D & Q_S) with respect to the applied bias. Analytical expressions of all the capacitances are obtained in terms of the mobile charge sheet densities at the source and drain ends. For the mobile charge sheet densities at the source and drain ends, we use explicit expressions of the same

type as in [3] for Surrounding-Gate MOSFETs, since the charge control model considered here [2] has the same form. To validate our model, we have compared our modelled capacitance characteristics with 2D numerical simulations using DESSIS-ISE.

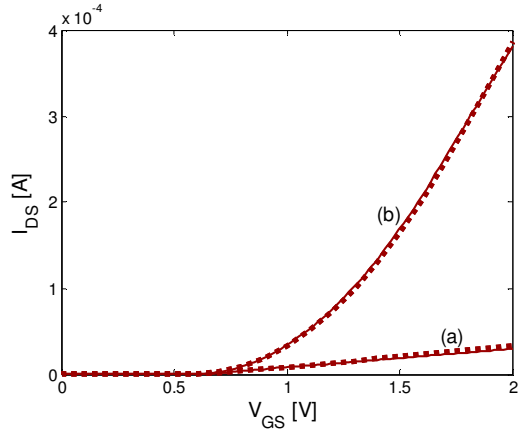

Fig.1: *Transfer characteristics, for V_{DS}=0.05V (a) and for V_{DS}=1V (b) in linear scale ,for t_{Si}=31nm . Solid line: analytical model; Symbol line: DESSI-ISE simulation*

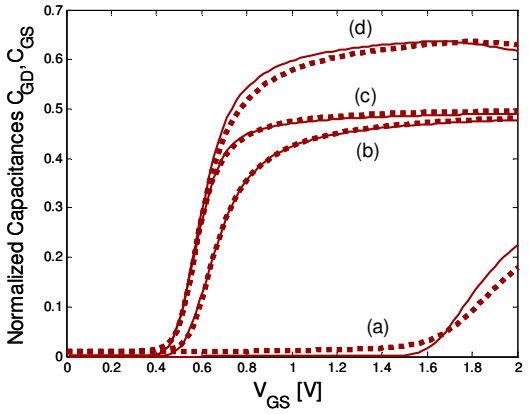

Fig.2: *Normalized GD capacitance (a, b) and GS capacitance (c, d) with respect to the gate voltage, for V_{DS}=0.05V (b,c) and V_{DS}=1V (a,d); t_{si}=31nm. Solid line: analytical model; Symbol line: DESSIS-ISE simulation*

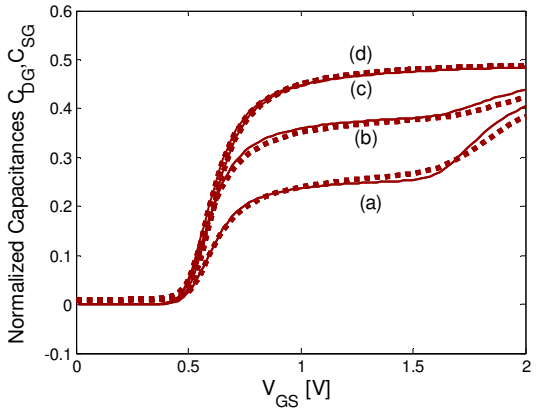

Fig.3: *Normalized DG capacitance (a, c) and SG capacitance (b, d) with respect to the gate voltage, for V_{DS}=1V (a, b) and V_{DS}=0.05V (c, d). t_{si}=31nm Solid line: analytical model; Symbol line: DESSIS-ISE simulation*

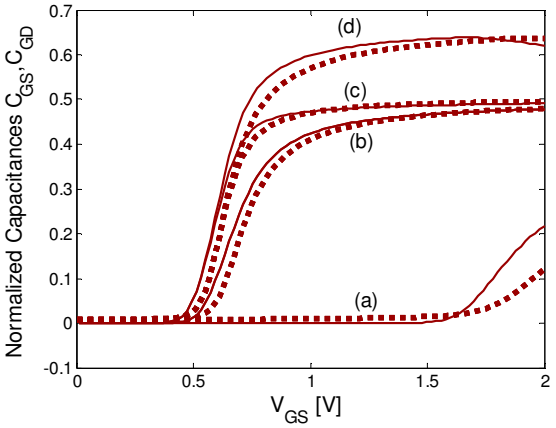

Fig.4: *Normalized GD capacitance (a, b) and GS capacitance (c, d) with respect to the gate voltage, for V_{DS}=0.05V (b,c) and V_{DS}=1V (a,d); t_{si}=20nm. Solid line: analytical model; Symbol line: DESSIS-ISE simulation*

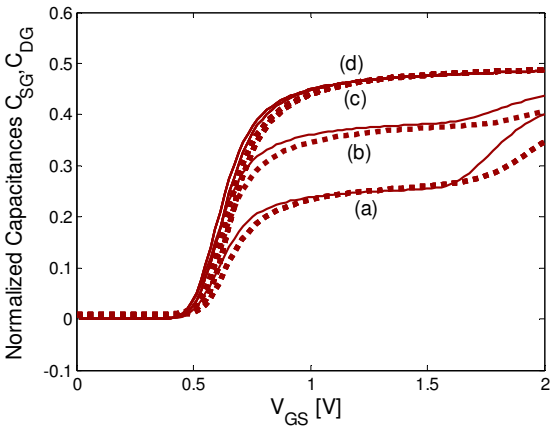

Fig.5: *Normalized DG capacitance (a, c) and SG capacitance (b, d) with respect to the gate voltage, for V_{DS}=1V (a, b) and V_{DS}=0.05V (c, d); t_{si}=20nm. Solid line: analytical model; Symbol line*: *DESSIS-ISE simulation*

We have also validated our drain current model. We have assumed L=1µm, W=1µm, t_{ox}=2 nm, t_{Si}=31 nm (Fig.1-3), t_{Si}=20 nm (Fig. 4-5).

4. Conclusions

We have presented a charge model for undoped UTB SOI MOSFETs which has been shown to accurately reproduce 2-D simulations of the capacitance characteristics in all operating regimes, for all V_{DS} biases and for different silicon film thicknesses, proving the accuracy of our model. As a result, our model has a great potential for the simulation of circuits using UTB SOI MOSFET

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Ballistic transport and RF Noise in ultra-scaled SOI MOSFETs: a Monte Carlo study

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1. Abstract

High-frequency noise and electronic transport phenomena in downscaled SOI MOSFETs are studied by means of an ensemble Monte Carlo simulator. The results indicate important ballistic features of transport in devices with gate lengths below 30 nm. Moreover, drain and gate noise sources tend to become practically equal to the noise sources obtained under a fully ballistic regime in which all scattering within the channel is eliminated, thus indicating a limit to the noise generated inside the channel of ultra-scaled devices.

2. Introduction

The outstanding improvement of the high-frequency performance of Silicon devices accomplished in the last years has been achieved mainly thanks to the downscaling of CMOS technology towards nanometer dimensions. This has turned out Silicon technology as an increasingly attractive candidate for the design of analog wireless applications operating in the RF and microwaves ranges. For such applications the noise generated by the device itself turns into a major concern. Moreover, in the case of ultra-scaled transistors, the onset of substantial amounts of carriers which are able to traverse the device channel without suffering any scattering mechanism (ballistic carriers) yields an increase of current that can be very significant, as pointed out by several authors [1, 2]. Since in the next few years the aggressive downscaling scenario projected in the International Technology Roadmap for Semiconductors (ITRS) [3] will provoke severe drawbacks in the performance of conventional CMOS devices, alternative configurations are strongly recommended, such as the Silicon-On-Insulator (SOI) technology [4]. The appearance of quasi-ballistic phenomena in SOI devices, together with the influence of short channel effects, velocity overshoot or the presence of hot carriers in the noise performance can be highly relevant and must be properly investigated.

In this work we present a Monte Carlo [5] investigation of the onset of quasi-ballistic transport and noise phenomena in ultra-scaled SOI transistors. The Monte Carlo method is one of the most adequate techniques to carry out such study, since it provides paramount information about the most relevant internal transport processes in semiconductor devices together with a complete consideration of the processes responsible for high-frequency noise generation inside the device due to its stochastic and microscopic nature.

2. Discussion

The structures investigated correspond to n-channel SOI MOSFET devices with gate lengths ranging from 180 nm (which is considered as the initial benchmark) down to 20 nm. The active layer thickness is 15 nm, with a front gate oxide 2 nm thick and the buried oxide thickness equal to 200 nm. The channel is considered to be p-doped (10^{18} cm^{-3}). Details about the Monte Carlo simulator, band structure and scattering mechanisms can be found in previous works [6 and references therein]. To carry out a complete spectroscopy of the electron movement inside the device channel, a counting region [7] extending from source-to-channel interface to drain-to-channel interface is taken into account. All the relevant parameters related to the movement of each carrier inside this counting region are recorded, thus providing average values and distribution functions of the transit time, number of scattering events undergone, etc. To make possible a fair comparison between the several scaled devices considered, constant electric field (100 KV cm^{-1}) scaling conditions are taken into account. For this sake, the drain-to-source voltage is properly scaled with the device gate length. Moreover, the gate voltage is tuned in order to keep an identical inversion charge (n_s=2·10^{12} cm^{-2}) for all the structures under study, which allows minimizing the influence of the threshold voltage roll-off.

Figure 1 shows the distribution function of the number of scattering mechanisms as a function of the gate length (L_g) obtained by the Monte Carlo simulation. As it can be observed, for long gate lengths the distribution function has a quite flat shape, as it corresponds to a transport regime mainly diffusive. For very short gate lengths the distribution function gets sharper, with a maximum corresponding to ballistic carriers (zero scattering mechanisms) for L_g = 20 nm, thus showing that quasi-ballistic transport is dominant. The study of the time between scattering events, mean free path, average number of scattering and their

distribution functions has also confirmed that for L_g smaller than 30 nm carrier transport shows important quasi-ballistic features.

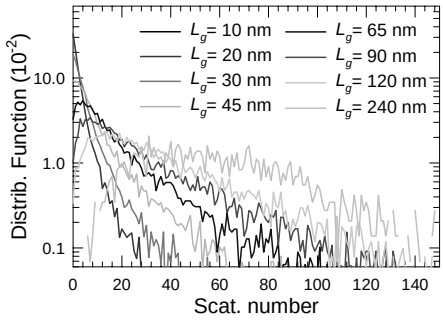

Fig.1: *Distribution function of the average number of scattering mechanisms as a function of Lg. Lg = 240 nm is also shown for comparison.*

Such a conclusion is reinforced by artificially eliminating in the simulation all scattering mechanisms within the channel. Under such conditions, it is possible to evaluate the maximum ballistic current (I_{off}). In Figure 2 we show the ratio between the current under the influence of scattering mechanisms and I_{off}: as it can be observed, the current tends to sharply approach the ballistic value for ultra-scaled devices.

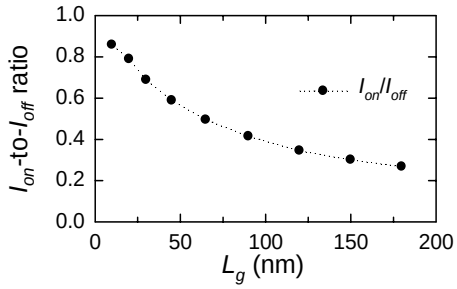

Fig.2: *I_{on} to I_{off} ratio as a function of the gate length.*

After examining the static performance of the transistor we carried out the analysis of the spectral density of drain (S_{ID}) and gate (S_{IG}) current fluctuations. Figure 3(a) shows the value of S_{ID} as a function of the gate length, together with the shot noise value $2qI$. As it can be observed, S_{ID} remains quite flat for long devices, but for L_g = 30 nm and below it sharply increases, significantly approaching the $2qI$ value. Concerning the gate current fluctuations, in Figure 3(b) we present the values obtained at 24 GHz as a function of the gate length, together with the results corresponding to the simulations carried out in the absence of scattering events inside the channel. First of all, for relatively long devices it is remarkable the gate noise reduction obtained in a ballistic framework. However, as it can be observed, both results tend to converge for L_g = 10 nm, thus confirming the quasi-ballistic nature of transport and high-frequency noise in that case. The comparative study of the differences observed when eliminating the scattering mechanisms for the different L_g investigated (not shown in the graphs) has evidenced that for short gate lengths the total drain noise is mainly governed by the noise produced at the source and drain wells.

3. Conclusions

A complete analysis of the appearance of ballistic carriers in SOI MOSFETs scaled to the nanometer range, including the investigation of high-frequency noise sources has been presented. Results show that for gate lengths shorter than 20 nm the noise performance of the transistor is mostly described by ballistic phenomena, thus representing a limit to the noise provided by the device. Moreover, the contribution of drain and source regions to the total drain noise becomes more relevant for ultra-scaled devices.

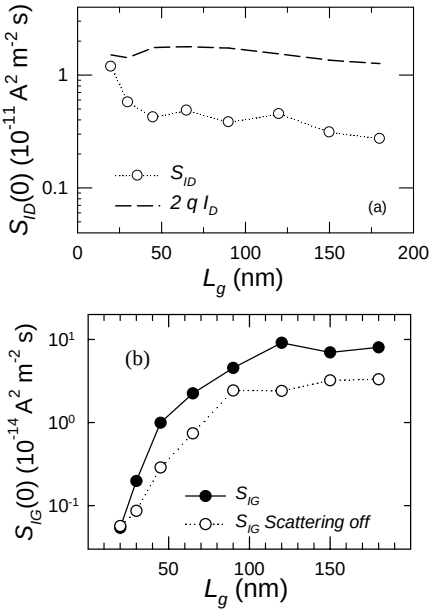

Fig.3: *S_{ID} as a function of the gate length and 2qI value (a) S_{IG} @ 24 GHz as a function of the gate length together with the results obtained in the absence of scattering events within the channel (b)*

4. Acknowlegments

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SESSION 5

SOI Material Characterization

CHAIR
C. Claeys
IMEC

REVIEW OF ADVANCED SUBSTRATE TRENDS

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1. Abstract

In this paper, based on some examples of recent realizations, we make a brief review of advanced substrates developed using the Smart Cut™ technology.

2. Introduction

In 1991, M. BRUEL from CEA-LETI invented the Smart Cut™ concept, especially suited for the mass production of high quality Silicon On Insulator (SOI) substrates fabrication [1]. Since this date, the maturity of SOI substrates has enabled to become a reference technology in the microelectronic market. Today R&D on advanced substrates is focused on the integration of new materials and functionalities in order to improve devices performances and enlarge application spectrum. This paper deals with advanced substrates for "More MOORE" and "More Than MOORE" applications and also deals with future "beyond CMOS" substrates.

3. More MOORE advanced substrates

Active layer engineering

The scaling of dimensions and introduction of new materials are the two ways used to follow the MOORE law. Advanced substrates developments are mainly engaged in the second way by inducing strain in the active layer (strain SOI [2]) in order to improve carrier mobility (Fig 1) or by using high mobility material as active layer (for example : Germanium for Germanium on Insulator substrates [4]) (Fig2).

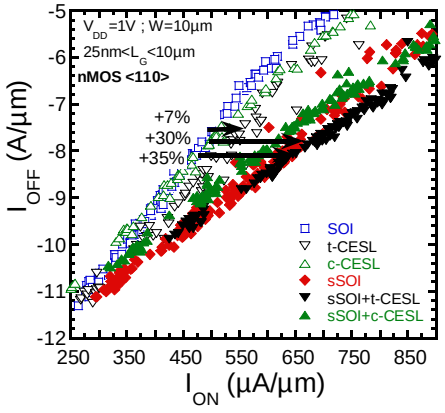


Fig.1: *Ion vs Ioff plot of nMOS on SOI or sSOI [3].*

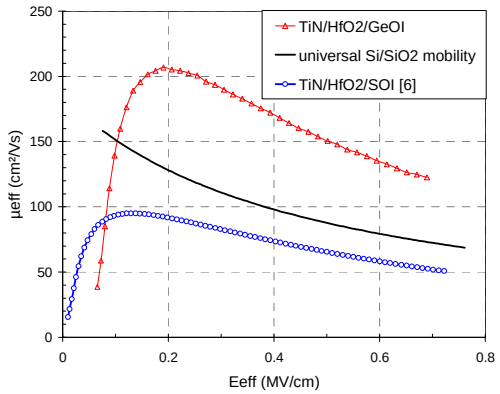


Fig.2: *Hole effective mobility measured on a L_g=W=10µm pMOSFET on a GeOI wafer [4] (red) and a state of the art SOI wafer (blue) with exactly the same gate stack [6]. The universal Si/SiO_2 mobility for holes appears as a black curve*

Buried Oxide (BOx) Engineering

For MOSFET, the buried oxide engineering is mainly studied to improve electrostatic behavior of devices (reduction of the DIBL) but also to realize multi Vt devices via a back biasing of the base substrate when the active layer is in the fully depleted regime (because both interfaces are electrostatically coupled). The Ultra thin BOx substrates developed recently exhibits Box in the 10-50nm range.

The introduction of other materials than SiO_2 in the BOx is another way to integrate "buried functionalities" in a substrate. Such functional layers are investigated for instance for thermal management, via the introduction of high thermal conductive layers such as nitride or diamond, or again as etch stop layers (Fig 3) [5] (for example via the introduction of Oxide/Nitride/Oxide stacks), etc… Concerning the thermal management, as for us, the most promising application is the "thermal spreading effect": when the thermal layer is highly conductive (for example Diamond whose thermal conductivity is 1000 times higher than SiO_2 one) the temperature inside a chip quite uniform due to enhanced lateral diffusion of heat. Thus, thanks to such layers, the "hot spot" issue is addressed and, thermally speaking, Silicon On Diamond may become more advantageous than a bulk substrate.

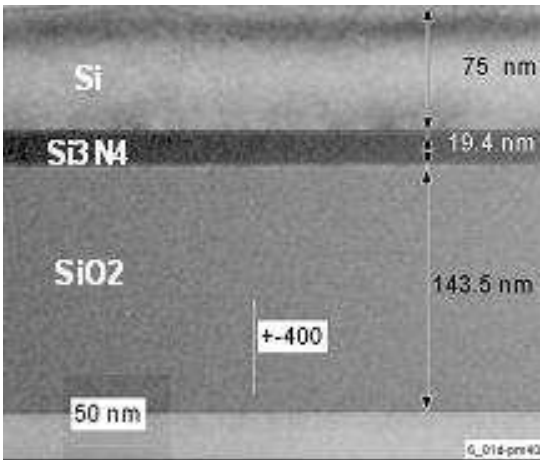


Fig.3: *TEM cross section of a Silicon-on-Insulating-Multilayer stack (adapted for etch stop application): Si top layer / Si_3N_4 20 nm / SiO_2 145 nm / Si bulk substrate. The bonding interface is SiO_2/Si_3N_4.*

3. More Than MOORE advanced substrates

The "More than MOORE" applications are commonly named CMOS options. Today, like design, these options are more differentiating activities than core CMOS and thus more and more efforts are dedicated to these approaches. Since Smart Cut ™ is a versatile method, it has been adapted to new materials for the development of substrates for new functionalities.

In the frame of Radio Frequency Micro Electromechanical Systems (RF MEMS), the realization of passive components such as Bulk Acoustic Wave (BAW) filters is a great challenge because it addresses the mass market of phone cell filters. Today BAW filters are made with thin polycrystalline layers of piezoelectric materials deposited on a metallic electrode. In term of performances, the improvement of the coupling parameter (K_t) of such devices by using thin and single-crystal layers of $LiTaO_3$ could be a strong advantage for band width enlargement.

To this aim, we are developing Lithium Tantalate On Metal On Insulator substrate (LTMOI). The first transfer of a thin ferroelectric layer ($LiTaO_3$) using the Smart Cut™ technology was demonstrated (Fig 4) and encouraging ferroelectric characteristics have been measured (hysteresis cycle).

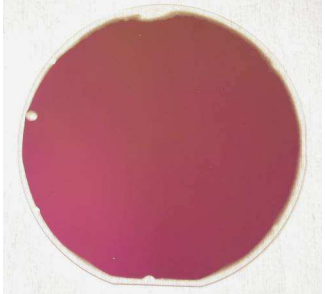


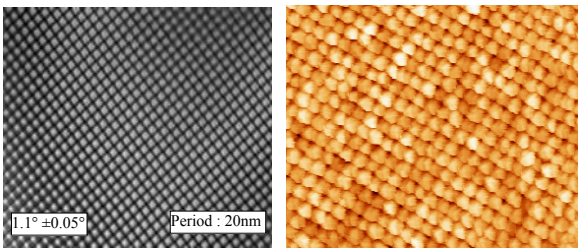
Fig.4: *Picture of a LTMOI substrate with thin ferroelectric layer transfer (300 nm of LiTaO3).*

In the next step we are going to validate these substrates by RF MEMS realization. Since $LiTaO_3$ exhibits also ferroelectric properties, these substrates are also under investigation for massive probe memory storage media (more than 1 Tb/cm²).

4. Beyond CMOS substrates

For 40 years reducing the feature size of transistors has made chips faster and cheaper. However, due to physical limits (we are reaching the quantum sizes) and technical/cost challenges, this scaling rule is less and less true with a classical approach. The beyond CMOS researches are looking for alternative concepts compared to classical CMOS technology.

By combining the Smart Cut™ process with a very simple method to control the crystalline misorientation of two bonded wafers, we realized a pure screw dislocation network with a periode accuracy below 1nm (Fig 5a) [7]. Using selective strain etching solution on these "twisted substrates", the periodic dislocation pattern is transferred to the wafer surface in order to obtain controllable surface nanopatterning with a pitch down to 20nm without any e-beam lithography (Fig 5b).



a) b)

Fig.5: *a)TEM plane view of a « twisted substrate ». b) Surface nanopaterning with a pitch of 20nm.*

This approach may have some classical nano-electronic applications but, it is not restricted to semiconductor materials and is also potentially useful for organizing inorganic or organic nanostructures, and thus can offer a pathway for self-assembly of new electronic, magnetic and optical nanosystems.

5. Conclusions

In this paper, we have underlined that Smart Cut™ is a generic and versatile technology which enables integration of new materials and functionalities in order to realize advanced substrates not only in the "More MOORE" domain but also for "More than MOORE" and "beyond CMOS" applications.

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On the extraction of dopant activation level for Boron-doped Thin Germanium-On-Insulator (GeOI)

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1. Abstract

This study aims at presenting our doping level extraction method and results on our Boron-doped GeOI wafers along with comments on the impact of the choice regarding the hole mobility model. The method is non-destructive and combines Monte Carlo Boron profile simulation with optical (thickness) and electrical (sheet resistance) measurements. An activation level of 2.7×10^{19} cm^{-3} has been found on our samples with thin Ge film thicknesses down to 30 nm and annealed 1min at 600°C.

2. Introduction

In state-of-the-art MOSFET, high mobility Ge-channel devices are being proposed as a solution to enhance the transport properties and compensate for the electrostatic limitations induced by scaling. As in thin SOI, a high S/D doping level is needed in GeOI MOSFET structures in order to reduce the access resistance and improve the device performance in terms of ON-state current.

From a quantitative point of view, an accurate evaluation of the activated impurities concentration is mandatory for predictive p/n or Schottky junctions modelling. Its value is often an indicator of the doping process quality[1],[2]. Nevertheless, an extraction performed either by Spreading Resistance Probe (SRP) profiling or by four-probe resistivity measurement always requires preliminary calibration or modelling for results interpretation.

The following method based on the knowledge of the implanted dopant profile is adapted to p-doped GeOI structures, and accounts for the Ge film thickness variations. In our case, Ge films as thin as 30 nm are used, which makes the substrates eligible for fabricating devices with gate lengths down to L_g=120 nm with a good electrostatic control of the channel for FD-GeOI.

3. Activation level extraction

Our samples were made out of 200mm GeOI wafers obtained by Smart Cut™ process with Ge (100) epitaxially grown on Si donor wafers[3]. The Ge film thicknesses ranged from 30 to 110 nm on the studied wafers. Active areas with Van der Pauw structures have been defined. Two successive BF_2 implantations have been performed (3×10^{14} cm^{-2}, 15 keV and 10^{15} cm^{-2}, 25 keV), followed by an activation annealing at 600°C during 1 min.

A Monte Carlo simulation of the chemical Boron concentration depth profile C(x) after both implantations has been performed using Crystal-TRIM[4] software, which had been recalibrated for Ge.

Because Boron atoms do not diffuse in Ge at 600°C[1], the assumption that the chemical dopant concentration profile remains unchanged after the activation annealing is acceptable. The electrically active B concentration profile $C_{act}(x)$ was defined between x=0 and x=T_{Ge} as the minimum between a constant activation level N_{act} and C(x) (**Fig.1**).

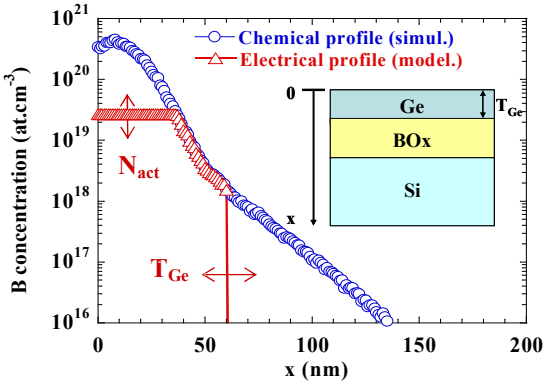

Fig.1: *Simulated as-implanted chemical Boron depth profile C(x) (sum of implantations: 3×10^{14} cm^{-2},15 keV and 10^{15} cm^{-2}, 25 keV), and modelled electrically active concentration depth profile $C_{act}(x)$ ($N_{act}=2.7\times10^{19}$ cm^{-3};T_{Ge}=60nm). Inset: schematic cross-sectional illustration of a GeOI wafer with Ge layer thickness T_{Ge}.*

The sheet resistance of a region with uniform Ge thickness is given by:

$$R_{sh} = \frac{1}{\int_0^{T_{Ge}} \sigma(x)\cdot dx} = \frac{1}{q\int_0^{T_{Ge}} \mu_h(x, C_{act}(x))\cdot C_{act}(x)\cdot dx} \quad \textbf{(1)}$$

Sheet resistance R_{sh} and the corresponding Ge thickness T_{Ge} are locally known, respectively determined by measurement on Van der Pauw structures and spectroscopic ellipsometry.

Theoretical curves $R_{sh}(T_{Ge}, N_{act})$ corresponding to this particular C(x) profile have been plotted (**Fig.2**)

according to the above equation. The variety of samples enabled to follow the calculated $R_{sh}(T_{Ge})$ behaviour over an extended range of thicknesses.

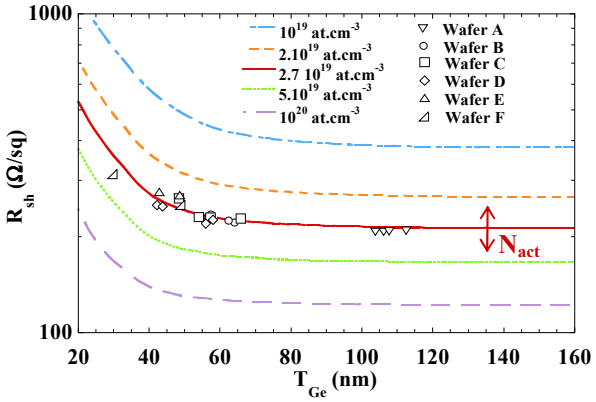

Fig.2: *Theoretical abacus plotting sheet resistance R_{sh} versus Ge thickness T_{Ge} for various activation levels N_{act} for the profile **Fig.1** (lines, hole mobility model from Golikova[6]). Experimental measurements are placed for N_{act} extraction (symbols).*

4. Impact of the mobility model on the activation level extraction

The knowledge of the hole mobility dependence on electrically active impurities concentration in Ge is of paramount importance, especially for high doping levels where the uncertainty on μ_h is amplified by the $\mu_h \times C_{act}$ product (cf. eq.**(1)**). Several models are reported which were developed on the basis of either Hall measurements[5],[6], bulk resistivity measurements[7], or fitting with data coming from both approaches[8]-[10]. The curves and experimental points are shown in **Fig.3**.

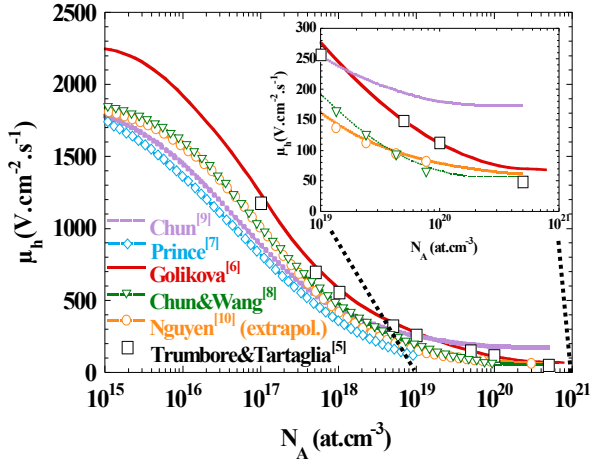

Fig.3: *Hole mobility in Ge versus acceptor impurities concentration according to ref. [5]-[10]. The model from Nguyen[10] is a Caughey-Thomas law which has been extrapolated here to concentrations superior to 10^{19} cm^{-3}.*

All models have been successively considered for the extraction, unfortunately yielding different values scattered over nearly one decade (**Fig.4**).

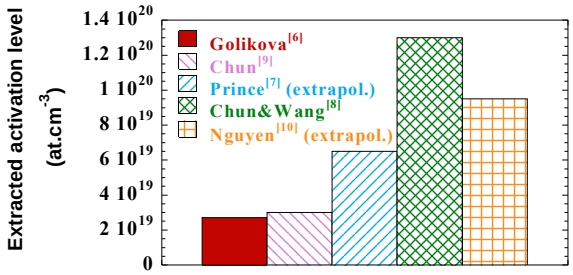

Fig.4: *Extracted activation levels with our method according to mobility models from ref.[6]-[10].*

For the present study, we have chosen to consider the data from Golikova[6] for the following reasons. Based on Hall measurements only, they include measurements from Trumbore and Tartaglia[5] and impurities concentrations higher than 10^{20} cm^{-3} while most of the other models require extrapolation. The best fitting value with our experimental points is in this case 2.7×10^{19} cm^{-3}, which is in the range of the state-of-the-art values for Boron-implanted crystalline Ge[1] and is suitable for functional GeOI pMOSFET fabrication[11].

Activation levels as high as 6×10^{20} cm^{-3} for Boron in GeOI ($T_{Ge}\approx270$ nm, SRP profiling) with a deep preamorphization implant (PAI) have been reported[2], but the controllability of this process is increasingly difficult with decreasing Ge thickness.

5. Conclusions

Thanks to our method combining dopant profile simulation, optical and electrical measurements with simple theoretical calculations, a Boron activation level of 2.7×10^{19} cm^{-3} has been extracted from our BF_2-implanted GeOI samples. Yet, the various hole mobility models yield values scattered over nearly a decade, stressing the need for caution in comparing directly with other activation results in Ge state-of-the-art.

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Acknowledgement

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Hydrogen as Source of High-Temperature Charge Instability in the Buried Oxide of SOI Structures and MOSFETs

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1. Introduction

The nature and mechanisms of high-temperature charge instability (HTCI) in gate dielectrics such as negative bias thermal instability (NBTI) and positive bias thermal instability (PBTI) are still widely debated in the literature [1]. In SOI FD MOSFETs the HTCI in the buried oxide (BOX) can play a significant role that results in the threshold voltage variations when devices are operated at high temperature. This paper is devoted to a comprehensive analysis of the HTCI in the SOI structures and FD MOSFETs fabricated on UNIBOND SOI wafers, and the demonstration of the charge generation, charge transport and neutralization in the BOX and of their link with the presence of hydrogen.

2. Experimental

FD inversion-mode (IM) SOI n-MOSFETs and n-type capacitors have been fabricated using UNIBOND material, in the same chip with identical CMOS process sequence. The thickness of the BOX, silicon layer and gate oxide were 400, 80 and 35 nm, respectively. In addition, other capacitors were made using a simplified process sequence on some starting UNIBOND wafers.
The drain current *vs.* back gate voltage $I_D(V_{BG})$, the drain current *vs.* measurement time $I_D(t)$ after different applied gate voltages have been measured on FD SOI MOSFETs in the 20^0C-320^0C temperature range. Besides, the dynamic currents through the BOX of CMOS capacitor $\Delta I(V_{BG})$ were studied. Thermally stimulated polarization/depolarization (TSP/TSD) currents with linear heating in the same temperature range on the silicon layer/BOX/silicon substrate capacitor structures were measured.

3. Results and discussion

3.1. Generation of HTCI

The HTCI in buried oxide was created by applying a negative voltage to the substrate of the SOI structure or SOI MOSFET at temperature higher than 200^0C. Under such conditions, a current peak was generated in the dynamic ΔIV_{BG} current through the BOX (Fig.1a). The peaks' amplitude increases with the increase of the hold time and measurement temperature. Analysis of the ΔIV_{BG} characteristics associates the observed current peaks to the transport of positive charges through the BOX. Using the dependence of the generated charge (calculated from the area under the current peak) on the hold time and hold temperature, an activation energy of the generation process can been estimated. The results show that, for UNIBOND SOI wafers, this process is not monoenergetic, and the activation energies range from 0.9 to 1.5eV. The generation of the current peak in the ΔIV_{BG} characteristics is completely correlated with the appearance of a drain current jump near zero V_{BG} in the $I_D(V_{BG})$ characteristics after negative bias has been applied to the substrate (Fig.1 b).

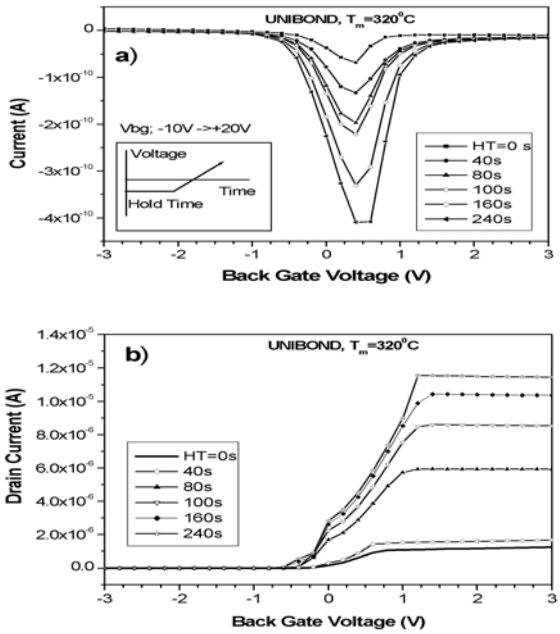

Fig.1: *(a) ΔIV_{BG} characteristics and (b) (I_DV_{BG}) characteristics for applied V_{BG}=-10V with different hold times.*

Measurements made using the TSD/TSP method shown that the application of a negative voltage to the substrate

of the virgin SOI structure results in the formation of wide current spectra in temperature range of 150 to 350^{0}C (Fig.2, curve 2) corresponding to negative charge transport from the BOX/substrate interface to the BOX/ Si film interface. The activation energies of that process range from 0.8 to 1.2 eV. It should be noted that after such a polarization sequence, subsequent temperature heating with positive bias on the substrate results in the appearance of a low-temperature current peak that occurs at 60^{0}C (Fig.2, curve 3) and an activation energy of approximately 0.3 eV. Thus, we can conclude that the high-temperature generation of mobile positive charges that are located near the BOX/substrate interface under negative substrate bias can proceed with electron injection and have activation energy from 0.9 to 1.5 eV.

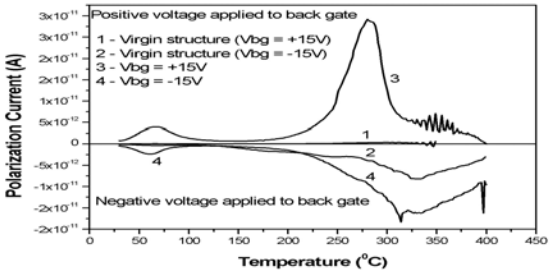

Fig.2: *Thermally-stimulated polarization (V_{BG}=-15V, spectra 2,4) and depolarization (V_{BG}=+15V, spectrum 3) currents in the SOI UNIBOND structure.*

3.2. Positive charge transport

Using of ΔIV_{BG} characteristics allows us to determine the diffusion coefficient, D, of the positive charge transport inside of the BOX after it generation. It has been shown that D can be written in the following form

$$D = 4x10^{-4}exp(-0.55/kT) \quad (cm^2/s)$$

and corresponds to proton transport more than other ion transport (such as Na^+, K^+) [2].

The peak observed at low-temperature TSD corresponds to mobile positive charges with an activation energy near 0.3 eV and is also probably associated with proton transport in the BOX. The decreased activation energy (compared with the results obtained from the ΔIV_{BG} measurement) can be linked to the higher electric field applied to the BOX during the TSD/TSP measurement. Thus, the process of proton generation can be described by the following reaction [3]

$$O_3 \equiv Si–H \;\; H–Si \equiv O_3 \rightarrow O_3 \equiv Si–H–Si \equiv O_3 + e^{(-)} + H^+ + 0.9\ eV$$

where the energy needed for the reaction is very similar to that obtained from our experiments, and the energy distribution can be associated with the spatial separation of Si-H bonds at the BOX/substrate interface.

3.3. Charge neutralization

If a positive voltage is applied to the substrate at high temperature (above 200^{0}C) after generation of mobile protons, a decrease of the drain current jump in the $I_D(V_{BG})$ characteristics is observed (Fig.3). This effect is evidence of neutralization of the generated mobile positive charge.

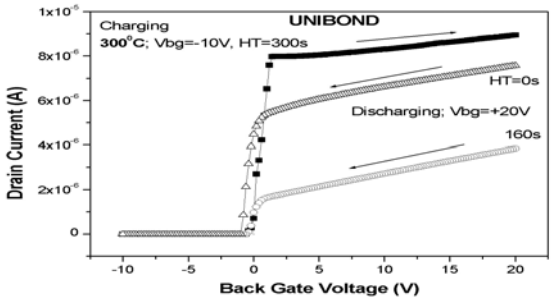

Fig.3: *Transformation of $I_D(V_{BG})$ characteristics after reversing the voltage sweep direction.*

To study the neutralization process the $I_D(t)$ characteristics at high temperature after switching of the substrate voltage from negative to positive have been investigated. It was shown that an increase of positive back-gate voltage increases the relaxation time of the positive charge neutralization (Fig.4a), that corresponds to a decrease of capture probability for the electrons injected into the BOX from the Si film by positively-charged hydrogen centers. The temperature dependence of time relaxation reveals an activation energy of approximately 1.0 eV. Such a temperature dependence is probably associated with a potential barrier which electrons have to overcome for being injected into the BOX from the back inversion channel, and TSD currents that present a peak at 300^{0}C can be explained by this electron injection process (Fig.2).

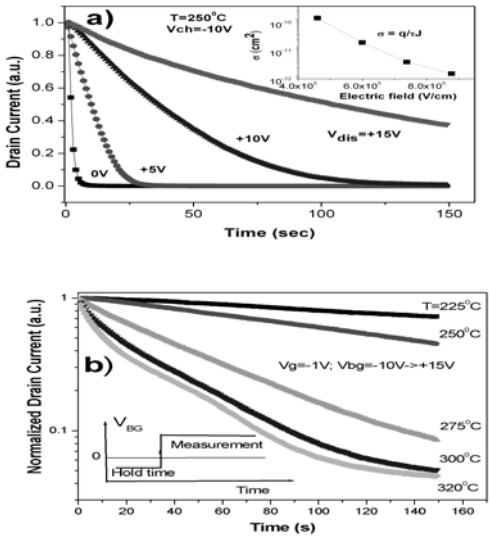

Fig.4: *Dependence of drain current relaxation (a) when applying a discharging voltage to the substrate, and (b) varying measurement temperature.*

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Evaluation of super-critical thickness strained-Si on insulator (sc-SSOI) substrate.

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1. Introduction

Si-On-Insulator (SOI) technology emerged in the 1970s and became gradually popular. Today, strained-Si on insulator (SSOI) has become a very important technology to realize high performance LSI, because strained-Si lead to enhance hole and electron mobilities due to energy-band modification. SSOI can provide advantages from both SOI and strained-Si, such as low-energy consumption and high speed operation without additional layer of SiGe [1]. However, the critical thickness avoiding defect generation in strained-Si was ultra thin, typically less than 15 nm, therefore conventional SSOI could not be applied for the partially-depleted (PD) MOSFET. Recently, SSOI with strained-Si layer thicker than the critical thickness, namely super-critical thickness SSOI (sc-SSOI), has been proposed. In this study, we present evaluation results of SSOI substrate in comparison with a conventional SSOI.

2. Experiment

Commercially available sc-SSOI with 70 nm SOI layer and conventional SSOI with 15 nm SOI were evaluated. The BOX thickness was 145nm. Wafer inspection system installed with UV laser called TOPCON WM-7000 was used for pit-type defects observation. The film thicknesses and their uniformities were measured by spectroscopic ellipsometry. X-ray topography (XRT) images were taken for sc-SSOI using synchrotron radiation at BL20B2 in SPring-8 (2007A1736). The X-ray incident angle and Bragg reflection were carefully chosen so that only SOI layer could be observed. Strong and well-collimated X-ray source at SPring-8 enabled us to achieve this. Strains and their uniformity were evaluated by using UV-Raman spectroscopy mapping technique with 364 nm excitation laser [2]. Both full wafer mappings for 300 mm wafers and detailed closed-up in 20 x 20 μm^2 area were obtained. The surface morphologies were also observed in conjunction with strain micro mappings by AFM. Strain depth profile was characterized by in-plane X-ray diffraction (XRD) with changing the X-ray incident angle to control probing depth of X-ray. Dependence of (400) Bragg spacing perpendicular to the surface on the X-ray incident angle was measured at BL46XU in Spring-8 (2007A1216). Energy of the incident X-ray was 12.0 keV, the critical angle for total reflection of Si substrate was 0.147°.

3. Results and Discussion

Fig.1 shows surface defects observed by UV-installed wafer inspection system. Some straight defects along <110> direction were observed. To verify crystalline structure of these defects, XRT images were taken as shown an example in Fig. 2. Cross-hatched defects were observed all over the 300mm wafer. We have made careful analyses by changing XRT conditions of Bragg reflection with slight sample tilt and concluded the defects were rather complex structures than simple ones with low-index Berger's vector.

Fig.3 and 4 shows in-plane strain distributions in the 300 mm wafers for the conventional SSOI and sc-SSOI, respectively. In both cases, (a) full wafer and (b) magnified close-up mappings were obtained using UV-Raman spectroscopy. The penetration depth of this UV laser (364 nm) is estimated to be 5 nm, therefore the strain at the top surfaces could be evaluated. The full wafer mappings showed slightly different strain distributions although both had higher tensile strain at the center than the edge. In conventional SSOI, the strain was also higher tensile at the top of the wafer and gradually relaxed toward bottom. Meanwhile, in sc-SSOI, the distribution was rather concentric. However, the range of the distribution was approximately the same. The magnified close-up images showed similar in both cases with cross-hatched pattern which should originate in the strain distribution in the donor wafers, while surface morphologies were completely smoothed out.

The Raman spectra obtained from sc-SSOI using visible (532 nm) excitation indicated two peaks from both entire SSOI film and base substrate. The full width at half maximum (FWHM) of the peak from SSOI 2.74cm^{-1} was larger than that from base substrate 2.69cm^{-1} implying poor crystal quality.

To verify the strain depth distribution, in-plane XRD measurement was performed. Fig.5 shows the observed 400 peak profiles at various X-ray incident angles. Since all observed XRD peaks angles were the same as shown in Fig.5, we conclude the strain was quite uniform along depth direction. Further increase of incident angle allowed us to observe peaks from both SSOI and base wafer simultaneously as shown in Fig. 6. It is apparent that the FWHM of the peak from SSOI was much larger than that from base substrate, reflecting poor crystal quality.

4. Summary

Both strain distribution and crystal quality in strained Si of sc-SSOI and conventional SSOI were measured by UV-Raman spectroscopy and in-plane XRD. In full wafer mapping for each SSOI, the strain had higher tensile at the center than at the edge. Crosshatch contrasts corresponding misfit dislocations were observed in the magnified close-up in both SSOI. By in-plane XRD, it is apparent that the FWHM of the peak from SSOI was larger than that from base substrate, reflecting poor crystal quality.

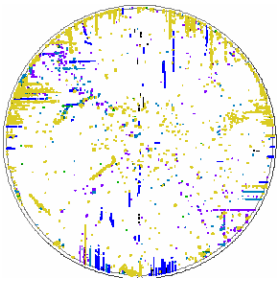

Fig. 1 Surface defects in sc-SSOI substrate observed by wafer inspection system

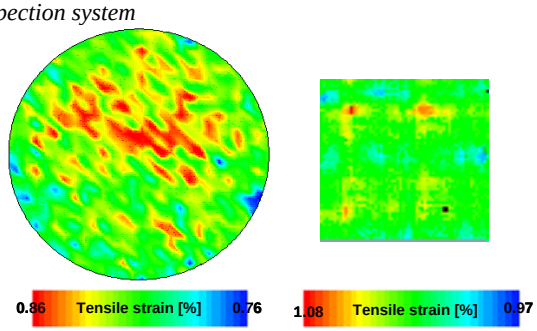

Fig.3 Strain distribution in conventional SSOI for (a) 300 mm full wafer, and (b) magnified close-up in 20 x 20 μm^2 area

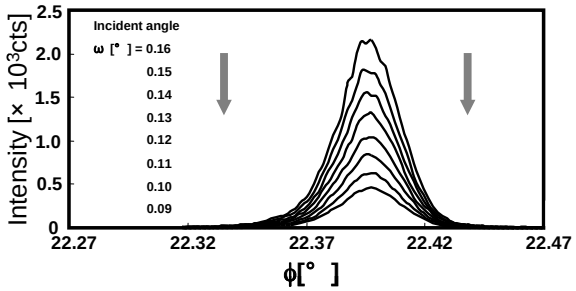

Fig.5 In-plane XRD for sc-SSOI with changing incident X-ray angle indicating strain depth profile.

No clear difference was detected between conventional SSOI and sc-SSOI.

Acknowledgments

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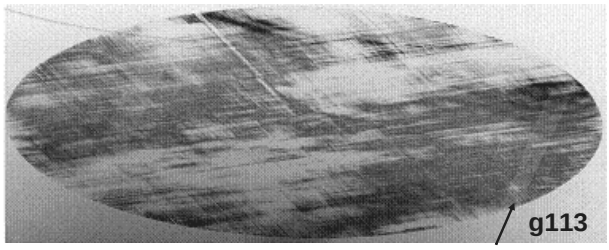

Fig. 2 XRT image of sc-SSOI substrate.

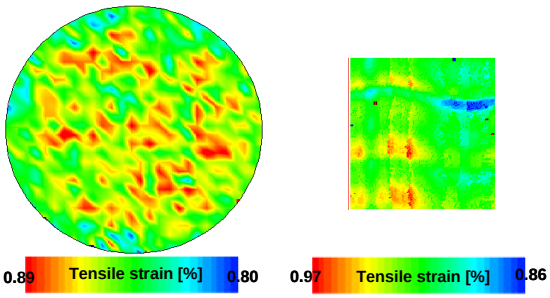

Fig.4 Strain distribution in sc-SSOI for (a) 300 mm full wafer, and (b) magnified close-up in 20 x 20 μm^2 area.

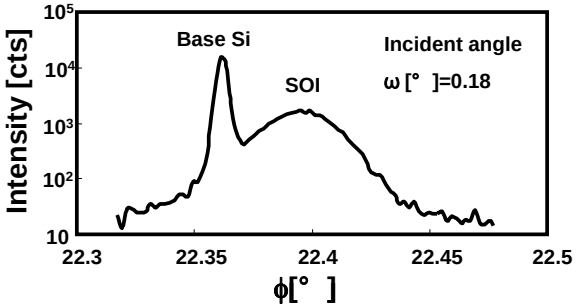

Fig. 6 In-plane XRD for sc-SSOI with incident angle at 18° with double peak from SOI and base Si.

SESSION 6

RF Passive Devices

CHAIR
J.-P. Raskin
Université catholique de Louvain

High-Performance Thick Copper Inductors Integrated in Advanced High Resistivity SOI RF CMOS technology

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1. Abstract

This paper presents high Q and high current on-chip inductors fabricated on High Resistivity (HR) substrate using an Advanced SOI CMOS technology with a 3 µm Thick Copper Back End of Line (BEOL) module. According to measurement results, reported SOI inductors offer quality factor Q greater than 27 and a current capability up to 16 mA/µm @ 125 °C in an Advanced Thick Copper BEOL dedicated to RF power applications.

2. Introduction

As CMOS technology continues scaling down allowing operations in the gigahertz region [1], the opportunity is given to the low-cost integration of RF/Digital/Analog blocks on the same chip for System On Chip (SOC) applications. However, to reach the desired and cost effective performances, a large spectrum of technologies is required today. Generally, antenna switches are based on GaAs pHEMT technology, Power Amplifiers are designed using GaAs HBTs, whereas baseband and power management ICs are strictly achieved with a CMOS process. Integration in Front-End increasing, technology will drive the partitioning towards Digital-Only in deep submicron CMOS process and RF/Analog in a higher voltage CMOS one. In this quest, SOI technology appears as a good candidate since the advantage is well-known for the Digital part, both from performances and consumption points of view. Actually, high performance antenna switches have already been integrated on SOI [2] and very recently, the feasibility of Power Amplifier on SOI has been demonstrated [3]. The last key issue but not the least, concerns the integration of high performances (including high current) passive components in a Standard Digital technology.

In this paper, we will explore this particular point, first by reviewing the insulating behavior of HR SOI material, and then proposing an analysis of optimized HR SOI inductors dedicated to power applications. For the first time, results concerning inductors using a Thick Copper BEOL module on HR SOI are presented.

3. Advantage of HR SOI Substrate for the integration of RF Passive Components

Integrating high quality passive components in standard silicon technology is not an easy task, the fundamental limitation of conventional bulk technologies (both CMOS and BiCMOS) being inherent to high substrate losses.

However, very recently, high quality passive components (coplanar waveguide transmission line with less than 1dB/mm of losses @ 100GHz) integrated in Advanced 130 nm SOI CMOS technology using Soitec® High Resistivity Unibond substrate have demonstrated performances comparable to the state of the art III-V technologies up to W band (75-100GHz).

This insulating behavior of SOI material has been demonstrated up to 220 GHz. To illustrate this point a 180 GHz band pass filter realized in STMicroelectronics HR SOI technologies is presented Fig. 1.

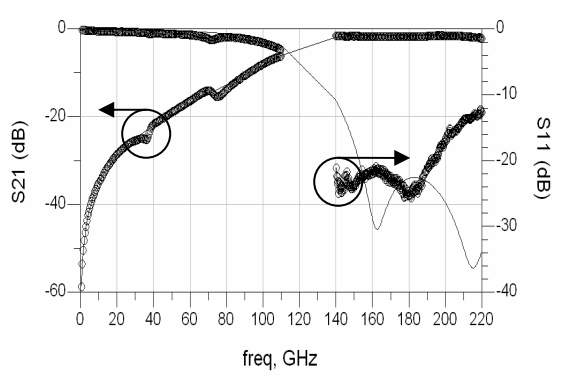

Fig.1: *Performances of 180 GHz CPW band-pass filter achieved on HR SOI CMOS technologies [5]*

4. HR SOI Inductors dedicated to power applications

As integration level is increasing, metal thickness is typically thinned to decrease the achievable pitch. Inter-layer dielectrics diminishing too in Advanced technologies, it becomes more and more difficult to obtain High-Q on-chip inductors in Standard Bulk

processes. Actually, the highest-Q integrated inductors in Bulk technologies are achieved over a Patterned Ground Shield (PGS) to limit the losses in the substrate using only one thick top level of BEOL to reduce the resistive losses, and the parasitic capacitance with the PGS [4]. In SOI, the opportunity to use high-ohmic substrates (ρ>1000 Ω.cm), which suppress substrate losses [5], allows to avoid this PGS use. As a consequence, better quality factor Q can be achieved. Moreover, since there is no substrate loss in HR SOI, inductors can be fabricated as close as possible to the substrate. Then, inductor can be stacked using the whole BEOL down to Metal 1 (cf. Fig. 2), which allows a coil resistance optimization. This new class of inductor has been benchmarked with conventional bulk one, demonstrating an improvement up to 30% of achievable maximum Q factor @ 5 GHz (Table 1) [6].

	Bulk	HR SOI
Q @5GHz	15	20

Table.1: Benchmarking of a 0.82 nH inductor achieved in 65 nm CMOS bulk and HR SOI technologies.

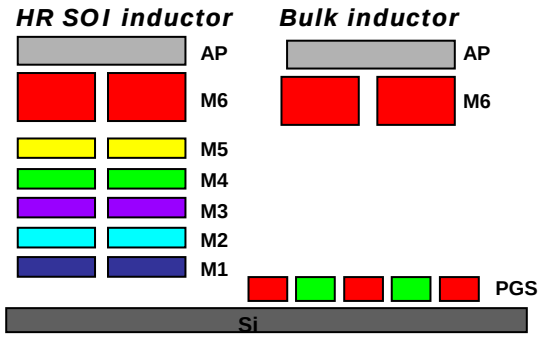

Fig.2: *General architectures of HR SOI and Bulk high Q inductor.*

5. Thick Copper Technology on HR SOI: Integration of High Performance Integrated Inductors

For this study, octagonal symmetrical inductors were fabricated on a High Resistivity (HR) substrate in an Advanced SOI CMOS technology using a Damascene Copper Back End. The technology consists in six metallization levels, an aluminium capping layer AP, and dielectric layers between all conductive layers with a dielectric constant equal to 4 (Fig. 2). For the first time, a 3 µm Thick Copper Module has been implemented at the last metal level to investigate achievable quality factor and maximum current capability of inductors realized with HR SOI technology. The crossing point of the studied inductor (Fig. 3) is made of the stack (M1-M5+ AP) and with M6 alone (Fig. 2). Its geometrical characteristics are the following ones: R_{int}= 40 µm, w=18 µm, spacing= 10 µm, 2 turns.

One-port S-parameter measurements up to 50 GHz were performed on the achieved inductor using an Agilent HP8510C VNA and Cascade Microtech Infinity GSG RF probes. De-embedding was performed using a dedicated open structure to remove pad contribution [7]

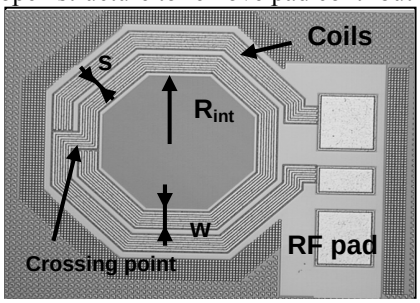

Fig.3: *Used RF pad, and studied inductor image.*

Thanks to the combination of Thick Copper and HR SOI technology, a 0.8 nH high performance inductor is obtained presenting a Q factor over 27 at 3.5 GHz, and a cut-off frequency exceeding 36 GHz (Fig. 4).

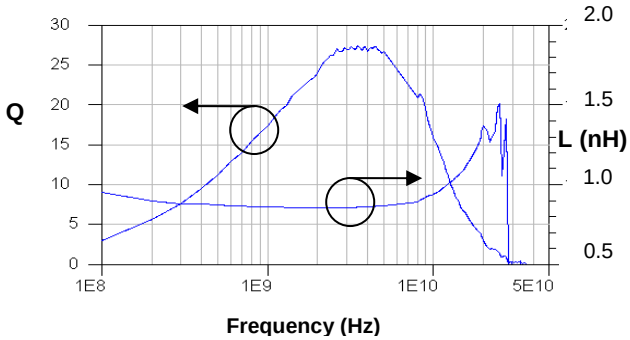

Fig.4: *Measured quality factor Q and L value of studied inductor combining HR SOI technology and Thick Copper module.*

Concerning the current capability of such an inductor, it reaches 288 mA @ 125 °C.

6. Conclusions

In this paper, state of the art inductor (Q of 27 @ 3.5GHz) achieved in an Advanced low cost HR SOI RF CMOS technology using a Damascene Copper BEOL with a 3 µm thick last copper level has been presented for the first time. This high Q inductor can reach a maximum current of 16 mA/µm @ 125°C, which confirms the potentiality of SOI technology for the integration of low cost power applications on silicon.

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Temperature and Bias Dependent Performance of Coplanar Waveguide on High Resistivity Silicon Substrate with Passivation Layer

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1. Abstract

This paper presents the attenuation (α) and the extracted relative substrate permittivity (ε_r) of coplanar waveguide (CPW) transmission lines on oxidized high resistivity (HR-Si) substrates with and without a polysilicon (PSi) passivation layer. The temperature and bias dependence of the attenuation under different operation points are evaluated from 40 MHz to 40 GHz. Measured results show that the use of a passivation layer successfully removes the bias-dependence of oxidized HR-Si substrates, not only at room temperature but also up to 200 ºC. An increase in the attenuation with temperature due to substrate resistivity change is also observed for both substrate types, with and without passivation layer. HR-Si using a polysilicon layer as passivation layer presents attenuation values 4 dB/cm lower in all the investigated frequency range, for temperatures up to 200°C and bias ranges from -20 V to 20 V, than a comparable oxidized HR-Si substrate.

2. Introduction

In the last few years big efforts and research have been undertaken in the aim to open new markets to silicon technology. Its low cost and maturity make silicon an ideal technology for many applications. In particular, the introduction of HR-Si substrates has converted silicon into a suitable technology for high frequency applications [1]. However, for many RF high temperature applications, low losses, thermal and bias operation point stability performance are a key point. It is known that oxidized HR-Si suffer from parasitic surface conduction (PSC) at the Si/SiO_2 interface, thereby reducing the effective resistivity of the wafer by several orders of magnitude [1]-[2]. In addition, surface charge concentration also depends on the applied bias voltage, leading to bias-dependent losses. Both issues can be overcome by introducing a trap-rich passivation layer, such as PSi [3] or crystallized amorphous silicon [4], between the oxide and the HR-Si substrate. The traps literally capture the free carriers, thereby enabling the substrate to recover its nominal resistivity value. At high temperature, it has been demonstrated [5] that despite the increase of intrinsic mobile carriers (n_i) inside the Si substrate with temperature increase, losses of CPW lines lying on HR-Si remain lower than those for standard resistivity substrates up to 200°C.
In the next paragraphs the behavior of CPW lines on HR-Si with and without passivation layer is presented and compared under different temperature conditions and bias voltages.

3. Experimental Results

A set of CPW lines with a characteristic impedance of 50 Ω were fabricated on top of two oxidized HR-Si substrate (ρ > 5 kΩ.cm), with and without a 300 nm-thick PSi layer, obtained by LPCVD deposition at 625ºC. The thickness of the top SiO_2 layer was 50 nm for both substrates. The strip, slot, and planar ground widths of the 1 µm-thick aluminium CPW lines were 38, 18 and 213 µm, respectively.
Microwave measurements from 40 MHz to 40 GHz were made using a Vector Network Analyzer and an on-wafer RF probe station. The central strip of the line was biased with a voltage from –20 V to 20 V that was applied simultaneously at both signal pads of the GSG RF probes through bias-tees. Besides, the wafer temperature was varied by heating the wafer chuck from room temperature to 200 ºC.
Figs. 1 and 2 show the measured attenuation and extracted relative permittivity of a 8000 µm-length CPW line at room temperature and at zero bias. It can be observed that due to PSC effects, the attenuation at 20 GHz of the CPW on HR-Si without PSi is much higher (6.2 dB/cm) than expected for a HR-Si substrate. As observed in Fig. 1, thanks to the use of a passivation PSi layer, CPW losses are reduced by at least 4 dB/cm at 20 GHz, recovering the HR characteristics of the Si substrate. As it can be observed, the extracted relative substrate permittivity corresponds, for both substrates, to that of silicon, around 11.7. The bias-dependence attenuation and its reduction for oxizided HR-Si without and with passivation, respectively, are confirmed in Fig. 3. As expected, the attenuation of the CPW line on HR-Si under different temperature conditions also varies with bias voltage. This is not the case when a passivation layer is introduced (Fig. 5). For both

substrates, Fig. 6 shows that the attenuation increases with temperature due to the increase of n_i in the substrate. Even if the passivation layer is efficient for trapping the mobile carriers generated at the Si substrate-oxide interface and not in the substrate volume, the passivated substrate presents at least 4 dB/cm lower losses also for temperatures above 150°C.

4. Conclusions

The attenuation of a CPW line under different temperatures and voltage bias points and lying on a HR-Si with and without passivation layer was analyzed. Bias independence when using HR-Si with a passivation layer was demonstrated from room temperature up to 200 °C. HR-Si with passivation layer presents lower losses than classical oxidized HR-Si substrates for all of the studied operation points (DC bias and temperatures), foreseeing the use of this technological solution for high temperature applications.

Acknowledgements

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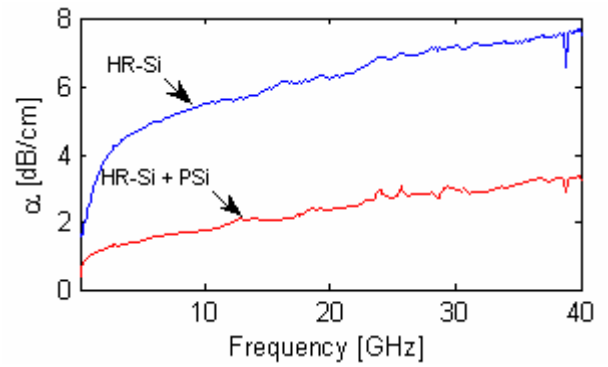

Fig. 1: *Attenuation of CPW line for zero bias at ambient temperature.*

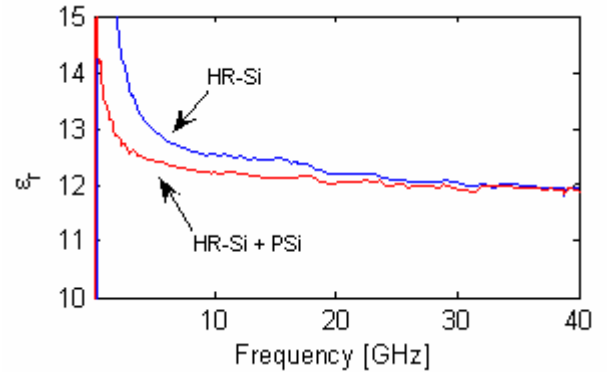

Fig. 2: *Extracted Relative Permittivity of a HR-Si substrate with and without PSi layer.*

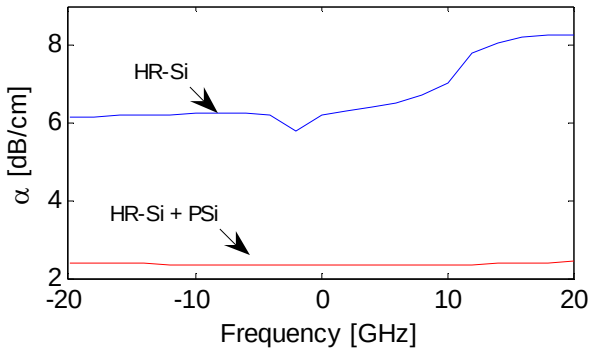

Fig. 3: *Attenuation vs. DC bias for a CPW line on HR-Si substrate with and without a PSi layer at room temperature.*

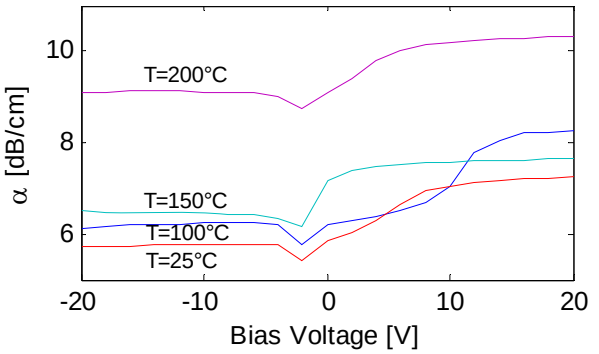

Fig. 4: *Attenuation vs. DC bias at various temperature conditions for a CPW line on HR-Si substrate.*

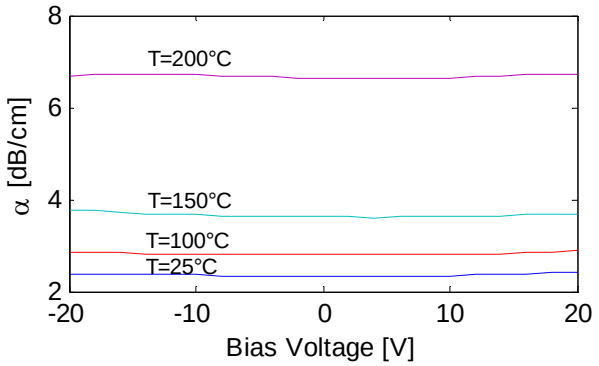

Fig. 5: *Attenuation vs. DC bias at various temperature conditions for a CPW line on HR-Si substrate with PSi layer.*

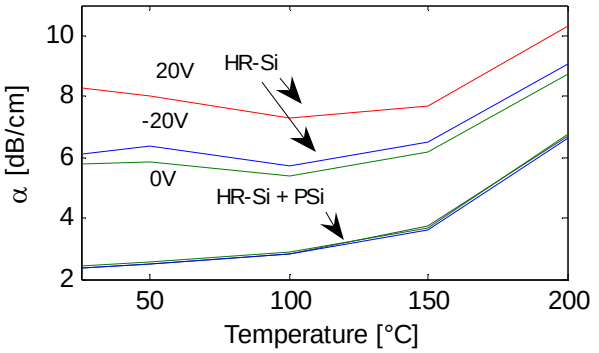

Fig. 6: *Attenuation vs. Temperature at three different DC bias points for a CPW line on HR-Si with and without PSi layer.*

Temperature Behavior of Spiral Inductors on High Resistivity Substrate in SOI CMOS Technology

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***Abstract*— This paper reviews and analyzes a physical model for integrated planar spiral inductors on high resistivity substrate in Silicon-on-Insulator (SOI) technology. The inductors has been characterized over a temperature range from 25 to 200^oC. The temperature variation of each model parameters have been investigated. The model has been confirmed with measurement results for wide temperature range. These performance trends can be a good guideline for practical inductor designs in RFICs for high temperature applications.**

***Index Terms*— SOI, Inductor π-model, Quality factor, High resistivity substrate (HRS), High-Temperature effect.**

I. Introduction

The Silicon-on-Insulator (SOI) CMOS technology has become a competitive technology for radio transceiver implementation of various wireless communication systems due mainly to low-power, low-cost, higher level of integrability, high performance mixed-mode circuits, etc. [1]-[2]. Nowadays, an increase number of integrated inductors are required for building compact analog blocks of multi-standard mixed-mode IC's. In the past decades, great efforts have been devoted to the modeling, optimization and design of the spiral inductors on silicon and GaAs substrates. The approaches, such as using high resistivity substrate and high conductive metal layers, thick dielectric layer or selectively etching off substrates, stacking metal layers, and even differentially driven inductors, have been reported [3]. However, none systematic study on the performance trend of spiral inductors with temperature has been reported in the literature, except in [4]. In the present paper, a model is built up in order to characterize the inductors behavior at high temperature.

II. Physical Model of a Spiral Inductor

In most cases, integrated spiral inductors are used in a frequency range that is far away from its first self-resonance frequency (SRF). In this case, integrated spiral inductors on silicon can be accurately characterized by a physical π-model as shown in Fig. 1 [5]-[6].

The inductance and resistance of the spiral and underpass are represented by the series inductance, L_s, and the series resistance, R_s, respectively. The overlap between the spiral and the underpass leads to direct capacitive coupling between the two terminals of the inductor. This feed-through path is modeled by the series capacitance, C_s. The oxide capacitance between the spiral and the silicon substrate is modeled by C_{ox1} and C_{ox2}. The capacitance and resistance of the silicon substrate are modeled by C_{Si1}, C_{Si2}, and R_{Si1}, R_{Si2}, respectively. These values mainly vary with the overall track area for a given substrate and inductive structure.

III. Temperature Behavior Analysis

In this section, a temperature characterization of the spiral inductor is presented. The inductor has been characterized over a temperature range from 25 to 200^oC and a frequency band up to 20 GHz. The layout of the characterized spiral inductor is presented in Fig. 1(a). The tested inductor has a conductor width W of 12 μm, conductor spacing S of 3 μm, inner diameter D_i of 100 μm and number of turns N_T of 4.5. The spiral inductor has been fabricated on 130-nm SOI CMOS technology using a high resistivity substrate ($\rho \approx 2$ kΩ.cm).

The extracted parameters of π-model are shown in Fig. 2. After VNA calibration and appropriate de-embedding, we extract first the parameters L_s, R_s, C_{ox} and R_{Si} at low frequency, and then C_{Si1} and C_{Si2} at high frequency. The parameter C_s is extracted at self-resonance frequency of the inductor [6].

The measurements show a large impact of temperature on the parasitic series resistance R_s (degradation of 52% is noted when temperature varies from 25 to 200^oC). The characteristic of R_s versus temperature is plotted in Fig. 3. As expected, R_s increases with temperature and varies linearly with the temperature according to

$$R_s(T) \approx R_s(T_0) + \theta(T - T_0) \quad (1)$$

where $R_s(T_0)$ is the series parasitic resistance at ambient temperature and the parameter $\theta = \partial R_s(T)/\partial T \approx 0.011$ $\Omega.^oC^{-1}$.

The different parasitic capacitances show a negligible temperature dependence (7% for the considered temperature range). The temperature variation does not impact the substrate and oxide dielectrics (ϵ_{Si} and ϵ_{ox}). So the temperature dependence of C_{ox} and C_{Si} is mainly due to the geometrical variation of DUT at high temperature (welding of the tested die with temperature).

The extracted quality factor Q defined by Q=$-$imag(Y_{11})/real(Y_{11}) for various temperatures is presented in Fig. 3. The measurements show a degradation of 32% of maximum quality factor when temperature varies from 25 to 200^oC. The temperature degradation of Q is mainly due to the R_s increase.

The extracted π-model parameters at T=25^oC and at 200^oC are summarized in Table I. The experimental and simulation results show the validity of the proposed model for a wide temperature range considering only the temperature variation of the parameter $R_s(T)$ as presented in Fig. 4.

The simulations are performed using the π-model (Fig. 1(c)) which takes into account the temperature variation of $R_s(T)$

according to the linear law described in (1). The results show a good agreement between simulation and measurement results.

IV. Conclusions

We studied the impact of temperature on the parameters of π-model integrated spiral inductors fabricated in a 130-nm SOI CMOS technology. We note a degradation of 32% of the quality factor when the temperature varies from ambient to 200^oC. We report that thanks to the use of a high resistivity substrate, only the parasitic serie resistance contributes to the temperature degradation of the quality factor.

Acknowledgments

The authors wish to thank ST-Microelectronics, for chip fabrication. This work has been funded by The Walloon Region (Convention n° 03/1/5623).

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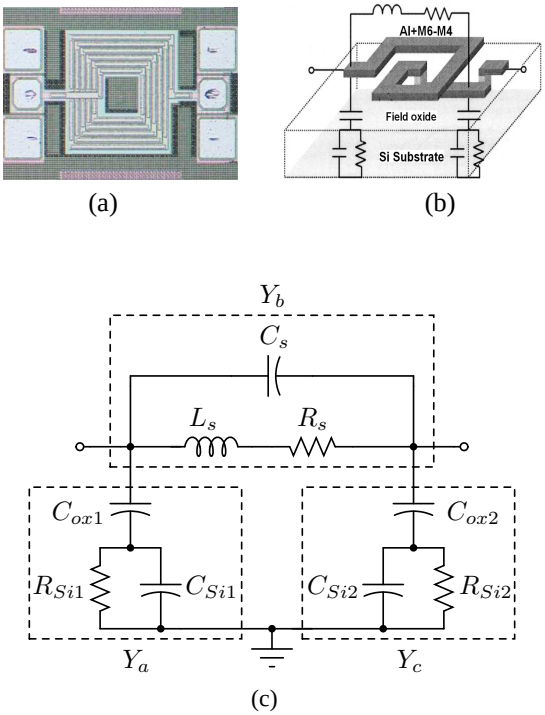

Fig. 1. (a) Chip microphotographs, (b) 3-D view, (c) the lumped physical equivalent model of a spiral inductor on silicon.

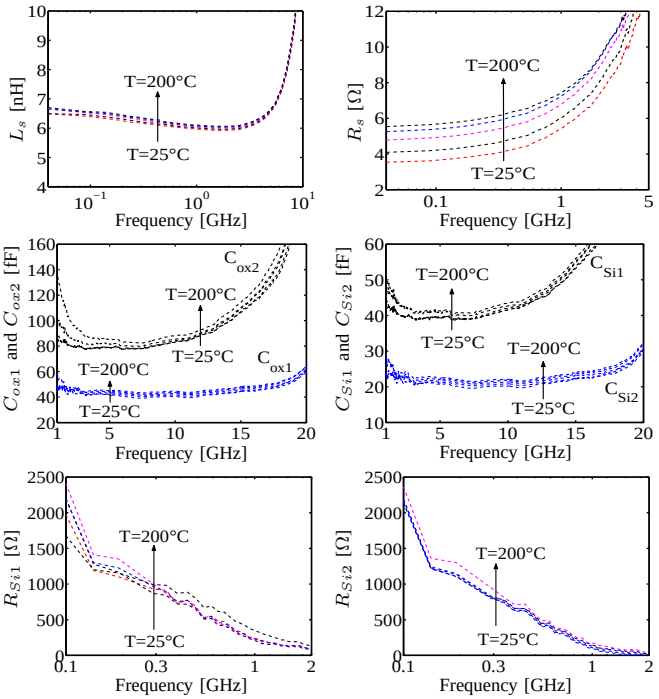

Fig. 2. Extracted π-model parameters of 4.5-turn inductor for various values of temperature.

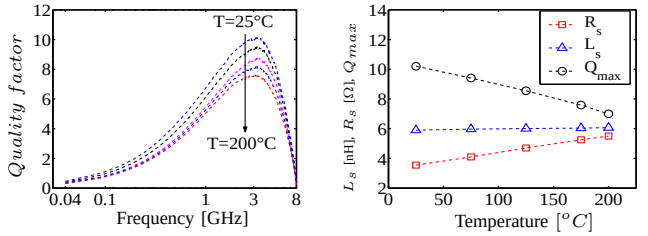

Fig. 3. Extracted quality factor of spiral inductor for various values of temperature.

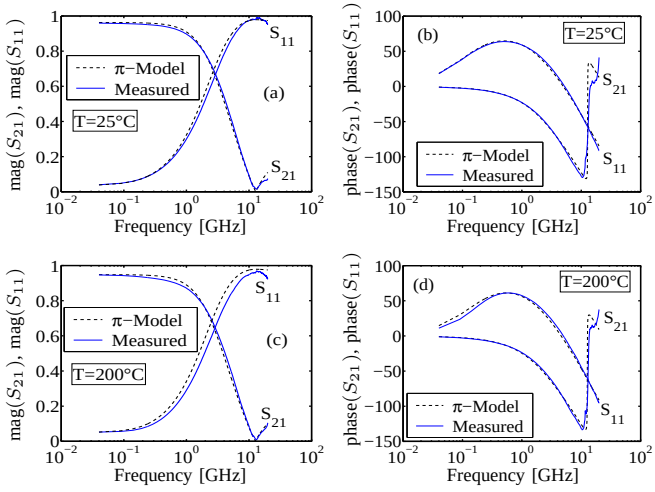

Fig. 4. Comparison of S-parameters (magnitude and phase) between π-model simulation and measurements, (a) and (b) for T=25^oC, (c) and (d) for T=200^oC for 4.5-turn spiral inductor.

	L_s [nH]	R_s [Ω]	C_{ox1} [fF]	C_{ox2} [fF]	C_{si1} [fF]	C_{si2} [fF]	Q_{max}
T=25^oC	5.9	3.6	41	79	20.5	39	10.2
T=200^oC	6.07	5.5	43	83	22	41	7
Er [%]	2.9%	52%	4.9%	5.1%	7.3%	5.1%	32%

TABLE I

Summary of π-model parameters of spiral inductor for room temperature and 200^oC.

SESSION 7

SOI Device Physics and Characterization I

CHAIR
F. Gámiz
Universidad de Granada

Substrate bias effects on the performance of Schottky-barrier SOI nMOSFETs

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Abstract

The experimental results on the enhanced performance of Schottky-barrier SOI nMOSFETs (SB MOSFET) with substrate bias (V_{BS}) are discussed. Erbium silicide was used to form Schottky barrier source/drain of SOI nMOSFET. With appling V_{BS}, the drain current ratio (I_{ON}/I_{MIN}) and subthreshold swing can be improved from $1.8x10^6$ to $1.0x10^7$ and from 75mV/dec to 66mV/dec at low V_{DS}, respectively. Our results show that SB nMOSFET is a very promising device if the optimum guideline for V_{BS} can be provided.

1. Introduction

The barrier height in SB MOSFETs should be low enough to have a high drain current and to prevent two different slope in subthreshold region. Although erbium silicide SB nMOSFETs have been fabricated with good characteristics, the performances of SB nMOSFETs are still inferior to PN junction devices due to the lack of optimized silicide technology [1-3]. Recently, simulation work showed that the performance of SB nMOSFETs can be enhanced by the modulation of barrier height with V_{BS} [4].

In this work, SB nMOSFETs with quite acceptable perfromance have been fabricated and the experimental results on the enhanced performance with V_{BS} are presented.

2. Device fabrication

Fig.1 shows the schematic diagram of the fabricated erbium-silicided n-type Schottky barrier MOSFET. A <100> p-type silicon-on-insulator wafer doped with boron was used. The doping concentration of the SOI film is $1.0x10^{15}cm^{-3}$. The thickness of the SOI wafer and BOX are 100nm and 200nm, respectively. The 8nm gate oxide was grown by thermal oxidation and the gate material is phosphorus-doped n-type polysilicon. A 100nm-thick erbium layer was sputtered. Before erbium sputtering, the base pressure was about $1.0x10^{-7}$ Torr to prevent the contamination of erbium during sputtering process. The erbium silicide was formed by using RTA at 500℃ for 5 min. During the annealing process, the pressure within the RTA chamber was controlled below $1.0x10^{-6}$ Torr to prevent the oxidation of erbium. The nonreacted erbium was removed by using the mixture of H_2SO_4 and H_2O_2 for 10 min. The gate length and width of fabricated devices were 2um and 20um, respectively.

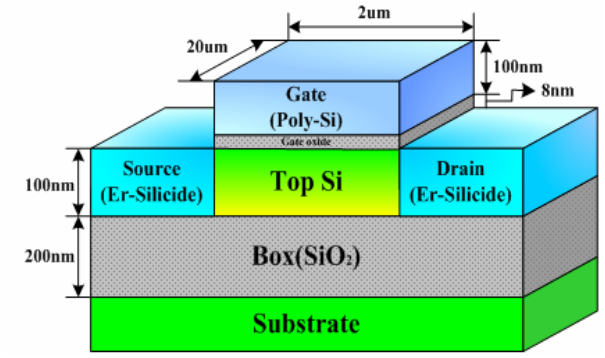

Fig.1 Schematic diagram of SB nMOSFET

3. Results and discussion

From the typical transfer characteristics of SB MOSFET as shown in Fig.2, the saturation drain current (I_{ON}) is 1.3uA/um at V_{GS}=2V and the minimum drain current (I_{MIN}) is $7.2x10^{-7}$uA/um. Therefore the I_{ON}/I_{MIN} ratio reaches about $1.80x10^6$ and the inverse subthrehold slope is about 75mV/dec at V_{DS}=0.05V.

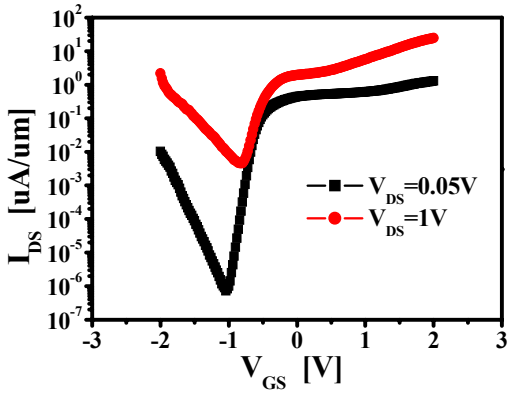

Fig.2 Typical transfer characteristics of SB nMOSFET

The transfer curve of the fabricated device is shown in Fig.3 as a function of substrate bias. It can be clearly seen that when a negative V_{BS} is applied, I_{MIN} decreases, and that the point of I_{MIN} moves toward positive V_{GS} values. At the same time, I_{ON} decreases slightly, and the leakage current in the off state (I_{OFF}) increases. The V_{GS}

for I_{MIN} corresponds to the position where tunneling current (T_N) becomes larger than thermoionic current (T_H). The reason for V_{GS} shift is that T_H dereases with increasing a negative V_{BS}. This result indicates that the width and height of the barrier are modulated with V_{BS}. Fig. 4 plots the comparison of the SB MOSFETs performance with V_{BS} varying from -12V to 1V. I_{OFF} has minimum value at V_{BS}=0V and increases with increasing negative and positive V_{BS}. It can be observed that I_{MIN} has U-like shape and it has a minimum value of $7x10^{-8}$ uA/um at V_{BS}=-4V. I_{ON} decreases slightly with increasing negative V_{BS}. And thus I_{ON}/I_{MIN} ratio increases from $1.8x10^6$ at V_{BS}=0V to $1.0x10^7$ at V_{BS}=-4V. Under the bias conditions V_{BS}<-4V, I_{MIN} increases due to increasing tunneling hole current. And at positive V_{BS}, I_{MIN} also increases due to the large T_H. Therefore we can maximize I_{ON}/I_{MIN} ratio with modulation of Schottky barrier height and width appling V_{BS}.

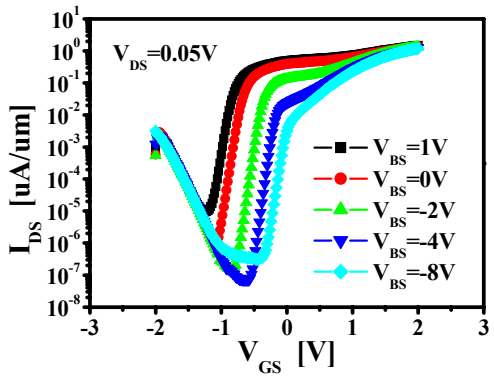

Fig.3 Transfer curve of SB nMOSFET with V_{BS}

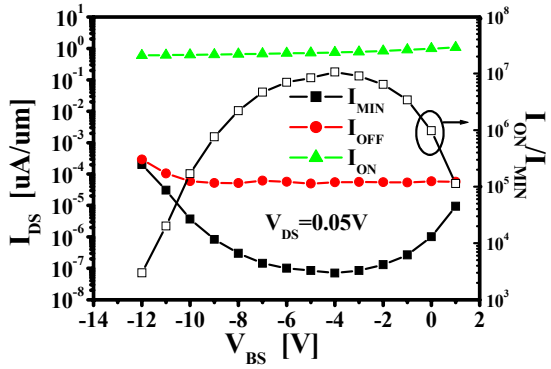

Fig.4 Comparison of the SB nMOSFETs performances with V_{BS}

The V_{TH} variation with V_{BS} in Fig.5 shows that V_{TH} is increased due to the increase of barrier width when a negative V_{BS} is applied. It is also observed that V_{TH} is decreased when V_{DS} is increased. This is due to the drain-induced barrier lowering (DIBL) effects. DIBL is defined as the difference in threshold voltage when the drain voltage is increased from 0.05V to 1.0V.

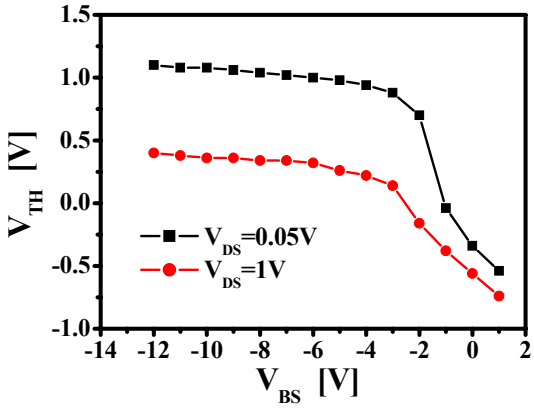

Fig.5 V_{TH} variation with V_{BS}

Fig.6 shows S and DIBL as a function of V_{BS} at V_{DS}=0.05V. It can be seen that S is improved from 75mV/dec at V_{BS}=0V to 66mV/dec at V_{BS}=-4V. However, DIBL is increased from 0.22V at V_{BS}=0V to 0.72V at V_{BS}=-4V. Futher investigation is needed to understand why DIBL is largest at around V_{BS}=-2V. Therefore, there is a trade-off between I_{ON}/I_{MIN} ratio, S and DIBL when the substrate is negatively biased. The optimized V_{BS} can enhance the performance of Schottky barrier nMOSFET. With considering of I_{ON}/I_{MIN} ratio, S, and DIBL, we can clearly see that the optimum bias is around V_{BS}=-1.0V for this device.

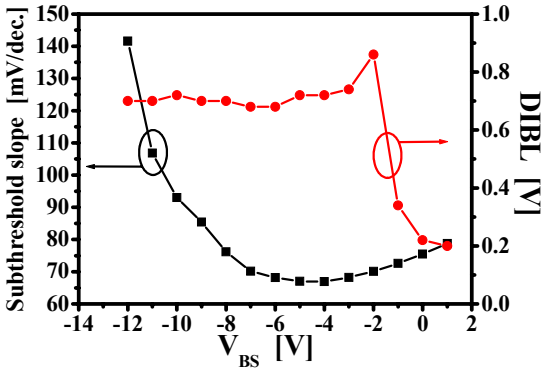

Fig.6 S and DIBL versus V_{BS}

4. Conclusions

Erbium silicide SB nMOSFETs with quite aceeptable performance have been fabricated. Our experimental results show that the drain current I_{ON}/I_{MIN} ratio and subthreshold swing can be improved from $1.8x10^6$ to $1.0x10^7$ and from 75mV/dec to 66mV/dec at low drain voltage, respectively, if a substrate bias is applied.

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A Radiation Study of High-Resistivity SOI Substrates for High Energy Physics Applications

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Abstract

SOI substrates are important for the fabrication of monolithic active pixel high energy physics particle detectors. In this work self-aligned circular geometry MOS transistor test structures were fabricated on ion split bonded SOI substrates to evaluate the interface between the high resistivity handle silicon and the SOI buried oxide. Pre- and post- proton irradiation transistor measurements are presented, showing an increased SOI buried oxide trapped charge of only 3.45×10^{11} cm^{-2} for a dose of 2.7 Mrad.

Summary

High energy physics ionising particle detectors are generally implemented using a pixelated sensor device with separate readout circuitry. An alternative is to fabricate a monolithic active pixel detector which integrates the readout electronics and the sensor device in one substrate. This solution not only eliminates the hybridisation process, but also provides thinner devices suitable for inner layers of particle physics vertex detectors. Silicon On Insulator (SOI) structures are ideal for monolithic detectors, combining reverse biased p^+-n^- pixel diodes in a fully depleted high resistivity n-type substrate 'handle' layer and readout electronics in a low resistivity 'device' layer, interconnected by vias through the insulating SOI buried oxide (BOX) [1]. The electrical integrity of the interface between the SiO_2 BOX layer and the high resistivity Si handle wafer is crucial to minimise dark current in the completed detector. This paper describes the use of self-aligned gate circular geometry p-channel MOS transistor test structures fabricated in ion split bonded silicon SOI substrates to examine this interface. These transistors employ the handle layer p^+ pixel diode diffusions as source and drain electrodes, with the BOX layer as the gate dielectric.

The SOI wafers were prepared using ion split technology [2]. P-type device wafers (10-20 Ω-cm) were implanted with H_2 (3×10^{16} cm^{-2}) through a 100 nm pad oxide layer. A 500 nm BOX layer was grown on high resistivity (4 kΩ-cm) n-type FZ handle wafers at 1050°C using a hydrox process, before bonding to the device wafers. For this application it is important that the SOI BOX layer is grown on the handle wafers so that the bond interface is between the BOX and the device wafer. The bonded wafer pairs were then ion split annealed at 500°C for 2 hrs in N_2 to give a 500 nm transferred SOI device layer, before a final 2 hr bond strengthening N_2 anneal at 1050°C.

Circular geometry MOS transistor test structures with gate lengths of 30 and 100 µm were fabricated in this SOI substrate. Figure 1 shows the cross-sectional view of the completed structures. Firstly, phosphorus diffusion (1000°C) was used to form a n^+ contact layer at the back of the n^- substrate. Sacrificial LPCVD Si_3N_4 was then employed as a mask when wet etching source and drain regions in the SOI device layer and the BOX layer. Boron diffusion (1000°C) was used both to create the p^+ source and drain electrodes in the n^- substrate, and at the same time to further dope the SOI device layer for use as the gate electrode. Low temperature SiO_2 was then deposited and patterned to form contact windows, before sputtering and patterning 3 µm Al/Si as the metallisation. A 450°C H_2/N_2 anneal completed device processing.

The completed MOS transistors were DC tested using a HP4155A parameter analyser in a dark, electrically screened enclosure. Output and transfer characteristics, along with p^+-n^- substrate diode leakage were obtained. The threshold voltage of the transistors was positive at a value of + 0.2 V. A negative threshold voltage was expected in the range 1-2 volts, dependent on fixed charge density. The presence of small doses of boron in the high

resistivity silicon due to trace environmental or chemical contamination would result in the threshold voltage becoming positive. SIMS analysis of the substrates has been undertaken and there is no evidence of boron contamination. Theory suggests that for this structure a threshold voltage of +0.2 V would be achieved for an extremely low oxide fixed charge density of 1x10 cm^{-2}. It has previously been observed by some of the authors, and others, that wafer bonding can lead to the creation of negative fixed oxide charge located initially at the bond interface [3]. Subsequent anneals can reduce the magnitude of this negative charge, and similar changes in charge magnitude are also observed at the handle wafer interface. This mechanism would explain the reduction in fixed charge to the ultra-low value extracted from the measurement data presented here.

The devices were then irradiated at CERN with 24 GeV protons with doses of $7.9x10^{11}$, $1.1x10^{12}$, $9.5x10^{12}$ and $9.6x10^{13}$ cm^{-2} (equivalent to the range 22 krad to 2.7 Mrad). Figure 2 shows the effect of irradiation on the transfer characteristics of a typical 100 µm gate length transistor. A similar result was observed on 30 µm gate length transistors, and the threshold voltage shift as a function of proton irradiation dose for both device geometries is shown in Figure 3. The increasing negative shift in threshold voltage with higher proton doses is due to the build up of ionised positive charge in the BOX layer at the SiO_2/Si interface. The maximum proton dose of 2.7 Mrad has caused a threshold voltage shift of approximately 8 V, indicating that the trapped charge in the 500 nm gate oxide has changed by only $3.45x10^{11}$ cm^{-2}. This structure has not been optimised, but these results show that high resistivity handle wafers retain their integrity even after experiencing device processing thermal budget, and show the suitability of the SOI substrate for integration of detection devices with IC technology.

Acknowledgement:
The authors wish to acknowledge the financial support provided by the UK Particle Physics and Astronomy Research Council, and the assistance of Maurice Glaser at CERN.

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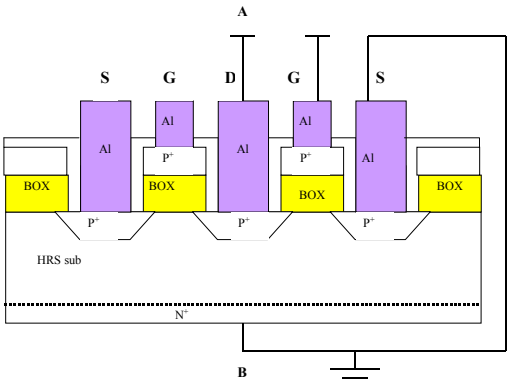

Fig. 1. Schematic cross section of the circular MOST.

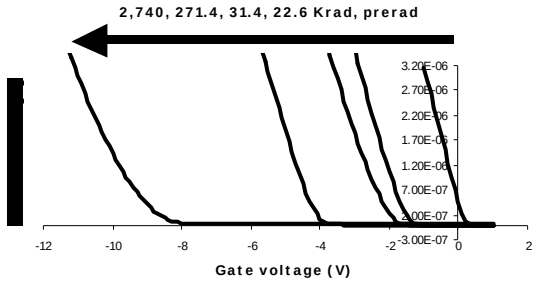

Fig. 2. Transfer characteristics of 100 µm gate length transistor before and after proton irradiation.

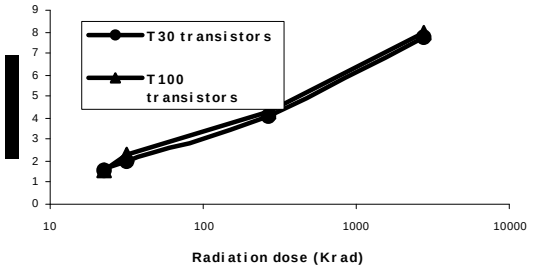

Fig. 3. Transistor threshold voltage shift as a function of proton irradiation dose.

Comparison Between Analog Performance of Standard and Strained Triple-Gate nFinFETs

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1. Abstract

This work shows a comparison between the analog performance of standard and strained Si (sSOI) n-type triple-gate FinFETs with high-κ dielectrics and TiN gate material. Different channel lengths and fin widths are studied. It is demonstrated that both standard and strained FinFETs with short channel length have similar analog properties whereas the increase of the channel length degrades the Early voltage of the strained devices, consequently decreasing the device intrinsic voltage gain.

2. Introduction and Device Fabrication

The FinFET is a promising device structure for the sub-100 nm CMOS era due to the excellent gate control of the channel charges allowing for excellent short-channel immunity.

The use of process-induced mechanical strain demonstrated improvements of the carrier mobility leading to higher current drive without penalties in off-state current. The use of biaxially strained material (or sSOI) is one of the possible techniques to obtain a strained silicon layer.

In this work we studied triple-gate nFinFETs fabricated on SOI wafers with 145 nm buried oxide thickness according to the process described in ref. [1]. The top silicon layer thickness (which is the fin height -H_{Fin}) is 60 nm and 55 nm for standard and sSOI FinFETs, respectively. After the silicon film definition a 1 nm thick interfacial thermal oxide is grown followed by the deposition of 2 nm HfO_2. A 5 nm thick TiN layer is then deposited and 100 nm thick polysilicon capping completes the gate stack. No channel doping or halo implantation is applied during the processing. Nickel silicidation is used in all device electrodes. Following the same process flow devices are fabricated on a sSOI wafer with 1.5 GPa intrinsic biaxial tensile strain.

3. Results and Discussion

The impact of strained material adoption on the performance of FinFETs is initially verified by looking at the maximum transconductance ($g_{m,max}$) in linear region (V_{DS}=50 mV) as a function of the fin width (W_{Fin}) for single fins ranging from 20 nm to 870 nm with channel length (L) of 10 µm. The percentage improvement on $g_{m,max}$ (and hence on the carrier mobility) decreases from about 75% for W_{Fin}=870 nm to 56% for W_{Fin}=20 nm. For the wider fin the conduction occurs mainly at the top in the (100) plane whereas for the narrow one the (110) plane in the sidewalls is dominating. This result indicates a dependence on the crystalline orientation with of the carrier mobility improvement provided by the strained material, as demonstrated in ref. [2]. As demonstrated in ref. [1] the reduction on W_{Fin} transforms the strain from biaxial to uniaxial, affecting the $g_{m,max}$ gain. Also the series resistance (R_S) is higher for the narrow sSOI FinFETs due to the smaller H_{Fin}.

The dependence on the channel length has been verified for multiple fin structures composed by 30 parallel fingers with W_{Fin}=20 nm at V_{DS}=0.1 V, as presented in fig. 1.

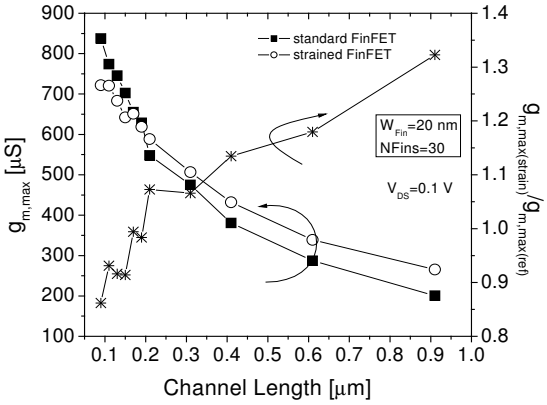

Fig. 1 – *Measured $g_{m,max}$ as a function of L at V_{DS}=0.1V for FinFETs with W_{Fin}=20 nm.*

It is clear from fig. 1 that the use of strained material only results in better transconductance (and hence mobility) for devices longer than 0.20 µm. This reduced $g_{m,max}$ enhancement at shorter L can attributed to the non-scalability of R_S [3]. The improvement on $g_{m,max}$ of strained FinFET increases with L up to 1.33 for 0.91 µm long transistors.

In order to compare the analog properties of both FinFETs the Early Voltage ($V_{EA} \approx I_{DS}/g_{DS}$, I_{DS} being the drain current and g_{DS} output conductance) has been

evaluated as a function of W_{Fin} for single fins of L=10µm biased at a gate voltage overdrive ($V_{GT}=V_{GS}-V_T$, V_{GS} is the gate voltage and V_T is the threshold voltage) of 0.2 V and V_{DS}=0.6 V, as presented in fig. 2. As for the $g_{m,max}$ the V_{EA} is also influenced by a W_{Fin} reduction. For W_{Fin} wider than 370 nm the V_{EA} is larger in strained FinFETs whereas for narrower fins the V_{EA} can become about 4 times smaller than for standard FinFET at W_{Fin}=20 nm. Using the extracted values for g_m and g_{DS} at V_{GT}=0.2 V and V_{DS}=0.6 V the voltage gain ($A_V=g_m/g_{DS}$) has been calculated and the results are also plotted in fig. 2. The W_{Fin} reduction causes a degradation on A_V if compared to the results for standard FinFET. On the other hand, wider strained FinFETs overcome the A_V of standard one.

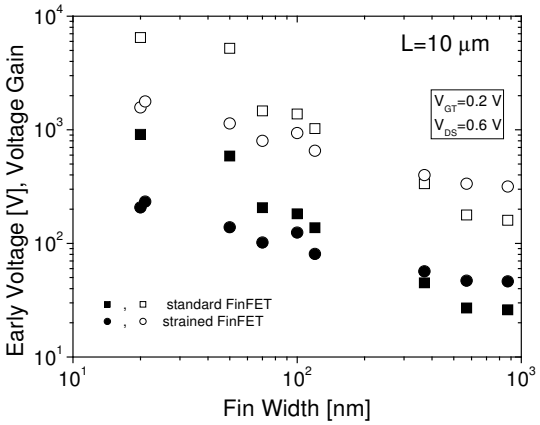

Fig. 2 – *Measured Early Voltage and Voltage Gain as a function of W_{Fin} at V_{GT}=0.2 V and V_{DS}=0.6 V. Closed symbols refer to V_{EA} and opened symbols to A_V.*

The variation of V_{EA} and A_V with L for multiple fins with W_{Fin}=20 nm is presented in fig. 3, also at V_{GT}=0.2 V and V_{DS}=0.6 V.

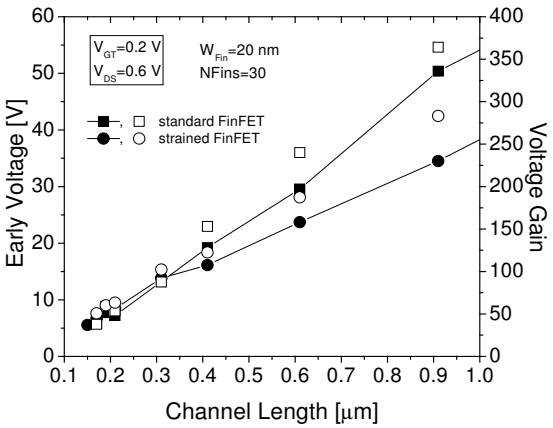

Fig. 3 – *Measured Early Voltage and Voltage Gain as a function of L at V_{GT}=0.2 V and V_{DS}=0.6 V for multiple fin structure with W_{Fin}=20 nm and 30 parallel fins. Closed symbols refer to V_{EA} and opened symbols to A_V.*

As the channel length increases, the effect of strain becomes more pronounced and starts degrading V_{EA} with respect to standard FinFETs. This effect is in agreement to what is presented in fig. 2, where long-channel narrow FinFETs presented reduced V_{EA} compared with standard ones, independently if single or multiple fingers are considered, undermining the influence of R_S as the multiple fingered structures have reduced R_S. For shorter L, as the effect of strain practically disappears, the V_{EA} becomes similar. Following the same tendency given by V_{EA}, the A_V is nearly the same for shorter devices. On the other hand, for longer devices the A_V of standard FinFET overcomes the results for strained ones by more than 30%. Notwithstanding the strained FinFET presents better g_m the degradation demonstrated in fig. 3 for V_{EA} results in an increase of g_{DS} that overcomes the benefits of g_m leading to worst A_V. On the other hand, for narrow FinFETs the effect of strain is favorable to both g_m and g_{DS}, resulting in larger A_V than in standard FinFETs.

Following ref. [4] the measured V_{EA} depends on the intrinsic device Early Voltage (V_A), the series resistance and the carrier mobility. On the other hand, the V_A depends mainly on Drain Induced Barrier Lowering (DIBL). In both types of structures under investigation, with single or multiple fingers, the R_S is nearly the same for standard and biaxially strained FinFETs. In order to evaluate the possible parameters affecting the differences of V_{EA} expressed in figs. 2 and 3 the inverse subthreshold slope (S) and DIBL parameters were extracted for L=0.21 µm and 0.91 µm. In both cases the S and DIBL are quite similar when changing from standard to strained devices. The S (extracted with V_{DS}=0.05 V) decreases from 64 mV/dec. to 62 mV/dec. and DIBL (V_{DS}=0.1 V and V_{DS}=0.6 V) decreases from about 10 mV/V to 3 mV/V when increasing L. The combination of these results ensures that no short-channel effects are taking place. This suggest the degradation of V_A for narrow FinFETs induced by the application of strain is the cause of V_{EA} degradation.

4. Conclusions

A comparison between the analog performance of FinFETs made in standard material and biaxially strained substrates has been reported. Independently of the W_{Fin} under study, the presence of strain in long-channel transistors is effective to improve the carrier mobility. On the other hand, the narrower strained FinFETs presented a degradation of the Early Voltage with respect to standard FinFETs. This degradation is only observed for longer devices, where the effect of biaxially strain is more effective. Although the transconductance improvement is larger for longer devices, the associated degradation of the ouput conductance (and hence Early Voltage) degrades the voltage gain. Shorter devices present similar Early Voltage and voltage gain as the effect of strain is nearly absent on these devices.

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How Crucial is Gate Misalignment for Low–Voltage Operation in Double Gate SOI MOSFETs?

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1. Abstract

In this work, we show the usefulness of gate–underlap architecture to significantly extend the tolerable limit of gate misalignment in Double Gate (DG) devices. DG MOSFETs with high degree of misalignment and optimal underlap design can perform comparably or even better than self–aligned non–underlap devices. These results are significant as the stringent process requirements for achieving self–alignment in planar DG devices can be considerably relaxed.

2. Introduction

DG MOSFET has received considerable attention in recent years due to the inherent suppression of short channel effects (SCEs), volume–inversion effect and excellent scalability [1-3]. DG devices fabricated with channel in the plane of the wafer (standard configuration) pose the difficult problem of aligning the top and bottom gates. The alignment of dual gates is crucial to high performance because gate misalignment results in an extra capacitance as well as a loss of electrostatic control [4-5]. In this work, we propose a design methodology to alleviate the critical issue of gate misalignment in low–voltage DG devices thereby significantly relaxing the process control requirements for achieving self–alignment.

Undoped DG devices (Fig. 1(a)) have been simulated using 2D simulator, ATLAS [6] with gate length (L_g) of 25 nm, gate oxide thickness (T_{ox}) = 1.3 nm and film thickness (T_{si}) = 10 nm. Gate bias (V_{gs}) was always maintained below threshold voltage (V_{th}) in order to analyze the impact of gate–misalignment for Ultra–Low–Voltage (ULV) applications. Analog/rf figures of merit (FOM) were extracted at current density (I_{ds}) of 10 µA/µm and drain bias (V_{ds}) of 0.2 V. Source/drain extension (SDE) region profile (Fig. 1(b)) was modeled as $N_{SD}(x) = (N_{SD}(x))_{peak}\exp(-x^2/\sigma^2)$, where $(N_{SD})_{peak}$ is the peak source/drain doping, σ the lateral straggle [7-8] was varied from 7.5 to 15 nm, d (= 5 nm/dec) is the source/drain doping gradient (evaluated at front gate edge) and s the spacer width lie in the range of 12 (= $0.5L_g$) to 60 (= $2.4L_g$) nm.

3. Results and Discussion

Figs. 2–3 show the dependence of cut–off frequency (f_T) and intrinsic voltage gain (A_{VO}), respectively, on m/L_g, along with the results of DG devices with non–underlap (abrupt) SDE regions. f_T was extracted as the frequency at which short circuit current gain (h_{21}) is 0 dB. An increase in gate misalignment (m) leads to a severe degradation in analog/rf FOMs in DG devices with abrupt SDE regions. Please note that the degradation in analog/rf FOM will be nearly symmetric with respect to ± m/L_g because FOMs were extracted at lower current density (= 10 µA/µm). Results for gate–underlap DG devices show that a high degree of gate misalignment can be tolerated without degrading performance. Analog/rf FOM remain constant up to m/L_g = 0.25 for σ in the range 7.5 to 15 nm. Underlap devices with $m/L_g \leq$ 0.5 perform better than self–aligned devices with abrupt SDE regions if $\sigma \geq$ 10 nm. DG devices with m/L_g = 0.75 perform significantly better at σ = 12.5 nm. The optimal range of straggle values needed to accommodate gate–misalignment without compromising the performance lie within the range 10–15 nm.

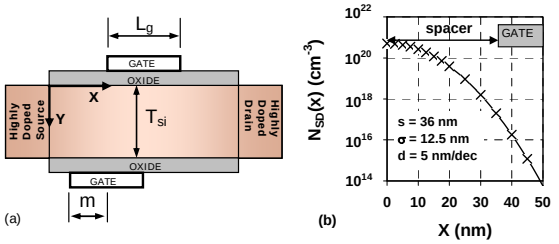

Fig. 1: *(a) Schematic diagram of a DG MOSFET with back gate misaligned by a factor m = -0.5L_g. Negative (positive) m/L_g values represent back gate misaligned towards the source (drain). (b) Variation of source doping profile along the channel for σ = 12.5 nm with d = 5 nm/dec. Please note that only half of the device structure has been shown in (b).*

As shown in fig. 4, underlap devices with m/L_g = 0.5 for $\sigma \geq$ 10 nm achieve higher peak transconductance–to–current ratio ($(g_m/I_{ds})_{peak}$) values than self–aligned non–underlap DG devices. Underlap architecture is particularly advantageous in the weak/low-moderate inversion regions, as the current flow is mainly due to diffusion of carriers and large straggle values (~ 12.5 nm) do not degrade the performance. In strong inversion region (~ g_m/I_{ds} = 5 V^{-1}), large σ values and wider spacers introduce additional parasitic resistance, which results in current ratio $((I_{ds})_{Underlap}/(I_{ds})_{Non-underlap}) < 1$ i.e. degradation of transconductance (g_m) at higher I_{ds}.

Fig. 5 shows the variation of total gate capacitance (C_{gg})

and Early voltage ($V_{EA} = I_{ds}/g_{ds}$, where g_{ds} is the output conductance) with σ. Underlap design results in the relative reduction of C_{gg} (at σ = 12.5 nm) by 25% at m/L_g = 0.5. An even more significant aspect of underlap design is the substantial improvement in V_{EA}. The improvement in V_{EA} is nearly 1.8 times at σ = 10 nm and 4 times at σ = 12.5 nm with m/L_g = 0.5. As shown in fig. 6, g_m initially increases up till σ = 10 nm and remains constant thereafter in DG devices with m/L_g = 0.5. An increase in σ at a given d results in longer effective channel length thereby suppressing SCE [8]. This reduction in SCEs translates into a higher g_m value due to better gate controllability. The improvement in g_m along with a reduction in C_{gg} translates into in higher f_T values even in misaligned gate–underlap DG devices.

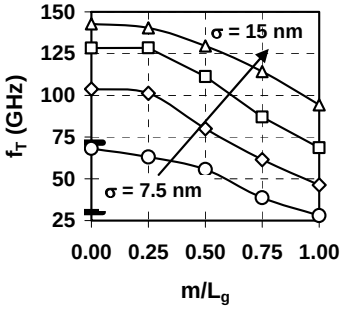

Fig.2: *Variation of cut-off frequency (f_T) extracted at I_{ds} = 10 μA/μm and V_{ds} = 0.2 V as a function of m/L_g ratios for various σ values. The horizontal line on the y–axis represents f_T values for the self/best (m/L_g = 0) and worst (m/L_g = 1) aligned DG devices with non–underlap (abrupt) SDE regions. $(f_T)_{Self-aligned,\ Non-underlap}$ = 71.6 GHz and $(f_T)_{Worst-aligned,\ Non-underlap}$ = 30 GHz. Notations: o—o σ = 7.5 nm, ◊—◊ σ = 10 nm, □—□ σ = 12.5 nm and Δ—Δ σ = 15 nm.*

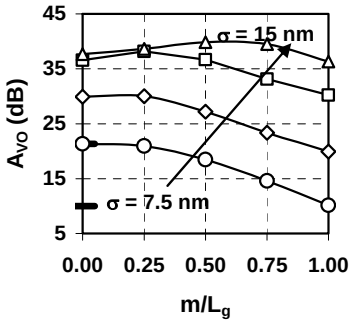

Fig.3: *Variation of intrinsic dc gain (A_{VO}) extracted at I_{ds} = 10 μA/μm and V_{ds} = 0.2 V as a function of m/L_g ratios for various σ values. The horizontal line on the y–axis represents A_{VO} values for the self/best (m/L_g = 0) and worst (m/L_g = 1) aligned DG devices with non–underlap (abrupt) SDE regions. $(A_{VO})_{Self-aligned,\ Non-underlap}$ = 21.4 dB and $(A_{VO})_{Worst-aligned,\ Non-underlap}$ = 10 dB. Notations are same as in fig. 2.*

5. Conclusions

Gate–underlap DG devices operated at low current levels are useful for ULV analog/rf applications as both gain and speed of devices can be significantly improved in misaligned structures. Underlap architecture is advantageous as it

(i) Relaxes the stringent process control requirements to achieve a perfect–alignment in a planar DG MOSFET,

(ii) Significantly extends the tolerable limit of gate misalignment at nanoscale regimes without compromising the performance.

Acknowledgement

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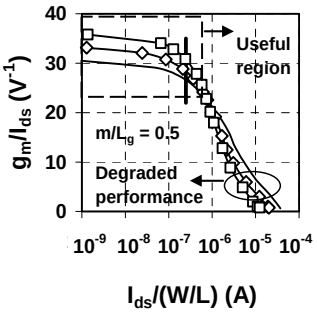

Fig.4: *Variation of g_m/I_{ds} ratio with normalized drain current ($I_{ds}/(W_g/L_g)$) extracted at I_{ds} = 10 μA/μm and V_{ds} = 0.2 V for m/L_g = 0.5 and d = 5 nm/dec. The vertical line at $I_{ds}/(W_g/L_g) = 2.5 \times 10^{-7}$ A represents I_{ds} = 10 μA/μm. The useful region for device operation is denoted in the figure by dashed rectangle. Notations: — Non–underlap (abrupt) SDE regions with m/L_g = 0, ◊—◊ σ = 10 nm and □—□ σ = 12.5 nm.*

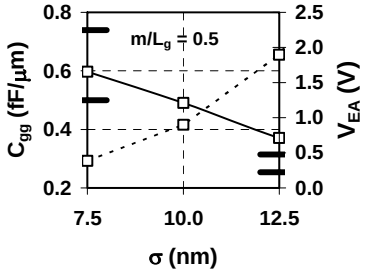

Fig.5: *Variation of C_{gg} and V_{EA} with σ for m/L_g = 0.5. The horizontal line on the y–axis represents C_{gg} and V_{EA} values for the self/best (m/L_g = 0) and worst (m/L_g = 1) aligned DG devices with abrupt SDE regions. Notations: — C_{gg}, - - V_{EA}, $(C_{gg})_{Self-aligned,\ Non-underlap}$ = 0.5 fF/μm, $(C_{gg})_{Worst-aligned,\ Non-underlap}$ = 0.74 fF/μm, $(V_{EA})_{Self-aligned,\ Non-underlap}$ = 0.5 V and $(V_{EA})_{Worst-aligned,\ Non-underlap}$ = 0.22 V.*

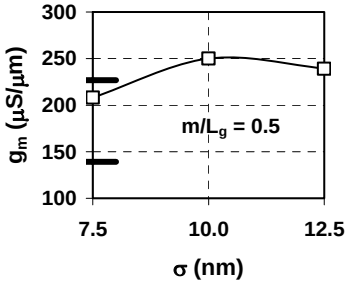

Fig.6: Variation of g_m with σ for m/L_g = 0.5. The horizontal line on the y–axis represents g_m values for the self/best (m/L_g = 0) and worst (m/L_g = 1) aligned DG devices with abrupt SDE regions. $(g_m)_{Self-aligned,\ Non-underlap}$ = 227 μS/μm and $(g_m)_{Worst-aligned,\ Non-underlap}$ = 139 μS/μm.

SESSION 8

SOI Device Physics and Characterization II

CHAIR
J. Alderman
Tyndall National Institute

Evidence for Substrate Bias Effects in SOI ΩFETs

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1. Abstract

It is generally accepted that, due to strong coupling of the lateral gates, narrow SOI Multiple-Gate FETs (MuGFETs) are immune to substrate effects [1]-[3]. Nevertheless, in this work we present experimental evidence for significant substrate bias effects in narrow SOI ΩFETs, consisting in the strong variation of the drive current, transconductance and gate-induced drain leakage current (GIDL), with invariant threshold voltage, subthreshold slope and DIBL. The origin and possible implications of the observed effects are discussed.

2. Introduction

The MuGFET is known as the most promising device architecture for nano-scaled CMOS technologies [1]–[3]. The multiple-gate structure and a thin (narrow-fin) Si body provide a strong electrostatic gate control of the potential in the body, suppressing short-channel effects [4],[5]. Next to that, the strong gate coupling of the lateral gates greatly reduces the back-gate influence in narrow-fin SOI MuGFETs [1]-[3]. It has been shown that, in Ω-gate FETs with very narrow fins, the threshold voltage, subthreshold slope and DIBL are virtually unaffected by back-gate or substrate bias [3]. The purpose of this work is a further investigation of the substrate effects in MuGFETs, using extensive measurements, with the emphasis on narrow ΩFETs. We experimentally demonstrate that, in *short-channel* narrow ΩFETs, substrate bias can dramatically change the on-current, transconductance and GIDL, which is attributed to modulation of the electric field and carrier distribution in the source/drain extensions and gate-to-extensions overlap regions. These effects should be taken into account in the predictions of the MuGFET's reliability and performance. They can be used for diagnostics of advanced MuGFETs.

2. Device Description

ΩFETs have been fabricated on SOI substrates. The fabrication process is described in [6],[7]. The gate stack consisted of a nitrided oxide with 1.8 nm EOT and MOCVD TiN, capped with 100nm poly-Si. High angle As implantation was used to dope the extensions and 45 nm PECVD nitride spacers were formed. No SEG was used to reduce the S/D resistance. After spacer etch, As+P HDD implantations were done, followed by a 1050^0C spike anneal and a standard NiSi process. The measured devices are undoped-channel 5-fin NMOSFETs. The fin height H_{fin} is 60 nm, and the buried oxide thickness is 145 nm. The fin width W_{fin} varies from 1 μm down to 25 nm. The gate lengths L_g from 10 μm down to 40 nm are considered.

4. Measurement Results and Discussion

The drain current I_d and transconductance g_m were measured as a function of the gate voltage V_g for various substrate biases V_{sub}. Measurements at low V_d for different gate lengths L_g are presented in Figs.1 and 2. For W_{fin}=25 nm a change in V_{sub} from –40 V to +40 V does not cause any change in subthreshold slope S and threshold voltage V_{th} (logarithmic-scale $I_d(V_g)$-curves in Fig.1(a-c), Fig.2 (a)), as expected for narrow-fin ΩFETs [3]. However, V_{sub} causes a change in the on-current I_{on}, which is evident from the linear-scale $I_d(V_g)$-curves in Fig.1(a-c). This change strongly depends on L_g. It is only faintly visible for L_g=10 μm, whereas it is rather pronounced for L_g=1 μm, and becomes very large for L_g=80 nm. In the 80-nm-long narrow-fin device, g_m also strongly varies with V_{sub} (Fig.1 (d)). This variation of g_m and I_{on} is reduced in the devices with larger W_{fin}, in which the back-gate induced V_{th}-shift is however more pronounced (Fig.2).

Similar features, namely, strong variation of I_{on} and g_m with V_{sub} without noticeable change of V_{th} and S are observed in narrow-fin 80-nm-long devices at high V_d (Fig.3). DIBL is also unaffected by V_{sub} for both W_{fin}=25 nm and W_{fin}=35 nm (insets in Fig. 3(c, d)). However, V_{sub} has a pronounced effect on GIDL, and this effect is much stronger for W_{fin}=35 nm than for W_{fin}=25 nm (Fig.3 (c, d)).

Insensitivity of S, V_{th} and DIBL to V_{sub} in our narrow-fin ΩFETs suggests that the observed V_{sub}-effects are not related to the variation of the potential in the channel region or at the channel edge. Indeed, as is evident from Fig. 4(a), in strong inversion the variation of the total resistance $\Delta R_{tot}(V_{sub})$ in the 80-nm- and 1-μm-long devices is exactly the same, indicating that the observed V_{sub}-effects are not related to the channel region, rather they are due to regions outside the

channel. Most probable reason seems to be modulation of the extensions series resistance R_s. Fig.4(b) shows R_s as a function of V_{sub} extracted using $I_d(V_g)$-measurements at low V_d on the long-L_g devices with different L_g (1-10 μm). One can see that R_s strongly changes with V_{sub}. For W_{fin}=25 nm, change in V_{sub} from –40 V to +40 V reduces R_s nearly by half. This is rather surprising, since our devices have heavily-doped extension regions (~10^{20} cm^{-3}) and a conventional gate-overlapped structure. It may be caused by incomplete activation of the dopants, dopant loss and increased extent of amorphization in narrow-width extension regions, resulting in a lower electrically active doping concentration in real devices [8]. The variation of GIDL with V_{sub} can be attributed to modulation of the electric field in the gate overlap region, and its suppression for reduced W_{fin} can be explained by an increased role of the internal gate fringing field.

4. Conclusions

We have presented experimental evidence for significant substrate bias effects in short-channel narrow ΩFETs. One is the drastic change of the on-current and transconductance attributed to modulation of the extension resistance. Another effect is the variation of GIDL attributable to a change of the electric field in the overlap region. This means that short-channel narrow ΩFET can be sensitive to parasitic substrate effects (hot-carrier, radiation effects, etc). Since the observed effects are rather sensitive to actual doping profiles in the extensions and overlap regions, they may be helpful in diagnostics of advanced MuGFETs, taking into account that it is very difficult to predict 3D dopant profiles in real MuGFETs. Furthermore, they should be considered in the predictions of the MuGFET's true performance potential determined by the drive current.

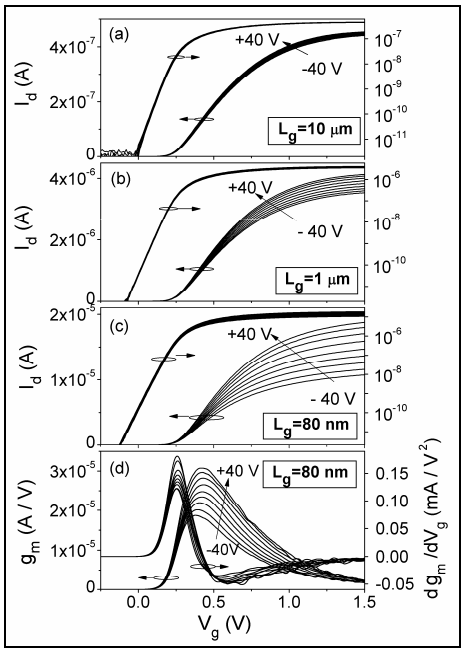

Fig.1: *Effect of V_{sub} on the transfer characteristics in linear and log scales in ΩFETs with W_{fin}=25 nm and different L_g: (a, b, c); (d) first and second derivatives of $I_d(V_g)$-curves for L_g=80 nm, showing variation of g_m and invariability of V_{th}.*

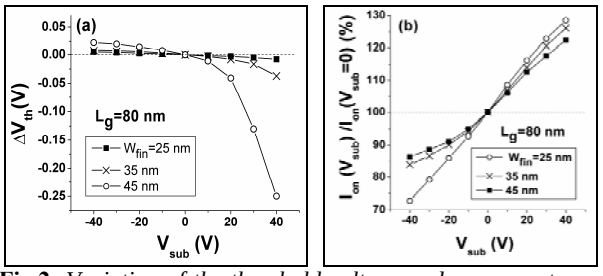

Fig.2: *Variation of the threshold voltage and on-current as a function of substrate bias (relative to those at V_{sub}=0) in the devices with L_g=80 nm and various fin widths (V_d=20 mV).*

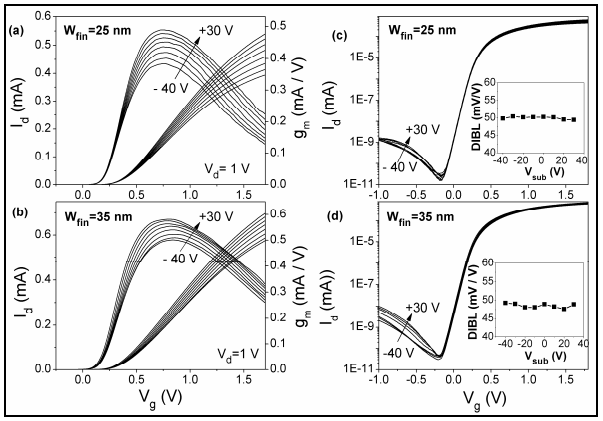

Fig.3: *Transconductance and transfer characteristics for 80-nm-long ΩFETs at V_d=1 V for various V_{sub}: (a. c) W_{fin}=25 nm, and (c, d) W_{fin}=35 nm. Insets in (c, d) show DIBL versus V_{sub}.*

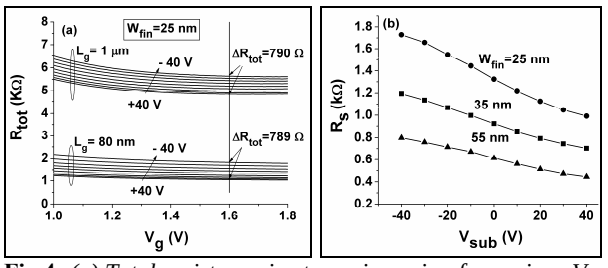

Fig.4: *(a) Total resistance in strong inversion for various V_{sub} in 80-nm-long and 1-μm-long devices with 25-nm-wide fins. (b) Series resistance as a function of substrate bias for various fin widths, extracted from long-L_g device measurements.*

Acknowledgements

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Study of STI power LDMOS transistors in a Thin-SOI technology

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1. Abstract

Many efforts on development of complex Smart Power circuits with smaller feature size technologies have been recently made. LDMOS transistors are typically used as switches in these circuits, their integration being based on the use of the LOCOS at the surface of the drift region to reduce the electric field peak at the LDMOS gate edge. Recently, STI (shallow trench isolation) has been contemplated as a solution for integrating high voltage LDMOS transistors although it is not sufficiently effective in reducing the surface electric field peak in the case of low voltage devices (20-30V) [1-2]. The benefits of applying the STI concept to higher voltage Thin-SOI LDMOS (in the range of 80V) is analysed in this paper.

2. Introduction

This paper is addressed to the study of 80V STILDMOS transistors in a Thin-SOI technology by means of 2D numerical simulations. Thin-SOI substrates have an active area of 2 µm in order to achieve a constant doping profile along the T_{SI} substrate. The BOX layer is 0.4 µm keeping in mind the thermal stability and the $R_{ON} \times C_{oss}$ factor which must be minimized in order to improve the frequency performance. Extensive 2D numerical simulation results allow to compare the electrical performance of the proposed STI LDMOS structure with that of a conventional LDMOS in terms of breakdown voltage, specific on-resistance, transconductance (g_m), and cut-off frequency (f_T).

3. Results

The simulated LDMOS and STILDMOS cross-sections (cell length of 9.5 µm) are shown in Fig.1. As it can be seen, the STI partially covers the drift region, and the subsequent high energy N-drift implantation gives rise to a VLD drift doping profile along the drift region. The resulting VLD doping profile is determined by the dose and energy of the N-drift implant, and by the STI length (L_{STI}) and depth (T_{STI}). The simulated R_{ON-sp} and V_{BR} values of the proposed STILDMOS in comparison with the LDMOS with L_{Poly} values of 1.5 and 2 µm are shown in Fig. 2. According to this figure the specific on-resistance is slightly higher in the proposed STI structure in comparison with LDMOS structures due to the lowest N-drift integration charge and the lowest accumulation region length. However, the R_{ON-sp}/V_{BR} trade-off of the proposed structure is remarkable higher.

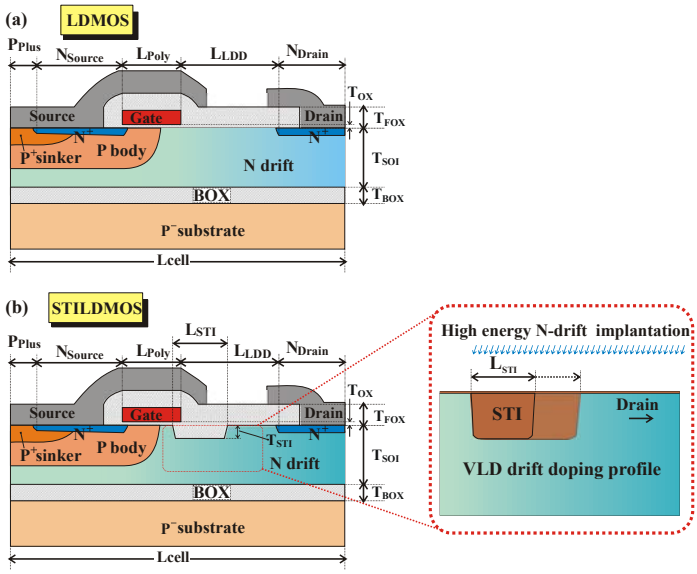

Fig.1: *LDMOS (a) and STILDMOS (b) cross-sections.*

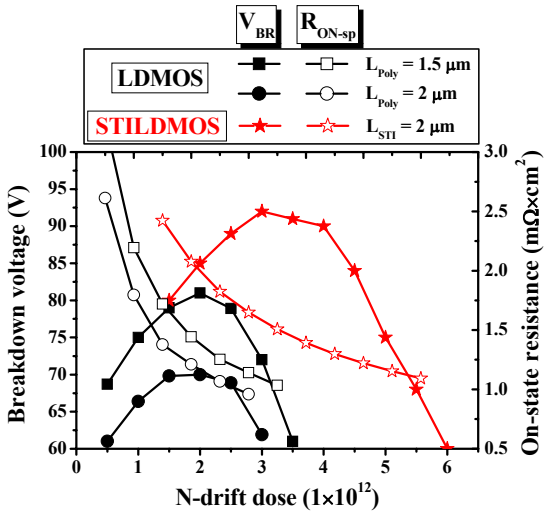

Fig.2: *Simulated V_{BR} and R_{ON-sp} versus N-drift implantation dose.*

In addition, the electric field contours at breakdown in the LDMOS and STILDMOS are indicated in Fig. 3. It can be seen that the STI and the VLD doping profile

allow for a reduction of the surface electric field peak at the gate edge, the electric field distribution being more uniform along the whole drift region instead the typical U-shape shown by the conventional LDMOS, as seen in Fig. 4. In addition, small-signal simulations have also been performed to analyse the frequency performance. Fig. 5 shows the g_m and f_T evolutions as a function of gate voltage in both structures with the best $R_{ON\text{-}sp}/V_{BR}$ trade-off obtained from Fig. 2 (N-drift dose of 2 and 4×10^{12} cm^{-2} for LDMOS and STILDMOS, respectively). Although the LDMOS structure shows a wider g_m plateau than its STI counterpart, the reduction of the accumulation region accounts for a higher f_T value in the proposed STILDMOS.

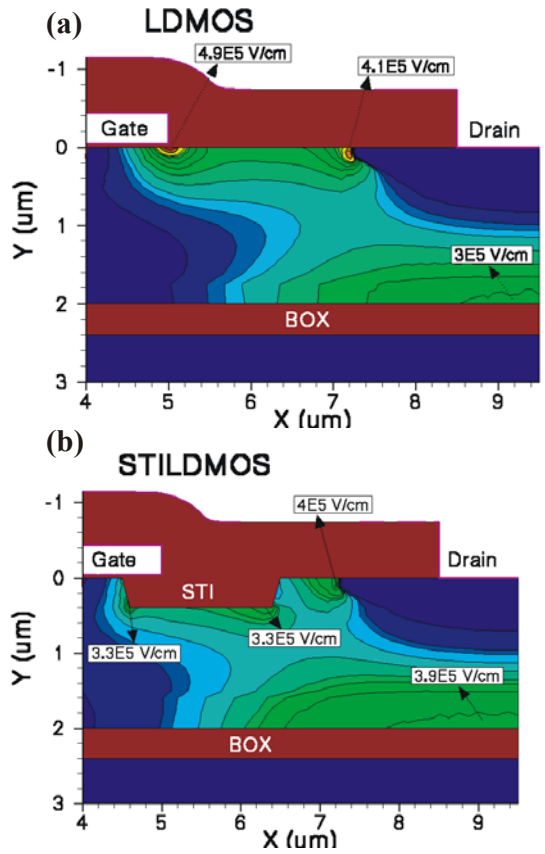

Fig.3: *Electric field contours in LDMOS and STILDMOS structures at V_{BR} of 70 V (N-drift dose of 2×10^{12} cm^{-2}) and 92 V (N-drift dose of 3×10^{12} cm^{-2}), respectively.*

4. Conclusions

An LDMOS structure with STI partially covering the drift region (STILDMOS) has been analysed and compared with a conventional RF LDMOS in a Thin-SOI technology. It has been shown that the $R_{ON\text{-}sp}/V_{BR}$ trade-off can be significantly increased in the proposed STILDMOS structure. Besides, the STI formation helps to reduce both the electric field and the accumulated charge at the body/drift surface region, thus improving the reliability and frequency response, respectively. Summarising, the proposed STILDMOS structure is a suitable power candidate in SOI Smart power and high frequency applications.

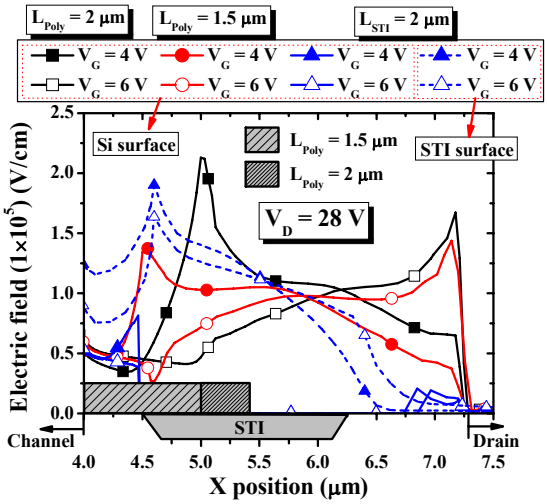

Fig.4: *Electric field distribution along the surface drift region at the LDMOS and STILDMOS structures for V_G = 4 and 6 V at V_D = 28 V.*

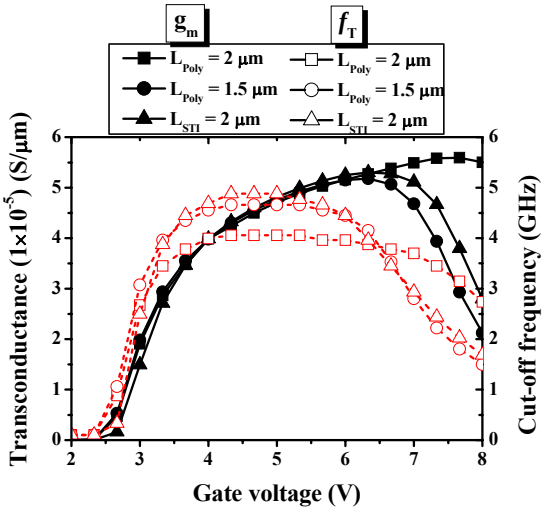

Fig.5: *Simulated transconductance and cut-off frequency versus gate voltage in LDMOS and STILDMOS for N-drift dose of 2×10^{12} and 4×10^{12} cm^{-2}, respectively.*

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Unusual Noise Behavior Versus Temperature in nFinFETs on Silicon on Insulator (SOI) Substrates Processed with Different Strain Techniques

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1. Abstract

The impact of strain techniques on the low frequency (LF) noise in nFinFETs on SOI substrates devices is reported. Five process conditions with different stressor methods are studied. A carrier number fluctuation dominant flicker noise has been observed for all devices studied. An unusual noise spectrum was observed specifically for the devices which received a Selective Epitaxial Growth (SEG) process. A detailed study of noise versus temperature (150K-300K) was performed on these devices.

2. Introduction

A great enhancement in performance of CMOS devices can be achieved by strain technologies without adding process complexity. In [1], two categories of strain techniques have been distinguished: biaxial global strain, whereby stress is introduced across the whole wafer; uniaxial local strain, based on the use of strained compressive or tensile contact etch stop layers (CESL) for pMOS and nMOS devices, respectively, or the use of SEG to integrate silicon germanium (SiGe) in the source and drain regions. Selective biaxial-uniaxial strain hybridization amplifies the enhancement in performance. The impact of hybridized strain technologies on the performance of FinFET transistors fabricated on SOI was reported in [2].

The LF noise behavior for conventional MOSFETs using strain techniques has been investigated in [3]. A factor two lower 1/f noise spectral density has been found for the strained silicon (sSi) substrate nMOSFET compared to the device with a standard substrate, if no diffusion of germanium (Ge) to Si-SiO_2 interface occurs. No clear change in the 1/f noise has been noticed for the studied uniaxial local strain techniques.

In this work, the impact on LF noise in submicrometer FinFETs on standard SOI (SOI) or strained SOI (sSOI) substrates is investigated. A comparison of the noise behavior at room temperature between different stress combinations is discussed. An unusual noise behavior is observed for the devices processed with a SEG technique. For these devices also a low temperature noise study is carried out.

3. Experimental

Devices studied are FinFETs with fin length 0.15µm, fin width 25nm, 5 fins parallel. For SOI substrate, the height is 65nm, and for sSOI substrate the height is 55nm. For the later, the biaxial tensile stress is 1.5GPa. The high-K gate stack consists in HfO_2/TiN/poly, which has a measured equivalent oxide thickness of 1.9 nm. The tensile CESL employed for some devices introduces a stress of 800-MPa. The SEG S/D regions were grown at 750C using an ASM Epsilon 2000 tool. The detailed device fabrication can be found in [2].

Five technologies have been studied. The FinFETs on SOI substrate and on sSOI substrate were used as references. Other studied FinFETs are SEG on SOI, SEG combined with CESL on SOI and CESL on sSOI.

The devices were operated in linear operation with drain-source voltage V_{DS}=50mV. On wafer LF noise measurements at room temperature have been performed using the BTA9812 preamplifier and noise analyzer combined with an HP35665A spectrum analyzer. The low temperature noise measurements were performed from room temperature down to 150K, using a 2 in "LAKESHORE TTP4" prober.

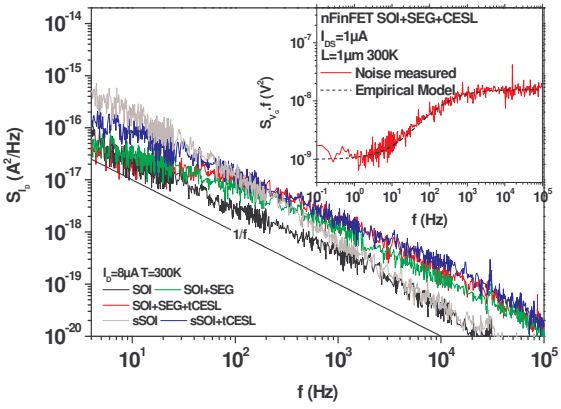

Fig.1: *Noise spectral density for the 5 technologies studied at room temperature (T=300K) with drain current I_D=8µA. The inset shows an unusual noise behaviour observed for all device processed with SEG technique.*

4. Result

A flicker noise has been found for all the devices studied (figure 1). Current noise spectral density at 25Hz normalised by the drain current and area versus drain current is presented in figure 2. The same trend of the parameter $(Gm/I_D)^2$, where Gm is the trans-conductance, indicates that the flicker noise is carrier number fluctuation dominant. In figure 2, no clear difference on noise magnitude has been found for all the devices studied except for the sSOI devices.

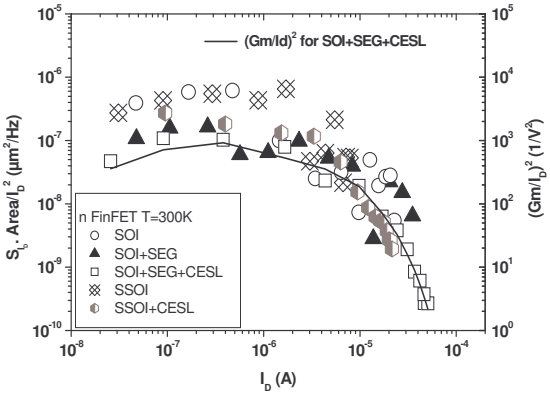

Fig.2: *Normalized drain current noise spectral density versus drain current at f=25Hz for the 5 technologies studied at room temperature.*

An unusual noise behaviour emerges specifically for these devices using SEG, as shown in the inset of figure 1. A study of LF noise versus temperature has been performed from room temperature down to 150K for SOI+SEG+CESL devices (figure 3).

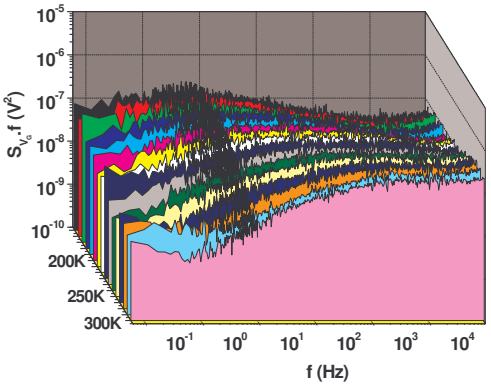

Fig.3: *Input-referred noise spectral density multiply by the frequency measured from 150K to 300K with a step of 10K for SOI+SEG+CESL device in linear operation and I_D=10µA for all temperature studied.*

The unusual noise behaviour was observed for all the temperatures studied. Several contributions could be extracted from the spectrum (inset of figure 4): two Lorentzian contributions and a spectrum behaviour which can be empirically modelled with two 1/f like noise components using the following equation.

$$Model = \frac{K_l}{f} + \frac{K_h}{f} \cdot \frac{1}{1+\frac{f_h}{f}} \cdot \frac{1}{1+\frac{f}{fb}}$$

where K_l is the level of the first 1/f noise component; K_h is the level of the second 1/f noise; f_h and f_b are the high and low cut-off frequencies.

Using the empirical model, we find that the two Lorentzian noise components have a characteristic frequency f_0 which changes with temperature. These Lorentzian noises may be due to the defects in silicon film. A method proposed in [4] allows identifying these defects by plotting in an Arrhenius diagram, the variation of $\ln\left[(T^2/2\cdot\pi\cdot f_0)\right]$ versus $1/(kT)$, where k is the Boltzmann constant. The difference of energy level between the conduction band energy and the trap energy E_T with $\Delta E=E_C-E_T$ and the capture cross section σ could be extracted. The first defect observed has ΔE=0.266 eV and $\sigma = 2.52\cdot10^{-21}$ cm^{-2}, while the second one has ΔE=0.362 eV and $\sigma = 3.98\cdot10^{-18}$ cm^{-2} (figure 4).

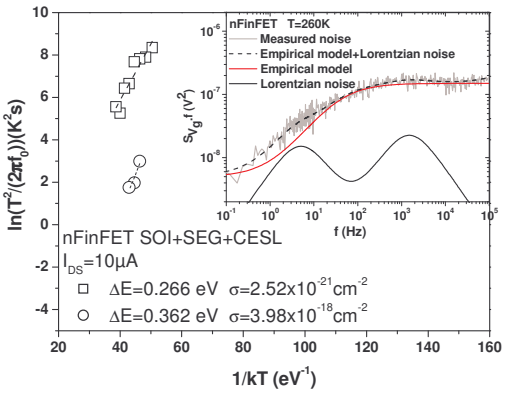

Fig.4: *The variation of the characteristic frequency f_0 of each Lorentzian versus temperature enables to deduce the ΔE and σ by plotting an Arrhenius diagram.*

5. Conclusions

No clear difference in flicker noise amplitude is observed for all devices studied. An unusual noise behaviour emerges for the devices using the SEG strain technique. A low temperature noise study on these devices shows that this unusual behaviour appears at all temperatures studied. An empirical model has been proposed with two 1/f noise components. Two additional Lorentzian behaviours have been observed may be attributed to the defects in the Si film.

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Co-existence of two-dimensional electron and hole gases in thin double-gate SOI FETs

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1. Abstract

The double-gate SOI FET structure enables field effect induced closely spaced electron-hole bi-layer. We report on fabrication of a batch of double-gate SOI devices where electron and hole layers have individual contacts. Room temperature transport characteristics of a device with SOI layer thickness of 22 nm show the co-existence of electrons and holes at high push-pull double-gate bias.

2. Introduction

Since the pioneering transport experiments of coupled electron-hole (EH) system by Sivan, Solomon, and Shtrikman [1], EH bi-layer transport has continued to be a topical subject. Recently, a closely spaced and purely field effect induced EH bi-layer was reported in a III-V double quantum well [2]. Such field effect induced EH system is also possible in a double-gate SOI FET as depicted in the energy band diagram of Fig. 1. Here we report on fabrication and transport measurements of a double-gate EH SOI FETs, which have individual contacts to the electron and hole layers. These devices enable interesting transport experiments and may also provide new device functions.

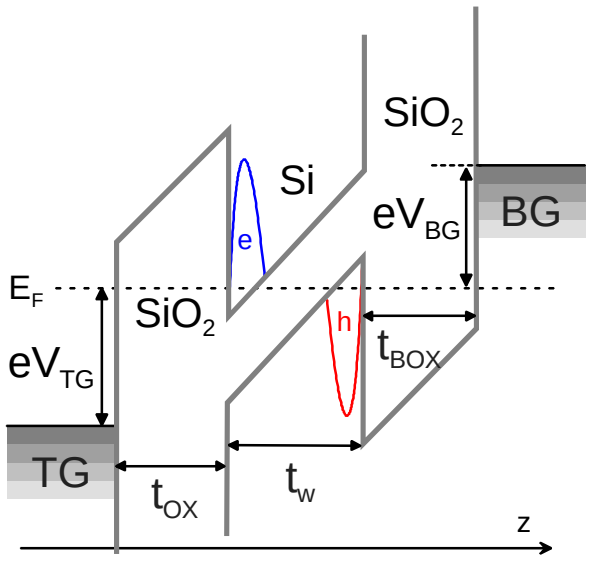

Fig.1: *Field effect induced electron-hole bi-layer in a double-gate SOI FET. High top gate (TG) voltage V_{TG} and back gate (BG) voltage V_{BG} with opposite polarity bend the conduction and valence bands and introduce the electron and hole gases in the Si channel layer. In the experiments the Si quantum well channel thickness t_W is 22 nm. E_F denotes the Fermi level.*

3. Experimental

The double-gate SOI FETs were fabricated on commercially available bonded SOI wafers by utilizing wafer bonding (which enabled the n+ back gate) and standard CMOS fabrication steps. The device fabrication followed closely the procedures reported in Refs. [3,4]. The only exception was that some of the devices had p+ and n+ contact regions in order to create independent contacts to the electrons and to the holes in the Si channel. The batch of the EH devices included various channel shapes and lateral dimensions from 400 nm to several 10 μm. Here we report on room temperature results measured from a four probe device depicted in Fig. 2. For this device the width-length ratio is W/L = 50 μm /200 μm and the Si channel thickness t_W = 22 nm. The top gate oxide thickness (t_{OX}) and buried oxide thickness (t_{BOX}) are 50 nm and 82 nm, respectively.

4. Results and discussion

The measurements were performed in the linear response regime, when the coupled EH system is described by a set of linear equations

$$\begin{pmatrix} I_e \\ I_h \end{pmatrix} = \mathbf{G}\begin{pmatrix} V_e \\ V_h \end{pmatrix}, \qquad \mathbf{G} = \frac{W}{L}\begin{pmatrix} G_{ee} & G_{eh} \\ G_{he} & G_{hh} \end{pmatrix} \qquad (1)$$

where I_i and V_i are the current and the voltage of the different layers ($i = e$ for electron layer and $i = h$ for hole layer) as depicted in Fig. 2 (a). The matrix **G** is the conductance matrix and its inversion gives the resistance matrix **R** whose off-diagonal elements define the drag resistance components R_{eh} and R_{he}.

Here we focus on the diagonal elements $G_{ee,hh}$, which can be associated with the effective mobilities $\mu_{e,h}$ according to $G_{ee,hh} = en_{e,h}\mu_{e,h}$ ($n_{e,h}$ being the carrier

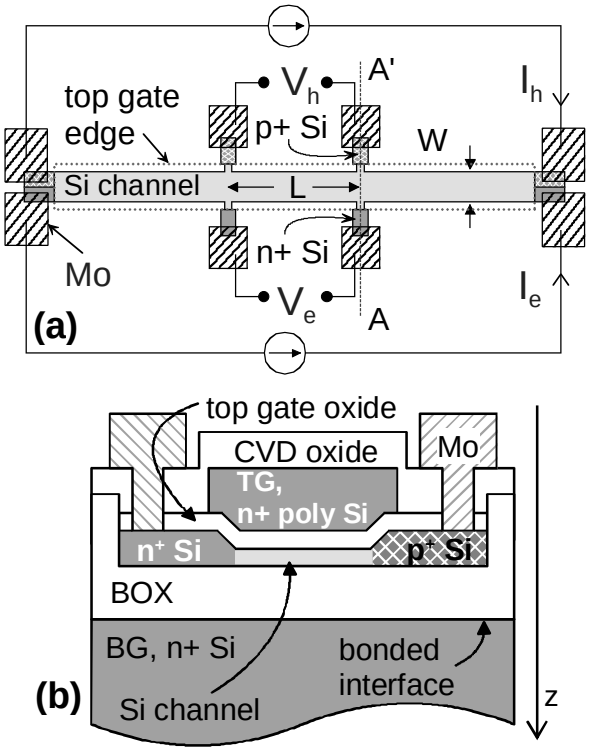

Fig.2: *(a) Shematic illustration of the lateral device geometry utilized in the experiments (W/L=50μm /200μm). The contact windows are excluded for the sake of clarity. All metallization related to the gate contacts is also excluded. The current contacts at the ends of the bar are greatly simplified: in actual devices they are a tightly spaced multi finger structures. (b) Cross-section along line AA'. The Si channel thickness is 22 nm and the heavily doped contacts are ~75 nm thick. The z-axis refers to Fig. 1.*

densities of the individual layers). Figure 3 shows the room temperature diagonal elements as a function of the top and back gate voltages measured from a device with t_w = 22 nm. The conductance of the electron and hole layers behave qualitatively similarly, but there is a big difference in the magnitude due to different mobilities. When the push-pull bias between the gates is not too large only either G_{ee} or G_{hh} differs from zero. In these double-gate bias regimes the $V_{TG,BG}$ dependency of the conductance contours can be identified to the gate bias symmetry dependency of the mobility reported in Ref. [3].

In the upper left corner and in the lower right corner in Fig. 3 both G_{ee} and G_{hh} are finite. Therefore, in these double-gate bias regimes the push-pull gate bias is sufficiently large to introduce electrons and holes to the opposite Si-SiO_2 interfaces in the spirit of the scheme depicted in Fig. 1. Note that in the upper left (lower right) corner G_{ee} (G_{hh}) depends only weakly on V_{TG} due to partial screening of the hole (electron) layer.

In addition of the room temperature characterization (Fig. 3) we have also performed EH drag experiments and detailed low temperature transport measurements including, e.g., Hall carrier density and mobility

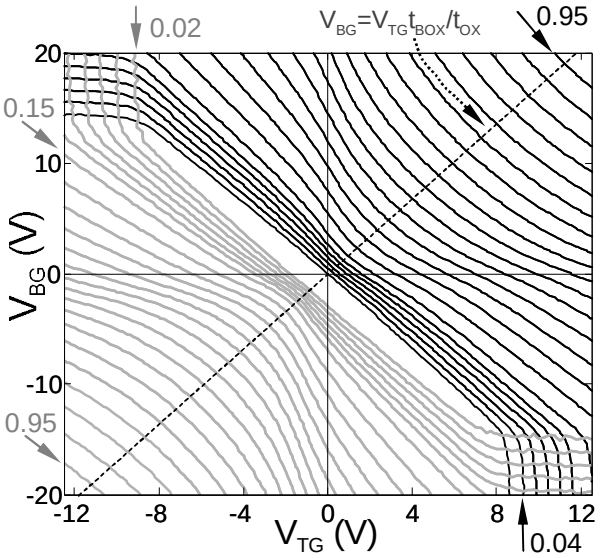

Fig.3: *Normalized constant conductance contours of electron (black) G_{ee} and hole (gray) G_{hh} layers of a double-gate SOI FET at T = 300 K. The data is measured from a large area device depicted in Fig. 2(a). The conductance is normalized in such a way that G_{ee} = 1 (G_{hh} = 1) at the upper right corner (lower left corner). The normalization factors are 5.83×10^{-4} 1/Ohm for electrons and 1.96×10^{-4} 1/Ohm for holes. The contour spacing is 0.02 and 0.05 for $G_{ee,hh} \leq 0.12$ and $G_{ee,hh} \geq 0.15$, respectively. Few values for $G_{hh,ee}$ contours are explicitly illustrated. The dashed diagonal line is the balanced gate bias line along which the effective potential inside the Si quantum well channel is symmetric.*

determination. The results of these experiments will be discussed in the possible full contribution.

5. Conclusions

The double-gate SOI FET structure enables field effect induced closely spaced electron-hole bi-layer (Fig. 1). These electron-hole devices can be fabricated by simply introducing n+ and p+ regions that make contact to the individual layers (Fig. 2). We have fabricated a batch of such devices. Room temperature transport characterization of a large area four probe device with SOI channel thickness of 22 nm was reported. The conductance components of the electron and hole layers were simultaneously finite at high push-pull double-gate bias (Fig. 3). This is a direct proof of the co-existence of electrons and holes in the device.

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Evaluation of Ni(SiGe) and Pt(SiGe) contact resistance for FD-SOI pMOS metallic source and drain

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1. Abstract

Specific contact resistivity between germano-silicides (PtSiGe or NiSiGe) and SiGe was studied through four probes like structures. Starting from condensation, Ge content was tuned between 15 and 30%. The presence of Ge degrades the contact resistance between the germano-silicide and pSiGe compare to PtSi on pSi.

2. Introduction

Because of gate length decrease, access resistance has to be optimized to remain lower than the channel resistance. ITRS specifications for 2010 plan a 125Ω-µm parasitic series source/drain resistance for ultra thin body fully depleted transistors. Thus replacement of the semi-conductor in source/drain by a metal may be attractive to reach this target. However a trade-off has to be found between contact resistivity of the metal and the semi-conductor and their contact area [1].

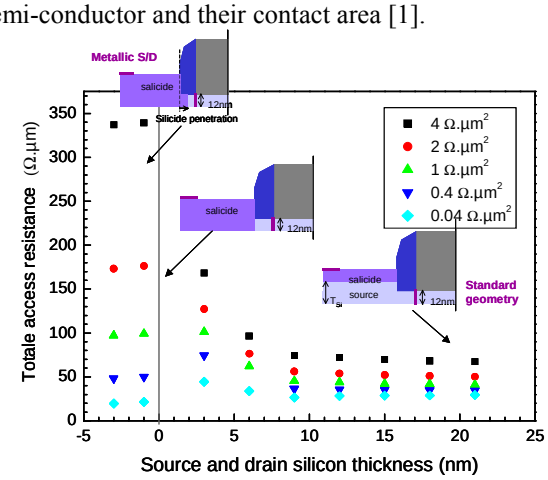

Fig.1: *Analytical simulation of access resistance as function of source and drain Si thickness*

We have performed analytical simulation to calculate the resistance between the contact and the channel (crowding resistance was not taken into account). As shown on Fig 1, a 0.04Ω.µm² contact resistivity is required for metallic source and drain to show an improved resistance compared to the standard geometry. For higher resistivities, access resistance keeps on increasing with silicide penetration as sheet resistance of the silicon layer is inversely proportional to its thickness. On the other hand, embedded SiGe source and drain are used as stressors [2]. Material investigation is thus required to understand and optimize metal/SiGe contact resistivity. Horizontal four probes structures were required in order to properly extract the contact resistivity. Indeed, usual Kelvin structures were not accurate since they do not consider lateral silicide formation and geometrical confinement of silicide, which could modify the growth properties (phase stability, kinetics, strain…).

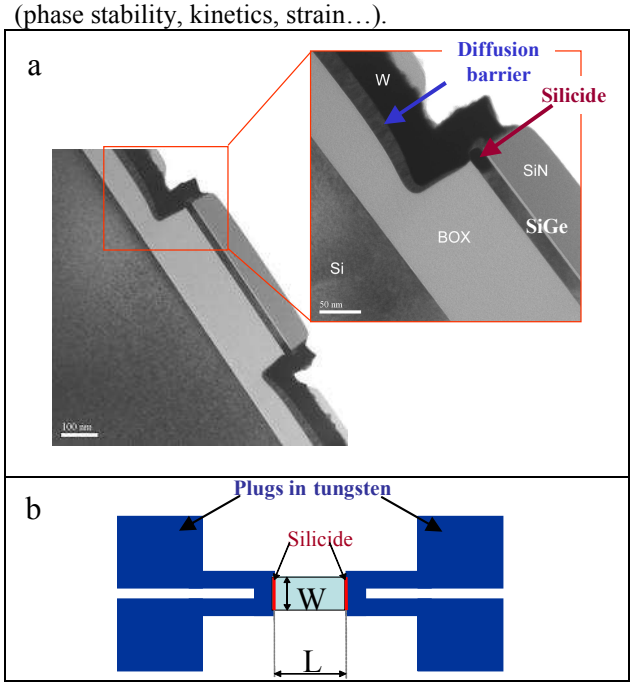

Fig.2: *TEM cross section and a plane view scheme of structures*

Therefore, new structures were designed (Fig. 2a) on which such parameters can be studied. On 200mm SOI wafer (100), active zones were patterned on Si 20nm and lateral Si accesses are thus made for silicidation. Moreover, current crowding effect [3] is avoided since electrical lines remain linear between both silicides. Consequently, the exact geometry is known allowing to extract the resistivity using variable length and width. Fig. 2b shows a plane view scheme of structures. From

electrical measurements, we plotted a linear variation of silicon resistance as function of its length. The resistance extrapolated at L=0 corresponds to M(SiGe)/SiGe contact resistance. In this work, we focus on Pt and Ni germano-silicide formed onto $Si_{1-x}Ge_x$ obtained by condensation and implanted with BF_2. Dopants have been homogenized in SiGe by a Rapid Thermal Annealing (RTA) at 950°C during 30s. An additional tilted implantation of BF_2 was performed in order to heavily dope SiGe surface before silicide formation. Lateral Ni (12nm) and Pt (16nm) salicidation was applied prior to diffusion barrier deposition and W plugs.

2. R_C of Pt($Si_{1-x}Ge_x$) vs Ni($Si_{1-x}Ge_x$)

Solid state reactions of a metal on $Si_{1-x}Ge_x$ occurred with the growth of different phases according to the annealing temperature. The lower resistivity phase is obviously targeted. We thus determined temperature windows for both Pt and Ni on $Si_{1-x}Ge_x$ (x=0.15 and 0.3). On Fig. 3, we report the sheet resistance (R_S) as function of 30s RTA annealing of Ni on SiGe 15% and Ni and Pt on SiGe 30%. Above 600-650°C Rs increases dramatically due to layer agglomeration and/or phase transition. Low resistive Ni($Si_{1-x}Ge_x$), characterized by XRD, is reached above 400°C whatever Ge contain and keep stable onto SiGe until 750°C. Nevertheless, for high Ge concentration, Ni($Si_{1-x}Ge_x$) R_S starts to increase after 500°C. This was explained by a Ge rejection from Ni($Si_{1-x}Ge_x$) which drives to decrease the agglomeration temperature [4]. Pt reactions show that high resistive compound is present until 500°C. The minimum resistance is achieved in 500-650°C range.

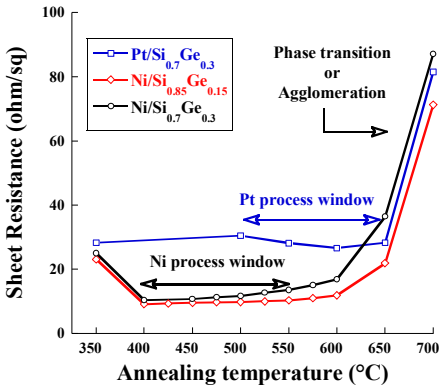

Fig.3: *Sheet resistance of 10nm of Pt and Ni on $Si_{1-x}Ge_x$ as function of RTA temperature.*

In the test structures Ni silicidation was realised by RTA of 30s at 450°C which avoids Ge segregation, while Pt process required a RTA of 60s at 550°C.
Firstly, our measurement method was tested on a reference interface Pt/pSi and we were able to extract contact resistivity in good agreement with published values which are ranging from 4 to 43Ω.µm² [5, 6, 7]. Then process optimization allowed us to further reduce PtSi/pSi Rc down to 0.5 Ω.µm² [8].

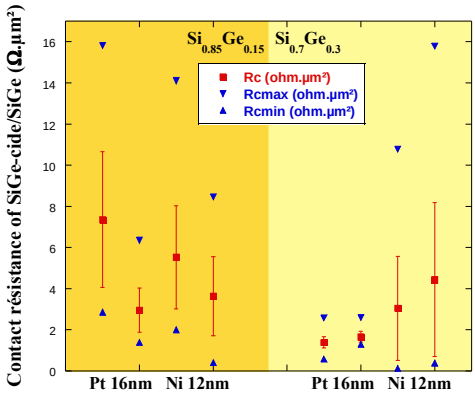

Fig.4: *Contact resistivity of Pt and Ni on SiGe 15 and 30%*

Lateral silicide forming metallic contact for source and drain was then demonstrated on SiGe with Pt and Ni (Fig. 4). Ni($Si_{1-x}Ge_x$) contact resistivity are very dispersive with an average around 4 Ω.µm² on both SiGe with 15 and 30%. Ge proportion does not seem to impact electrical properties of Ni-silicide/silicon interface. For Pt on SiGe, Rc around 1.5Ω.µm² has been achieved especially on SiGe 30% with a narrower dispersion. Although these Pt and Ni processes offer lower contact resistivity than literature, it remains too high from specifications set in fig. 1 but also higher than Pt on pSi. It seems that low schottky barrier of PtSi on pSi (Φ_B=0.25), a key parameters in contact resistivity, is degraded with the presence of Ge.

5. Conclusions

We have developed new structures allowing contact resistivity measurements between metallic source and drain and the channel. Those structures were successfully validated with PtSi on Si [8]. We showed here that Rc could be carried out from SiGe substrate up to 30% of Ge. Even if low Rc of Ni and Pt germano-silicide on SiGe have been measured, they are still too high to be competitive with PtSi on pSi (at least three times less resistive). To be attractive, interface engineering should be improved between metallic source and drain and the semi-conductor. One can think to additional heterogeneous implantation.

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