1. PUBLISHABLE SUMMARY

The main and last objective of EUROSOI Network is to establish Europe as the international scientific leader in Silicon on Insulator (SOI) Technology, Devices, Circuits and Systems. In this sense, the EUROSOI+ co-ordination efforts during this first reporting period have been focused on the starting of those activities which contribute to improving the role of the European Semiconductor Industry with regard to SOI and to the knowledge that will enable Europe to compete internationally.

Although EUROSOI achievements during FP6 have been many and very important for the European SOI technology, and the situation of SOI technology in Europe has greatly improved during the last three years, there are plenty of challenges at the near future. Even if we now are in the right direction, Europe is still far away from the pursued international leadership. After the elaboration of the State-of-the-Art report and EUROSOI Roadmap, we have identified the main actors, the strong points and weaknesses of Silicon-On-Insulator technology in Europe. All this information is collected in the EUROSOI Roadmap, where the challenges which will have to be faced in the future are also identified. Our first stage was a passive one (collecting and structuring the information). This second stage is being much more active; we are not only looking at around us, collecting and re-structuring the available information, but we have passed to the action in a more active role, developing the tasks, fostering creation of consortiums and leading the projects and proposals which give Europe and the European Semiconductor Industry the international leadership which they deserve as pioneers and big developers of SOI technology.

The best way to reach this goal is to try to spread the SOI technology all over Europe, making it accessible to any European semiconductor actor:

"We want that SOI technology is reachable to any European research group or Fabless Semiconductor company; we want that any circuit design has the chance to become a SOI circuit using European technology."

To do so, we have to work in three directions:

i) Training of researchers and engineers in the particularities of this technology, i.e., in the design of circuits taking advantage of SOI technology.

ii) Spreading and promotion of the benefits and advantages of SOI technology.

iii) Development of a platform which offers SOI technology for the actual fabrication of SOI circuits

It is widely accepted by the International Semiconductor Community that most of the electronic circuits (in the whole application spectra) will have a better performance, and therefore, they will be more competitive, if they are built using SOI technology. However, nowadays it is not easy to have access to this technology, even when we count in Europe with some of the most advanced SOI technologies all over the World.

Up to now, a lot of research activities have been pursued in Europe around SOI at different levels: substrate, device, and circuit. Since few years, advanced SOI technologies have been developed in research labs in order to address the downscaling required for 32nm nodes and below. Today such researches are mainly dedicated to technology development. Among the various ones, we can mention the LETI Fully Depleted SOI technology (developed with high-k and metal gate) that currently has enough maturity to

be evaluated at circuit level. So, it becomes obvious that a research-dedicated platform is necessary in order to address the circuit design aspects, focussing on the advantages of such technology for Low Power applications. Access to such platform is a long-time wish of European researchers. Hence, the main goal of EUROSOI+ is to coordinate the formation of such research-dedicated platform which will provide, through the integration in EUROPRACTICE, prototyping and Multi-Project-Wafers (MPW) in SOI open to all European companies using LETI SOI process in two-three years. We are co-ordinating all the activities which will make this platform a reality in 2010.

The following two points summarize EUROSOI+ activities during this period:

I. Training and promotional activities.

a. Website database (http://www.eurosoi.org)

i. **EUROSOI Virtual Journal**
http://www.eurosoi.org/articles.asp

ii. **EUROSOI Landmark publications**
http://www.eurosoi.org/landmark_publications.asp

iii. **EUROSOI Newsletters**
http://www.eurosoi.org/newsletters.asp

iv. **EUROSOI News&Announcements**
http://www.eurosoi.org/news.asp

v. **EUROSOI Training material database**
http://www.eurosoi.org/tutorials.asp

b. Organization of Training events and Tutorials

i. **Multigate SOI MOSFETs (January 23rd,2008, Cork, Ireland, 2008)**

1. **The SOI MOSFET: from Single Gate to Multigate** (Prof. Jean-Pierre Colinge, Tyndall)
2. **Physics of the Multigate MOS System** (Prof. Bogdan Majkusiak, Warsaw University of Technology)
3. **Mobility in Multigate MOSFETs** (Prof. Francisco Gamiz, University of Granada)
4. **Multigate MOSFET Technology** (Dr. Malgorzata Jurczak, IMEC)
5. **Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs** (Dr. Véronique Ferlet-Cavrois, CEA)
6. **Multigate MOSFET Circuit Design** (Dr. Gerhard Knoblinger, Infineon)

ii. **SOI from modelling to design (January 19th, 2009, Goteborg, Sweden)**

1. **Modelling of ultra thin body SOI nano-transistors** (*Prof. Luca Selmi*, University of Udine)
2. **Strained channel materials for SOI transistors** (*Prof.Siegfried Mantl*, Forschungszenter, Jülich, Aachen)
3. **SOI technology: an opportunity for RF designers**, *(Prof.Jean-Pierre Raskin*, Université Catholique de Louvain)
4. **From MEMS to embedded NEMS** *(Dr.Julien Arcamone*, CEA-LETI, Grenoble)
5. **Ultimately thin carbon on insulators : Graphene** (*Prof.Max Lemme,* Harvard University, Cambridge, Massachusetts)
6. **SOI Circuits: Do you want Partially Depleted or Fully Depleted Devices?** *(Prof.Jean-Pierre Colinge*, Tyndall National Institute, Cork)
7. **Digital SOI design in the nanometer era - from high-performance to ultra-low-power circuits** (*Prof.David Bol*, Université Catholique de Louvain)

c. Organization of Workshops.

i. **Fourth Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits** (Tyndall National Institute, Cork, Ireland, Jan 23-25th, 2008): http://www.tyndall.ie/eurosoi2008/
(56 communications, 80 attendants)

ii. **Fifth Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits** (Chalmers University of Technology, Goteborg, Sweden, Jan 19-21st, 2009): http://chalmers2009.eurosoi.org (60 communications, 90 attendants)

d. Discussion Panels. The opinion of SOI experts.

i. **"Key Issues in SOI: Solutions and Ideas",** chaired by Prof. Sorin Cristoloveanu, January 24th, 2008, Cork, Ireland

Participants:
Dr. Damien Bretegnier, SOITEC
Prof. Denis Flandre, UCL
Dr. Segei Okonin, Innovative Silicon
Dr.Olivier Faynot, CEA-LETI
Prof. Jean-Pierre Colinge, Tyndall

ii. **"What is the killing advantage of multiple-gate SOI MOSFETs: electrostatics and scalability, transport or functionality",** chaired by Prof. Sorin Cristoloveanu, January, 20th, 2009 Goteborg, Sweden

Participants:
Prof. Cor Claeys, IMEC
Prof. Jerry Fossum, University of Florida
Prof. Jean-Pierre Colinge, Tyndall
Dr.Olivier Faynot, CEA-LETI
Dr.Stephane Monfray, STMicroelectronics, Crolle
Prof.Francis Balestra, IMEP, SINANO Institute

e. Student and travel grants.

- 13 student grants for a total of 9390,24€ to attend EUROSOI workshops have been given to PhD students who works towards their PhD in European Universities in the field of SOI technology.
- 20 travel grants for a total of 13345,31€ have been also distributed among EUROSOI network partners to partially cover their registration and travel expenses to attend EUROSOI workshops.
- Other major conferences and promotional travels (21104€)

f. Scientific Exchanges

- 7 Exchange visits of EUROSOI members to other European Research Centers for a total of 19060,21€ have been funded by EUROSOI+ during this first reporting period.

g. Elaboration & Upgrading of Technical Focused Reports (TFRs).

i. **EUROSOI State of the art report:**
http://www.eurosoi.org/public/EUROSOI_State_of_the_art.pdf

ii. **EUROSOI roadmap.**
http://www.eurosoi./public/EUROSOI_Roadmap.pdf

iii. **EUROSOI who is who.**
http://www.eurosoi.org/public/EUROSOI_who_is_who.pdf

iv. **Benchmark of UTB vs. FinFET vs. DG SOI transistors. Which SOI device is favourite and for which application?**
http://www.eurosoi.org/public/D4.15.focused.report.utb_finfet_def.pdf

II. Development of EUROSOI fabrication & prototyping platform for the design of low-power SOI circuits.

a. Coordination of information exchange on LETI FDSOI technology. FDSOI wafers with functional devices have been provided to UCL, and IMEP. Also, electrical measurements have been provided to UGR. On November 17th-18th, Dr.Olivier Faynot from LETI organized in Grenoble a tutorial (free of charge for the EUROSOI members) focused on the training of European scientists on Fully Depleted SOI technology. Well recognized technologists, as well as international experts on devices and circuit design trained the attendees on SOI specific aspects, including: (1) Devices physics; (2) Technology description; (3) Modelling and circuit design; (4) Variability issues; (5) FDSOI platform development status. See the link: http://www.eurosoi.org/tutorialinfo.asp?id=7

b. Coordination of activities for the documentation, promotion and spreading of Research-dedicated Design Kit (RDK). The development of the research design kit is progressing in phase with what has been planned in the European project called DECISIF. This design kit contains a digital part that includes device model, Design Rules Control file and Layout Versus Schematic file. These files are essential to model and control the layout generated by the designers. This part is completed at 85%. The design kit contains also an analog part that includes Matching parameters, RF parasitics and related model (competed at 50%). The design kit finally contains an automated digital Design flow that includes Standard cell library and SRAM memory cuts. This last part is completed at 30%. With such level of achievement, the design kit can already be used to design some elementary circuits. It is scheduled to complete this design kit by mid-2009.

c. Promotion of the FDSOI technology.

Promotion of the FDSOI technology has been made by LETI during this period to the following companies:

- Presentation of the technology and results are regularly (every 3 months) made to SOITEC.
- Technology and electrical results have been also presented to ST Microelectronics in order to highlight the interest of such technology for Low Power applications.
- Promotion of FDSOI technology has also been done to AMD and ARM through a presentation at the SOI consortium meeting in November 2008. More detailed meetings will be planed for each company in 2009

d. Coordination of activities for the evaluation of the possible integration by the end of 2009 in the existing EUROPRACTICE structure.

We are now considered as one of the EUROPRACTICE projects (http://www.europractice.org/). We participated in the EUROPRACTICE Workshop held in Leuven on September 4th, 2008.