Project acronym:	R&D ACCESS
Project title	Access to research results on semiconductor design
	Project funded by the EC within the Seventh Framework
Project number:	ICT-2009-24663
Project duration:	01.10.2009 through 31.10.2012
Project partners:	Technoconsult ApS, DK (coordinator) Design And Reuse S.A., FR COREP, IT edacentrum GmbH, DE CEA-LETI, FR
Task:	**T1.3: Annual workshop on application specific nanoelectronics platforms**
Deliverable Number	**D1.3**
Deliverable Title	**Proceedings from annual workshop**
Nature:	Report
Dissemination level	Public
Delivery date:	30.07.2011
Covered period:	01.10.2009 – 30.07.2010
Authors:	Ivan Ring Nielsen (TC)
Lead beneficiary number:	1
Lead beneficiary:	Technoconsult
Contact:	Ivan Ring Nielsen Tel: +45 2212 5244 Fax: +45 4576 5708 email: irn@technoconsult.dk

Work Plan

Time	Deadline	Task	Partner	Deliverable / Results
		T1.3: **Annual workshop on application specific nanoelectronics platforms**	TC, COREP	
	15.02.2010	Meeting with potential speakers during DATE, Grenoble	TC	Draft contents and setup
		Arrange workshop venue at Minatec	CEA	
	05.03.2010	1st draft programme	TC, COREP, ECN	
	15.03.2010	2nd draft programme	TC, ECN	
	31.03.2010	Final programme	TC	Report rev. 1
	30.04.2010	Promotion material (flyer, programme, posters)	TC	
	31.05.2010	Workshop organization	CEA	Report rev. 2
	30.06.2010	Draft D1.3	TC	
	30.07.2010	Final D1.3	CEA, TC	Final Report

Table of Contents

1. Introduction

An annual workshop on application specific nanoelectronics platforms highlighting the future requirements with respect to Training, IP, Design Tools and Design Methodologies will be organised by TC and COREP in different places in Europe in order to stimulate the adaptation and introduction of new design flows supporting the advanced nanoelectronics processes.

In order to attract more participants to these workshops it will be sought organised as part of similar events like the European Workshop for Microelectronics Education (EWME), European Association for Education in Electrical and Information Engineering (EAEEIE) or Design, Automation & Test in Europe (DATE).

2. Workshop objectives

The workshop was organized as a half day event associated to other events going on in the Minatec conference center like “LETI Annual review”, “D43D Workshop” and “Workshop IR & Visible”. The intention was to piggyback from other related events. The objective of the workshop is to present and to discuss advances in semiconductor design knowledge with a focus on the provision of innovative knowledge originating from service providers and the R&D community.

The objective of the workshop is to present and to discuss advances in semiconductor design knowledge with a focus on the provision of innovative knowledge originating from service providers and the R&D community.

The workshop included presentations by innovative CAE vendors, design service providers and providers of semiconductor and IP. A presentation was devoted to the most recent research work on multicore platforms. The workshop was concluded with a presentation of the ambitious Nano-Tera programme, a Swiss 120 million CHF federal program on complex systems for health, security and the environment.

The workshop was attended by 24 participants (see list of participants in Section 6).

3. Overview of presentations

A design methodology is the process and the set of techniques of using specific tools and IP to design, validate and test systems. However, design methodologies are generally strongly related to the environment where they are defined or used (applicative domain, target implementation, special characteristics, etc.).

This document has several objectives. Firstly, it analyses the state-of-the-art and establishes the industrial requirements of design methodologies for the most relevant domains of semiconductor design. This analysis may help the R&D ACCESS partners to search within FP7, FP6, ENIAC and other programmes the relevant results concerning new methodologies. It should help us as first guidance for the active result search.

The second objective of this document is to start a discussion concerning the impact of new methodologies on two classes of industrial users, namely Large Enterprises (LE) and Small & Medium Enterprises (SME). This short discussion should be useful to complement the searching guidance accentuating the opportunities and issues in each case.

The third objective constitutes the proposal of a structure to organize the relevant results on design methodologies in the R&D ACCESS database. This organization structure is driven by the precedent discussions.

By knowledge requirements, we mean the set of best practices, tools, architecture templates, process flow or any other guidance required to design, validate and test systems in a way that is applicable with regards to the enterprise's means and industrial objectives.

The slides presented during the workshop are amended in Appendix in Section 6.

3.1. Introduction to innovation services available from R&D ACCESS

This presentation highlighted the problems that R&D ACCESS aims to solve, i.e. R&D Results are scattered among several 100s of EU projects, most projects have a life time of 3 years, after completion project websites tend to dry out and several project results are IPR protected. The solution proposed by R&D ACCESS is to make use of existing knowledge platforms like EDA Tools, EuroTraining, Design & Reuse.

The objective of the R&D ACCESS project is to identify R&D results on semiconductor design from FP7 projects and to provide these results to partners from outside the consortia.

The R&D ACCESS project provides a dissemination platform facilitating the access to project results generated in huge numbers of IP, NoE, STREP and CSA projects.

The key advantage of the R&D ACCESS consortium is that the partners are already leading their respective area of dissemination. This means that the dissemination platform is build on existing infrastructures that have proven their commercial as well as academic vitality. Combining these four platforms under a common ACCESS infrastructure with state-of-the-art web features like the use of taxonomy provide a unique results dissemination forum for FP7 project results.
As a result of this integrating approach the initial service include information on more than 500 annual nanoelectronics training courses, 15.000 updated IP/SoC products and information on more than 140 design tools developed within European projects.

Another benefit from joining existing knowledge providers is the access to a common user database of nearly 40.000 subscribers.

3.2. European EDA startups & innovation: a (non exhaustive) survey

Matthias Silvant from EDXAX`CT presented an overview of European EDA startups, taken from the perspective of an informal group of company managers. This group is meant to facilitate sharing of non competitive data and experience in a very informal way to make European innovation more visible. The EDA startups included in the survey are:

- ACML
- Edxact SA

- ASYGN
- CoFluent Design
- Concept Engineering GmbH
- CoSynth
- CWS
- DeFacTo
- Design & Reuse
- Docea Power
- Edacentrum
- HeedSoft
- Infiniscale
- Magillem Design Services
- ProximusDA
- Satin Technologies
- Teklatech
- TIEMPO
- XYALIS

The startups identified in this survey will be invited to join R&D ACCESS.

3.3. New design and verification methodologies

Ronan Lucas from Magillem Design Services gave a presentation on new design and verification methodologies. Magillem has developed an easy to use, state of the art platform solution to cover electronic systems design flow challenges in a context where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SOC. Based on a unique Xml standard format (IEEE1685), Magillem's solutions offer a complete cartography of a system (hardware and software) independent from tools and languages.

Magillem has a strong and long experience working with large corporations in electronics and industrial systems First-tier customers in electronics and industrial systems including among others Texas Instruments, Fujitsu, Bosch, Qualcomm, ST microelectronics, NXP, STEricsson, Thomson, Sonics, European Space Agency, Thales, Alstom, Astrium, EADS Airbus.

Magillem runs a joint lab with CEA in Grenoble on documentation/traceability/embedded software. The work on new design methodologies will be included in R&D ACCESS' platform on methodologies.

3.4. Which IP is needed by the semiconductor community?

Gabriele Saucier from Design & Reuse gave a presentation on which IP is needed by the semiconductor community. Design & Reuse is providing the IP input for the R&D ACCESS platform by means of added-value information in the field of electronic virtual component, i.e. IP (intellectual property) and SoC (system-on-chip).

D&R is the worldwide leader as a web and a B2B portal in the IP/SoC field. By IP should be understood Silicon IP as well as software IPs such as embedded software. This position has been reinforced over the years with its 150.000 page views per month, 15.000 daily updated IP/SOC products descriptions and the ongoing client/provider matching activity, D&R web stays worldwide unique. 150 companies have signed up a partnership agreement with D&R for providing their latest information to the market through D&R channel and taking the best benefit from its lead service and B2B matching opportunities.

The presentation focused on new services related to embedded software and the market consolidation for the key players, e.g. Synopsys, Cadence, Mentor Graphics, Xilinx, Altera and Lattice.

R&D ACCESS will consider including the embedded software IP online service.

3.5. Smart Multicore Embedded systems – Tool chains for multicore platforms in advanced technologies

As an example of a potential R&D ACCESS user, Francois Pacull from CEA-LETI gave a presentation of the ARTEMIS SMECY project addressing Tool chains for multicore platforms in advanced technologies.

The objective of the project is to provide compilation tool chains for a selected numbers of platforms and demonstrate the capability in a number of industry cases. The project approach is based on a common architecture, APIs, and design tool platform supporting several application domains.

The design tools and associated runtime support should be able to handle composability, predictability, parallelization and aggregation. Furthermore it must be able to consider performance and/or energy modeling.

The project's relevance to the overall ARTEMIS target is to reduce the design cost in embedded system field, to shorten development cycles, to increase manageable complexity (application & system) and to reduce effort and time (creation & re-validation and re-certification)

Three application domains are considered in the project: Radar signal processing and earth observation, Multimedia, mobile and wireless transmission and Stream processing (video surveillance).

The expected results to be considered by R&D ACCESS include Compilations chains, Know how for new compilation chains, Speed up for critical parts of the targeted applications and Requirements for future platforms.

3.6. The Swiss Nano-Tera programme

The Nano-Tera initiative aims at bringing Switzerland to the forefront of a new technological revolution driving engineering and information technology for health and security of humans and the environment in the 21st century.

Nano-Tera is a Swiss federal program funding 19 four-year research projects, 15 focused projects and 19 projects of education and dissemination. The total consolidated budget is over CHF 120 million, of which 50% is funded by Nano-Tera and 50% participants' own contributions.

The Nano-Tera initiative aims to bring Switzerland to the forefront of a new technological revolution, using engineering and information technology to improve the health and security of humans and the environment in the 21st century. The first call for proposals in 2008 brought 54 candidacies, from 24 academic and 25 industrial institutions. This unprecedented effort of the confederation has the ambitious goal to foster the reindustrialization of Switzerland and to lead the country to the highest position in complex large distributions systems and nanotechnology.

The goals are, for example, to detect in real time different health risks and conditions through body-integrated bio probing, to reveal security risks through smart buildings and environments, to save energy through ambient sensing, and to detect and monitor environmental hazards such as floods and avalanches from inaccessible positions on earth. The keyword is integration of various nano-scale technologies in tera-scale (complex) systems. Nano-Tera's challenge is to steer the convergence of people and teams from very different technological and cultural domains. Fostering research and crossbreeding of hardware and software technologies in the areas of implantable, wearable & ambient systems

R&D ACCESS is especially keen to gather new training courses arising from the 19 projects of education and dissemination. However, also IP, tools and methodologies might be able to benefit from the Nano-Tera results

4. Conclusions

The first R&D ACCESS workshop was successfully organized on 30 June, 2011 in Grenoble. The presentations provided the project partners with fruit for sought in the organization and set-up of the R&D ACCESS services. The direct and immediate input includes:

- The startups identified by EDXACT and Satin Technologies to be invited to join R&D ACCESS
- Magillem's work on new design methodologies to be included in R&D ACCESS' platform
- Inclusion of IP embedded software to be considered by R&D ACCESS
- Inclusion of smart multicore platforms in the design methodologies section
- Gather new training courses arising from the Swiss Nano-Tera programme

A second workshop will be organized during 2012.

5. Workshop programme

access www.rd-access.eu	Workshop **ACCESS to innovation in semiconductor design** 30 June 2011, Grenoble, France	COOPERATION

13.00	**Introduction to innovation services available from R&D ACCESS** Ivan Ring Nielsen, Technoconsult, DK
13.30	**European EDA startups & innovation: a (non exhaustive) survey** Matthias Silvant, EDXACT and Michel Tabusse, Satin Technologies, FR
14.00	**New design and verification methodologies** Ronan Lucas, Magillem Design Services SA, FR
14.30	**Which IP is needed by the semiconductor community?** Gabriele Saucier, Design & Reuse SA, FR
15.00	**Coffee break**
15.30	**Smart Multicore Embedded Systems** **- Tool chains for multicore platforms in advanced technologies** François Pacull, CEA-LETI, FR
16.00	**The Swiss Nano-Tera programme** Patrick Mayor, Nano-Tera, CH
16.30	**End**

Venue:

The workshop will take place at MINATEC, 3 parvis Louis Néel, FR-38000 Grenoble

Registration:

http://cea.insight-outside.fr/access/

Partners:

Technoconsult ApS, DK, Ivan Ring Nielsen
Design And Reuse S.A., FR, Gabriele Saucier
Consorzio per la Ricerca e l'Educazione Permanente, IT, Danilo Demarchi
edacentrum GmbH, DE, Andreas Vörg
Commissariat à l'énergie atomique, FR, Diego Puschini

Contact:

info@rd-access.eu

The workshop is organized by the FP7 R&D ACCESS project

6. List of participants

Fredric Rousseau	TIMA - UJF	France
Alexis Blanchemain	Design and Reuse	France
Danilo Demarchi	Politecnico di Torino	Italy
Paolo Motto	Politecnico di Torino	Italy
Romain Verly	CMP	France
Arthur Freitas	Grenoble Graduate School of Business	France
Philippe Metsu	proximusda gmbh	France
Eric Mercier	CEA-Leti	France
Christian Fabre	CEA LETI/DACLE/LIALP	France
Arun Rajendiran	Design & Reuse	France
Balram Naik Meghavath	Synapse-Design Automation	France
Arnaud Dehamel	STEricsson	France
François Pacull	CEA-Leti	France
Puschini Diego	CEA-Leti	France
Andreas Vörg	edacentrum GmbH	Germany
Haykel Ben Jamaa	CEA - Leti	France
Gilles Simon	CEA-LETI	France
Santhosh Onkaraiah	CEA	France
Ivan Ring Nielsen	Technoconsult	Denmark
Matthias Silvant	EDXACT	France
Michel Tabusse	Satin Technologies	France
Ronan Lucas	Magillem Design Services SA	France
Gabriele Saucier	Design & Reuse SA	France
Patrick Mayor	Nano-Tera	Switzerland

7. Appendix with presentation slides

WORKSHOP
ACCESS to innovation in semiconductor design

Access to Research Results on Semiconductor Design

13.00	**Introduction to innovation services available from R&D ACCESS** Ivan Ring Nielsen, Technoconsult, DK
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15.30	**Coffee break**
16.00	**The Swiss Nano-Tera programme** Patrick Mayor, Nano-Tera, CH
16.30	**End**

R&D project results

Access to Research Results on Semiconductor Design

Problems:

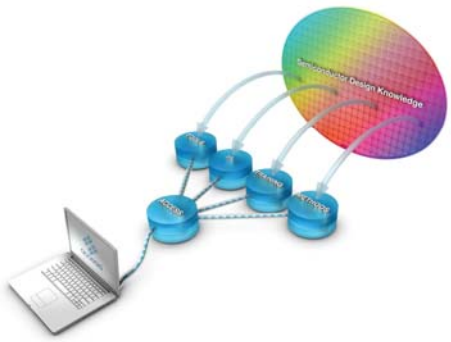
- Result are scattered among several 100s of EU projects
- Most projects have a life time of 3 years
- After completion project websites tend to dry out
- Several project results are IPR protected

Solution:

- Make use of existing knowledge platforms

Access to semiconductor design knowledge

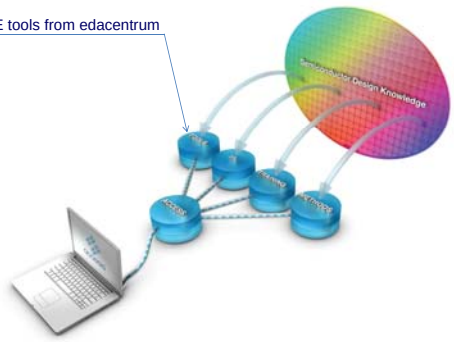
Access to Research Results on Semiconductor Design



Access to semiconductor design knowledge

Access to Research Results on Semiconductor Design

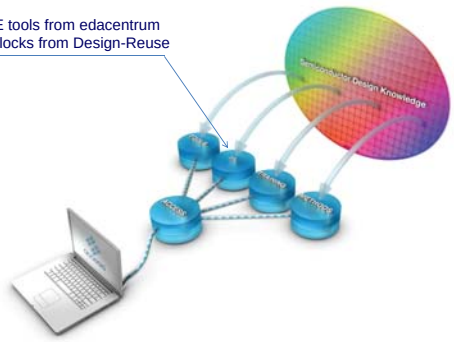
CAE tools from edacentrum



Access to semiconductor design knowledge

Access to Research Results on Semiconductor Design

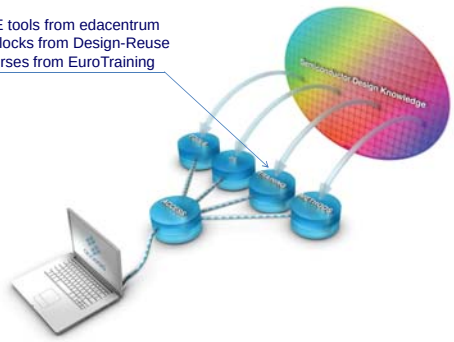
CAE tools from edacentrum
IP blocks from Design-Reuse



Access to semiconductor design knowledge

Access to Research Results on Semiconductor Design

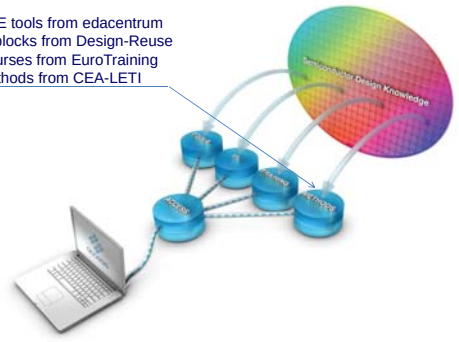
CAE tools from edacentrum
IP blocks from Design-Reuse
Courses from EuroTraining



Access to semiconductor design knowledge

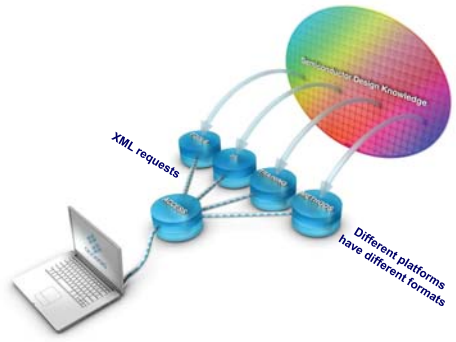
Access to Research Results on Semiconductor Design

CAE tools from edacentrum
IP blocks from Design-Reuse
Courses from EuroTraining
Methods from CEA-LETI



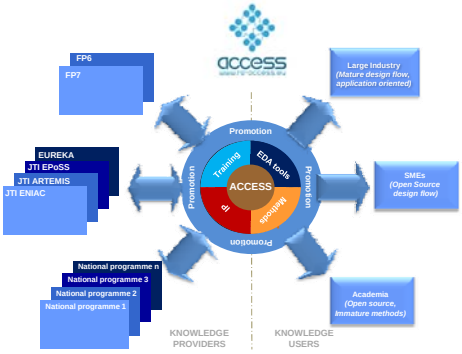
Access to semiconductor design knowledge

Access to Research Results on Semiconductor Design



Integrated knowledge platform

Access to Research Results on Semiconductor Design



Integrated knowledge platform

Access to Research Results on Semiconductor Design

Training:
- More than 400 training courses/year
- Provided by 72 professional training providers
- More than 200.000 monthy hits
- Nearly 12.000 European training subscribers.

EDA tools:
- More than 70 EDA members
- Information on 450 different EDA projects
- Nearly 12.500 EDA experts
- Over 6.800 EDA publications

IP:
- Intellectual Properties public web portal
- 15.000 updated IP/SoC product descriptions
- 150 companies with partnership agreement
- Weekly IP/SoC News reaches 25.000 subscribers

Methods:
- Covering SoC, MPSoC, NoC, SiP and FPGA
- Identification of new design methodologies
- Benchmarking of design methodologies
- Classification of advanced/mature methods

Training provider

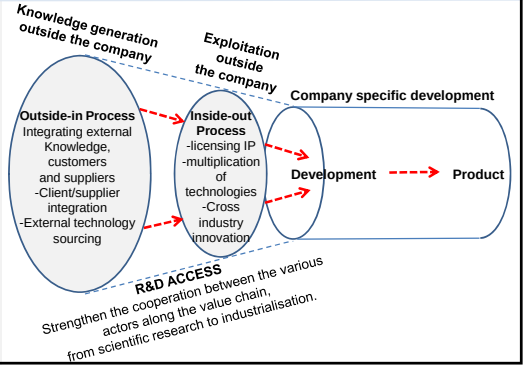
Quality Labelling:
- Validation check
- QL service
- e-bay style evaluation of material

Promotion:
- Monthly news
- Mailing list 12.000
- Promotional material

European Training Infrastructure:
- Web service
- 500 courses/year
- Maximizes the visibility
- Training roadmaps

Innovation models

Access to Research Results on Semiconductor Design



Benefits

Access to Research Results on Semiconductor Design

Technoconsult
Design & Reuse
COREP
Edacentrum
CEA-LETI

What are the benefits for the provider?

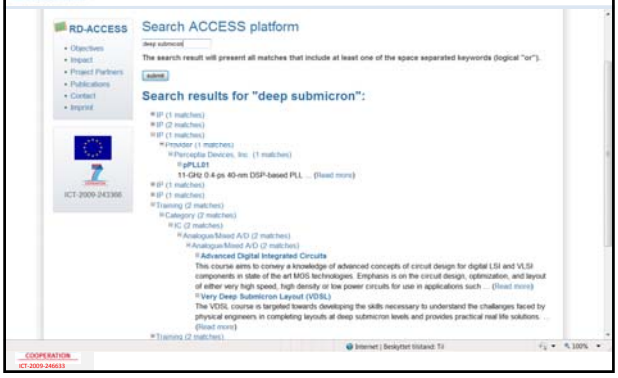
- A pan European dissemination platform
- Mailing lists reaching >40.000 semiconductor designers
- Support for design flow integration including training, IP, EDA tools and design methodologies

What are the benefits for the user?

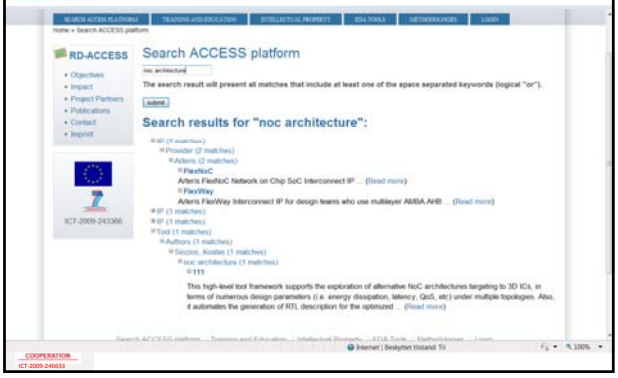
- ACCESS to European R&D knowledge infrastructure with initially more than 20.000 items
- ACCESS to one-stop-shop with single sign-on for semiconductor design knowledge
- ACCESS to annual workshops on application specific nanoelectronics platforms supporting the design in advanced processes

Searching

Search results



Search results - 2



European EDA startups & innovation: a (non exhaustive) survey

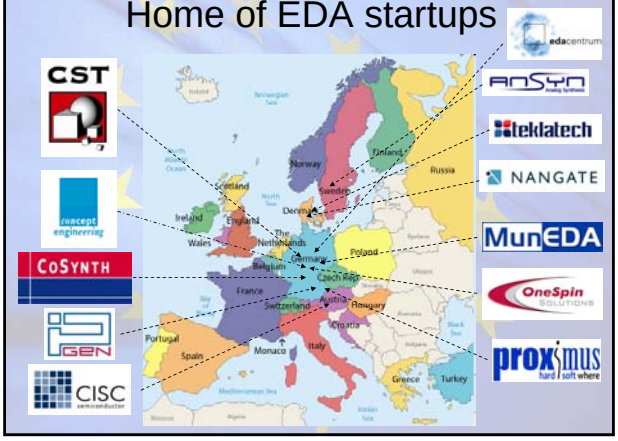
Mathias SILVANT, CEO EdXact
Michel TABUSSE, CEO Satin Tech.

Introduction

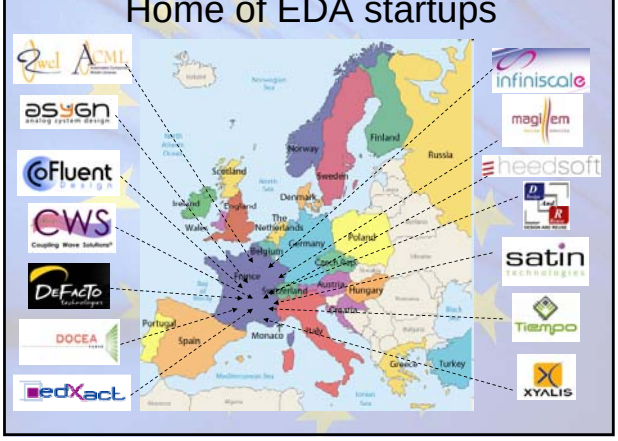
- This is NOT an exhaustive survey
- This is NOT a market report

- Instead …
- This is a group picture of European EDA startups, taken from the perspective of an informal group of company managers
- This group is meant
  1. to facilitate sharing of non competitive data and experience in a very informal way
  2. to make European innovation more visible

Home of EDA startups



Home of EDA startups



Working local, thinking global

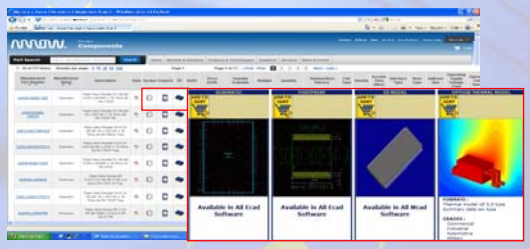
- Total EDA market approx. $ 4 bn = 2,8 Mrd. €
- Market : US 50%, Europe 20%, Asia 25%, ROW 5%
- Oligopoly: 80% of market held by 3 major US companies:
  Synopsys, Cadence, Mentor
- Compatibility and collaboration with « big 3 » is a must
- Important know-how and expertise in Europe

International Visibility

- Most important trade-fair:
  Design Automation Conference,
  USA, June 4-6.2011
- 204 exhibiting companies
- 15% new exhibitors
- More than 10% European headquarter
- Leading analyst's list of 30 « What's hot » contains: OneSpin, Docea, EdXact, Asygn

ACML

- www.2wcl.com
- Automated creation process for mechatronics ECAD/MCAD 3D thermal model



ASYGN

- Montbonnot, FR
- www.asygn.com
- Asygn specializes in the design and verification of analog/mixed-signal and RF systems. The company delivers application-focused solutions in order to deal with tough issues that traditional, generic approaches cannot handle. The company has had notable successes in the following applications: imaging arrays; MEMs and NEMs sensors; digital and fractional PLLs; high speed IOs.
- R&D Collaborations
  - PROMETHEUS : Parallel Computation
  - OPTIMYST: System Level Optimization.

CoFluent Design

- Le Chesnay, FR
- www.cofluentdesign.com
- CoFluent Design provides **standards-based system-level modeling and simulation** tools for executing use cases and predicting performance of multicore real-time embedded systems and chips.
- R&D Collaborations
  - MARTES,LAMBDA, ACROSS, PROMETHEUS

Concept Engineering GmbH

- Freiburg, Germany
- www.concept.de
- Concept Engineering provides Debugging and Visualization tools for RTL-level, Gate-Level and Transistor-Level as well as Visualization Engines for EDA tool developers (OEM business).
- In business since 1990 (21 years)
- Current Research Project: VisES
  2 Year funding via the German KMU-innovativ program (IKT)
  Research: System-Level Visualization Technology
  Project Partner: University of Bremen and industry partners

CoSynth

- Oldenburg, Germany
- www.cosynth.com
- CoSynth offers tools and design services for fast development of electronic solutions at system level. The SystemC based high-level synthesis methods are particularly suited for the design of hw/sw systems and FPGA solutions. Embedded hardware is developed from software algorithms with CoSynth's design methodology and an own high-level synthesis tool for C++/VHDL conversion.
- Public funding from EU and national sources
  - EXIST-Gründerstipendium (3/2010-2/2011)
  - Gründercampus Niedersachsen (4/2011-4/2012)

CWS

- Moirans, FR
- www.cwseda.com
- Coupling Wave Solutions S.A. provides the most complete solution for removing substrate, interconnect, package and pcb-related noise problems in integrated circuit (IC) design. Its WaveIntegrity™ platform dramatically reduces the impact of noise when combining analog/RF and digital blocks in a single IC/SoC or in a system-in-package (SiP).
- R&D Collaborations
  - ATHOLE : Low-power and Multi-processor systems ; partners ST, CEA-Leti, Thales and Verimag

DeFacTo

- Moirans, FR
- www.defactotech.com
- DeFacTo solutions enable designers to achieve “Design & DFT” closure at RTL by delivering a high quality suite of tools, which cover planning, analysis, insertion and debug needs. DeFacTo EDA tools HiDFT-SIGNOFF and HiDFT-STAR are silicon proven and are daily helping major semiconductor companies to increase predictability by strengthening Design and DFT quality at RTL and also by eliminating communication gap between DFT engineers and RTL designers.
- R&D Collaborations
  - ASTER: Architectures for high performance and static memories; partners ST, Dolphin, iRoC, G-Scop and TIMA

Design & Reuse

- Grenoble, FR
- www.design-reuse.com/
- Founded in 97, D&R became the worldwide leader as a web and a B2B portal in the IP/SoC field. With its 70k Unique Visitors / Month, 15k daily updated IP/SOC products descriptions and the ongoing client/provider matching activity, D&R stays unique worldwide.
- D&R licenses a Java/XML multi-application, configurable enterprise platform offering the most innovative and straightforward solution for Web Product cataloguing, intranet IP and Design Reuse Platform, External suppliers management and Web support.
- R&D Collaborations
  - ACCESS partners : CEA-Leti, Edacentrum, Eurotraining

Docea Power

- Moirans, FR
- www.doceapower.com
- Docea develops and commercializes a new generation of methodology and software tools for enabling faster and more reliable power and thermal modeling at the electronic systems level. Its Aceplorer™ software offers a consistent approach for executing architectural exploration and optimizing power and thermal behavior of electronic systems at an early stage of a project. At this level power savings can reach up to 80%.
- R&D Collaborations
  - CoSiP: Chip/package-system co-design ; partners ST, Infineon, Bosch, IRSEEM, MAGWEL

edacentrum

- Hannover, DE
- www.edacentrum.de
- edacentrum supports all activities to promote EDA in public. With regard to innovations in EDA edacentrum smoothes the transfer from academia to industry by promoting new EDA methods and tools. Therefore, edacentrum runs a database with innovative EDA tool demonstrators from different sources. One source is the yearly University Booth at DATE. The edaTools platform is open to all authors of innovative EDA tools. These EDA demonstrators are promoted at www.rd-access.eu/edatools/.
- R&D Collaborations in ENIAC, EU FP6 and FP7, CATRENE, IKT 2020 (German R&D program) e.g.
  - FP7 RD-ACCESS: Access to research results on semiconductor design; partners: CEA-LETI, COREP, D&R, edacentrum, Technoconsult

Edxact SA

- Voiron, FR
- www.edxact.com
- EdXact provides solutions for backend physical verification, providing layout extraction and analysis tools speeding up physical verification by an order of magnitude.
- Public funding from EU and national sources
  - CILOE (Bull, CS, Infiniscale, ProBayes, Leti, Tima): Parallel computing

HeedSoft

- La Roquette sur Siagne, FR
- www.heedsoft.com
- HEEDSOFT S.A.R.L develops and markets innovative solutions for the functional verification of circuits. Along years, the company has developed an in-depth expertise in the art of mixing several techniques like transistor abstraction, symbolic simulation and formal equivalence checking, in order to provide unique solutions for the formal validation of circuits at any level of abstraction, from Spice (full-custom) to RTL (even non-synthesizable) level.
- R&D Collaborations
  - none

Infiniscale

- Montbonnot, FR
- www.infiniscale.com
- Infiniscale provides variation-aware custom IC design solutions. These solutions include modeling, analysis and optimization of performances and parametric yield for analog and mixed-signal designs.

R&D Collaborations

– CILOE, Printronics, HONEY, MEDEA+, Mixipy, TDK4PE with partners such as ST, CEA-Leti, CEA-Liten, INES, SOITEC, UAB, UCL, CSEM…

IPGEN Microelectronics

- Bochum, GE
- www.ipgen.de
- IPGEN Microelectronics GmbH focuses on EDA solutions for analog/ mixed-signal (**1*Stone*®**) and design service related to design porting, specification adaptive analog IP creation/adaption and EDA assistance.
- The offered **1*Stone*®** product family strengthens the capabilities of available mixed-signal design frameworks towards design reuse. It utilizes design abstraction and refinement techniques to assist designers in organizing, structuring and administrating their complex analog design tasks from system abstraction down to mask layout level.
- IPGEN Microelectronics provides a cutting-edge, silicon-proven design automation solution that substantially reduces design effort for portable analog IP's and enhances quality and reliability significantly.

Magillem Design Services

Paris, FR / www.magillem.com

Magillem provides to customers in the electronic industry tools and services that drastically reduce the global cost of complex design. Magillem is a leading provider of tools and solutions for IEEE 1685 IP-XACT standard.

R&D Collaborations:

BACCARAT: Management of Timing Constraints in Electronic System Design Flows

BEYOND DREAMS: Design flow and environment for AMS systems

SOCKET: Design tool kit for critical systems

VERDI: Verification for heterogeneous Reliable Design and Integration

COMPLEX: Efficiency in Co-Development of Hardware and Software Engineers

SOFTSOC: Tools for generation of Hardware Dependent Software and drivers

TOISE: Trusted Computing for European Embedded devices and security aspects

pSAFECER: Safety Certification of software-intensive systems with Reuse

ProximusDA

- ProximusDA, Germany
- www.proximusda.com
- ProximusDA delivers products for system level architects, SOC verification engineers and SOC embedded software developers facing the heterogeneous parallel computing challenge. ProximusDA solutions extend the hardware transaction level methodology to embrace the software side providing a unified transaction level abstraction of the HW/SW system. ProximusDA's fast lightweight parallel task scheduling technology is used in the product itself and as a software IP stack for the embedded market.

R&D Collaborations

– none

Satin Technologies

- Montpellier, FR
- www.satin-tech.com
- Software solutions for electronic design quality monitoring ; design dashboards / checklist automation ; compliance reports
- R&D collaborations :
  - Crystal (design rules for mask manufacturing ; partners : Toppan, Xyalis, Atmel, LETI, ..)
  - Safety Standards (e.g. DO254)

Teklatech

- Copenhagen, DK
- www.teklatech.com
- Teklatech provides best-in-class electronic design automation (EDA) solutions to the ASIC design community. With innovations in power integrity and noise optimization technologies design engineers may reduce EMI and dynamic IR-drop. Teklatech's FloorDirector® tool is used to reduce dynamic current peaks and slopes in digital ASIC designs.

R&D Collaborations

– MODERN (ENIAC), NaNoC (FP7).

TIEMPO

- Montbonnot, FR
- www.tiempo-ic.com
- TIEMPO develops and markets a portfolio of EDA tools, IP cores and design services enabling chip manufacturers to design clockless (= asynchronous) chips, allowing maximum performance under extreme variability (process, voltage, temperature, data, tasks..), reduced energy consumption, lower noise and lower EMI.
- R&D Collaborations
  - MODERN : Modeling & design of reliable, process-variation aware circuits; partners: ST, NXP, Infineon, CEA-Leti, Thales...
  - ASTEC: Asynchronous technology for low power and secured embedded systems; partners: CEA-Leti, Grenoble INP, Sensaris

XYALIS

- Grenoble, FR
- www.xyalis.com
- XYALIS main tools includes CMP metal fill and MPW, Frame and Mask layout optimization. These tools brings advanced solution to the most important DFM issues found during the design and the photomask preparation.
- R&D Collaborations
  - CRYSTAL
    - DFM Photomasks inputs for EDA workflow
    - Atmel - CEA/LETI – Toppan Photomasks – Satin Technologies
  - HONEY
    - Cost Reduction oriented MPW floorplan software
    - Methodology and tool to calibrate the CMP models at no cost
    - STMicroelectronics

Conclusions

- European EDA is alive !
- Innovation & partnerships keep it on the leading edge

Verification & documentation flow with IP-XACT

2011 06 30 Grenoble

Ronan LUCAS : lucas@magillem.com

agenda

- Magillem company overview
- IP-XACT an IEEE Standard
- SoCKET Verification Flow
- DITA Documentation Flow
- Consistency between Flow

Company overview

Company profile

- 4 years of profitable double digit growth
- Listed on Euronext in Nov 2009 (MLMGL FR0010827741)
- Based in Paris(HQ, R&D), New York(office), Tokyo(office), Nice, Bristol, Caen, Seoul… , *Grenoble(office, R&D)*

Ecosystem

- First-tier customers in electronics and industrial systems : Texas Instruments, Fujitsu, Bosch, Qualcomm, ST microelectronics, NXP, STEricsson, Thomson, Sonics, European Space Agency, Thales, Alstom, Astrium, EADS Airbus..
- Joint Lab CEA/Magillem in Grenoble (documentation/traceability/embeded software)
- Member of the Board of Accellera and OCP-IP
- Cadence Alliance
- Partnership with TELNET (400 engineers for worldwide support)

What We Do

- Magillem has developed an easy to use, state of the art platform solution to :

⇒ cover electronic systems design flow challenges in a context

where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SOC.

- Main benefits include:
  - ⇒Maximizing Design and IP Re-use
  - ⇒Using a virtual platform to configure their system and IPs
  - ⇒Controlling the Design Flow
  - ⇒Exploring their Design Flow architecture and optimizing it
  - ⇒Improving their independence from CAD tools vendors
  - ⇒Improving interoperability, communication
  - ⇒Benefiting from better user interfaces to raise productivity
  - ⇒Relying on worldwide adopted standards

4

Magillem: a Partner to be considered

- Based on a unique Xml standard format (IEEE1685), Magillem's solutions offer :

✓A complete cartography of a system (hardware and software) independent from tools and languages : Rev.Enge

- ⇒ • Design life cycle management
- ⇒ • Obsolescence management

✓A platform to monitor third party vendors :

- ⇒ • for the full description of a hardware system at ESL and RTL : MPA
- ⇒ • for the description of the software system (registers) : MRV

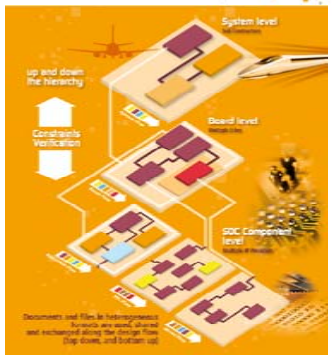
✓Magillem has a strong and long experience working with large corporations in electronics and industrial systems

5

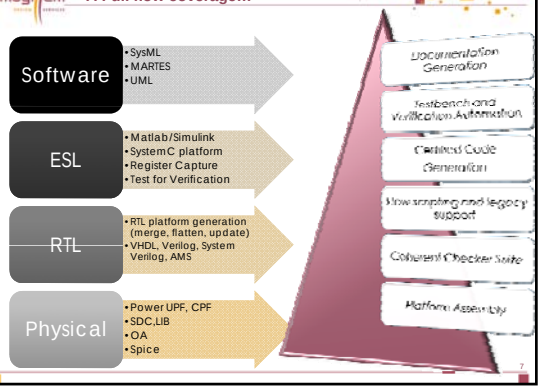
Ready for a complete System Design Capture

An Electronic Platform designed in a

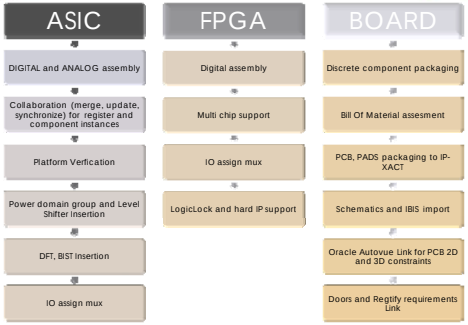
- Multi Site
- Multi Format
- Multi Methodologies
- Collaborative work
- context



A Full flow coverage…

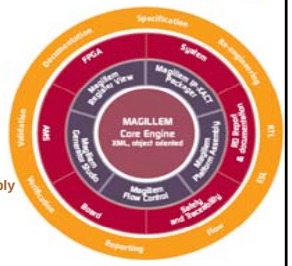


…targeting the scope of a system



The MAGILLEM 5.0 Platform

The Eclipse™ based Magillem Core is at the heart of a fully featured flow optimization suite comprised of :



IP level
- A packager of IP blocks (Magillem IP Packager),
- An IP-XACT and DRC Checkers Suite

Chip Assembly
- An ESL/RTL platform assembly (Magillem Platform Assembly),
- A Register Management tool (Magillem Register View).

Flow level
- A complete development environment (Magillem Generator Studio),
- A flow control tool (Magillem Flow Control)

agenda

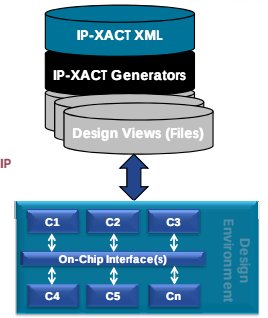
- Magillem company overview
- IP-XACT an IEEE Standard
- SoCKET Verification Flow
- DITA Documentation Flow
- Consistency between Flow

IP or System Descriptions

- Documenting attributes of an IP component
  - Interfaces and signals
  - Parameters
  - Memory maps and registers
  - File sets
  - Etc…
- Processing Information
  - Assembly
  - Synthesis
  - Test insertion
  - Verification
  - Etc…

IP-XACT for Component Descriptions.

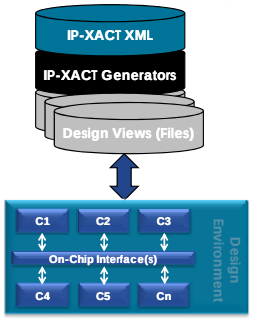
- IP-XACT is an IEEE1685 specification for documenting IP
  - Enables automated design creation and configuration
  - Tool independent
  - Machine readable
- Benefits
  - Documentation of all aspects of IP using XML databook format
  - Documentation of models in a quantifiable and language-independent way
  - Enables designers to deploy specialist knowledge in their design



- http://www.accellera.org/home

IP-XACT Descriptions

- e.g. Component XML describes
  - Memory maps
  - Registers
  - Bus interfaces
  - Ports
  - Views (additional data files)
  - Parameters
  - Generators
  - File sets

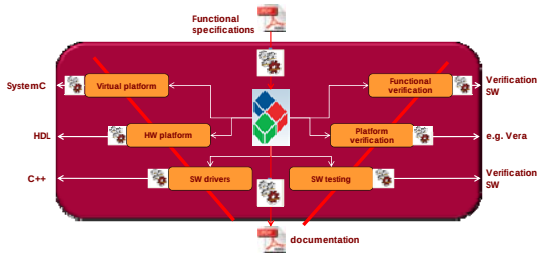


IP-XACT In the Design Flow

- ESL and RTL abstraction level
- HW and SW interfaces
- Language independent

Magillem Solution

automation



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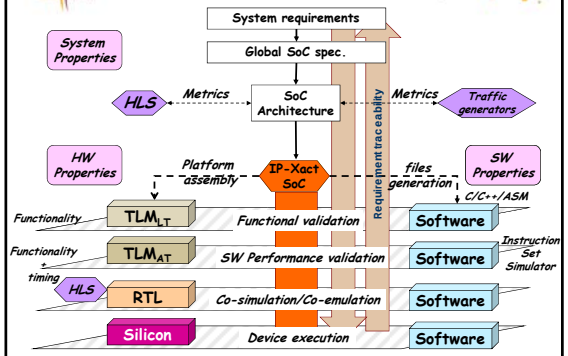
SoCKET Project

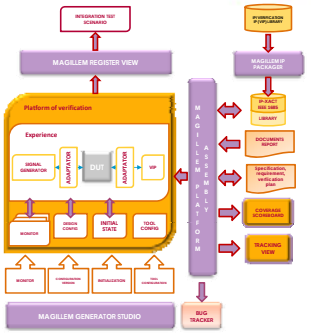
- Description:
  - SoCKET (SoC toolKit for critical Embedded sysTems)
  - French project with the Aerospace Valley and Minalogic pôles
  - Address the issue of design methodologies for critical embedded systems.
- Goals:
  - Define a "seamless" design flow which integrates qualification and certification, from the system level to integrated circuits and to software
  - Apply the SoC's design methodologies to critical embedded systems
- Industrial Partners:
  Airbus, Astrium, CNES, Magillem, PSI, STMicroelectronics, Thales
- Accademic Partners:
  TIMA, IRIT, Lab-STICC

SoCKET Platform



Assembly : Platform of Verification

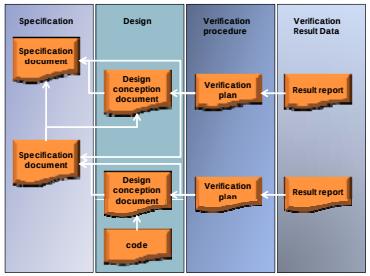
- import IP-XACT description
- DUT and Verification platform Assembly
  - Instantiation
  - Configuration
  - Interconnection
- Check & generation
  - Hardware Abstraction Layer
  - Netlist
  - Skeleton
  - Makefile



Traceability Management

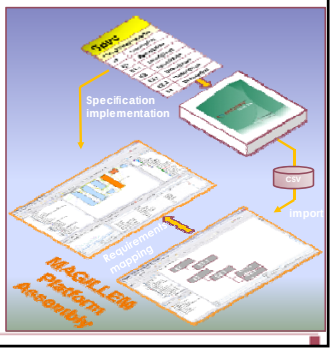
- Main Process Phases:
  - 1 – Capturing the need (capturing the requirements)
  - 2 – Analysing the requirements
  - 3 – Validating the requirements
  - 4 – Analysing deviations
  - 5 – Allocating the requirements
  - 6 – Verifying the requirements.
- All requirements must be:
  - identified by a single identification label,
  - allocated,
  - traced,
  - evaluated as regards maturity, priority, impact on the architecture,
  - validated,
  - verified according to an established procedure with defined means and must have an established satisfaction criterion (reaching an expected result).

Requirement traceability process



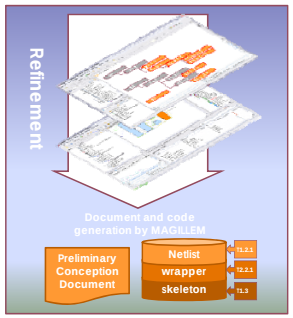
Phase 1: capture and mapping

- Build the platform from the specification with Magillem Platform Assembly (MPA)
- Load the requirements from the specification in a traceability tool
- Export the requirements tree
- Import the requirements tree in Magillem
- Map the requirements on the platform described in IP-XACT Standard (drag&drop)



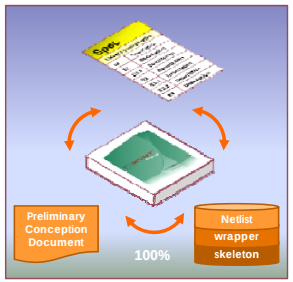
Phase 2: Refinement, implementation and generation

- Refinement of the Requirements done during the conception
- update the mapping on the platform described in IP-XACT
- generate Preliminary Conception document with Magillem Generators
- Tags intrusive implementation in the code with Magillem tools (SystemC, systemVerilog, vhdl):
  - Netlist : instantiation and connection of the components in top level
  - Wrapper : shell around an external IP
  - Skeleton : component description (hw and sw interface)



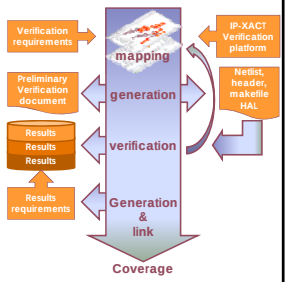
Phase 3: Check

- Cross checking the requirements in the spec, Preliminary Conception Document and source codes with a dedicated tool
- IP-XACT requirement description manage only one single source along the flow, during conception and implementation steps



Phase4: Verification

- Each requirement must be verified
- Map verification requirements on the IP-XACT verification platform where the DUT is instantiated
- generate Preliminary verification document, makefile, HAL, netlist
- run verification
- generate a results requirement document that links the verification requirement and results
- check requirement coverage with a dedicated tool and generate progress verification report



agenda

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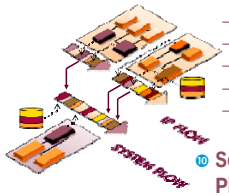
Documentation Flow

- **Problem targeted :**
  - No documentation flow
  - Reuse content of documentation
  - Difficulty and costly to maintain
  - Content and form not separated
  - Tied to a tool
  - Linked with others design flows



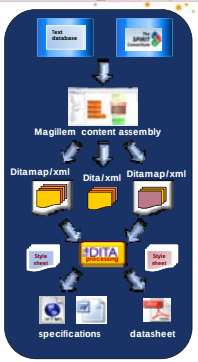
- **Solution : Magillem Content Platform**
  - Document is an IP or a System specific view
  - Meta-data description
  - Domain specific object management and handling

DITA Standard

- DITA (Darwin Information Typing Architecture)
- http://www.oasis-open.org/committees/dita/
- XML based, end-to-end architecture for authoring, producing and delivering documents
- OASIS Standard donated by IBM
- Modular content : structured information in a wide variety of environment
- Facilitate information sharing and reuse
- Maps: Link-based assembly of topics to create publications
- Specialization: New element types formally based on core DITA types

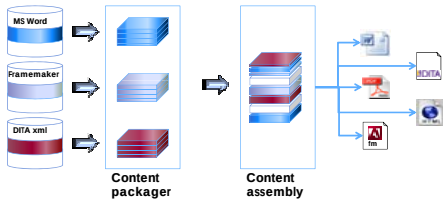
DITA Flow

- Import resources from different origin
- Reorganize and update the document
- Author the new document
- Generate DITA files
- Select the appropriate style sheet
- Generate the document in the right format



Import : Content Packaging with Magillem

- Identification and content versioning
- Text structure and content analysis
- Definition of Minimum Re-usable Unit
- Hierarchical object management
- Configuration, edition
- Multi-source integration



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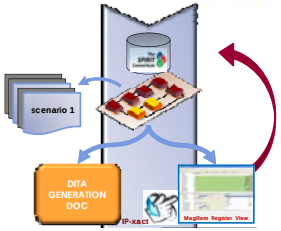
Consistence and coherence

- Shared information between flows

- Impact of modifications
- Risk analysis
- Update generated files or document
- Optimize non regression tests

IP-XACT shared information

- SW Registers Abstraction Layer by MRV
- IP-XACT database
- Selection of the scenario for non regression test
- SW Interface specification by DITA Generation Document



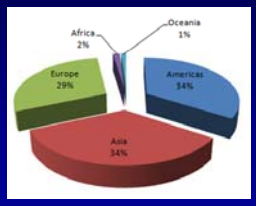
Which IP is needed by the semiconductor community?

Gabrièle Saucier
Philippe Coeurdevey

www.design-reuse.com

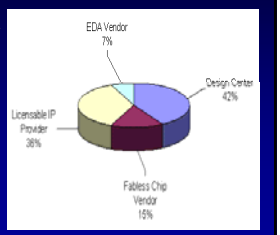
D&R Web site Eyes

- From 97 to 2000 D&R website most of the numbers grow and *then stay close to stable*
- Users
  - IP/SoC community was born
  - 15,000 daily updated IP/SOC products descriptions
  - 35.000 registered members
  - 70,000 Absolute Unique Visitors / Month (source: Google Analytics)
  - Geographic distribution was the most evolving parameter Asia and Far East growth
  - IP SoC News Letter
  - B2B Market Place (Wanted IPs)

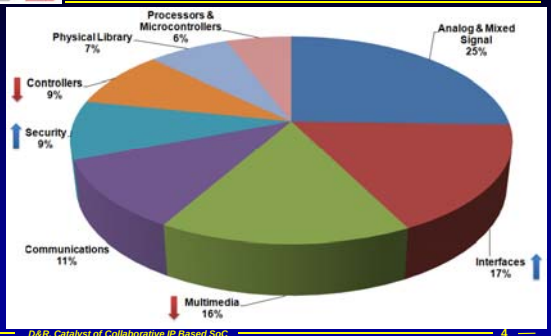


IP Providers

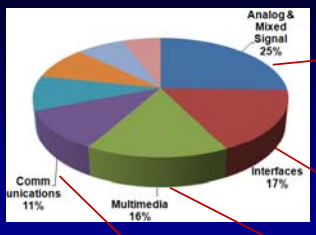
- Broad distribution of IP providers with regards to their core business
  - Shift from licensable IP providers (Star IPs) to other players: Design Center, EDA vendors, Fabless IC vendors, Foundries etc...
  - IPs are viewed as catalysts of a broader production/Product (EDA vendors, foundries, IC vendors...)
  - IP does not refer to the business model but to the "Intellectual production" of designers: Design innovation portal
- *D&R mission: Publish and report on innovation in the design area*



Sector attractiveness



Top Products



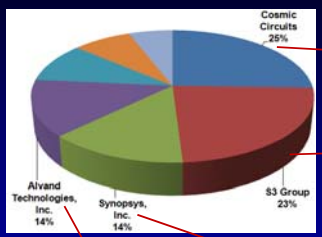
1. 802.11 A/B/G/N Direct Conversion Transceiver (RF Integration Inc.)
2. 802.15.4 (Zigbee, 6LoWPAN, RF4CE, ISM) PHY (RF Integration Inc.)
3. OSC - Crystal Oscillator Nano Power Series (SiliconGate)

1. USB3.0 PHY (Cadence, Inc.)
2. USB 3.0 Device IP Core (ASICS World Services, LTD.)

1. RF and Analog GPS/GNSS Front End for GPS, GLONASS, Galileo and Beidu (RF Integration Inc.)
2. 10/100/1000Base-T Gigabit Ethernet-Over-Copper PHY Core (TranSwitch Corp)

1. H.264/MPEG-4 AVC High-Profile / High-Definition Encoder (Allegro)
2. Multi-standards Dual-HD Video Codec IP Core with VP8 and MVC support (Chips&Media, Inc.)

Analog & Mixed Signal : Top Providers



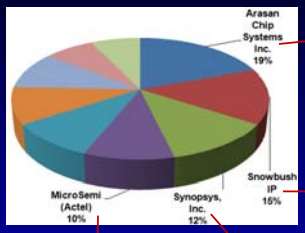
1. MIMO WLAN and WiMax AFE 802.11n 802.11g 802.16 802.16e platform
2. Analog Front end platform for WLAN and WiMAX single and multi-channel MIMO systems

1. Multi-mode Multi-band RF Receiver
2. 12-bit 2MS/s Dual Input ADC with temperature Sensor

1. 12-bit 80MSps ADC - Pipeline
2. 11-bit 800MSps ADC - Pipeline

1. 10-bit, 205MSPS Triple Channel Video AFE with sync processor
2. 24-bit, 96dB Dynamic Range, 8 to 192kHz Sampling Frequency Stereo Audio Codec with Multiple Analog IOs

Interfaces: Top Providers



1. USB 3.0 Device Controller - Compliant with AHB/AXI, OCP,PCIe or custom I/F
2. USB 3.0 Host Controller – Compliant with optional AHB/AXI/OCP, PCIe or custom

1. 1.0-6.5Gbps Multi-Standard SerDes
2. LP USB 3.0 SuperSpeed PHY

1. Smart Card Reader for APB
2. MIL-STD-1553 BC, RT and MT

1. High-performance DesignWare SuperSpeed USB 3.0 PHY
2. USB LPM-HSIC PHY

Multimedia: Top Providers

1. Multi-standard and Multi-stream Ultra High-Definition Video Decoder (H.264, MPEG-1/2, VC-1, JPEG) with MVC Support for 3D Video Applications
2. Camera Processor IP Cores up to 18 Megapixels

1. Multi-standards Dual-HD Video Codec IPCore with VP8 and MVC support

1. CL11061 MIPI-DPHY/sub-LVDS/SMIA-CCP2 multi-PHY Driver 1G/650Mbps
2. CL11111 SLVS-400(HiSpi)/sub-LVDS Multi-Driver 800M/680Mbps

1. H.264/AVC CAVLC Encoder--Single Core Max 800Mbps on ASIC
2. H.264/AVC CABAC Encoder--Single Core Max 200Mbps

Communication: Top Providers

1. 3GPP LTE Fast Fourier Transform (LTE-FFT)
2. 3GPP LTE Turbo Decoder

1. 10G KR SerDes in TSMC 40G (802.3ap)
2. 10G KR SerDes in TSMC 40G (802.3ap)

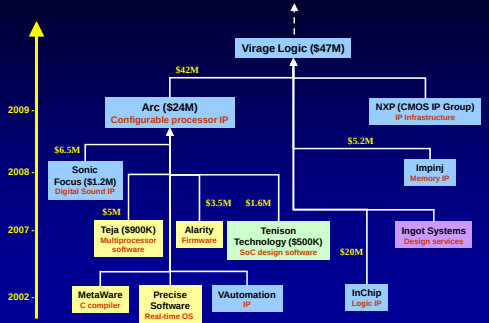
1. Tail Biting Viterbi decoder for 3GPP LTE
2. 802.11n (MIMO WLAN) LDPC decoder / encoder

1. Triple speed Gigabit Ethernet MAC (GEM)
2. Quad Serial Gigabit Media Independent Interface (QSGMII)

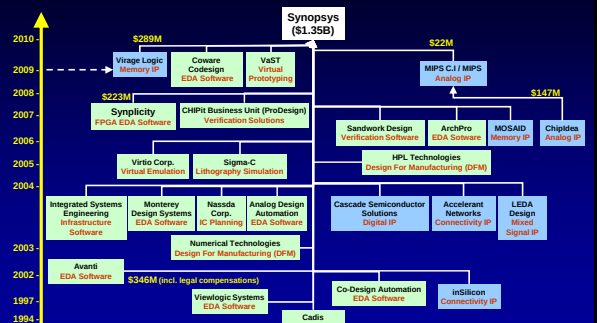
IP Provider and Life Cycle

- IP Provider profile
  - Analog, libraries: engineering skill and know how :technology follow up
  - Connectivity ,interface IP: Standard follow up
  - Innovative product differentiator: application specific subsystem
    - Arm and processor
- IP provider **Fabless***Design house***IC vendor**Equipment
- The market evolution
  - Less Asic design; Exponential growth in Asic Design cost
- Market consolidation Towards Large companies with vertical market segments
  - Accelerated IP Provider acquisition flow
  - Predictable? How does it affect IP community?

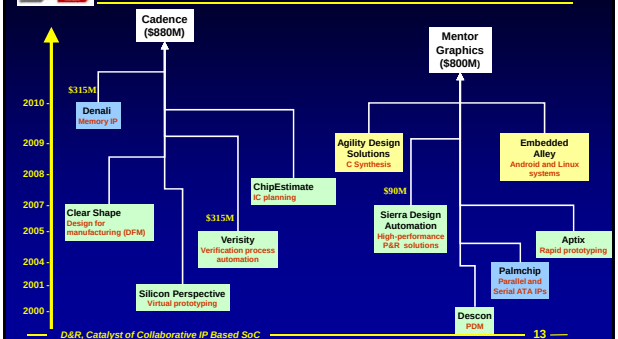
Embedded Systems :IP Provider and Market Consolidation



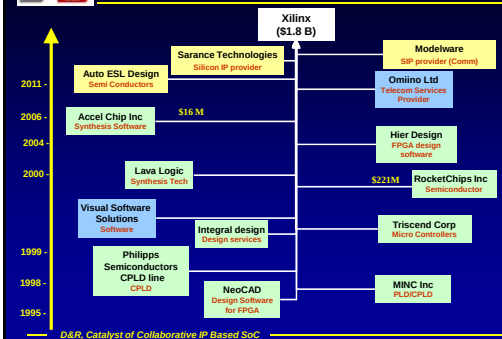
IP Provider and Market Consolidation Synopsys



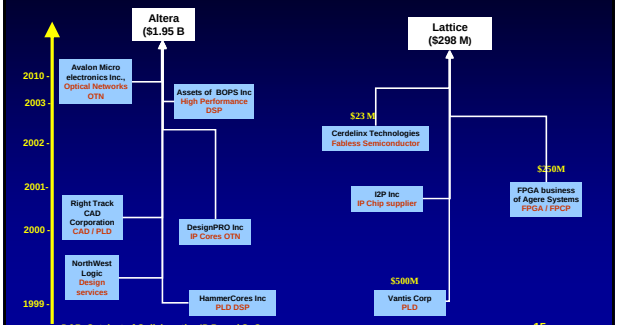
IP Provider and Market Consolidation
Cadence & Mentor



FPGA vendors: Market consolidation



FPGA vendors: Market consolidataion
Altera & Lattice



D&R Hot initiatives

- IP SoC Tour consolidation
  - Tel Aviv ,Santa Clara ,San Diego IP Soc village at DaC , Taiwan ,China..
- Wanted IP Market Place
  - IP rep Service (Emerging Market Countries)
- Foundry Gateways
  - Standardized foundry process status
  - TSMC and SMIC Gateway

And next..
Embedded Software IP online Sales

- D&R B2B "Wanted IP" experiences
  - IP community widely spread around the world
  - Strategic IPs for project can be in the hand of a "remote " small provider
  - Time to market can require extremely fast decision
- Dialog and confidence must be established promptly
- Transactions have to be activated across countries
- D&R initiatives
  - Accurate and detailed IP publishing data
  - D&R REP services in market emergent countries
  - Knowledgeable preferred partners network
  - Offers to be a transaction node
  - Ecommerce infrastructure when appropriate

Why Embedded Software IPs as a first trial

- Motivation
  - Embedded software IPs are of major and growing importance for Embedded systems
  - Some are "Low" priced and difficult to be sold with sales marketing overhead
  - Worldwide dispersed IP providers (India ,Asia, Europe)
- Need
  - Integrated marketing & sales, delivery ,purchase environment

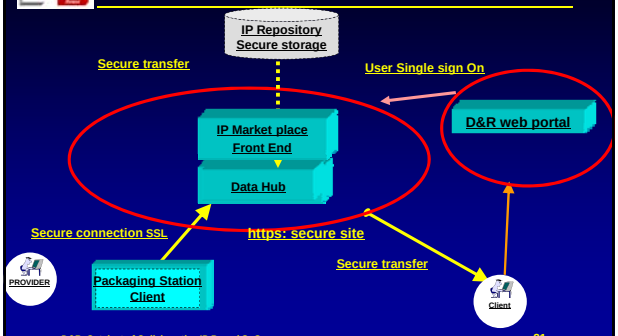
Why Embedded Software IPs as a first trial

- IPs have to be tuned to a customer environment
- Challenges
  - Environment can be abstracted
    - Platform with a core and an O.S
  - General purpose Eval package
  - Standard license agreement
- Fast Refinement
  - Tuned delivery for the client in a short time
  - Definitive license agreement

Creating an e commerce satellite

- Embedded Software IPs already published on D&R public website www.design-reuse.com
- D&R Well connected to the IP providers community
  - Entry point: D&R website
  - Visibility enhanced for D&R preferred partners
- A satellite
  - Lead are triggered on the public website
  - Users access easily a satellite platform
  - User Single sign on bridge transfers user profile to the satellite
- Infrastructure available :D&R secure IP Management Platform

Secure e Commerce Infrastructure



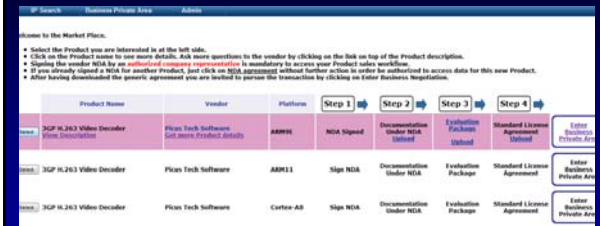
Business Workflow :From a shared to a private area

- Shared area :The user
  - Signs NDA : approved by the vendor
  - Gets information, dialogs with the vendor
  - Downloads Eval package
  - Downloads standard license agreement
- Private area
  - The user enters private discussion with the client
  - A definitive license agreement is posted by the vendor with pricing offer
  - The vendor informs D&R that the negotiation reached a conclusion

Transaction Workflow

- Private area
  - The user Signs definitive license agreement
  - A pro forma bill is posted
  - The user
    - Downloads the pro forma bill
    - Pays by bank transfer or online by credit card
  - The vendor/D&R uploads the definitive user specific delivery in the repository (under revision control)
  - The user downloads the delivery
  - D&R pays back to the vendor deducting D&R interest

Transaction work flow :Shared area



Transaction Work flow: Private area

Business Model

- Vendor should be a D&R preferred partner so that
  - Visibility is high
  - D&R follows the provider life cycle and affords first level of guarantee to buyers
  - Marketing and leads are properly organized
- The vendor grants to D&R X% of vendor fee
  - deducted from the amount given by the buyer for a sales conducted on the ecommerce site
  - Paid directly

More options available for the vendor

- Optional Management Best Practices
  - Client Delivery are archived and put under revision control in a repository
  - Delivery history available
  - Alert to client when a new version is available
- Bug panel
  - Entry of bug declaration (internal or client specific)
  - Bridges to affected client
  - Warning and patches to client

Conclusion

For understanding the IP world and the IP trends

For Sharing
- Reusing
  - Buying
    - Selling
      - Managing IPs

Join D&R community

www. Design-Reuse.com

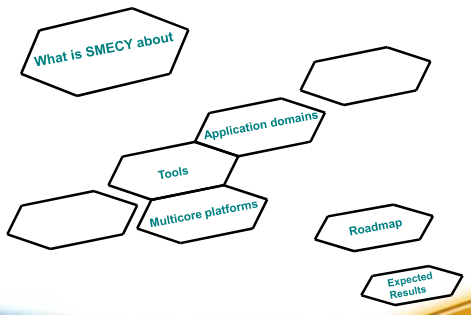
SMECY

Tool chains for multicore platforms in advanced technologies

Workshop ACCESS to innovation in semiconductor design
30 June 2011, Grenoble, France

Francois Pacull
CEA-LETI Minatec, Grenoble, France

Content of this presentation



SMECY

Project ARTEMIS
funding both at National and European level
Artemis JU 100230

- **Start date:** Feb, 2010
- **Duration:** 36 Months
  Partners: 29
  Countries: 9
- **Budget:** 20 M
- **Total Effort:** > 1800 pm
- **Coordinator:** CEA (France)

Advanced
Research &
Technology for
EMbedded
Intelligence and
Systems

SMECY context

- **Currently number of cores per chip increases (already above 100)**
  Trend is not going to change
- **Multicores no longer manageable by hand**
  Would be too complex to optimize
- **Variability of cores (computing units)**
  Correction by software required
- **Difficulties to express / extract / exploit parallelism**
  Both at application and platform level

SMECY Objectives

- **To provide compilation tool chains**
  for each of the identified platforms and demonstrated in a number of industry cases.
  - A common architecture, APIs, and design tool platform, several application domains
  - Interoperable tool suites to support massive real-time data-processing
  - Design tools and associated runtime support able to:
    handle composability, predictability, parallelization and aggregation.
    consider performance and/or energy modeling.
    provide analysis, verification, scalability and appropriate levels of safety.
- **Relevant to the overall ARTEMIS target:** ***to reduce the design cost in embedded system field***
  To shorten development cycles,
  To increase manageable complexity (application & system)
  To reduce effort and time (creation & re-validation and re-certification)
- **Driven by**
  A number of industry cases from ARTEMIS domains.
  Different platforms (academic and industrial)

Geographic distribution

European Initiative
Response to
Asian and US efforts in this area

Put together the different actors in term of competencies and concerns around the usage of multi-cores

Different view points & concerns

Research: (13)
- UTIA, BUT,
- DTU,
- VTT,
- CEA, UJF/Verimag,
- AUTH, UOI,
- POLITO, UNIBO, POLIMI,
- TUDelft,
- HH,

Industrial: (10)
- NetHawk, Tellabs,
- TRT-FR, TVN, ST-GNB2,
- HAI,
- SELEX-SI, ST-Italy,
- SWM,
- TRT-UK,

SME: (6)
- HPC, Skylab,
- F2M, RTE,
- ACE,
- CIP

Competencies

Applications
- Skylab, TVN,
- F2M, SMW,
- HAI,
- SELEX-SI,
- TRT-UK,
- CIP

BUT, ST-Italy, Tellabs, NetHawk, VTT, TUDelft, UJF/Verimag, HH, AUTH

Platforms
- UTIA,
- ST-Italy, ST-GNB2,

Tools
- HPC, CEA, UJF/Verimag, TRT-FR, ST-GNB2
- HH, RTE,
- VTT, NetHawk, Tellabs,
- ACE, TUDelft,
- DTU,
- AUTH, UOI,
- UNIBO, POLITO,POLIMI, ST-Italy
- UTIA, BUT, CIP

The quest

For years we looked for the grail:

One fits all
"The Single Universal Compilation Chain"

All applications
All programming paradigms
All target platforms (multi-cores in our case)

The realistic quest

The grail does not exists but …
… it is possible to have something efficient

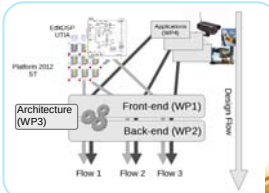
Once
programming paradigm/application domain
and
platform
are fixed

With reasonable effort we can:
go from one programming paradigm to another
or
go from one platform to another

What is SMECY about ?

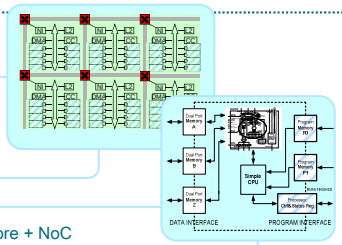
Providing tool chains adapted both

at the application domains
and
the targeted platform



2 Platforms

Industrial (ST)
Academic (UTIA)



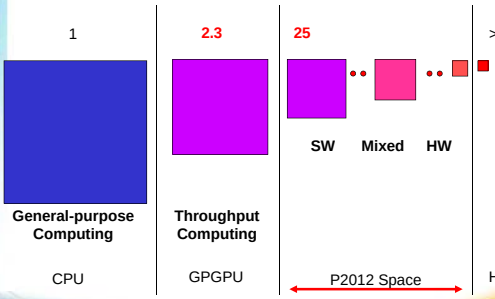
1 homogeneous manycore + NoC
1 FPGA accelerators,
standard RISC with heterogeneous HW accelerators

Platform 2012

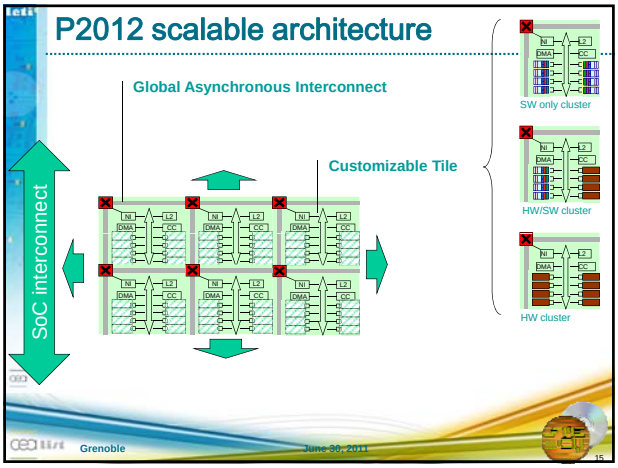
- R&D many-core platform for efficient acceleration targeting 32nm technology and beyond
- Scalable computing tiles with independent power and clock domains (3D stacking ready)
- Asynchronous NoC interconnect ➔ GALS architecture
- Shared memory clusters with customizable ST processor, hardware synchronization and multichannel DMA
- Multiple programming models (Native, OpenCL)

P2012 positioning

GOPS/mm²/W in 32 nm



P2012 scalable architecture

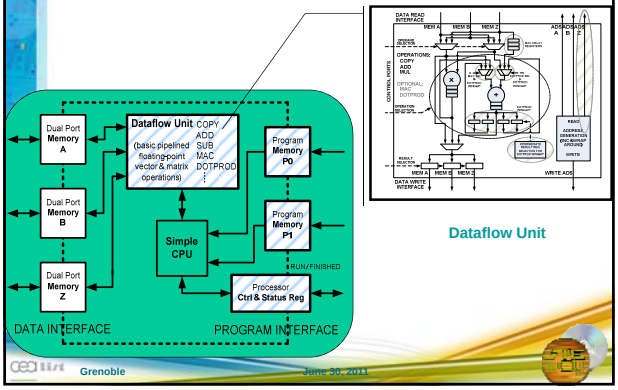


Platform EdkDSP

Computation = HW computation + SW computation

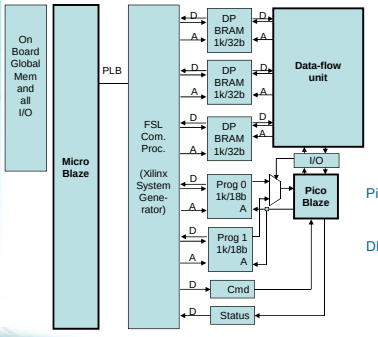
- **Hardware – Basic Computing Element (HW accelerator)**
  Elementary kernels computed on batches of data (DFU)
  data flow
  User kernel computed as sequence of elementary kernels (sCPU)
  control flow
- **Software – host CPU**
  User function call (kernel) implemented in hardware (host CPU)

Basic Computing Element (BCE)



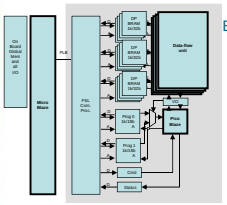
Dataflow Unit

BCE in EDK

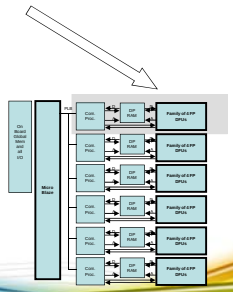


PicoBlaze is scheduling sequences of batch operations
DFU supports a selected set of vector operations

BCE Scalability

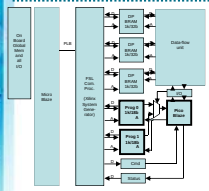


Extension: 4SIMD



Multiple 4SIMD

BCE Flexibility:



Reprogramming

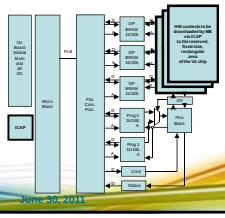
Change of PicoBlaze firmware in few clock cycles

Reprogram while executing

Reconfiguration

Change of HW data path in more clock cycles

Substantial change of HW (floating- vs. fixed-point)



Applications

Domain 1

RADAR SIGNAL PROCESSING AND EARTH OBSERVATION
- Passive Coherent location (PCL) radar
- Space Time Adaptive Processing (STAP)
- Active Electronically Scanned Array (AESA) radar
- Measurement and Analysis of Time-Varying Targets

Domain 2

MULTIMEDIA, MOBILE AND WIRELESS TRANSMISSION
- Orthogonal Frequency Division Multiplexing (OFDM) modem
- Audio Decoding
- Software Spectrum Sniffer for Cognitive Radio Systems in the ISM Band.
- Mobile Network Protocol Analyzer
- Video Processing on Mobile nodes

Domain 3

STREAM PROCESSING
- Video surveillance
- Video encoding
- Object Detection
- Wavelet image processing.
- High Dynamic Range Image Processing
- 3D Graphics Particle Rendering
- Time-Space Features Processing

3 Clusters

EdkDSP + STREAM PROCESSING (VIDEO SURVEILLANCE)

P2012 + MULTIMEDIA, MOBILE AND WIRELESS TRANSMISSION

P2012 + RADAR SIGNAL PROCESSING AND EARTH OBSERVATION

3 clusters
Platform + domain

To exploit specificities of platform and application domains

Cross fertilisation inter-clusters

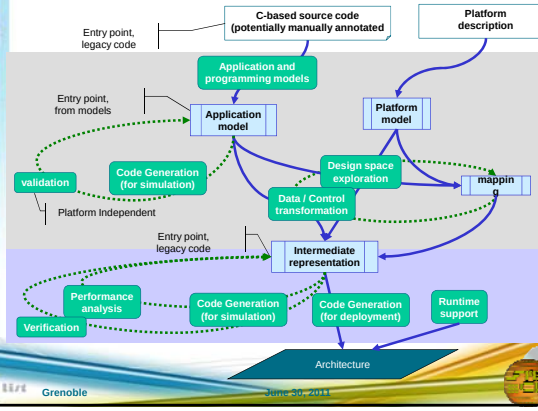
WP4: Application domains

WP1 Front - End

WP2 Back - End

WP3 Architecture

The big picture



Tools

CoSy (ACE)
- Modular toolbox for compiler construction
- In: C, C++, Embedded C
- Out: Assembly, C, static analysis results.

OMPi (UOI)
- C Source-to-source OpenMP compiler
- In: ANSI C with pragmas (OpenMP, OMPi-specific)
- Out: ANSI C with calls to OMPi's runtime lib

BIP (UJF Verimag)
- Framework for building complex systems by coordinating a set of atomic components
- In: the BIP language
- Out: analysis: debugging, deadlock, performance

DOL/BIP (UJF Verimag)
- Generator and analyzer of a mixed HW/SW system from the application, description of HW, mapping
- In: DOL specification: C + HW platform + mapping
- Out: BIP System model, performance evaluation

ABSOLUT (VTT)
- Tool for performance modelling and evaluation
- In: ANSI C, single or multi-threaded (POSIX).
- Out: Performance data, utilisation, I/O traffic, processing times of services

HAMMER (HH)
- Mapping of actor-oriented programs on parallel HW
- In: a graphical and/or Java description of SW
- Out: execution analysis (graphical)

BlueBee (TU Delft)
- Tool chain to port applications to heterogeneous multi-core platforms
- In: ANSI c
- Out: ANSI C with pragma's or binary

CodeComments (DTU)
- Compiler to automatically parallelize, vectorize and transform loop nests in the source code
- In: sequential ANSI C
- Out: Modified/refactored ANSI C /optimized binary

SPEAR (TRT-FR)
- Graphical model-based tool to implement data-streaming applications on parallel machines.
- In: C kernels (graph from scratch or from an IR)
- Out: parallelised code or XML IR with // choices

P2012 SDK(CEA / ST)
- SDK for Platform 2012
- In: (MIND, OpenCL, NPL constructs)
- Out: Binary for P2012 virtual Platform.

LISSOM (BUT)
- Generator of tools (assembler, disassembler, linker, simulator, C compiler) and hardware prototype
- In: ASIP model in the ISAC language
- Out: C compiler

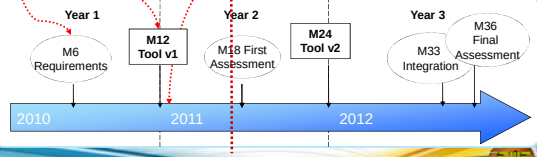
Par4All (HPC)
- Source-to-source parallelizing tool generating parallel programs from a sequential code
- In: C, Matlab with loop-nest with potential //sme
- Out: Source code + pragmas for lower tools; source code for Par4All Accelerator

EdkDSP SDK (IUTIA)
- C compiler, assembler and linker and 2 application interfaces to the EdkDSP accelerators.
- In: limited ANSI C with API function calls.
- Out: binary for the accelerator's microcontroller.

Work in progress (past)

We are at t0+17

- Application providers
  - have proposed a large number of applications (>15)
  - have exhibited the critical bottlenecks
- Tool providers
  - have delivered standalone tools
- We have defined 4 use cases



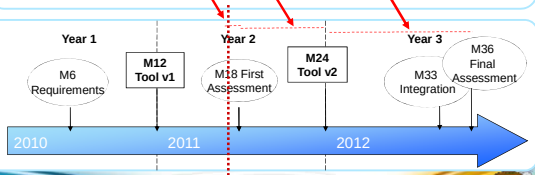
Work in progress (currently)

- **The tools are evaluated on applications critical samples**
  - Usability,
  - Utility,
  - Efficiency,
- **Tool providers work on interconnecting different tools**
  - Intermediate representation,
  - Gateway in between the tools
- **Run time mechanisms are experimented**
  - Fault tolerance,
  - …

Work in progress (next steps)

Next Steps

- T0+18
  - Assessment of the tools
  - Organization in clusters (tool chain)
- T0+24
  - Refined tool chains // Integration new mechanisms (e.g. FT, energy mgt, …)
- T0+36
  - Integration of the tool chains // Improvement // Assessment



Conclusions

- **Programmability of multicore platforms is one of the big challenges**
  - No single silver bullet
  - Consider both platform and application characteristics
- **Semi-automatic is already ambitious**
- **SMECY brings together advanced and already matured approaches**
- **Expected results**
  - Compilations chains
  - Know how for new compilation chains
  - Speed up for critical parts of the targeted applications
  - Requirements for future platforms

Contacts

- **contact@smecy.eu**
- **http://www.smecy.eu**

Domain 1

RADAR SIGNAL PROCESSING AND EARTH OBSERVATION

- Passive Coherent location (PCL) radar
- Space Time Adaptive Processing (STAP)
- Active Electronically Scanned Array (AESA) radar
- Measurement and Analysis of Time-Varying Targets

Some of the interesting aspects

- Huge amount of data,
- Intensive matrices computation,
- Targeted gain 2 level of magnitude (time) for some critical parts,
- …

Domain 2

MULTIMEDIA, MOBILE AND WIRELESS TRANSMISSION

- Orthogonal Frequency Division Multiplexing (OFDM) modem
- Audio Decoding
- Software Spectrum Sniffer for Cognitive Radio Systems in the ISM Band.
- Mobile Network Protocol Analyzer
- Video Processing on Mobile nodes

Some of the interesting aspects

Mobility,
Energy management constraints,
…

Domain 3

STREAM PROCESSING (VIDEO SURVEILLANCE)

- Video surveillance
- Video encoding
- Object Detection
- Wavelet image processing.
- High Dynamic Range Image Processing
- 3D Graphics Particle Rendering
- Time-Space Features Processing

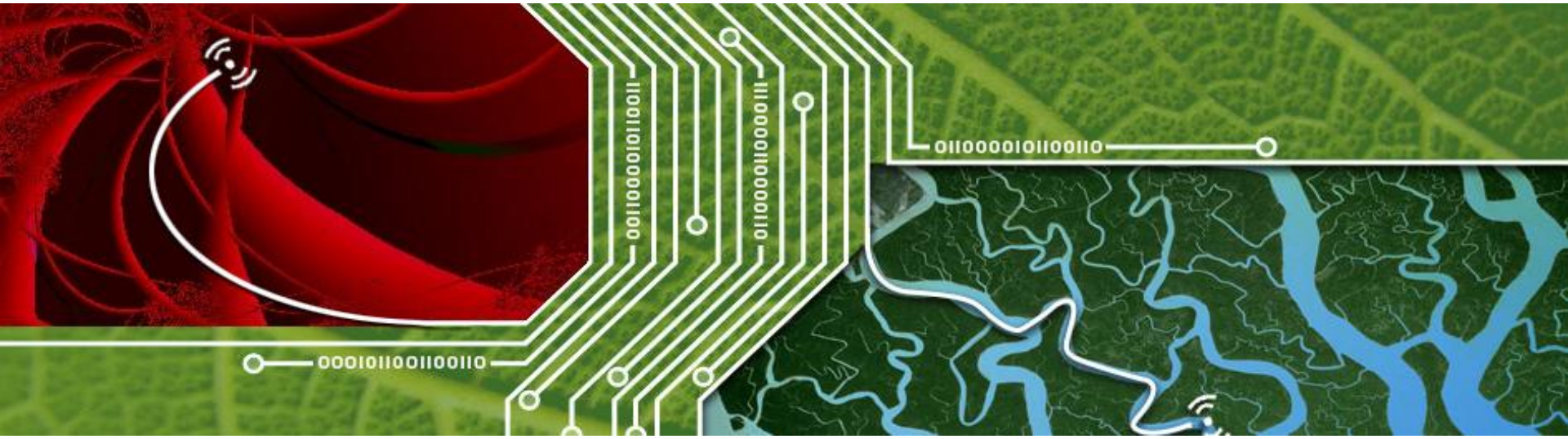
Some of the interesting aspects

Streaming,
Demanding algorithm,
…

nano-tera.ch

swiss scientific initiative in health / security / environment systems

Patrick Mayor



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Mission

Research, Design & Engineering of complex systems (tera-level)

for Health, Security and Environment

using micro- and nano technologies

Fostering research and crossbreeding of hardware and software technologies in the areas of implantable, wearable & ambient systems

Convergence of technologies in these areas: fertile ground for innovation

- Develop new markets
- Improve living standards
- Better the quality of health, security & environment systems
- Foster a vision of engineering with social objectives
- Promote related educational programs

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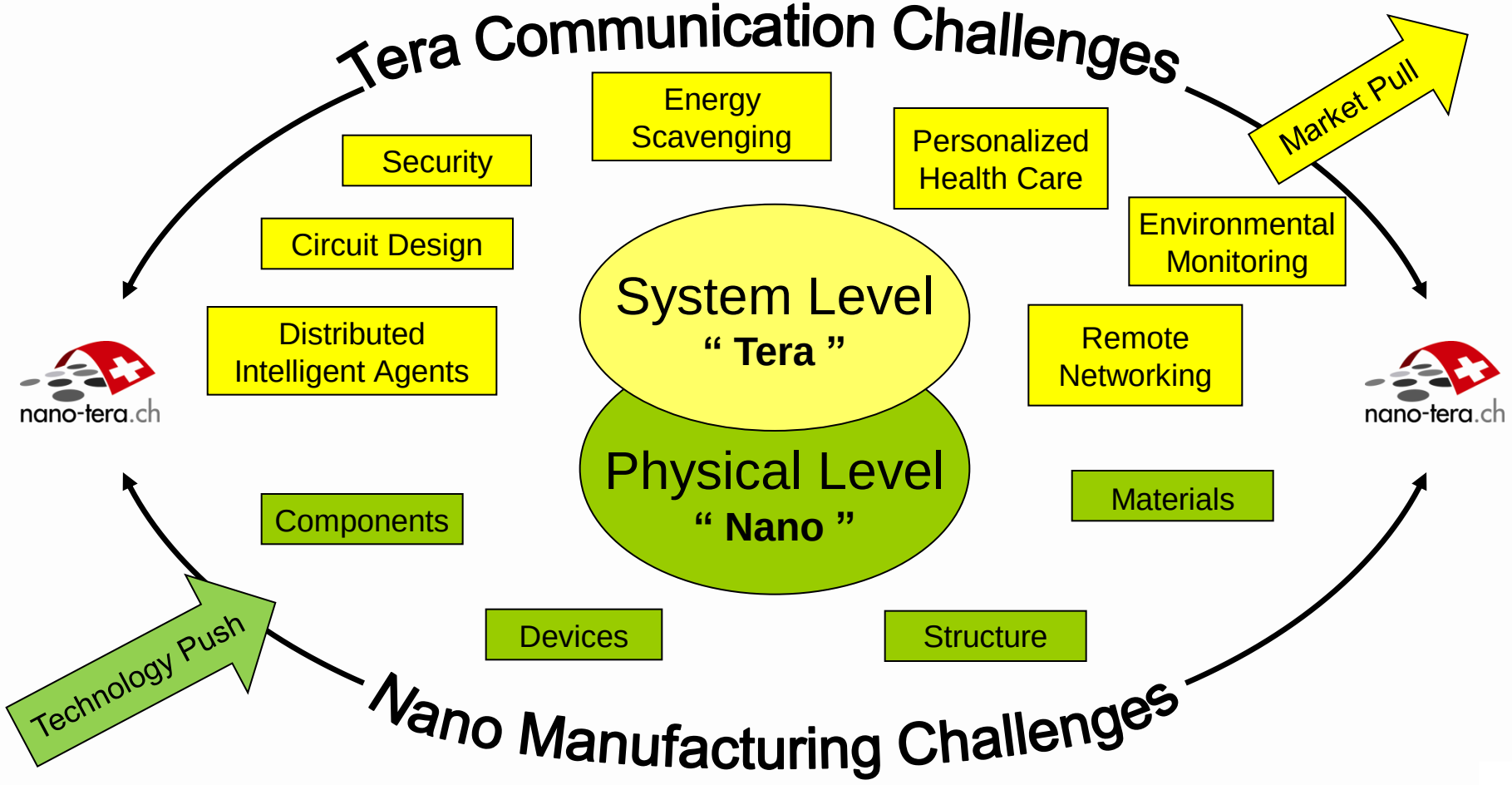
Converging Challenges



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Projects

➢ RTD — Research, Technology, Development — 19 projects

- Call 2008 ➡ 10 projects started in 2009 *(duration: 4 years)*
- Call 2009 ➡ 9 projects started in 2010 *(duration: 3 years)*

➢ NTF — Nano-Tera Focused — 15 projects

Regular calls 2008-2010 (now closed)

➡ 2 projects completed
13 on-going projects *(duration: 1-2 year)*

➢ ED — Education & Dissemination — 18 activities

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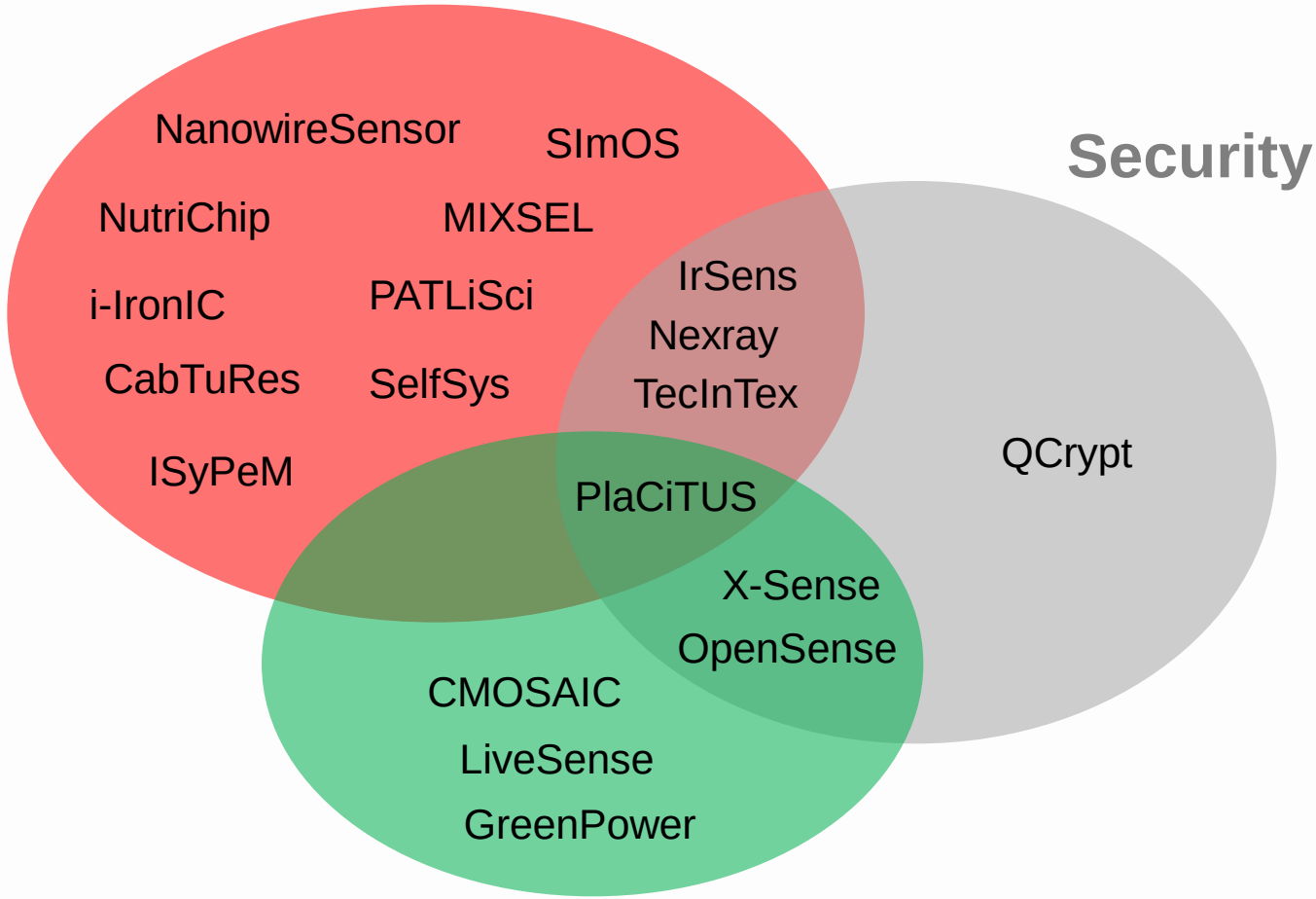
RTD Projects by themes

19 RTD projects
3-4 years



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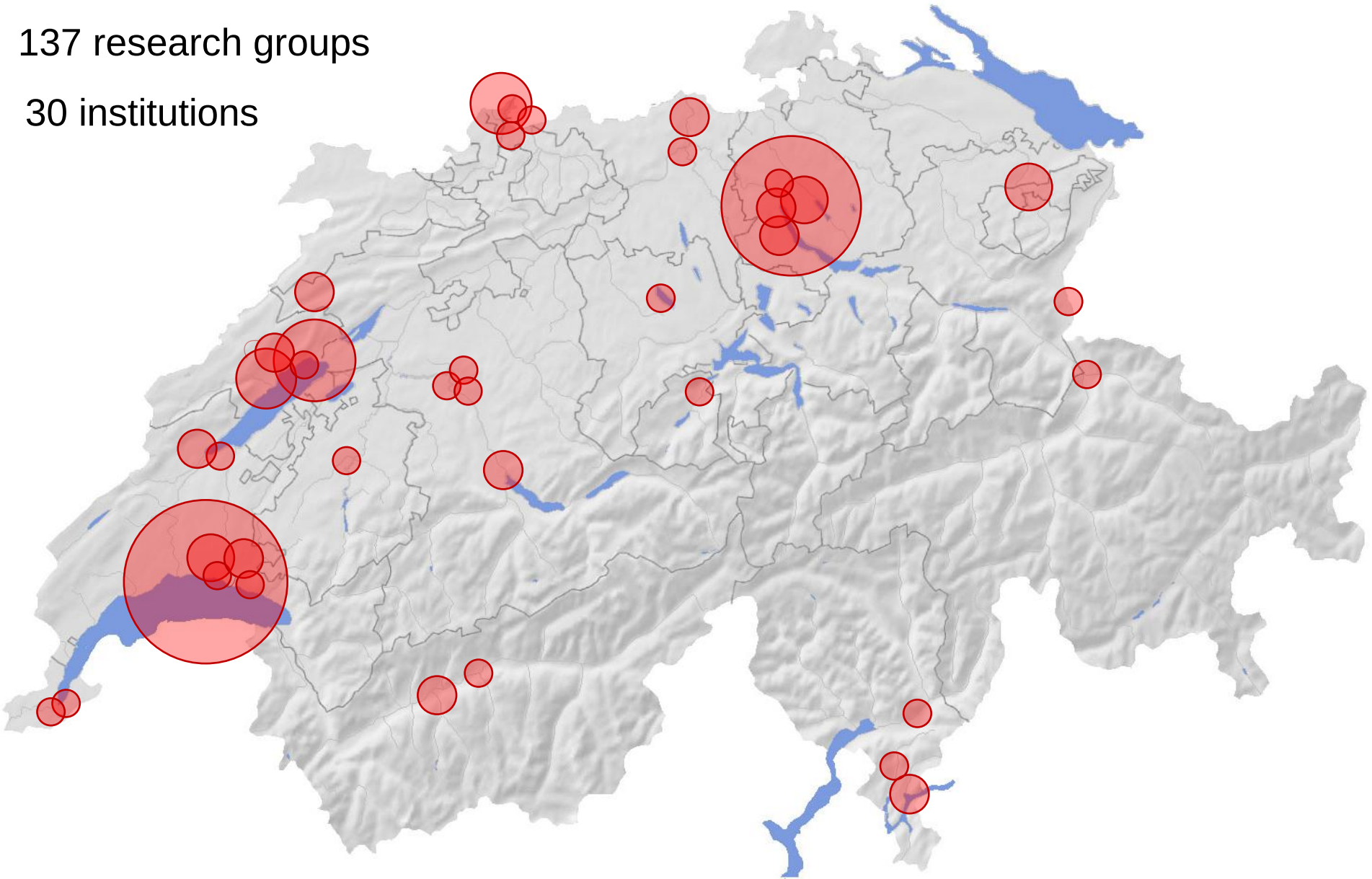
137 research groups

30 institutions



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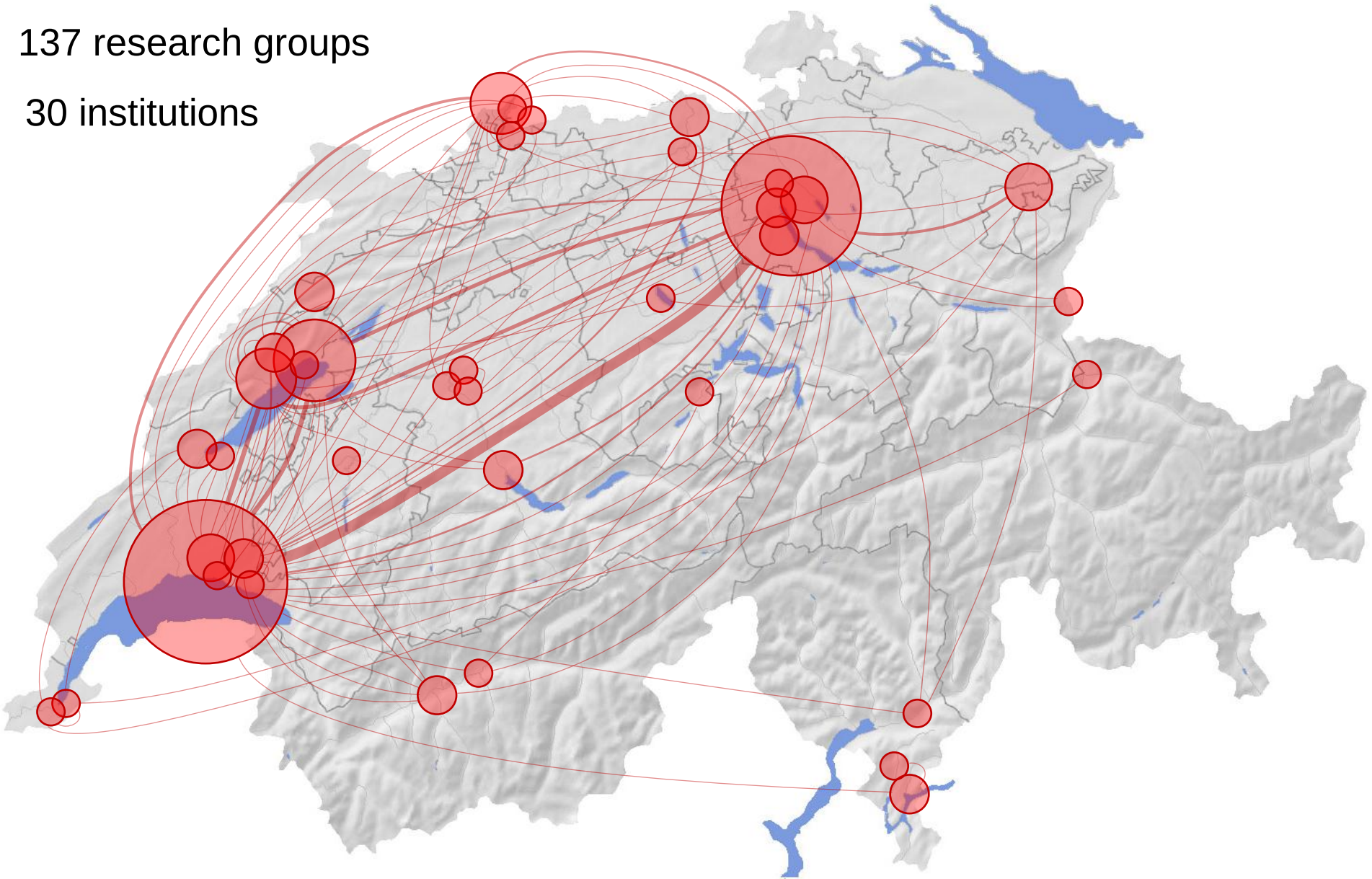

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Dissemination: conferences

183 presentations of Nano-Tera projects given in conferences worldwide in 26 countries

(as of Oct. 2010)

Nano-Tera.ch: key figures

- **52** projects (19 RTD – 15 NTF – 18 ED)
- **30** research institutions involved as Co-PIs
- **137** research groups
- ~**600** researchers
- ~**120** PhD thesis supported

- Over **100** papers published *(as of Oct. 2010)*

- Total nano-tera.ch allocation:
  - **60M CHF / 50M €** in cash
  - **60M CHF / 50M €** in matching money
  - **1.8M CHF / 1.5M €** for matching funds of technical universities

Enabling technologies

- Micro/Nano-electronics
- Sensors
- MEMS / NEMS
- Software, information & communication

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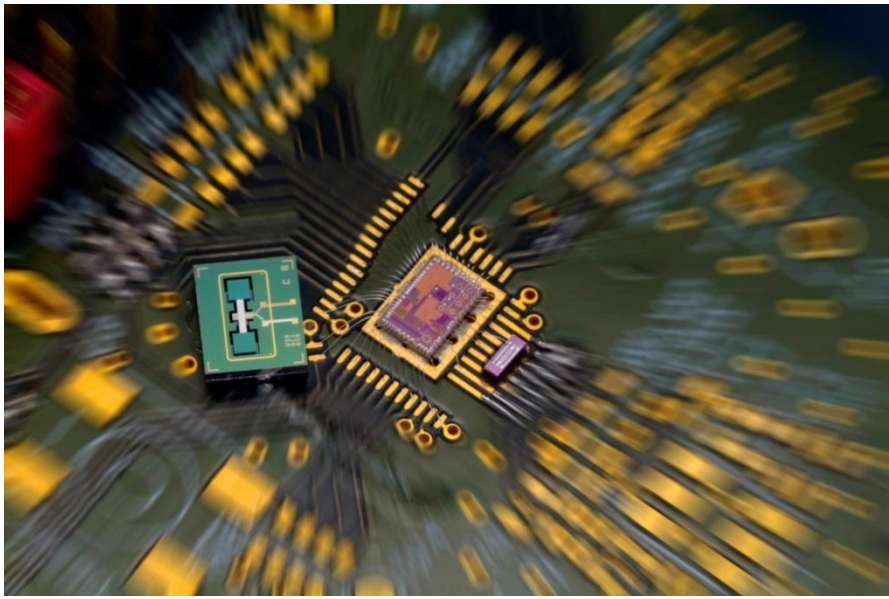
Micro/Nano-electronics

Search for new applications of semiconductor technologies with extended functionalities & combined technology-system innovation…

More than Moore avenue

- Realizing sensors & M/NEMS
  + integrating them with micro/nano-electronics circuits
- Designing new devices in new technologies
  (e.g. silicon nanowires & carbon nanotubes)
  to leapfrog extremely downscaled CMOS



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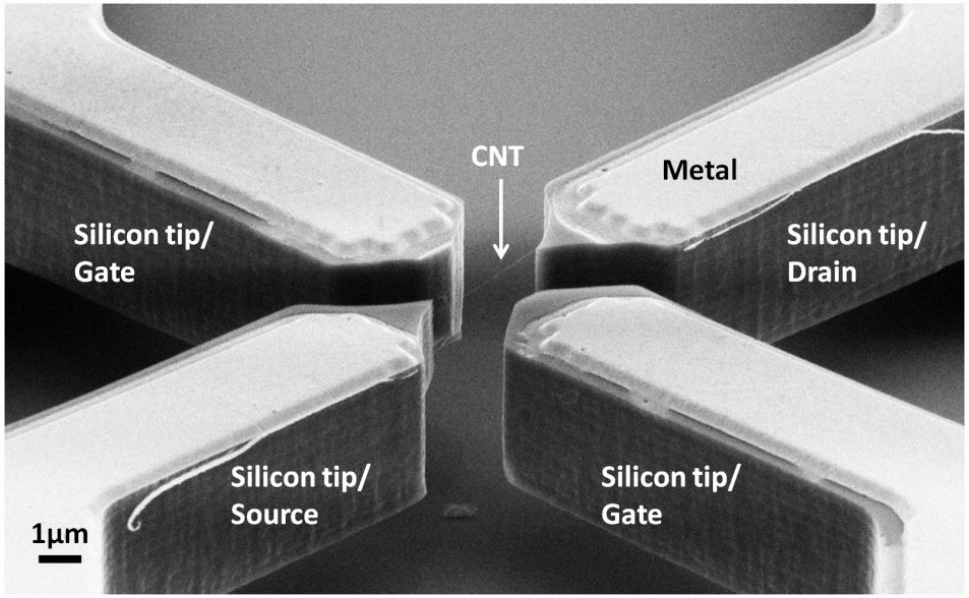
MEMS / NEMS

Micro/nano electro-mechanical systems:

➡ provide interface functions (sensors & actuators) between micro/nano-electronics & environment

- Key example: macro-molecular carbon nanotubes
- Enabling devices for numerous tera-scale systems & useful as energy sources
- Parts of micro-/nano-electronics systems (systems-in-package), providing functions such as…

  - resonators
  - filters
  - switches
  - RF components



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Software, information & communication

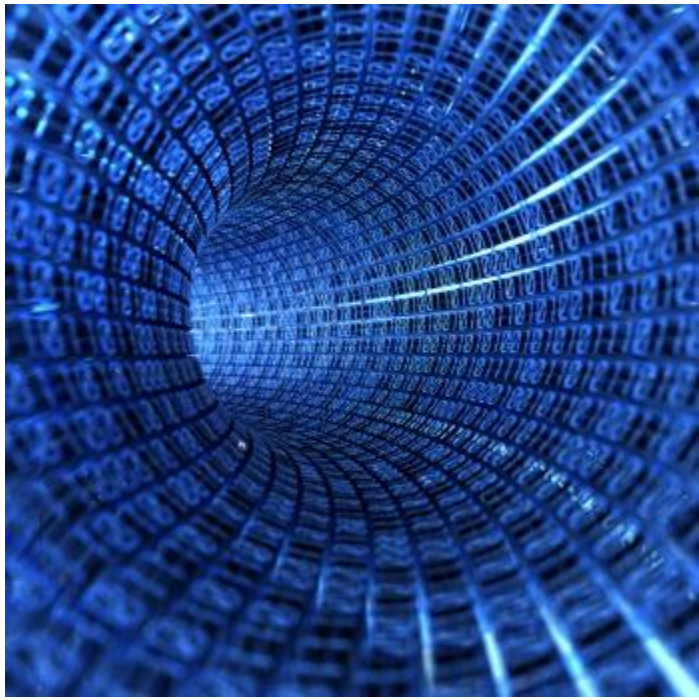
Tera-scale distributed embedded systems:

Huge sets of nodes performing
information acquisition, processing & communication
at high speed & low power consumption

Tera-scale distributed information processing systems generate huge amounts of data, to be processed, stored & transmitted over large-scale heterogeneous wireless networks

Challenge

Provide safe and reliable results from large scales of small and unreliable components



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Sensors

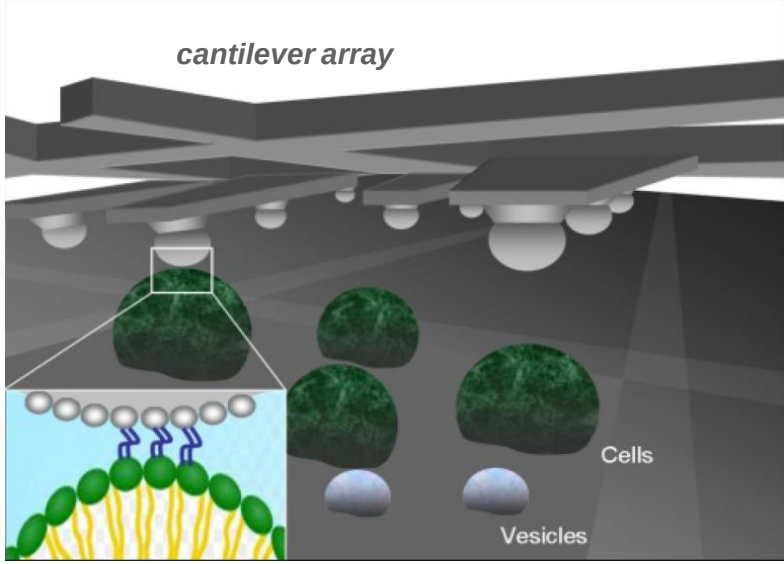
Creating systems for environmental & biomedical applications…

➡ requires new sensors & their integration with micro/nano-electronic technology

Until now... sensors (chemical gas / liquid / glucose-level sensors…)
often developed as stand-alone devices, with few integrated applications

Some new challenges

- ultra-low powered cantilever or nanotube arrays
- single photon detectors
- cell- and microfluidics-based chips
- bio-compatible coatings



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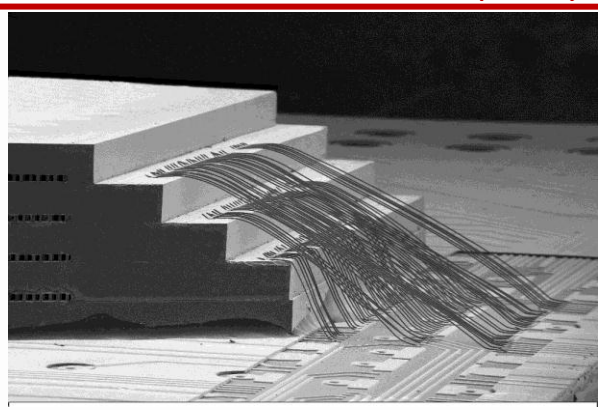
CMOSAIC

3D stacked architectures with interlayer cooling

John Thome (EPFL)



Contributing to the realization of a 3D stack of silicon chips with a functionality per unit volume that nearly parallels that of a human brain!

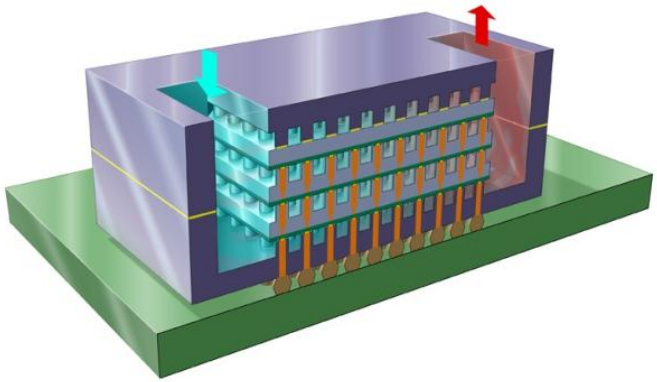
The key issue: heat needs to be removed !
[each layer dissipates 100-150 W/cm^2]

These 3D integrated circuits need novel electro-thermal co-design

Interdisciplinary problem approached at various levels:

- architecture
- microfabrication
- liquid cooling
- two-phase cooling
- nano-fluids

- So far: **26** publications – work presented in **17** major conferences
- Prof. John Thome: awarded the 2010 ASME Heat Transfer Memorial Award at the 14th International Heat Transfer Conference in part for his extensive research on microscale flow boiling.



Educational activity: D43D

Tutorial course:
Manufacturing, design and thermal issues in 3D integrated systems

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PlaCiTUS

Platform circuit technology underlying heterogeneous nano and tera systems

Qiuting Huang (ETHZ)

In the last decades: downscaling of CMOS technologies has led to higher transistor density & speed performance

… but… at the cost of severe degradation in quality metrics!

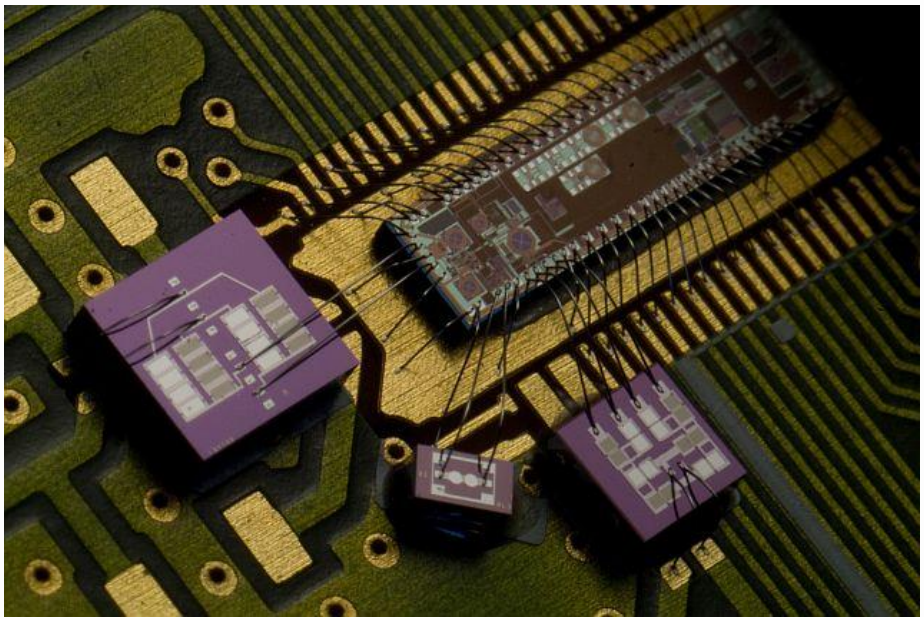
- Increase of process parameter variations
- Degradation of component matching
- Increase of leakage currents
- Stronger short channel effects
- Ever lower supply voltage

Profound structural changes are required !

Goal here: **Build a platform for the design of complex mixed-signal system-on-chip in nano-scale CMOS for health, security & environment applications**

Demonstrators in the following areas

- Generic sensor interface/data acquisition
- Passive telemetry
- Wireless body area networks
- Wireless sensor networking
- Wireless wide area networks



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LiveSense

Cell-base autonomous biosensing microsystem

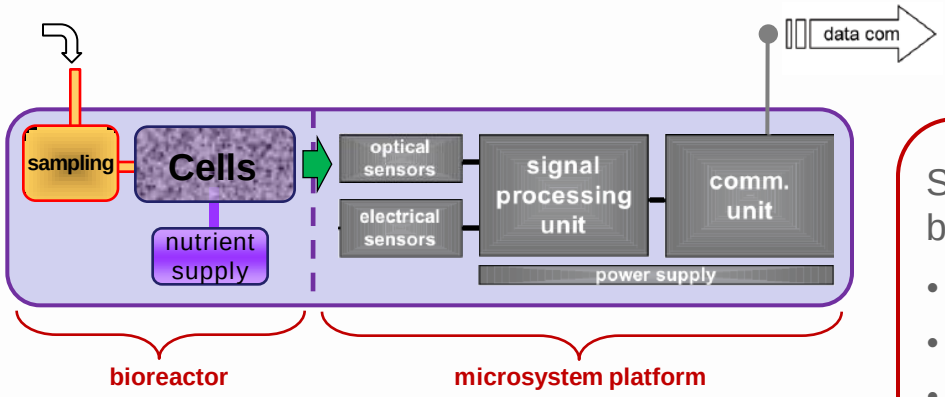
Philippe Renaud (EPFL)

Environmental monitoring – warning system for the health of a biotope

➡ need a set of autonomous remote nodes able to locally collect samples and send information

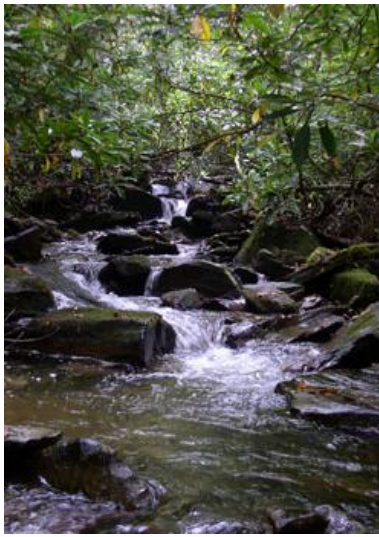
Cell-based biosensors provide a biologically relevant response to toxic compounds and mixtures

canary used as «biosensor» in coalmines



Strong interactions between partner teams:

- study of the cell models
- development of microbioreactor
- secondary sensors to detect the cell response
- integration of a demonstrator to be deployed in a river



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IrSens

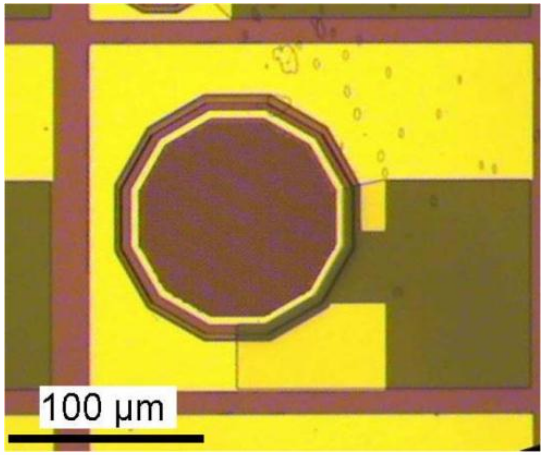
Integrated sensing platform for gases and liquids in the near and mid-infrared range

Jérôme Faist (ETHZ)

Versatile sensing platform based on optical spectroscopy

high sensitivity for both gases & liquids • low price • low power consumption

Semiconductor optical sources & detectors ➡ Vertical Cavity Surface Emitting Laser
Quantum Cascade Laser + Detector

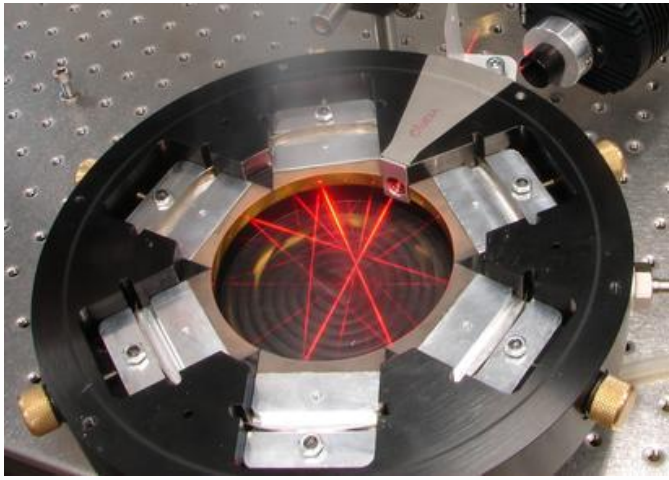


Optical sensing in the gas phase

Human breath analysis

QCLs as powerful light source in the mid-infrared

Detection of a bacteria with isotopic ratio measurements in exhaled CO_2



Optical sensing in the liquid phase

Multi wavelength semiconductor laser source (mid-infrared QCLs & near-infrared VCSELs)

Detection of drugs & doping agents in human fluids

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CabTuRes

Low-power nano-sensors based on tunable CNT electro-mechanical resonators

Christofer Hierold (ETHZ)

Carbon Nanotubes (CNTs): unique structural / mechanical / electronic properties

Small mass & high stiffness ➡ when doubly clamped, huge resonant frequencies are reachable (>1GHz)

Demonstrate concepts for ultra-low power, highly miniaturized functional blocks for sensing & electronics…

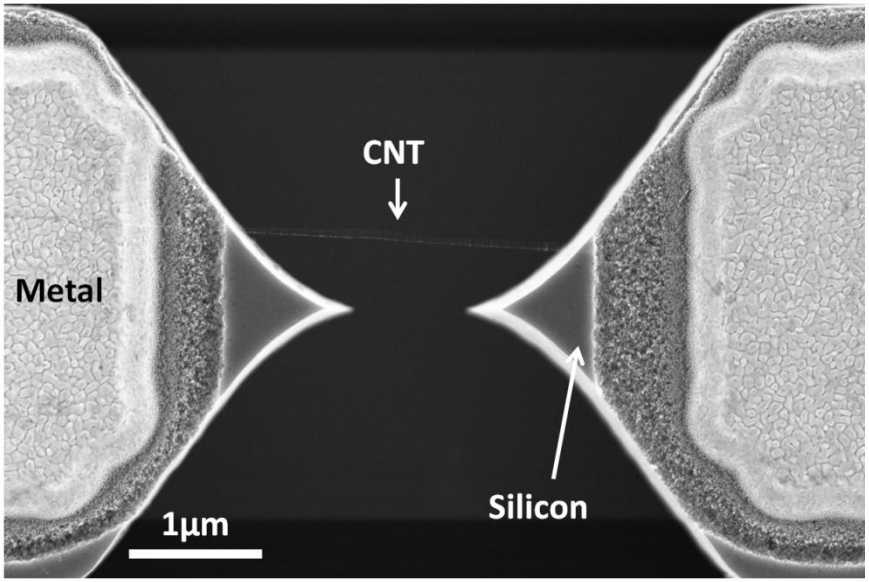
Mass balances for sensing

Mass loading creates shift in resonant frequency – with huge sensitivity to tiny mass changes

➡
- Measure gas molecule densities
- Weigh nano bodies (proteins, viruses…)
- Measure strain/stress/pressure…

Electronics applications

- tunable RF voltage controlled oscillators
- NEMS filters & detectors



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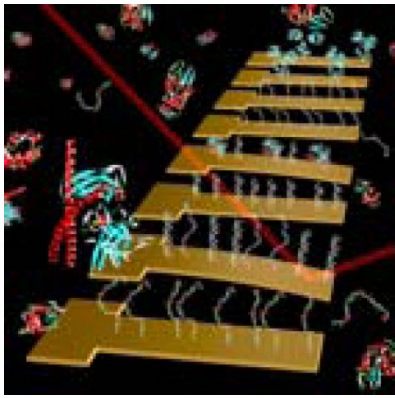
PATLiSci

Probe array technology for life science applications

Harry Heinzelmann (CSEM)

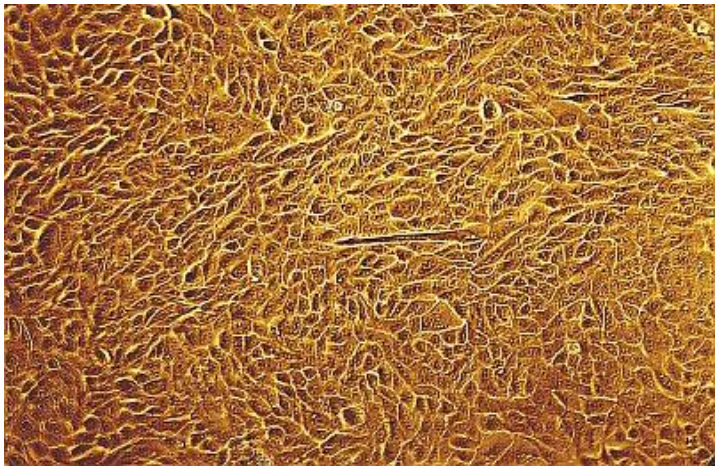


Micro-mechanical force sensors (micro-cantilevers) exhibit properties that make them usable as highly sensitive probes to detect molecular species adsorbed to them

➡ Develop probe array techniques for life science applications, particularly in the context of cancer research

Indeed, cancer spread in the body depends on…
- ➢ stiffness of cancer cells
- ➢ adhesion forces of cancer cells to other cells

Nano-mechanical properties of **cells** & cell-cell interactions are therefore crucial in cancer research!



Expected breakthroughs

- ➢ Advancement of personalized medical diagnostics
- ➢ Direct impact on pharmacological research & cell-based drug screening

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ULP-Logic

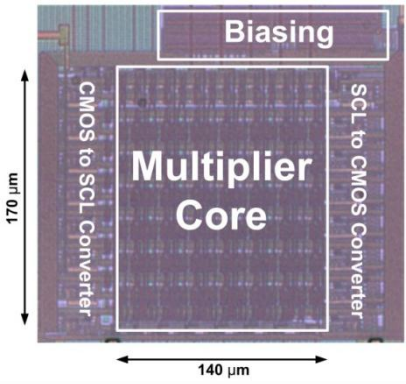
Sub-threshold source-coupled logic circuits for ultra low power applications

Yusuf Leblebici (EPFL)

Ultra-low power digital systems crucial in many modern applications

In sub-threshold MOS devices… lower speed of operation
power consumption difficult to control

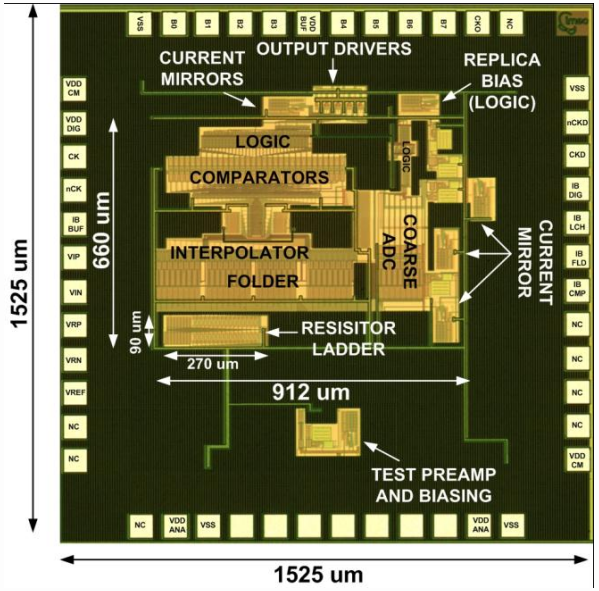
Here: sub-threshold **source-coupled logic** circuits as a new family of ultra-low power circuits capable of operating at relatively high frequencies



Linear adjustment of power consumption and speed of operation over a wide range

➡ Large potential for implementing ultra low power digital systems!

Computing with leakage currents!



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Application areas

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Wearable embedded systems

Providing the gateway between humans and information systems…

Characteristics

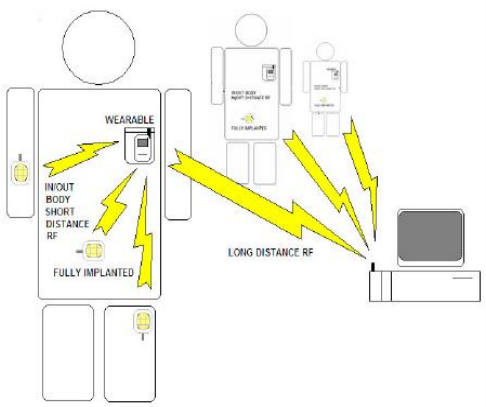
- Long periods of autonomy
- Complex functionality
- Substantial computational power

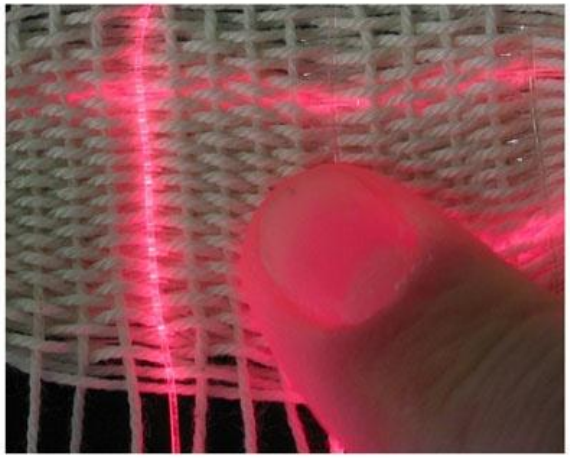
Application targets

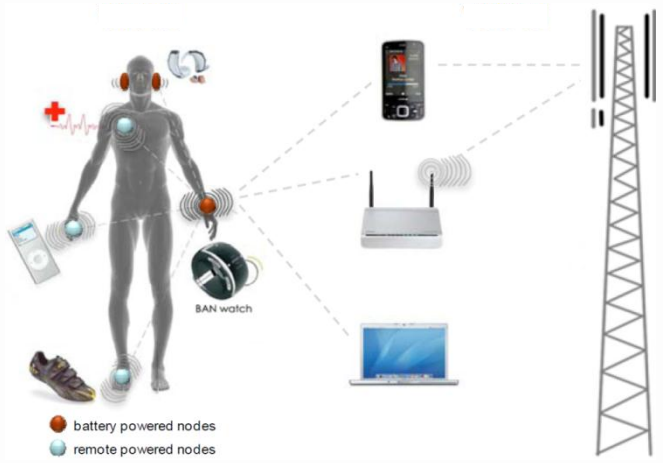
- Monitoring of professional & recreational sportsmen
- Diagnosis and/or treatment of patients
- Enhancement of security & safety of individuals

➡ personalized **health management**

through implanted devices – smart clothing – intelligent nutrition/drug monitoring & delivery systems…







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TecInTex

Technology integration into textiles: empowering health

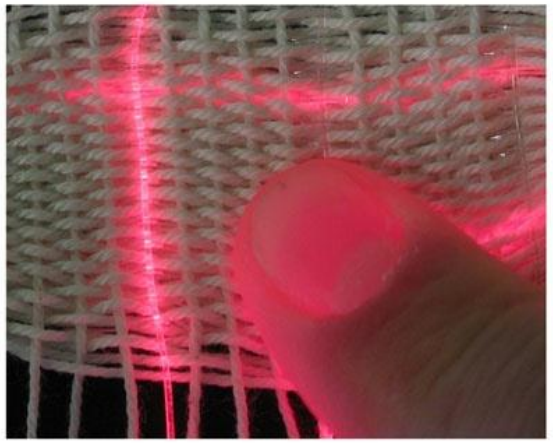
Gerhard Tröster (ETHZ)

Sensing capabilities close to the human body ➡ monitor activity, motion, health…

Incorporate built-in technological elements in our everyday textiles & clothes

Existing E-textiles: low processability, wearing comfort, washability…

➡ Goal: | get the crucial core modules to design & manufacture truly wearable functional clothes



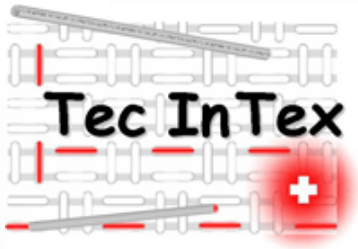
- electronic fibers ➡ point-to-point connection inside the fabrics
- optical fibers ➡ sensitive to changes in the contacting liquid env. (bio-sensing appl.)
- sensor yarns & stripes
- transducer between optical & electrical signals

Active near infrared spectroscopy sock

Peripheral vascular disease affects 30% of adults

Early detection possible (near IR spectroscopy), but conventional sensors are cumbersome

➡ Light wearable system in sock to monitor tissue oxygenation continuously & non-invasively



Intelligent underwear for paraplegic people

Pressure ulcers
big problem of paraplegic and bed ridden patients

➡ Build a comfortable device to detect the risk for pressure ulcers in order to enable preventive measures

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EMPA csem UniversitätsSpital Zürich Swiss Paraplegic Centre

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i-IronIC

Implantable/wearable system for online monitoring of human metabolic conditions

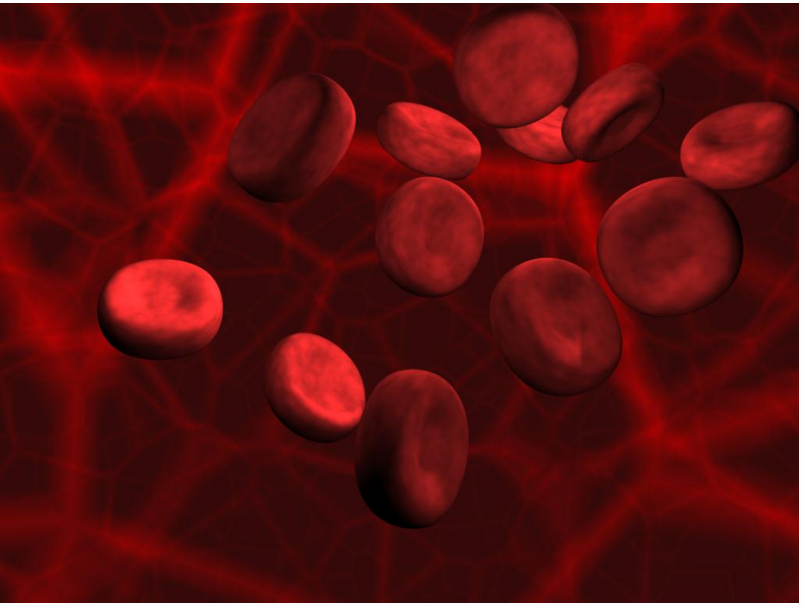
Giovanni De Micheli (EPFL)

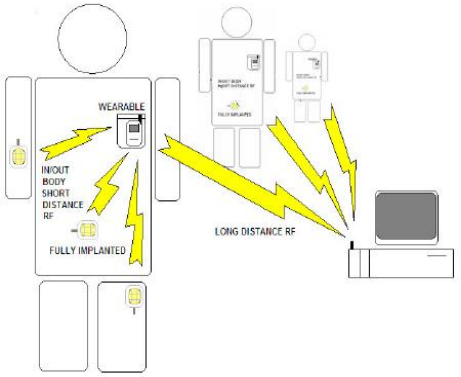
Goal: Study an innovative • multi-metabolites • highly integrated • fully implantable • real-time monitoring system for human metabolism

Currently available wearable systems for health monitoring:
no metabolites measurements! (only glucose monitoring for diabetic patients)

Many different molecules are crucial to monitor:

- lactate
- ATP
- cholesterol





Expected breakthroughs

- Fully implantable sensors system
- Multi-panel sensors to sense several metabolites (lactate, cholesterol, ATP, etc.) in parallel, in real-time
- New software algorithms for signal analysis
- New CMOS design for the fully-implanted, complex and low-consumption electronics for sensing and remote powering

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Ambient systems

Large-scale distribution of auto-configurable networks of miniature sensor nodes

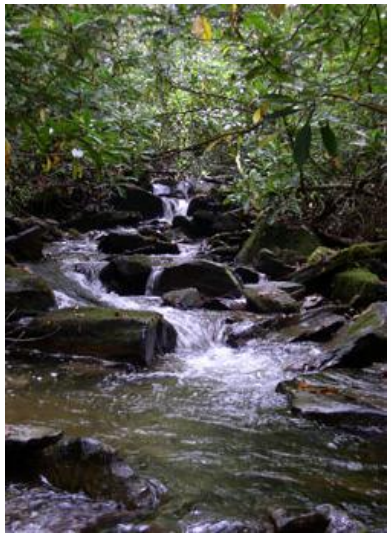
to sense – network – inform – actuate – interact with the physical environment, the devices or humans

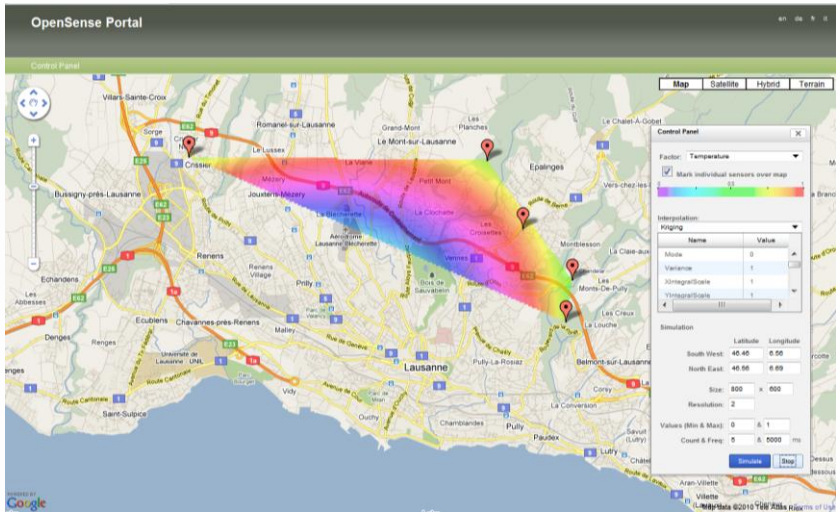
Next generation information technology, with devices that are…

- highly distributed
- networked
- heterogeneous
- largely self-organizing
- embedded into the environment

Application areas

- Environmental monitoring
- Smart buildings & workplaces
- Smart transportation systems
- Virtual-world applications





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OpenSense

Open sensor networks for air quality monitoring

Karl Aberer (EPFL)

Goal: **Address key challenges in communication & information systems for urban air quality monitoring**

Sensing infrastructure:

- Mobile sensor nodes on public buses & private mobile devices
- Wireless sensing and communication infrastructure

➡ open technology allowing for the integration of diverse sensors into a single environmental model

Ultimate goal

Provide an open & extensible platform
for monitoring air quality in real-time,
for better understanding environmental phenomena
& their effects

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X-Sense

Monitoring alpine mass movements at multiple scales

Lothar Thiele (ETHZ)

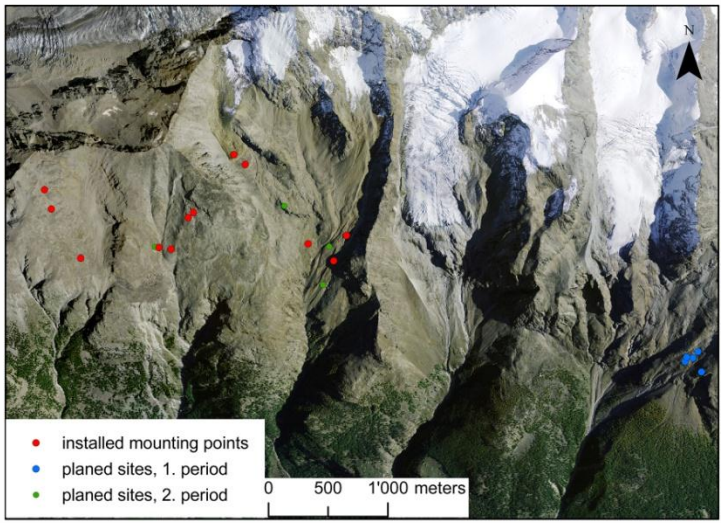
Global climate change:

Destructive geological processes make slopes unstable, inducing landslides

- Develop a monitoring & warning system for the spatial and temporal detection of newly formed hazards
- Extend the quantitative understanding of these systems and predictive capabilities

Main goals of the research

- Develop dependable wireless sensor technology for **environmental sensing under extreme conditions**
- **Integrate various sensing dimensions and scales**
- Extend the spatial scope from **local** measurements to **large-scale** information (derived from IN-SAR satellite remote sensing)
- **Applications**:
  Geophysical and climate-impact research,
  Early warning against landslides & rockfall



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Education & Dissemination activities

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Educational Activities

D43D	Manufacturing, design and thermal issues in 3D integrated systems *May 26-28, 2010*
MicroCool	Summer school on microscale cooling of 3D integrated systems *June 5-10, 2011*
NT summer school	Micro-Nano for large distributed systems *August 22-26, 2011*
WIMEMS	Doctoral school NAMIS 2011: micro- and nanosystems based technology for wireless applications in environment *September 12-13, 2011*
EASY	Educational workshops on energy efficient autonomous systems: a collaborative framework between Nano-Tera and Guardian Angels for a Smarter Planet December 2011
FEDAMaT	Nano-Tera workshop on future electronic design automation methodologies and tools

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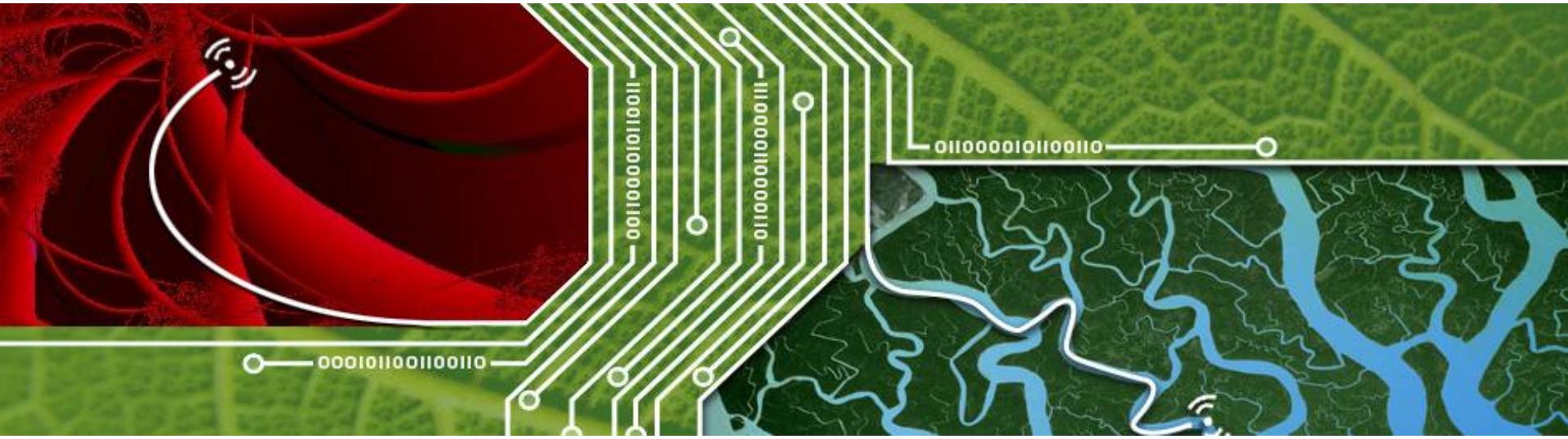

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