Confidential

ICT-2009.3.2-248603-**IP**

Modelling,Control and Management of Thermal Effects in Circuits of the Future

	WP no.	Deliverable no.	Lead participant
therminator	**WP8**	**D8.2.2**	**POLITO**

First report on dissemination activities

Prepared by	**Alberto Macii (POLITO)**
Issued by	**THERMINATOR WP8 Leader**
Document Number	**THERMINATOR/D8.2.2/v1**
Dissemination Level	**Confidential**
Date	**15/01/2011**

Document

Title	First report on dissemination activities
Type	Deliverable PU
Ref	D8.2.2
Target version	V1_1
Current issue	V1_1
Status	Released
File	D8.2.1.doc
Author(s)	Alberto Macii (POLITO)
Reviewer(s)	PCT
Approver(s)	PCT
Approval date	15/01/2011
Release date	25/01/2011

Distribution of the release

Dissemination level	PU
Distribution list	

History

Rev.	DATE	Comment
0.1	22-12-2010	Initial version
1.0	05-01-2011	Revised version, approved by all partners
1.1	25-01-2011	Check and ship out

This page was intentionally left blank.

Contents

1 Introduction

As mentioned in Deliverable D8.2.1, the objective of Task T8.2, whose first year of activity is summarized in this document, is to spread Europe-wide the knowledge gained during the execution of the THERMINATOR project. As initially planned and described in D8.2.1, the approach that was taken for achieving this goal consisted of three types of actions:

1. Set-up and maintenance of the THERMINATOR web-site, which will make available to the European design community, documents and reports describing technical and scientific achievements, information on training options, scientific publications, a mailing-list and a mechanism to create awareness of the THERMINATOR public events.
2. Publication of scientific articles in books, technical journals, conference and workshop proceedings with international scope and visibility.
3. Promotion of the R&D effort performed by the THERMINATOR Consortium through press releases in international, national and local/regional newspapers and magazines, as well as in international, national and regional/local events such as fairs and exhibits, emphasizing the fundamental role that EU funding has on the development of nanoelectronics research in Europe.

Concerning the THERMINATOR web-site, a specific Task is dedicated to its creation, updating and maintenance (Task T8.1). Details on the chosen web-site structure and architecture, as well as access statistics are given in Deliverable D8.1.1. Therefore, this item of the dissemination plan is no further discussed in this document.

The dissemination activities regarding publication of articles and papers, as well as additional advertisement initiatives such as participation to conferences, fairs and other public events, are surveyed, on a partner-by-partner basis, in details in Section 2 of this document. In particular, a common reporting template was defined in order to allow the Project Officer and the Reviewers to easily identify the different kinds of actions that each involved partner has undertaken.

On the other hand, promotion of the THERMINATOR activities through press releases was undertaken at the Consortium level. Details on the performed actions are given in Section 3.

Section 4 gives details on the organization of a special half-day within an important international workshop (THERMINIC) on thermal-related research topics.

Finally, Section 5 provides a brief outlook of the dissemination initiatives that will take place in the second year of the project.

2 Dissemination Activities of Individual Partners

2.1 ST

Publications

G.Greco, S. Rinaudo,
"Automatic Layout Optimization of Power Discrete Devices Using Innovative Distributed Model Techniques"
ECMI 2010, Wuppertal, Germany, July 2010.

G.Bazzano, D. G. Cavallaro, G. Greco, A. Grimaldi, S. Rinaudo,
"2D Thermal Propagation Analysis of Discrete Power Devices Based on an Innovative Distributed Model Technique and CAD Framework",
THERMINIC 2010, Barcelona, Spain, October 2010.

2.2 NXP

Publications

M. Braccioli, A. Scholten, G. Curatola, E. Sangiorgi, and C. Fiegna,
Proc. Ultimate Integration on Silicon Conf., 81 (2010).

A.J. Scholten, G.D.J. Smit, R.M.T. Pijper, L.F. Tiemeijer, A. Mercha, and D.B.M. Klaassen,
IEDM Tech. Digest, 190 (2010).

D.L. John, F. Allerstam, T. Roedle, S.K. Murad, and G.D.J. Smit,
IEDM Tech. Digest, 186 (2010).

2.3 POLITO

Publications

Calimera A., Bahar R.I, Macii E., Poncino M.,
"Temperature-Insensitive Dual-Vth Synthesis for Nanometer CMOS Technologies Under Inverse Temperature Dependence,"
IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, , 2010, Vol. 18, ISSN: 1063-8210

Calimera A., Bahar R.I, Macii E., Poncino M.,
"Dual-Vt assignment policies in ITD-aware synthesis,"
MICROELECTRONICS JOURNAL, 2010, ISSN: 0959-8324**2010**

Calimera A., Bahar R.I, Macii E., Poncino M.,
"Temperature-Insensitive Dual-Vth Synthesis for Nanometer CMOS Technologies Under Inverted Temperature Depedence,"
IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 2010, Vol. 18, ISSN: 1063-8210

Calimera A., Macii A., Macii E., Poncino M., Rinaudo S.,
"THERMINATOR: Modeling, control and management of thermal effects in electronic circuits of the future,"
THERMINIC 2010, Barcelona, Spain, October 2010.

Caldera M., Calimera A., Macii A., Macii E., Poncino M.,
"Minimizing temperature sensitivity of dual-Vt CMOS circuits using simulated-annealing on ISING-like models,"
THERMINIC 2010, Barcelona, Spain, October 2010.

Participation to Conferences and Workshops

DATE-10: IEEE Design Automation and Test in Europe
Dresden, Germany, March 2010.

GLSVLSI-10: ACM/IEEE Great Lakes Symposium on VLSI,
Providence, RI, May 2010.

ISCAS-10: IEEE International Conference on Circuits and Systems,
Paris, France, May 2010.

DAC-10: ACM/IEEE Design Automation Conference,
Anaheim, CA, June 2010.

ISLPED-10: ACM/IEEE 2010 International Symposium on Low Power Electronics and Design, Austin, TX, August 2010.

PATMOS-10: IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation, Grenoble, France, September 2010.

THERMINIC 2010: International Workshop on Thermal Investigation of ICs and Systems,
Barcelona, Spain, October 2010.

ICCAD-10: IEEE/ACM International Conference on Computer-Aided Design,
San Jose, CA, November 2010.

Other presentations (courses, seminars, etc.)

Macii E.,
"Power Analysis and Low Power Design",
ALARI Master Course,
Lugano, Switzerland, January 2010.

Macii E.,
"Leakage power minimization and thermal effects compensation in digital nanometer CMOS circuits",
First IEEE CASS Summer School, Physical Design of Reliable Circuits,
Porto Alegre, Brazil, January 2010.

Macii E.,
"Thermal-Aware Design: Challenges and Advanced Solutions",
Microelectronics Summer School,
Florianopolis, Brazil, May 2010.

Calimera A., Macii A., Macii E., Poncino M.,
"Modeling, design and CAD for low-leakage nanometer CMOS circuits and systems",
Conference Tutorial,
ISCAS-10: IEEE International Conference on Circuits and Systems,
Paris, France, May 2010.

Atienza D., Ayala J.L., Calimera A.,
"Thermal Modeling and Management for 2D/3D MPSoC Platforms",
Conference Tutorial,
ICECS 2010: IEEE International Conference on Electronics, Circuits, and Systems,
Athens, Greece, December 2010.

2.4 OFFIS

Publications

S. Rosinger, M. Metzdorf, D. Helms and W. Nebel,
"Behavioral-Level Thermal- and Aging-Estimation Flow",
Proc. of 12th Latin-American Test Workshop (LATW), 2011.

2.5 BME

Publications

A. Timár, A. Poppe, M. Rencz,
"A Novel Approach of Logi-thermal Simulation Methodology and Implementation for ASIC Designs",
Proceedings of the 17th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES'10), Wroclaw, Poland, June 2010.

A. Timár, Gy. Bognár, A. Poppe, M. Rencz,
"Electro-thermal co-simulation of ICs with runtime back-annotation capability",
THERMINIC 2010, Barcelona, Spain, October 2010.

A. Timár, Gy. Bognár, A. Poppe, M. Rencz,
"Electro-thermal co-simulation of ICs with runtime back-annotation capability",
I*nternational Journal of Microelectronics and Computer Science*
Volume 1, Number 3, 2010, pp. 287-292, ISSN 2080-8755

2.6 IFX

Other presentations (courses, seminars, etc.)

K. von Arnim,
"Device options for low power technologies and SOC implementation",
Technology Short Course, Symposium on VLSI Technology, Honolulu, June 2010.

2.7 FHG

Publications

R. Jancke, A. Wilde, R. Martin, S. Reitz,
"Modeling and Simulation of Electro-Thermal Interaction Effects in Electronic Circuits and Devices",
Fraunhofer Multiphysics Konferenz 2010, Bonn, Germany, June 2010.

R. Jancke, A. Wilde, R. Martin, S. R. P. Schneider,
"Simulation of Electro-Thermal Interaction.",
Electronics System Integration Technology Conference, ESTC 2010, Berlin, Germany, September 2010.

2.8 CSEM

Other presentations (courses, seminars, etc.)

C. Piguet,
"Low-Power Systems-on-Chips", *ENSEIRB*, Bordeaux, France, January 2011.

2.9 MUN

Publications

Colaci A., Boarin G., Roggero A., Civardi L., Roma C., Ripp A., Pronath M., Strube G.
"Systematic Analysis and Optimization of Analog/Mixed-Signal Circuits Balancing Accuracy and Design Time",
SBCCI 2010 23rd Symposium on Integrated Circuit and Systems Design,
Sao Paolo, Brazil, September 2010.

Conte A., Di Martino A., Miccichè M, Roma C.,
"Extraction Methods of VHDL/VerilogA Models for Analog Blocks, Usable Inside Time Domain Simulations",
MUGM2010 - MunEDA User Group p Meeting 2010, Munich, Germany, October 2010.

Trautner U., Geden B., Pronath M.,
"Synopsys Custom and Analog Mixed-Signal Overview & MunEDA WiCkeD Integration",
MUGM2010 - MunEDA User Group p Meeting 2010, Munich, Germany, October 2010.

Daglio P., Raciti E., Roma C., Geden B.,
"Advanced WiCkeD usage: a methodology for process variations impact analysis on huge circuits taking advantages of Synopsys CustomSim XA",
MUGM2010 - MunEDA User Group p Meeting 2010, Munich, Germany, October 2010.

2.10 CEA-LETI

Mansouri, I. et al,
"A run-time distributed cooperative approach to optimize power consumption in MPSoCs",
SOCC'10: the 23rd IEEE International SOC Conference. Nevada, USA.

Mansouri, I. et al.,
"An embedded Game Theoretic approach for energy management in NoC-based SoC",
ISVLSI: proceedings of the 2010 IEEE Computer Society Annual Symposium on VLSI,
Lixouri, Greece.

Mansouri, I. et al, "On Energy Management in NoC-based System-on-Chip",
Journal of Low Power Electronics, Vol. 6 N° 4, December 2010.

3 Dissemination Through Press Releases

At the beginning of the project, ST took the lead on the preparation of the text to be used in press releases related to the THERMINATOR project. The text went through a number of revisions among the partners of the Consortium, and the consensus on the final content was reached at the beginning of March 2010.

The document was finally released to the press by the ST press office on April the 1st, 2010. Also available in the THERMINATOR web-site (http://www.fp7-therminator.org/drupal/): the announcement delivered to the media is shown hereafter:

THERMINATOR project warms efforts to cool semiconductor design solutions

Catania, April 1st 2010 -- The partners in a new EU-funded research project today announced details of the multinational/multidisciplinary program: "THERMINATOR – Modeling, Control and Management of Thermal Effects in Electronic Circuits of the Future". This 3-year project is designed to maintain the strong positions that Europe's semiconductor and electronics equipment companies have achieved in highly competitive application areas such as automotive systems and factory automation where the semiconductor devices are often required to work under harsh conditions with temperatures in excess of 100°C.

Thermal effects have always been important in determining the performance, cost and reliability of both the device itself as well as for the application in which it is used. For example, packages that are able to sustain high temperatures are expensive, as are heat-sinks and cooling systems. In addition, high operating temperatures tend to cause performance degradation or even malfunctioning of circuits and components, thus reducing the reliability of the end application. For this reason, models that predict the thermal characteristics of semiconductor devices have long been included in the EDA (Electronic Design Automation) software that chip manufacturers use to design their devices. However, these existing design tools are not sufficient in terms of being able to handle the new materials and extremely small structures that will be required in future applications and technologies where heat/power management is of vital importance.

"European companies have achieved strong positions in important markets such as automotive and industrial electronics", said Salvatore Rinaudo, Therminator project coordinator and Industrial and Multisegment Sector CAD R&D Director at STMicroelectronics. "To enable them to fully exploit the opportunities opened up by the semiconductor technologies of the future, including CMOS and alternatives to CMOS, new, thermal-aware design paradigms are required."

The project will draw on the complementary expertise of industrial partners (semiconductor manufacturers and EDA suppliers), research institutions and universities to meet three key goals:
1) To devise innovative thermal models, usable at different levels of abstraction, and to interface/integrate them into existing simulation and design frameworks;
2) To develop new, thermal-aware design solutions, customized for the different technologies and application domains of interest;
3) To enhance existing EDA solutions via thermal-aware add-on tools that will enable designers to address temperature issues more effectively using their existing design flows.

The total cost of the project is €11M, part of which will be contributed by the European Union under the Information and Communication Technologies (ICT) theme of the Seventh Framework Programme (FP7).

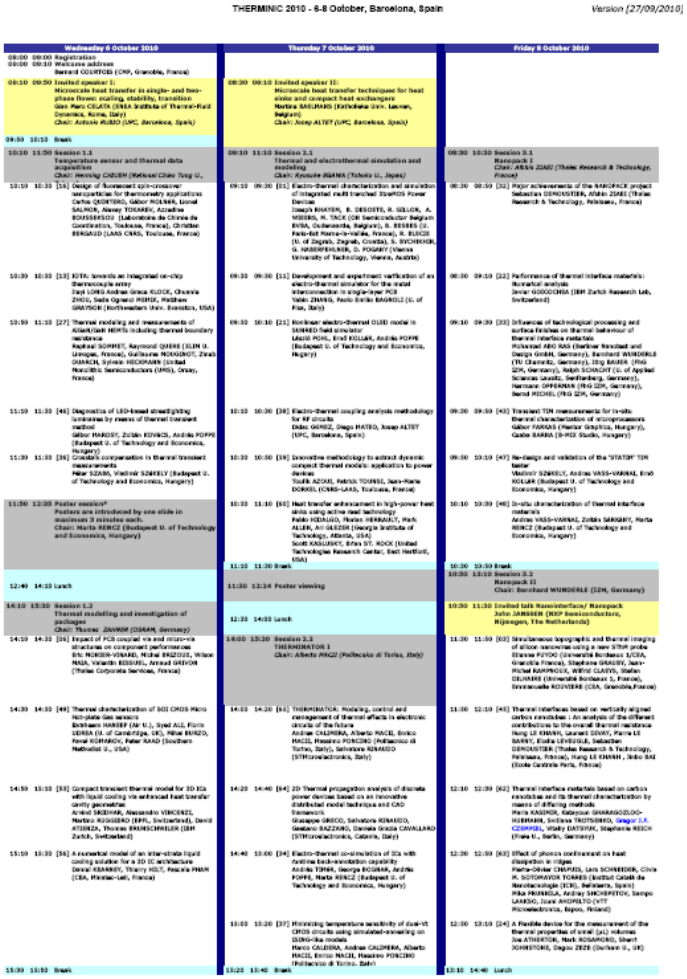
The partners and locations involved in the project are: STMICROELECTRONICS (Italy), INFINEON TECHNOLOGIES (Germany), NXP SEMICONDUCTORS (The Netherlands and Germany), ChipVision Design Systems AG (Germany), Gradient Design Automation, Incorporated (United States), MUNEDA GmbH (Germany), SYNOPSYS, Inc. (Armenia and Switzerland), BUDAPESTI MUSZAKI ES GAZDASAGTUDOMANYI EGYETEM (Hungary), CSEM CENTRE SUISSE D'ELECTRONIQUE ET DE MICROTECHNIQUE SA (Switzerland), FRAUNHOFER-GESELLSCHAFT ZUR FOERDERUNG DER ANGEWANDTEN FORSCHUNG E.V (Germany), IMEC (Belgium), CEA LETI (France), OFFIS e.V. Germany, POLITECNICO DI TORINO (Italy), ALMA MATER STUDIORUM-UNIVERSITA DI BOLOGNA (Italy)

4 Dissemination Through Dedicated Workshop Special Session

THERMINIC (International Workshop on Thermal Investigation of ICs and Systems) Workshops are a series of events to discuss the essential thermal questions of microelectronic microstructures and electronic parts in general. In particular, **THERMINIC 2010** (http://cmp.imag.fr/conferences/therminic/therminic2010) addressed in addition to the "traditional" thermal management problems, also stress and thermal-stress-related-reliability issues, both in micro- and opto-electronics fields. These issues, including various nanotechnology applications, are of significant importance and of high interest to the engineering community engaged in the field of thermal phenomena in "high-tech" systems.

In **THERMINIC 2010** (6-8 October 2010, Barcelona, Spain), THERMINATOR partners have organized a special half-day dedicated to disseminate the project results to the thermal management community. This special session, chaired by Prof. Alberto Macii from Politecnico di Torino, consisted of six technical papers strictly related with the research topics followed and developed within the THERMINATOR project.

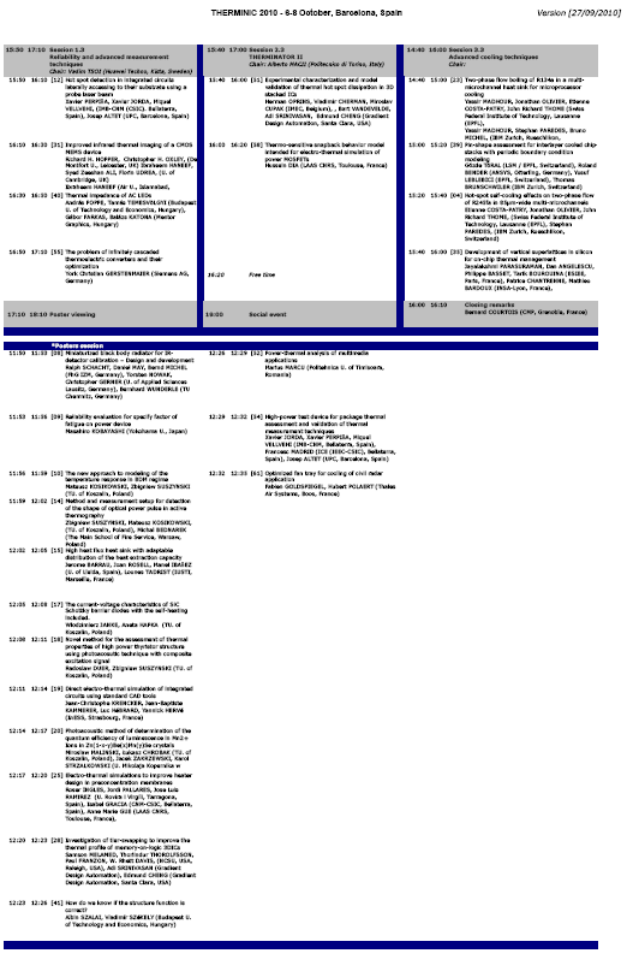
The technical program is shown hereafter and can be found at this url: http://cmp.imag.fr/conferences/therminic/therminic2010/Therminic10_Technogram.pdf


THERMINIC 2010 - 6-8 October, Barcelona, Spain Version [27/09/2010]

Wednesday 6 October 2010

Thursday 7 October 2010

Friday 8 October 2010


THERMINIC 2010 - 6-8 October, Barcelona, Spain Version [27/09/2010]

5 Dissemination Plan for Second Year

The dissemination activities for the second year of the project will continue along the same lines followed so far. The number of publications, as well as the participation of partners to different kinds of dissemination events (e.g., conferences, symposia, workshops, exhibits, forums, fairs) is expected to increase as the research and development work of the project will progress, as the material available for dissemination will naturally grow and become more stable.

A detailed dissemination plan (updated) will be described in the deliverable D8.2.3 expected at month M18.

As a final remark, all partners involved in R&D activities have renewed and reinforced their full commitment to the dissemination of the THERMINATOR results to the international community; a report summarizing the work performed in the second year of the project will be filed by month M24 (Deliverable D8.2.4).