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Second report on dissemination activities

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Contents

1 Introduction

The objective of Task T8.2, whose second year of activity is summarized in this document, is to spread Europe-wide the knowledge gained during the execution of the THERMINATOR project. Due to the good results obtained during the first year of the project, the THERMINATOR partners decided to follow the same guidelines used for the first year, thus implementing the same actions: (i) Maintain the THERMINATOR web-site, (ii) publication of scientific articles in books, technical journals, conference and workshop proceedings, (iii) publication of press releases in international, national and local/regional newspapers and magazines, as well as in international, national and regional/local events such as fairs and exhibits

The dissemination activities regarding publication of articles and papers, as well as additional advertisement initiatives such as participation to conferences, fairs and other public events, are surveyed, on a partner-by-partner basis, in details in Section 2 of this document. In particular, a common reporting template was defined in order to allow the Project Officer and the Reviewers to easily identify the different kinds of actions that each involved partner has undertaken.

Section 3 gives details on the organization of two special half-days within an important international workshop (THERMINIC) on thermal-related research topics.

Section 4 describes the actions taken by partners for promoting the THERMINATOR activities through press releases.

Finally, Section 5 provides a brief outlook of the dissemination initiatives that will take place in the third year of the project.

2 Dissemination Activities of Individual Partners

2.1 ST

Publications

Paolo *Magnone, Claudio Fiegna, Giuseppe Greco, Gaetano Bazzano, Enrico Sangiorgi, Salvatore Rinaudo*, "**Modeling of Thermal Network in Silicon Power MOSFETs**", Proceedings of the IEEE 12th ULIS 2011, 14-16 March 2011, Cork, Ireland

G.Bazzano, D. G. Cavallaro, G. Greco, A. Grimaldi, S. Rinaudo "**Stress and Reliability of Power Devices: an Innovative Thermal Analysis Approach to Predict a Device's Lifetime***", PCIM Europe 2011, Nuremberg, 17-19 may 2011.*

G.Bazzano, D. G. Cavallaro, G. Greco, "**An Analog Behavioral Thermal Macro-model Aimed at Representing an Elementary Portion of a Discrete IGBT Power Device***",* Proceedings of the IEEE 17th THERMINIC 2011, Paris (France), Sep 27-29, 2011.

F. Moschella, G. Gangemi , E.Macii, M. Rencz, S.Rinaudo, **"The THERMINATOR Project: Midway Achievements and Perspectives",** Proceedings of the IEEE 17th THERMINIC 2011, Paris (France), Sep 27-29, 2011.

2.2 SYNOPSYS

Publications

Melikyan V., Durgaryan A., Petrosyan H. , Stepanyan A., "**Power Efficient, Low Noise 2-5GHz Phase Locked Loop**," Proceedings of the 31st international scientific-technical conference "Electronics and nanotechnology", Kiev, Ukraine, April 12-14, 2011.-pp. 66-71

Melikyan V., Poghosyan A., Durgaryan A., Petrosyan H., Simonyan M., "**Method of Parametrical Optimization of Multi-Core Processors,**" Proceedings of the 31st international scientific-technical conference "Electronics and nanotechnology", Kiev, Ukraine, April 12-14, 2011.-pp. 126-130

Melikyan V., Petrosyan H., Durgaryan A., Topisirović D., "**New Retention Flop Architecture with Phase Frequency Detection (PFD) Capabilities,**" Proceedings of the 55th Electronics, Telecommunications, Computers, Automatic Control and Nuclear Engineering (ETRAN) Conference, Banja Vrućica, Serbia, 2011.-P.EL4.2-1-4

Melikyan V., Durgaryan A., Petrosyan H., Topisirović D., "**A Fully Differential Phase-Frequency Detector Design for Low Noise Phase Locked Loop Applications**," Proceedings of the 55th Electronics, Telecommunications, Computers, Automatic Control and Nuclear Engineering (ETRAN) Conference, Banja Vrućica, Serbia, 2011.-P.EL4.3-1-4

Roldman R., Melikyan V., Babayan E., "**Method of Electro-Thermal Co-Simulation of Integrated Circuits**," Proceedings of the 8th International Conference of "Semiconductor Micro- and Nanoelectronics", Yerevan, Armenia, 2011.-P.207-213

*Melikyan V., Durgaryan A., Petrosyan H., Melikyan N., "***Automatic PLL Activation Mechanism from Power Gated State**," Proceedings of the 8th International Conference of "Semiconductor Micro- and Nanoelectronics", Yerevan, Armenia, 2011.-P.214-217

Melikyan V., Eminyan N.S., Chobanyan S.G., Beglaryan N.H., "**Design Method of Low-Leakage Hybrid 9T-SRAM**," Scientific journal of National Academy of Science and State Engineering University of Armenia. Vol. 64, N 3, Yerevan, Armenia, 2011.- pp. 265-274

Melikyan V., Durgaryan A., "**Programmable Current Biasing for Low Noise Voltage Controlled Oscillators**," Proceedings of IEEE East-West Design & Test Symposium (EWDTS'11), Sevastopol, Ukraine, 2011.-P.47-50

Melikyan V., Roldman R., Babayan E., "**Digital Circuits Verification with Consideration of Destabilizing Factors**," Proceedings of the 6th IEEE International Design and Test Workshop (IDT) in Conjunction with IEEE International Conference on Electronics, Circuits and Systems (ICECS), Beirut, Lebanon, 2011.-P.93-98

Participation to Conferences and Workshops

International conference "Moscow-Bavarian Joint Advanced Student School", Zelenograd, Russia, March 21-25, 2011 - 3 reports

55th International Conference on Electronics, Telecommunications, Computers, Automatic Control and Nuclear Engineering (*ETRAN'11*), Banja Vrućica, Serbia, June 6-9, 2011 - 2 reports

8th International Conference of "Semiconductor Micro- and Nanoelectronics", Yerevan, Armenia, July 1-3, 2011 - 2 reports

ASIA Power Architecture Conference, Shenzhen, China, September 1, 2011 - 1 report

9th *IEEE East-West Design & Test Symposium (EWDTS'11)*, Sevastopol, Ukraine, September 9-12, 2011 - 1 report

International conference "Education, Science and Economics at Universities. Integration to International Educational Area", Yerevan, Armenia, September 26-30, 2011 - 1 report

6th IEEE International Design and Test Workshop (IDT) in Conjunction with IEEE International Conference on Electronics, Circuits and Systems (ICECS), Beirut, Lebanon, December 10-14, 2011 - 1 report

Other presentations (courses, seminars, etc.)

*Chan-Su Yun, Tommaso Cilento, Guenther Zandler, "***TCAD: Modeling of CMOS Degradation Mechanisms and Modeling/Calibration of FinFET Devices including Thermal Effects**", Therminator tutorial, Sept. 23, 2011, Munich (Germany)

Vazgen Melikyan, "**Thermal and Electro-Thermal Simulation: Achievements and Trends",** 8th International Conference of "Semiconductor Micro- and Nanoelectronics", July 1-3 2011, Yerevan, Armenia

*Vazgen Melikyan***, "Methods of Low Power IC Design: Development Trends and Challenges",** Moscow-Bavarian Joint School Conference, March 20-27 2011, Zelenograd, Russia

Shushan Karapetyan, **" Low Power Design Methods: Design Flows and Kits",** Moscow-Bavarian Joint School Conference, March 20-27 2011, Zelenograd, Russia

*Shushan Karapetyan, Vazgen Melikyan***, "Low power design tutorial with 90nm Educational Design Kit",** Moscow-Bavarian Joint School Conference, March 20-27 2011, Zelenograd, Russia

2.3 POLITO

Publications

Sassone, *A.; Wei Liu; Calimera, A.; Macii, A.; Macii, E.; Poncino, M.;* "**Modeling of thermally induced skew variations in clock distribution network**", THERMINIC'11: IEEE Workshop on Thermal Investigations of ICs and Systems, pp.1-6, 27-29 Sept. 2011

Lingasubramanian, K.; Calimera, A.; Macii, A; Macii E.; Poncino, M.; "**Sub-row sleep transistor insertion for concurrent clock-gating and power-gating,**" Lecture Notes in Computer Science, Springer, Vol. 5951, pp. 214-225, 2011, doi: 10.1007/978-3-642-24154-3_22

de Lima Silva, L. M.; Calimera, A.; Macii, A.; Macii, E.; Poncino, M.; "**Power Efficient Variability Compensation Through Clustered Tunable Power-Gating**," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol.1, no.3, pp.242-253, Sept. 2011, doi: 10.1109/JETCAS.2011.2163689

Calimera, A.; Loghi, M.; Macii, E.; Poncino, M.; "**Buffering of frequent accesses for reduced cache aging,**" GLSVLSI'11: ACM Great Lakes symposium on VLSI, pp. 295-300, May 2011

Rinaudo, S.; Gangemi, G.; Calimera, A.; Macii, A.; Poncino, M.; , "**Moving to Green ICT: From stand-alone power-aware IC design to an integrated approach to energy efficient design for heterogeneous electronic systems,**" DATE'11: Design, Automation & Test in Europe Conference & Exhibition, pp.1-2, 14-18 March 2011

Calimera, A.; Loghi, M.; Macii, E.; Poncino, M.; , "**Partitioned cache architectures for reduced NBTI-induced aging**," DATE'11: Design, Automation & Test in Europe Conference & Exhibition, pp.1-6, 14-18 March 2011

Participation to Conferences and Workshops

DATE-11: IEEE Design Automation and Test in Europe
Grenoble, France, March 2011.

GLSVLSI-11: ACM/IEEE Great Lakes Symposium on VLSI,
Lausanne, Switzerland, May 2011.

ISCAS-11: IEEE International Conference on Circuits and Systems,
Rio de Janeiro, Brazil, May 2011.

DAC-11: ACM/IEEE Design Automation Conference,
San Diego, CA, June 2011.

ISLPED-11: ACM/IEEE 2010 International Symposium on Low Power Electronics and Design,
Fukuoka, Japan, August 2011.

PATMOS-11: IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation, Madrid, Spain, September 2011.

THERMINIC 2011: International Workshop on Thermal Investigation of ICs and Systems,
Paris, France, September 2011.

ICCAD-11: IEEE/ACM International Conference on Computer-Aided Design,
San Jose, CA, November 2011.

Other presentations (courses, seminars, etc.)
Enrico Macii, "**Power-Gating for Leakage Control and Beyond in Nanometer CMOS Circuits**", Keynote speech at IEEE Prime Asia 2011 Macau, China, October 6, 2011.

Enrico Macii, "**Power Analysis and Low Power Design**", ALARI Master Course, Lugano, Switzerland, February 2011.

Andrea Calimera, Alberto Macii, "**Thermal-Aware Design Techniques for Digital ICs – Basics**", Therminator Course, Torino, Italy, December 2011.

Andrea Calimera, Alberto Macii, "**Circuit- and Physical-Level Thermal-Aware Design Techniques for Digital ICs**", Therminator Course, Torino, Italy, December 2011.

2.4 IMEC

Publications

Steve Stoffels, Denis Marcon, Karen Geens, Xuanwu Kang, Geert Van Der Plas, Marleen Van Hove and Stefaan Decoutere, "**High Temperature Calibration of a Compact Model for GaN-on-Si Power Switches**", Therminic 2011, Paris, 27-29 September 2011, pp. 159-163

Oprins, H.; Cherman, V.; Vandevelde, B.; Stucchi, M.; Van der Plas, G.; Marchal, P. and Beyne, E., "**Steady state and transient thermal analysis of hot spots in 3D stacked ICs using dedicated test chips,**" 27th Annual IEEE Thermal Measurement, Modeling and Management Symposium (SEMI-Therm), March 20-24, 2011, 131-137.

Oprins, H.; Srinivasan, A.; Cupak, M.; Cherman, V.; Torregiani, C.; Stucchi, M.; Vandevelde, B.; Van der Plas, G.; Marchal, P. and Cheng, E., "**Fine grain thermal modelling and experimental validation of 3D-ICs**," Microelectronics Journal, Vol. 42 (4), April 2011, pp. 572-578.

Participation to Conferences and Workshops

SEMI-Therm-11: 27th Annual IEEE Thermal Measurement, Modeling and Management Symposium, San Jose, CA, USA, March 20-24.

THERMINIC 2011: International Workshop on Thermal Investigation of ICs and Systems, Paris, France, September 2011.

2.5 FHG

Publications

A. Burenkov, J. Lorenz, "**Self-heating effects in nano-scaled MOSFETs and thermal aware compact models,"** THERMINIC, 17th International Workshop on Thermal investigations of ICs and Systems, Paris, France, 27-29 Sept. 2011, EDA Publishing, Collection of papers, pp. 17-18.

R. Jancke, S. Reitz, A. Heinig, R. Martin, J. Stole, A. Wilde, "**Thermal modeling of 3D stacks for floorplanning,"** THERMINIC, 17th International Workshop on Thermal investigations of ICs and Systems, Paris, France, 27-29 Sept. 2011, EDA Publishing, Collection of papers, pp. 153-158.

Participation to Conferences and Workshops

A. Burenkov, "**TCAD Simulations of Nano-CMOS Including Self-Heating,"** contribution to Therminator Tutorial at Intel Mobile Communication, Sept. 23, 2011, Munich (Germany)

THERMINIC: 17th International Workshop on Thermal investigations of ICs and Systems, Paris, France, 27-29 Sept. 2011

THERMINATOR **MunEDA - Workshop and Training** hosted by NXP Hamburg 2011 Dec 06-07; Participants: NXP, Fraunhofer, MunEDA

2.6 OFFIS

Other presentations (courses, seminars, etc.)

Sven Rosinger, Malte Metzdorf, Patrick Knocke, "**High-level Thermal Estimation Flow**", IEEE Xplore - Educational Courses.

2.7 BME

Publications

A. Timár, **M. Rencz**
Studying the influence of chip temperatures on timing integrity.
In: 12th IEEE Latin-American Test Workshop. Brazil, 27-30. 03. 2011.

A Timár, **M. Rencz**
Studying the Influence of Chip Temperatures on Timing Integrity Using Improved Power Modeling.
JOURNAL OF LOW POWER ELECTRONICS 7: pp. 1-10. (2011)

A Timár, **Gy. Bognár**, **M. Rencz**
Improved power modeling in logi-thermal simulation.
In: 17th International Workshop on Thermal investigations of ICs and Systems. Paris, Paris, France, 27-29. 09. 2011.

Gergely Nagy, András Poppe
A Novel Simulation Environment Enabling Multilevel Power Estimation of Digital Systems.
In: Proceedings of the 17th International Workshop on THERMal INvestigation of ICs and Systems (THERMINIC'11). Paris, France, 27-29. 09. 2011, pp. 149-152. (ISBN: 978-2-35500-018-8)

Participation to Conferences and Workshops

See Section 3 of this document.

2.8 IMC

Other presentations (courses, seminars, etc.)
*Joachim Assenmacher***, "Comparison of compact modeling strategies between BSIM and PSP incl. Temperature modeling",** Therminator tutorial, Sept. 23, 2011, Munich (Germany)

Christian Pach, Klaus von Arnim, **"Low Power CMOS technologies: A digital view"**, Therminator tutorial, Sept. 23, 2011, Munich (Germany)

2.9 CSEM

Publications

B. Kheradmand Boroujeni, C. Piguet, Y. Leblebici, "**Optimal Logic Architecture and Supply Voltage Selection Method to Reduce the Impact of the Threshold Voltage Variation on the Timing**", JOLPE - Vol. 7, N° 2, April 2011

C. Piguet, "**Green Electronics**", Keynote Talk at NewCAS, Bordeaux, 27-29 juin 2011

Other presentations (courses, seminars, etc.)

C. Piguet, "**Microelectronics for Systems-on-Chips**", EPFL Course, winter 2011 semester

C. Piguet, "**Microelectronics**", ALaRI Course, winter 2011

2.10 MUN

MUGM – MunEDA User Group Meeting is an open annual international workshop and conference organized by project partner MunEDA. At MUGM topics for design analysis, modeling, optimization and IP porting will be discussed and presented by the participants. The presentations are available for participants throughout the MunEDA Webpage. MUGM is also a recommended forum for publications and presentations of governmental funded research projects where MunEDA is participating. For more information have a look on the MUGM webpage with http://www.muneda.com/MUGM. MunEDA offers this platform also for its project partners also to present about their project activities and results such as in THERMINATOR.

Furthermore MunEDA took part, presented, organized and exhibited in several conferences , workshops and fairs worldwide in 2011 such as DAC Design Automation Conference 2011 San Diego USA, DATE Design and Test in Europe 2011 Grenoble France, EDS-Fair Electronic Design and Solutions Fair 2011 Yokohama Japan, SNUG Synopsys User Group Meeting 2011 San Jose, HSPICE SIG 2011 Santa Clara USA, MTS MunEDA Technical Seminar 2011 Japan Yokohama, MTF MunEDA Technical Forum Korea Seoul Korea, Analog 2011 Erlangen Germany, Nanoelectronics Forum 2011 Dublin Ireland and many other events. For more information please see http://www.muneda.com/Events.

Publications

Pronath M., Sobe U., Graupner A., Boehme E., "**Conversion and Optimization Flow for Analog IP Porting**", DAC Design Automation Conference 2011, San Diego, USA, June 2011

Strube G., Ripp A.,"**Trends with Analog Mixed-Signal Design**", Analog 2011 Conference, Erlangen, Germany, November 2011

Neubert R., Rotter P., "**Parameter Calibration and Cascaded Simulations - Infineon**", MUGM MunEDA User Group Meeting 2011, Munich, Germany, November 2011

Other presentations (courses, seminars, etc.)

THERMINATOR Joined Contribution Synopsys-MunEDA at MTF Korea 2011 Jan 21 Seoul Korea hosted by MunEDA: Synopsys Custom and Analog Mixed-Signal Overview & MunEDA WiCkeD Integration (incl. WiCkeD Integration Demo into Synopsys Hspice, CustomSim (HSIM, NanoSim, XA) and CustomDesigner) http://www.muneda.com/User-Group-Meetings_Korea-2011

THERMINATOR MunEDA –Workshop and Training hosted by STMicroelectronics Catania 2011 Feb 26-29: Participants: STMicroelectronics, MunEDA

THERMINATOR MunEDA-Workshop and Training hosted by STMicroelectronics Crolles 2011 Sep 05-09; Participants: STMicroelectronics, MunEDA

THERMINATOR MunEDA-Workshop and Training hosted by STMicroelectroncis Castelletto 2011 Oct 05-06; Participants: STMicroelectronics, MunEDA

THERMINATOR MunEDA-Workshop and Training hosted by Infineon Villacon 2011 Nov 07-09; Participants: Infineon, MunEDA

THERMINATOR **MunEDA- Workshop and Training** hosted by NXP Hamburg 2011 Dec 06-07; Participants: NXP, Fraunhofer, MunEDA

2.11 UNIBO

Publications

U. Roy, E. Sangiorgi, C. Fiegna. (2010). **Self-Heating Effects in Analog Bulk and SOI CMOS Circuits**. *2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology Proceedings*. 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology. Shanghai, China. November 1-4, 2010. (pp. 1782 - 1785). ISBN: 978-1-4244-5799-1. : IEEE Press.

Paolo *Magnone, Claudio Fiegna, Giuseppe Greco, Gaetano Bazzano, Enrico Sangiorgi, Salvatore Rinaudo,* "**Modeling of Thermal Network in Silicon Power MOSFETs**", Proceedings of the IEEE 12th ULIS 2011, 14-16 March 2011, Cork, Ireland

Participation to Conferences and Workshops

2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology, Shanghai, China

2011 Ultimate Integration on Silicon Conference, Cork, Ireland

Other presentations

R. Guerrieri, "**Design of electronic systems**", University Of Bologna course, spring 2011 semester

R. Guerrieri, "**Digital signal processing Architectures**", University Of Bologna course, spring 2011 semester

3 Dissemination Through Dedicated Workshop Special Sessions

THERMINIC (International Workshop on Thermal Investigation of ICs and Systems) Workshops are a series of events to discuss the essential thermal questions of microelectronic microstructures and electronic parts in general. In particular, **THERMINIC 2011** (http://cmp.imag.fr/conferences/therminic/therminic2011) addressed in addition to the "traditional" thermal management problems, also stress and thermal-stress-related-reliability issues, both in micro- and opto-electronics fields. These issues, including various nanotechnology applications, are of significant importance and of high interest to the engineering community engaged in the field of thermal phenomena in "high-tech" systems.

As in 2010, in **THERMINIC 2011** (27-29 September 2011, Paris, France), THERMINATOR partners (leaded by BME) have organized two special half-days dedicated to disseminate the project results to the thermal management community. This special session consisted of nine technical papers strictly related with the research topics followed and developed within the THERMINATOR project.

The technical program can be found at this url:
http://cmp.imag.fr/conferences/therminic/therminic2011/FinalProgramTH11.pdf

Below some details regarding the presentations given in these two half day special sessions:

Therminic 2011, Therminator Special Sessions
Paris, 27-29. September 2011. – participants: 80

- **Therminator Special Session I.**
  1. *An Analog Behavioral Thermal Macro-model Aimed at Representing an Elementary Portion of a Discrete IGBT Power Device* (Gaetano Bazzano, Daniela Grazia Cavallaro, Giuseppe Greco)
  2. *Self-heating Effects in Nano-scaled MOSFETs and Thermal Aware Compact Models* (Alex Burenkov, Jürgen Lorenz)
  3. *3D Electro-Thermal Simulations of Analog ICs carried out with Standard CAD tools and Verilog-A* (Jean-Christophe Krencker, Jean-Baptiste Kammerer, Yannick Hervé and Luc Hébrard)
  4. *Modeling of Thermally Induced Skew Variations in Clock Distribution Network* (Alessandro Sassone, Wei Liu, Andrea Calimera, Alberto Macii, Enrico Macii and Massimo Poncino)
- **Therminator Special Session II.**
  1. *Improved power modeling in logi-thermal simulation* (András Timár, György Bognár, Márta Rencz)
  2. *A Novel Simulation Environment Enabling Multilevel Power Estimation of Digital Systems* (Gergely Nagy, András Poppe)
  3. *Thermal Modeling of 3D Stacks for Floorplanning* (Sven Reitz, Andy Heinig, Roland Martin, Jörn Stolle, Andreas Wilde)
  4. *High Temperature Calibration of a Compact Model for GaN-on-Si Power Switches* (Steve Stoffels, Denis Marcon, Karen Geens, Xuanwu Kang, Geert Van Der Plas, Marleen Van Hove, Stefaan Decoutere)
  5. *Single-Chip Cloud Computer Thermal Model* (Mohammad Sadegh Sadri, Andrea Bartolini, Luca Benini)

4 Dissemination Through Press Releases

MunEDA

- *MunEDA WiCkeD Supports TSMC AMS Reference Flow 2.0 for 28nm*

http://www.businesswire.com/news/home/20110603005406/en/MunEDA-WiCkeD-Supports-TSMC-AMS-Reference-Flow

Hsinchu, Taiwan, R.O.C. - Friday, June 3rd, 2011

MunEDA, developer of the industry's broadest family of advanced circuit analysis, modeling and optimization solutions, today announced that TSMC has included MunEDA's WiCkeDTM circuit analysis environment in TSMC AMS Reference Flow 2.0, one of the critical components in TSMC 28nm design infrastructure. WiCkeD covers a wide range of essential tasks in interactive and automatic specification-driven custom circuit design with statistical circuit analysis. Using MunEDA WiCkeD with TSMC process technologies helps designers improve the robustness of circuit designs against parametric process variation, achieve performance, power and area requirements, and improve efficiency to reduce design time.

"MunEDA's WiCkeD software has been validated for our AMS Reference Flow 2.0," said Suk Lee, director of Design Infrastructure Marketing at TSMC. "WiCkeD's sensitivity and worst-case analysis methodologies deliver good benefits to designers using TSMC 28nm process technology. We are happy to collaborate with MunEDA on statistical circuit analysis."

"We are proud that TSMC has incorporated MunEDA WiCkeD as a part of the TSMC AMS Reference Flow 2.0," stated Michael Pronath, MunEDA vice president of Products & Solutions. "Our collaborations with TSMC and our mutual customers show that specification-driven design and statistical design are important for design success in advanced process technologies."

Circuit designers use MunEDA's WiCkeD circuit analysis and sizing environment to balance specs, area, power, reliability and robustness. WiCkeD can automate manual circuit design tasks in IP porting and cell migration to maximize designers' efficiency. It helps them overcome challenges of analog/mixed-signal (AMS) circuit design in sub-100nm technologies posed by lower core voltages, less headroom, more on-chip variation and other effects that can affect the performance, power, and yield of critical circuits.

MunEDA WiCkeD is in industrial use by leading semiconductor companies worldwide, in the areas of mobile communication, medical, memories, automotive and consumer electronics. Key application areas include low-power AMS/RF circuit design, high-speed digital I/O, and memory.

<< Comment for THERMINATOR: The adoption of MunEDA technology by TSMC to be integrated into their reference flow is a key achievement that such technology gets available for the project partners but also for the industry through TSMC worldwide support channel.>>

- *STARC (Semiconductor Technology Academic Research Center Japan) selected MunEDA WiCkeD after evaluation of variation aware circuit design tools to reduce design time and effort*

http://www.starc.jp/about/release/110124-1-j.pdf

<< Comment for THERMINATOR: The adoption for MunEDA technology by STARC is a key step on the way to enter the Japanese market with enhanced European EDA technology. >>

5 Dissemination Plan for the Third Year

The dissemination activities for the third year of the project will continue along the same lines followed so far. The number of publications, as well as the participation of partners to different kinds of dissemination events (e.g., conferences, symposia, workshops, exhibits, forums, fairs) is expected to be stable or even increase as the research and development work of the project will progress, as the material available for dissemination is now stable.

As last year, all partners involved in R&D activities have renewed and reinforced their full commitment to the dissemination of the THERMINATOR results to the international community; a final report summarizing the work performed in the third year of the project will be filed by month M36 (Deliverable D8.2.5).