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Modelling, Control and Management of Thermal Effects in Circuits of the Future

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Final THERMINATOR Roadmap

Prepared by	**B. Giacalone, G. Gangemi**
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Author(s)	Biagio GIACALONE9STP), Giuliana GANGEMI(ST)
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3 References

IPCA – THERMINATOR Consortium Agreement,
D8.4.1 “First Release of Market Survey”
D8.4.5 “Preliminary THERMINATOR Roadmap”

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Remark

In addition to the THERMINATOR consortium, the content of this document is considerably complemented with projected data and statistics coming from reference organizations, mainly from **ITRS** (**I**nternational **T**echnology **R**oadmap for **S**emiconductors).

As the majority of the partners are members of ITRS to refer to such documents was the most effective way not to duplicate unnecessarily the effort and to be sure not to break any confidentiality, as the matter is quite sensitive.

1 THERMINATOR Final Roadmap: Focus

In the previous report: “Preliminary THERMINATOR Roadmap”, the roadmap was described in most of the fields linked with semiconductor industry, this to create a very “up-to-date” global vision of the trends and the guidelines. The objective of this deliverable is focalized on aspects concerning the Design Technology (DT) domain, because the focus and the scope of THERMINATOR was Thermal Aware Design Technology.

2 THERMINATOR Final Roadmap: Introduction

THERMINATOR has span different aspects of the thermal-aware design, from modelling to optimization, from design solutions to design methods and tools usable at different levels of abstraction and for different technology families, thus getting in touch with different customers. STMicroelectronics, IMC and NXP Semiconductors, the three major European semiconductor manufacturers and systems-on-silicon providers, participated in the project, thus it is foreseeable that THERMINATOR results will be usable at production level if promptly taken up by the three companies as well as by the EDA vendors also partners in the project.

A foreseeable significant increase in the ability of European semiconductor industry to design and manufacture with reduced failure risks (reduced costs and augmented reliability) and in a more efficient manner (reduced time-to-market) will lead to new electronic devices and systems fully exploiting the opportunities given by the future silicon technologies. This will help companies to outdo their competition, therefore strengthening Europe's position as a leading supplier of electronic components, a key factor in revolutionizing different applications in health, safety and security, transport and provision of environmentally friendly sustainable applications. This will support the competitiveness of industrial strongholds, such as automotive, avionics, industrial automation, consumer electronics, telecom and medical systems. In all these domains Europe's leadership heavily relies on the capacity to engineer and produce electronic components, integrating them into products across all sectors.

3 THERMINATOR Roadmap

Most of evaluations were in the previous report; here additional considerations are given about the Design Technology challenges.
We can divide these challenges in:

- Near Term
  - ✓ Power Management and Thermal Management
  - ✓ Design Productivity and Design for Manufacturability

- Long Term
  - ✓ Design of Concurrent Software
  - ✓ Design for Reliability and Resilience

The THERMINATOR Project directly addresses the Power and Thermal Management challenges, so a description of these issues will be given in the following paragraphs; then, an analysis of how they affect DT complexity will be proposed.

3.1 Power Management

Power management must be addressed early in the design phase, at the architectural level, to ensure a long-enduring unit.
The first step in power management is optimization of power consumption in the system. This needs to start at the beginning of the design stage, when the functional specification of the system is translated into register-transfer-language (RTL) code describing the implementation of the electronic system on a behavioural level. There may be many possible implementations that will result in the same system function, all varying widely in power consumption. A good designer will draw upon experience to optimize the RTL code to implement the necessary functionality in a power-efficient way. But given the size and complexity of electronics in modern systems, analysing RTL

code organically is becoming impractical. Instead, this requires the support of dedicated optimization tools capable of analysing the full complexity of the system implementation. Reducing a component's power consumption also reduces the amount of heat it generates, which helps ensuring that the system will operate more reliably in its target operation environment. Optimized power management, therefore, is an integral part of thermal management of a system.

3.2 Thermal Management

In addition, thermal management of the electronic system is required to ensure the functionality of an electronic system. Thermal management has become increasingly challenging with the trend toward miniaturization. As electronic components consume power, they also generate heat that has to be removed from components to avoid overheating and loss of reliable operation. In addition, often thermal dissipation represents the main bottleneck to integration

As a consequence, thermal management cannot be treated as an afterthought anymore; it has to be an integral part of system design. Thermal management requires optimization of heat generation and heat dissipation, making it a multiphysics problem.

3.3 Overall Challenges

DT faces two basic types of complexity—*silicon complexity* and *system complexity*—that follow from roadmaps for manufacturing technologies.

Silicon complexity refers to the impact of process scaling and the introduction of new materials or device and interconnects architectures. Many previously ignorable phenomena now have great impact on design correctness and value:

- *Non-ideal scaling of device parasitics and supply/threshold voltages* (leakage, power management, circuit/device innovation, current delivery)
- *Coupled high-frequency devices and interconnects* (noise/interference, signal integrity analysis and management, substrate coupling, delay variation due to cross-coupling)

· *Manufacturing variability* (statistical process modelling and characterization, yield, leakage power, with implications for, and impacts on, library characterization, analog and digital circuit performance, error-tolerant design, layout reuse, reliable and predictable implementation platforms)

· *Complexity of manufacturing handoff* (reticle enhancement and mask writing/inspection flow, NRE cost)

· *Scaling of global interconnect performance* relative to device performance (communication, synchronization)

· *Decreased reliability* (gate insulator tunnelling and breakdown integrity, joule heating and electromigration, single-event upset, general fault-tolerance)

· *Codesign* (additional complexity of codesign of multiple chips and packages, especially with the introduction of 3D stacking technologies with Through-Silicon Vias (TSVs))

Silicon complexity places long-standing paradigms at risk, as follows: 1) system-wide synchronization becomes infeasible due to power limits and the cost of robustness under manufacturing variability; 2) the CMOS transistor becomes subject to ever-larger statistical variability in its behaviour; and 3) fabrication of chips with 100% working transistors and interconnects becomes prohibitively expensive.

Available implementation fabrics (from direct-mapped custom through general-purpose software-programmable) easily span four orders of magnitude in performance metrics and there is added opportunity to leave value on the table via ill-advised guardbands, abstractions, or other methodological choices. These challenges demand more broadly trained designers and design technologists, as well as continued mergers between traditionally separated areas of DT (synthesis-analysis, logical-physical, etc.).

System complexity refers to exponentially increasing transistor counts enabled by smaller feature sizes and spurred by consumer demand for increased functionality, lower cost, and shorter time-to-market. Many challenges are facets of the nearly synonymous *productivity* challenge. Additional complexities (system environment or component heterogeneity) are forms of *diversity* that arise with respect to system-level

SOC integration, and 3D integration. Design specification and validation become extremely challenging, particularly with respect to complex operating contexts. Trade-offs must be made between all aspects of value or quality, and all aspects of cost. Implied challenges include:

- *Reuse*—support for hierarchical design, heterogeneous SOC integration (modelling, simulation, verification, test of component blocks) especially for analog/mixed-signal
- *Verification and test*—specification capture, design for verifiability, verification reuse for heterogeneous SOC, system-level and software verification, verification of analog/mixed-signal and novel devices, self-test, intelligent noise/delay fault testing, tester timing limits, test reuse
- *Cost-driven design optimization*—manufacturing cost modelling and analysis, quality metrics, co-optimization at die-package-system levels, optimization with respect to multiple system objectives such as fault tolerance, testability, etc.
- *Embedded software design*—predictable platform-based electronic system design methodologies, codesign with hardware and for networked system environments, software analysis and verification
- *Reliable implementation platforms*—predictable chip implementation onto multiple circuit fabrics, higher-level handoff to implementation
- *Design process management*—design team size and geographic distribution, data management, collaborative design support, “design through system” supply chain management, metrics and continuous process improvement

Together, the silicon and system complexity challenges imply *superexponentially increasing complexity* of the design process. To deal with this complexity, DT must provide concurrent optimization and analysis of more complex objectives and constraints, acknowledge added considerations such as design reuse and manufactured system cost in the design optimization, and encompass added scope such as embedded software design and interfaces to manufacturing. The sheer breadth of silicon and system complexities is also a challenge to roadmapping of DT and the electronic design automation (EDA) industry.

Five *crosscutting challenges* —1) design productivity, 2) power management, 3) design for manufacturability, 4) interference, and 5) reliability and resilience—underlie the design cost "meta-challenge" and have potential solutions that span all areas of DT.

Regarding Challenge 2*,* Power Management*,* the non-ideal scaling of planar CMOS devices, together with the roadmap for interconnect materials and package technologies, presents a variety of challenges related to power management and current delivery. Increasing power densities worsen thermal impact on reliability and resilience and performance, while decreasing supply voltages worsen leakage currents and noise. These trends stress on-chip interconnect. 3D technologies further complicate this problem as chips have to be codesigned to deliver power to co-stacked sub-systems. Leakage power varies exponentially with key process parameters such as gate length, oxide thickness and threshold voltage; this presents severe challenges to both analysis and optimization in light of both scaling and variability.

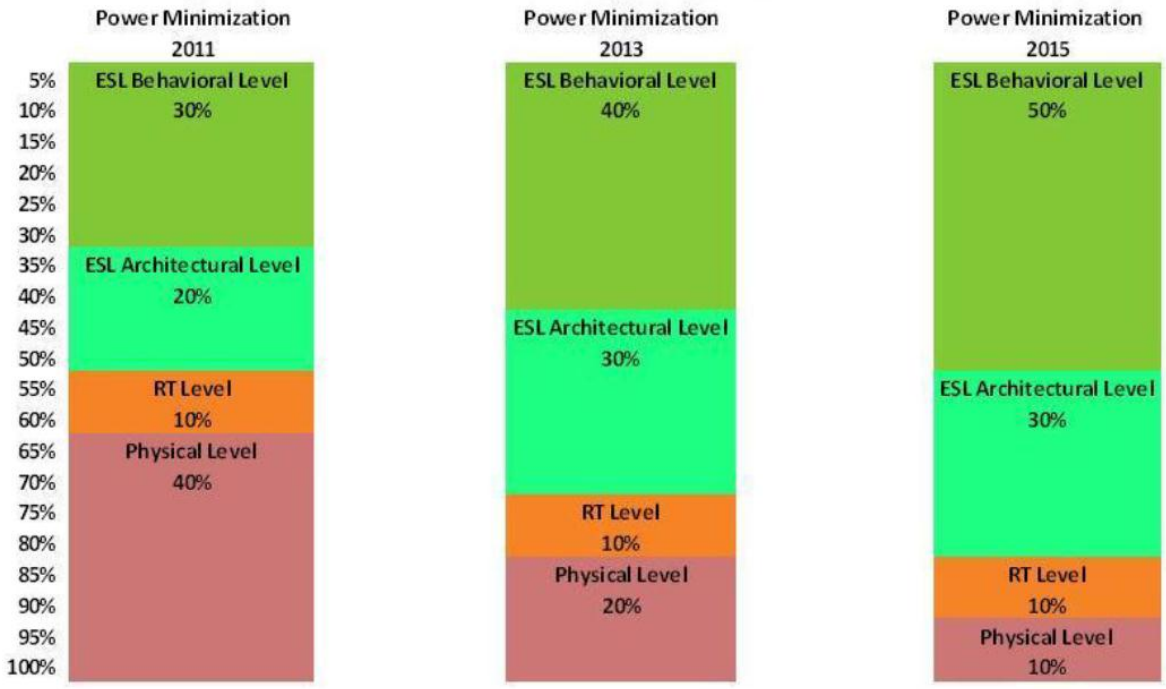


Fig. 1

Figure 1 gives a roadmap for the increasing role of system-level design in achieving the required system power minimization. In the figure, percentage values indicate the

fraction of power reduction that must be borne by the given phases of system design in future technology nodes.

4 Topics

4.1 Drivers

This section shows some of the technical issues addressed by the THERMINATOR research activities that the Consortium indicates as drivers for the scientific investigations on the matter as they will last beyond the THERMINATOR project duration and, without whose solution, the ***thermal*** issue cannot be considered to be under control.

4.1.1 Self-heating and hot spots

Heat generation in integrated circuits (ICs) causes a temperature increase around the power dissipating device (Figure 2). This causes self-heating. As the devices, located in various points of the IC, have different operating frequencies and power absorptions, several temperatures can be obtained in various points of the IC.

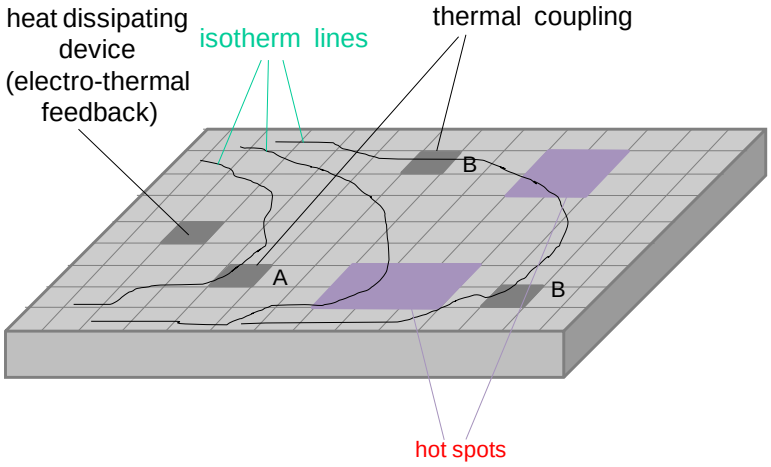


Fig. 2 Self Heating

For example Figure 3 shows the temperature distribution obtained by means of IC electro-thermal simulation.

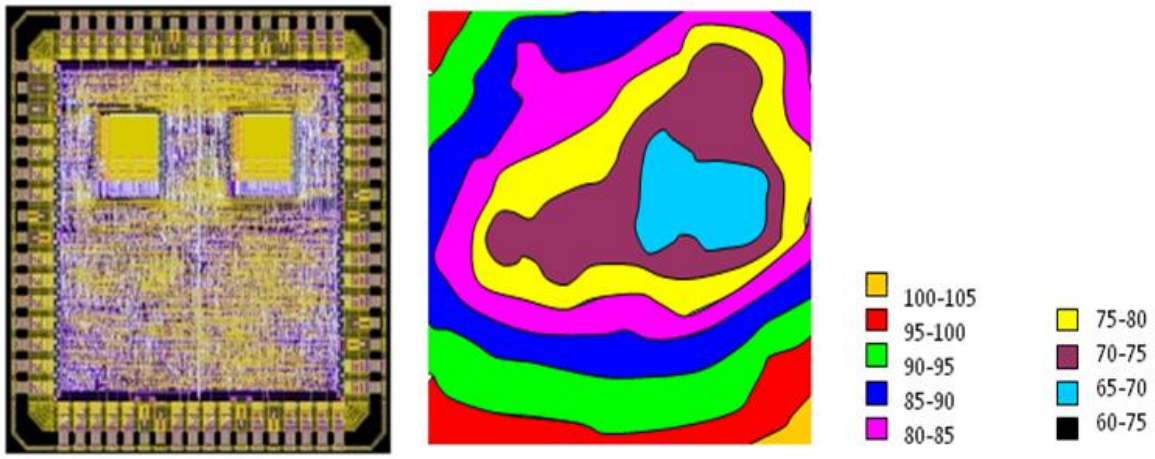


Fig. 3 Temperature distribution in IC

The inertia of semiconductor materials, from the viewpoint of temperature distribution, also contributes to the presence of different temperatures. In the result, occurring temperature peaks are also called hot spots (Figure 2).

4.1.2 Electro-thermal feedback

First of all, temperature increase modifies the heat dissipating device function. At the same time, it also affects the neighbouring devices. This is caused by strictly expressed dependence of device properties and parameters on temperature. The change of heat dissipating device properties due to temperature increase is called electro-thermal feedback, whereas the change of neighbouring device properties is called thermal coupling.

4.1.3 Thermal coupling and mismatch

If neighbouring devices are not placed in the same isotherm line, thermal mismatch will occur. Such mismatch can occur, for example, between points A and B, as illustrated in Figure 2.

4.1.4 Reduction of performance, life and reliability

The number of failures, detected in IC devices, exponentially depends on operating temperature (Figure 4). That is why when a device exceeds the specified temperature its performance, life, and reliability are essentially reduced.

Junction temperatures of 180°C are typical of many applications and yield device MTTFs (Median-Time-To-Failures) better than 1 million hours. Figure 5 shows examples of MTTF curves for different RF ICs. The illustrated curves show that various applications may require different maximum junction temperatures depending on MTTF requirements.

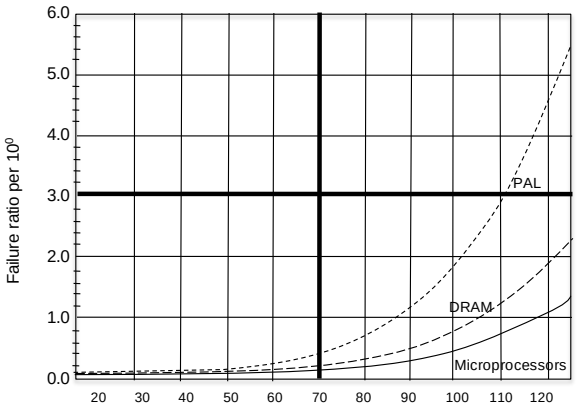


Fig. 4 Failure number dependence on junction temperature

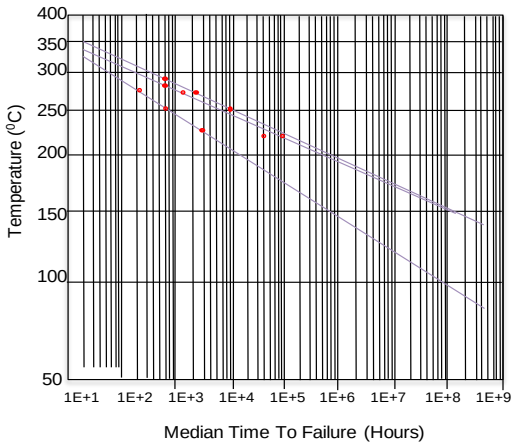


Fig. 5 Median-Time-To-Failures for Different ICs

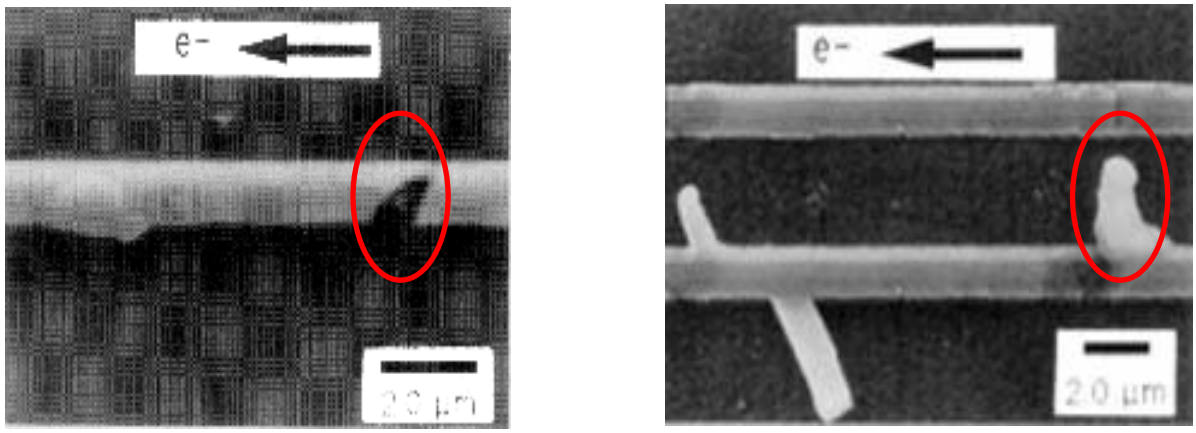
4.1.5 Electromigration issues

Electromigration is the momentum exchange between conducting electrons and diffusing metal atoms. It presents material problem. Electrons moving about “electron wind” impart momentum onto metal atoms during scattering events or collisions. Scattering occurs whenever an atom is out of place for any reason. Thermal energy causes atom vibration that in turns leads to scattering. After many collisions, the force averages out in the direction of electron flow.

Electromigration can cause two types of failures: void and open. In narrow interconnects, like those linking transistors and other components in integrated circuits, a break or gap can develop in the conducting material, preventing the flow of electricity: this is known as a void. Furthermore, it can cause atoms of a conductor to pile up and drift towards other nearby conductors, creating an unintended electrical connection (Figure 6).

The electromigration effect depends on current density temperature. It is not a function of current, but a function of current density. Larger current on narrower metal speeds up electromigration effect. The phenomenon is accelerated by elevated temperature.

The role of electromigration, which has always been present in ICs, for 90nm technologies and below considerably increases and is one of the most important of today’s technology challenges. A reduction of the structure (scaling) by a factor K increases the power density and thus the temperature proportional to K and the current density increases by K^2 whereby EM is clearly strengthened.



Open circuit

Short circuit

Figure 6 Type of failures caused by electromigration

4.2 Thermal requirements for EDA Tools

This paragraph describes the main EDA tools requirements concerning thermal issues that are hardly covered by today's instruments and that are expected to get more and more significant together with the evolution of technology and shrinking of circuit size. The requirements are grouped according to their purposes in logic synthesis, logic simulation, verification, characterization and logic/RF circuit design.

4.2.1 Logic synthesis tools

The steady growth of power consumption coupled with the shrinking dimensions of devices has caused a dramatic increase of power densities in sub-100nm technologies. High power densities directly translate into an increase of operating temperatures; furthermore, time and space power densities variations cause temperature gradients in the substrate and, as a consequence, non-uniform substrate temperature: Gradients of 50°C have been measured across the substrate in high-performance ICs.
With wider spatial/temporal thermal ranges, the performance of the circuit may vary significantly, although not all elements are affected in the same way. Concerning wires, as on-chip temperature rises, the metal resistivity of the global interconnects increases, leading to significant performance degradation. Concerning devices, recent works have shown that, in sub-90nm technologies, the propagation delay through a gate can vary in complex ways as temperature varies. That is, depending on various parameters, such as cell size, load, supply voltage, and threshold voltage (V_{th}), the delay can either increase as temperature rises (standard behavior) or decrease as temperature rises (Inverted Temperature Dependence).

The main limitation of standard synthesis tools is that they do not consider temperature as an explicit variable during the optimization loop. Instead, they apply conservative design strategies for which a static worst-case temperature (typically 125°C) is considered. Needless to say, these kind of approaches may fail in catching the right

thermally-induced behavior of both passive (i.e., interconnects) and active (i.e., transistors) devices under dynamic temperature variations. The generated circuits, therefore, are significantly prone to timing failures.

4.2.1.1 Synthesis of temperature-insensitive low-power circuits

In low-power nanometer-scale technologies an *Inverse Temperature Dependence (ITD)* phenomenon may appear in MOS transistors, such that cell delay may *decrease* as temperature increases. By characterizing cell delays using an industrial low-power nanometer-scale multi-V_{th} technology, two simple rules of thumb for cell behavior can be obtained: the delay of fast, low-V_{th} (LVT) cells increases as temperature increases, (i.e., the "classical" assumption), while the delay of high-V_{th} (HVT) cells decreases as temperature increases. In other words, the worst-case delay of a low-V_{th} cell occurs at high temperature, while, for a high-V_{th} cell, worst case delay is at the lowest temperature.

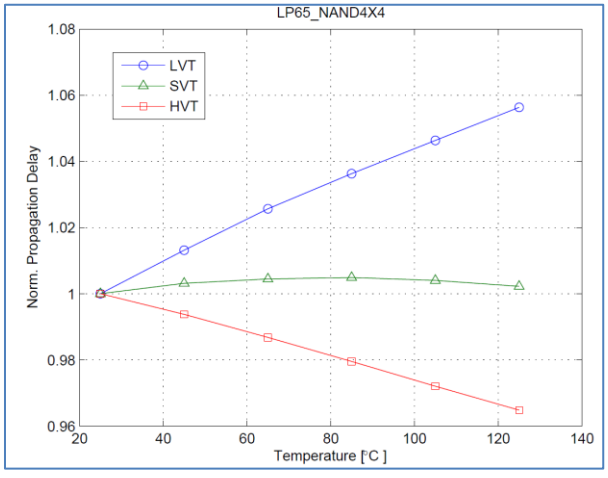


Fig. 7 Propagation Delay vs. Temperature for a minimum sized 4-input NAND

This new complicated aspect poses several limitations to timing-driven synthesis tools that do not consider the temperature as an explicit variable in their optimizations. For

instance, the common practice has been to synthesize designs using cell libraries characterized for the worst case (highest temperature T_{max}). However, since new technologies exhibit an ITD effect, high temperature does not necessarily correspond to the worst-case condition, so a circuit may have timing faults when operating at other temperatures. To compensate for these temperature effects, the designer may be conservative when setting the timing constraints (i.e., setting the desired timing to be faster than actually required). In this case, even if the path delays increase for temperatures other than T_{max}, one can guarantee that the global delay constraint is still met, however, it comes at the cost of higher power dissipation and/or circuit area.

It is clear that new low-power synthesis tools which can provide the designers with temperature-insensitive circuits are therefore required for modern design flows. Such tools will generate circuits which meet the given timing constraints over the entire range of allowed temperatures, while significantly reducing leakage power compared to circuits synthesized with a standard, i.e., non ITD-aware, commercial tool.

4.2.1.2 Synthesis of temperature-insensitive tunable clock-trees

Temperature-induced delay variations in interconnects are extremely critical for clock distribution networks whose delays must be carefully tuned to avoid synchronization errors. The clock-skew (defined as the maximum difference in the Arrival Time (AT) of the clock-edge at two flip-flops, Figure 8), which is a critical parameter for the correct functionality of the circuit, is also extremely sensible to temperature variations. Hence, clock analysis and clock synthesis tools cannot neglect the impact of spatial and temporal temperature variations in today's nanometer technologies.

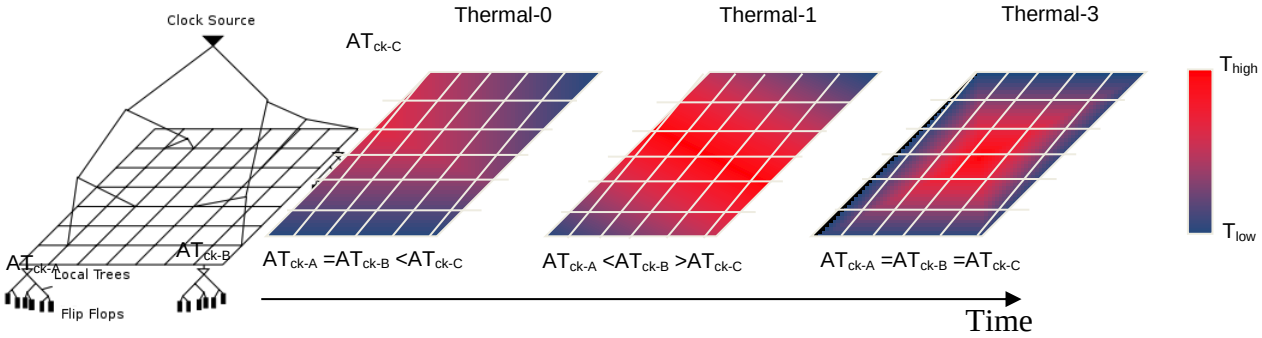


Fig. 8 Clock-Tree under dynamic thermal profiles

Although different techniques for temperature-aware design of clock distribution networks do exist, they only consider spatial gradients, namely, they are able to optimize clock distribution just for a given (non-uniform) temperature profile. What they cannot do is to account for the fact that on-chip thermal profiles can greatly change during system operation.

To bridge this gap, next generation of temperature-aware EDA tools will automatically implement closed-loop techniques for run-time temperature sensing and clock-tree tuning. Such design techniques, which are based on the use of dynamically tunable clock trees in conjunction with distributed on-chip temperature sensing, dynamically adapt the delays in the clock tree distribution network such that the thermally-induced clock-skew variations (spatial and temporal) are maintained below a pre-defined guard-band threshold.

4.2.2 Logic simulation tools

4.2.2.1 Logi-thermal methods and the roadmap for the application logi-thermal tools

Due to the uneven event density over the chip surface, digital blocks normally experience time-variable temperature gradients, and due to the fact that digital gates show a dependence on temperature, a merely digital, gate-level simulation may strongly deviate from the actual simulation results when the surface temperature profile of the chip is considered in calculating the actual delays of the individual gates. Self-consistency between the thermal behaviour and the digital behaviour of the chip needs to be maintained: when logic and thermal operation are traced together, we can speak of “logi-thermal simulation”. The major application of such a simulation is to make sure that during timing analysis thermal effects are considered (thermal-aware signal integrity check). In other words, to make sure that the digital circuit will properly function under all allowed thermal conditions.

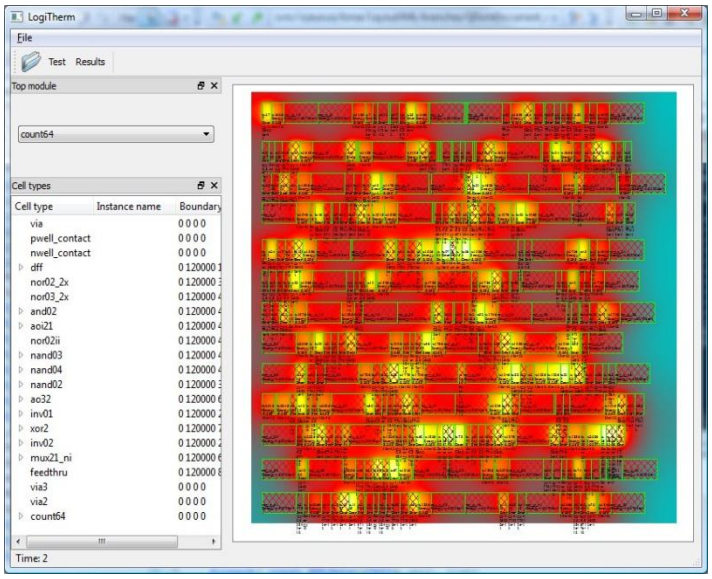


Fig. 9 logi-thermal simulator a Snap Shot

At the moment logi-thermal simulator engines are under development. These will allow designers to check the operation of their designs and perform adjustments if needed. The long-term goal is to incorporate this method in the digital design flow. The results obtained from it could drive place and route algorithms to provide layouts with a minimized possibility of hot spot formation. This would be a breakthrough in automated digital design as hot spots and thermal failures cause a major problem in modern VLSI devices.

4.2.2.2 Logi-thermal simulation methods and tools

The goal of logical simulation is to provide the designer early information on the system behavior, allowing testing the architecture early in the design life. Nonetheless it provides emulation and simulation capabilities to develop software before the hardware prototype is available and can be used efficiently for design space exploration.

As Power and Thermal requirements have become tight design constraints, logic simulation needs to perform not only functional and timing validation, but also power and thermal design validation.

Logical simulation can be pursued at different levels of abstraction.

Block level logical simulation is used to verify early in the design life cycle the correctness of the design and to support software design and performance analysis before hardware prototype is available.

After synthesis, gate level logic simulation is used to verify within the macro block the correctness and retrieve more realistic power and critical path delay estimation. Currently, thermal effects in logical simulation are accounted statically within the standard design flow ensuring the critical path delay meets the specifications under different ambient temperature conditions.

Unfortunately this approach does not consider the dynamic nature of temperature transients and cannot accurately account self-heating and thermal cross-coupling with other design components. To override this limitation, thermal transient and feedback interference between power, temperature and critical path must be modeled and accounted for horizontally along all the stages of logic simulation and a clear vertical

interface and design hierarchy must be defined and preserved between all the layers to efficiently tackle the multi-scale and multi-resolution nature of logi-thermal simulation.

4.2.2.3 Logi-thermal building blocks

As early introduced, horizontally the basic building blocks of logi-thermal simulations are a power model to convert the input stress pattern at a given working condition into the dissipated power. A thermal model & simulator to translate the dissipated power map into a thermal map. Finally a timing model capable to estimate the impact of the new thermal map in critical path delay variation. All these models account for the same chain of interaction in all the different vertical layers.

4.2.2.4 Logi-thermal gate-level simulation

After synthesis, gate level logic simulation allows accurate functional, critical path and power validation. To enable close loop logi-thermal simulation at this stage, technological libraries need to integrate models to take into account the effects of temperature changes during the simulation. Both gate level power consumption and critical path delay need to model explicitly the dependency with gate temperature.
The vertical integration with block level logi-thermal simulation requires the following key functionalities:

- Tools must preserve information on the hieratical structure of the design: Gate level components must have a link to the macro-block they belong to; gate level switching activity, input stress vectors, power and temperature traces must preserve a link with the macro block functional operation and with the component they are related to. This features will allow high abstraction logi-thermal simulators to use these results to self-learn, and refine the coarser model built in model used in block level simulation.
- Gate level logi-thermal simulation needs to gather information from block-level one. This information (for example, is the surrounding macro block and ambient temperature) will contain more realistic ambient surrounding information for the

gate level power, thermal and timing model for a given macro-block functional operation.

4.2.2.5 Logi-thermal block level simulation

The time scale achievable by logi-thermal gate level simulation, due to the high level of details considered, is usually not sufficient to evaluate the performance of the full design under typical uses cases and often is significantly below the thermal time constants requiring thermal transient approximations.
Virtual platforms, emulators and functional simulators, allow today to override this limitation. This is achieved by increasing the abstractions toward a functional description of the macro-block. The interfaces between the different macro-blocks are preserved, and functional model of interconnects are used to emulate not-idealities of the information flow. System level timing information can be obtained at this level by using an event driven simulation strategy.
The time resolution and the global view intrinsic of block-level logic simulation is suitable for system level dynamic optimization of the design and to identify the critical component of the design considering different usage conditions and accounting the interaction between major building blocks of the system.
At this level close loop logi-thermal co-simulation is a key feature to power and thermal system level design optimization.

In order to achieve that:

- Each macro block in the design needs to integrate a power, thermal and timing model suitable for the internal description abstractions. In order not to loose accuracy, the model internal parameters need to be tuned and self-extracted on the lower level (gate-level) logi-thermal simulation. This can be done by using system level techniques, data regression and model order reduction.
- To improve the accuracy of the full design block-level simulation needs to collect for each block the surrounding run-time information and feed it as design constraints and environmental conditions in the gate level simulation.

Thus, EDA tools for logi-thermal simulation need to have a common interface to keep a link between the different abstraction level components and simulation results. The multiscale nature of thermal problem cannot be tackled efficiently and accurately within a single abstraction layer, thus different logi-thermal simulators at different granularities need to be closely coupled and have a vertical information flow.

4.2.3 Verification tools

During IC design the calculation of temperature distribution is important because temperature affects both IC reliability and performance. It can be performed in two ways: Thermal Analysis and Electro-thermal simulation.

4.2.3.1 Thermal analysis

In case of thermal analysis during the calculation of temperature distribution, it is assumed that the power dissipation pattern is known and is realized through the solution of heat flow equation (Figure 10).

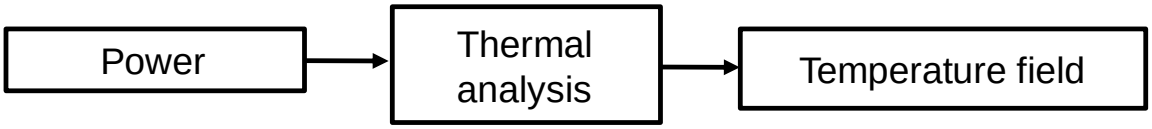


Fig. 10 Thermal Analysis

The idea of electrical analogy of temperature is in the base of electro-thermal simulation. It means that steady-state heat flow can be described by a resistive electrical network (Figure 11).

Electrical Analogy

$P = \frac{T_2 - T_1}{R_{TH}}$	$I = \frac{V_2 - V_1}{R}$
P	I
R_{TH}	R
T	V

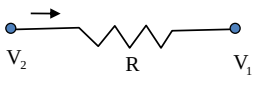


Fig. 11 Electrical analogy

The awareness of thermal issues and the need for thermal co-design has increased over the past few years. Thermal behaviour of ICs can be effectively improved by means of layout optimization and/or technology: thermal vias, substrate thinning, thermal shunts. The thermal optimization process, however, is not simple to accomplish due to the complex nature of 3D heat spreading effects and nonlinear thermal behaviour of solid-state devices. In addition, design criteria suggested by thermal optimization are often in conflict with other requirements, such as device downscaling and minimum thickness of the substrate. To solve this problem, it has become essential to resort to electro-thermal simulation tools, which determine, in a consistent manner, the electrical behaviour and the temperature distribution based on known circuit topology, layout, characteristics of the devices and input power.

4.2.3.2 Electro-thermal analysis

In case of electro-thermal analysis, it is assumed that the current itself is a function of device temperature and the determination of device current (i.e. power) and temperature is realized as a solution of coupled problem. IC electro-thermal simulation provides the possibility of examining the effects on device performance of structure and layout, without the need of making expensive prototype fabrication and characterization runs. Moreover, it helps in the choice of a suitable package, by indicating if the simulated package gives rise to an acceptable hot spot, or if a cheaper package could be used.

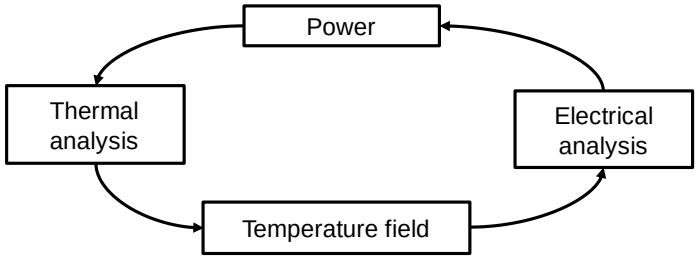


Fig. 12 Electro-thermal simulators

Electro-thermal simulators differ from circuit simulators as new features have been added. Firstly, devices are modelled by compact models provided by a thermal node. Secondly, thermal models are implemented for the evaluation of the temperature distribution on the basis of the power dissipated by the devices.

Creation of electro-thermal simulator is possible both on the basis of the present circuit simulators and by creating specific simulators. In the first case, the development of an integrated design platform, including a module for electro-thermal analysis, becomes possible. Besides, use of advanced device compact models and of different simulation modes (DC, AC, transient, etc.) is available. If thermal node is not available in the existing standard circuit simulator, a complex macro-model has to be built to introduce a thermal node.

In the second case, simple compact models tailored for specific applications can be easily implemented. Simple circuit construction from layout data becomes possible.

4.2.3.3 Compact Thermal Models

At present, the following electro-thermal simulation models are used: physical device simulation, including heat conduction, and electro-thermal simulation, using circuit simulation for the electrical analysis. The latter, in its turn, can be carried out by means of numerical methods, analytical methods and compact thermal models. In case of compact thermal models, temperature at device nodes and heat fluxes are expressed by simple relations that can be represented by simple equivalent electrical circuits.

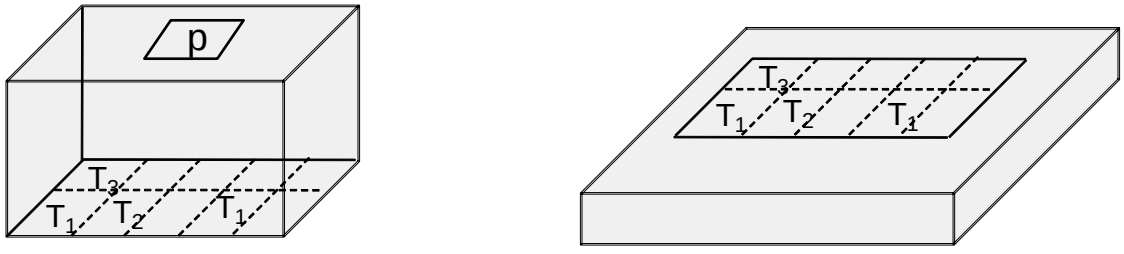


Fig. 13 Electro Thermal Simulators

Electro-thermal simulation of ICs can be realized by partitioning it in subparts with simple geometry (Figure 13). For each subpart a boundary condition independent (BCI) model is developed to distinguish the boundaries where heat exchange occurs in small elements whose temperature is assumed to be uniform.

Steady state model parameters are determined either by analytical models, or numerical simulation, or experimental measurements. In case of numerical simulation or experimental measurements for the transient analysis, thermal impedances can be approximated with a lumped element network. It can be represented by Cauer or Foster network (Figure 14) with 6-8 RC pairs.

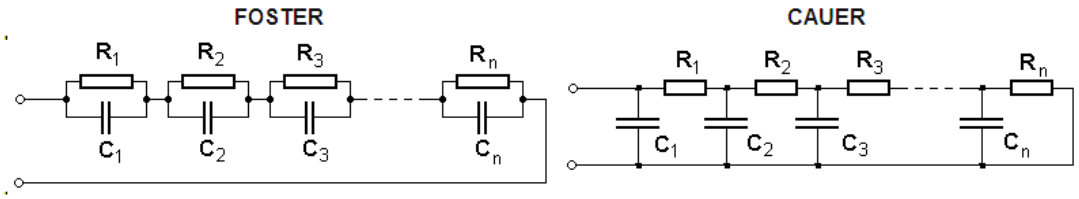


Fig. 14 Foster and Cauer Network

4.2.3.4 Electro-Thermal Simulation in 3D

In parallel to the development of IC fabrication technologies, chip areas and wire lengths continue to increase, causing problems as increased interconnect delays, power consumption and temperature. They have serious implications on reliability, performance and design effort. Three dimensional (3D) technology attempts to overcome some of these limitations by stacking multiple active layers into a monolithic structure (Figure 15). By expanding vertically rather than spreading out over a larger area, the chip space is better used, interconnects are decreased and transistor packing densities are increased, leading to better performance and power efficiency. Despite the advantages that 3D ICs have over 2D ICs, thermal effects are expected to be more pronounced because of higher power densities and greater thermal resistance along heat dissipation paths. With the advent of better processing technologies for 3D ICs, a

necessity has risen to create electro-thermal simulation tools functioning on new principles. Current electro-thermal simulation tools used for 2D ICs cannot be easily extended to 3D ICs. That is why the next development trend of electro-thermal simulation is conditioned by the development of 3D electro-thermal simulation methods and algorithms.

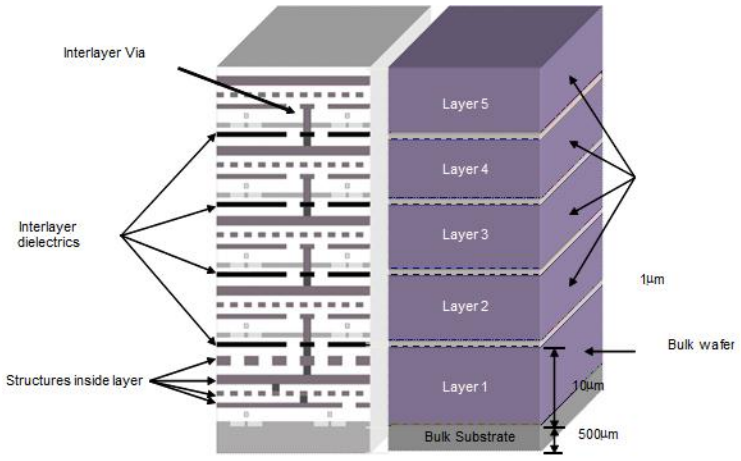


Fig. 15 3D IC Structure

In case of 3D, macroscale thermal analysis for full-chip profiles is already required such as against nanoscale analysis, considering electron-phonon interactions, because switching gates/blocks already act as heat sources (Figure 16) and time constants for heat of the order of ms or more. In this case, thermal equation represents partial differential equation, boundary conditions corresponding to the ambient, heat sink, etc. Self-consistency occurs as power is a function of temperature, which is a function of power. It is often handled using iterations. Finite difference method or finite element

method are also used for solution.

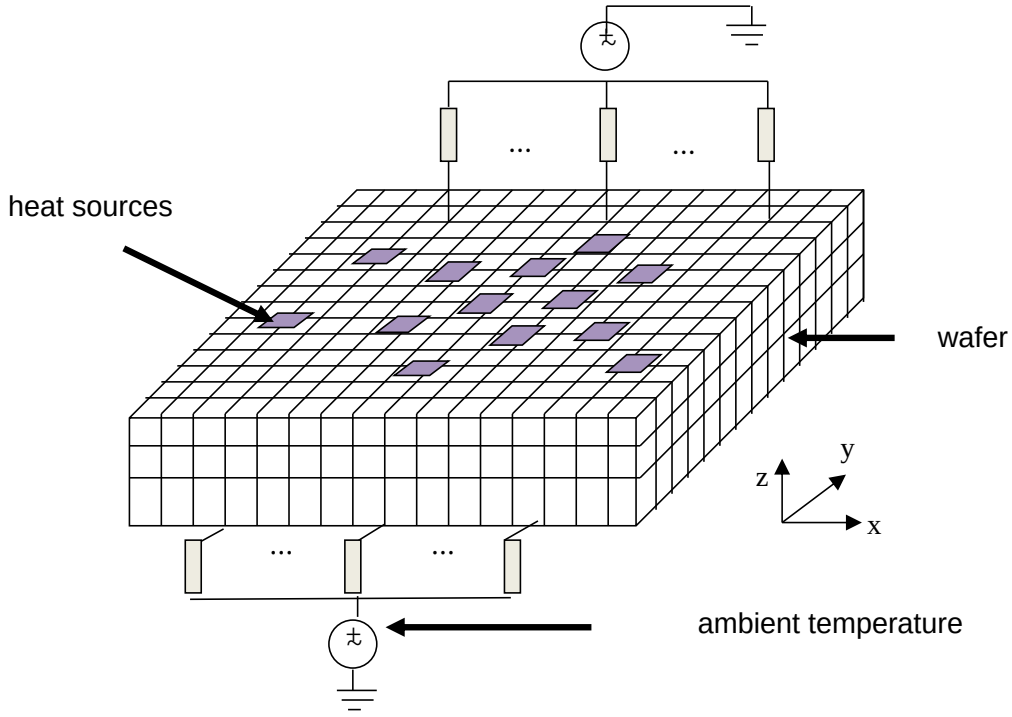


Fig. 2 Modelling heat sources in a 3D IC

4.2.4 Characterization tools

4.2.4.1 Thermal Models

Characterization tools play a key role in the definition of the impact areas the project targets. Within the THERMINATOR Project we set the premises for creating innovative models that combine the thermal behavior of the devices in a spice-like model card. The deliverables achieved in the project are only a first necessary step that traces the path for additional research and development activities that will take place even after the THERMINATOR duration.

By Characterization Tools we intend several kinds of tools that in the preliminary part of the project have been used for defining modeling and simulation methods and flows.

At project conclusion, putting together the most relevant results obtained in the modeling activities, new EDA tools aimed at characterizing silicon structures from the thermal point of view will be implemented according the EDA SW houses roadmaps.

While the results obtained will be immediately exploited by the industrial partners even in the project lifetime, after the project conclusion the SW houses shall evaluate the produced deliverables to exploit the project results in the best way.

It is important to better understand which characterization area the project activities impact. In general terms, we shall produce innovative thermal models and methodologies aimed at producing such models, able to better represent the silicon thermal behavior both in integrated circuits, discrete power devices and modules that could be used in all those tools that need *to fit the device electrical characteristics coming from measurements or TCAD simulations in relation to the device thermal behavior into a spice-like model card that can be simulated*. As example we mention the discrete power device thermal modeling field. This area imposes an accurate analysis on thermal effects since discrete power devices often cope with considerable amount of power. The right evaluation through opportune models of temperature variations will affect several device aspects, where the most important is, of course, its lifetime

estimation. This aspect has a particular relevance to the customers that must guarantee the final products in terms of reliability. In this particular case an innovative distributed thermal model has been developed (Figure 17) allowing designers to characterize discrete components (Power MOSFET, power BIPOLARS, IGBT, etc.) by using an approach that today is not possible to adopt with standard commercial tools. Through this approach it will be possible to predict how the temperature evolves on the device die during its active working condition. ***It is important to highlight that this methodology will take into account, at the same time, electrical and thermal behavior, so overcoming limits of main FEM tools that do not take into account, at the same time, both phenomena***. This new method will imply the use of a new thermal model whose use will be integrated in the flow.

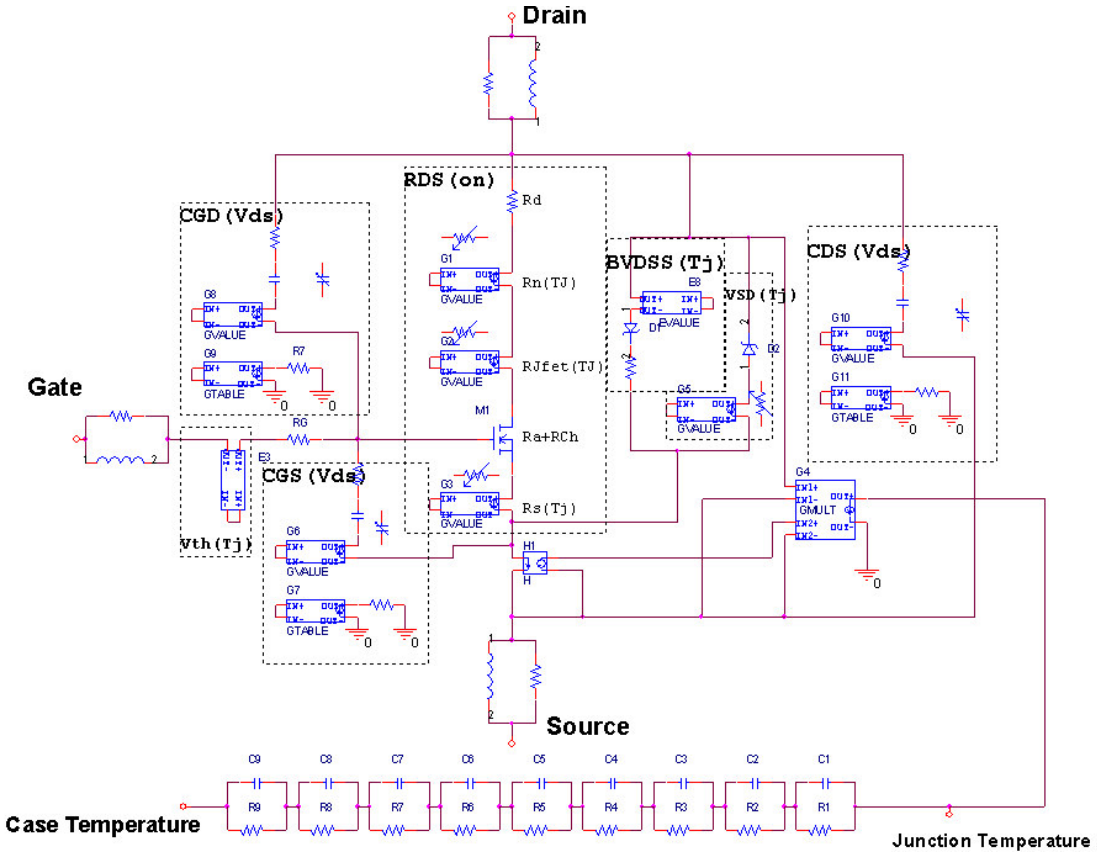


Fig. 17 Self-Heating power MOSFET macro model.

Even if this short analysis refers to discrete power devices, the same considerations hold valid for other characterization contexts.

The new models will require new accuracy and features from the characterization tools that shall open new topics of research in the field even after the THERMINATOR project conclusion.

4.2.5 Analog/RF Circuit design tools

4.2.5.1 Circuit analysis in presence of high temperatures and on-chip thermal gradients

Identifying suitable methodologies and tools for an accurate circuit analysis at high temperature and on-chip thermal gradient is of key importance to address the latest design requirements.

Firstly, it is no longer enough to rely on old methodologies based on the assumption that a specific temperature value will remain constant throughout all the performances. According to the old approaches, the operating parameters (temperature, power supply) were crossed to take into account all the possible operating conditions which could change the specifications of the circuit.

At the same time, higher order non-linearites and tightened time frame cannot be faced by the usage of the still widely spread analog manual design approaches determined by the designer capabilities.

Secondly, the growing power dissipated in different parts of the full chip area requires new electro-thermal models to better address the increasing impact of the thermal gradient, mainly generated by power MOS seen as a heat source.

At present, the high temperature effects have been successfully tackled by the newest design methodologies – based on analog/mixed signal simulators aimed at performing circuit analysis and optimization at different levels of abstraction.

In the near future, the new technological requirements should take into account the aforementioned thermal gradient effects in order to achieve first silicon success.

Once these electro-thermal models become available, a concurrent solution covering all the thermal behaviours for the whole system will likely overcome most of the thermal issues and in turn enhance the circuit robustness.

Basically, the released electro-thermal models allow the designer community to run specific electro-thermal simulation at different levels of abstraction as well as to perform analyses and optimisations once the above concurrent effects will lead the circuit out of specifications.

5 Conclusions

The process of designing and implementing a chip requires a large collection of *techniques*, or *tools*, and an effective *methodology* by which a designer's input predictably leads to a manufacturable product. While considerable attention is given to the tools needed, the equally important subject of design methodology is often neglected. Each technology generation requires designers to consider more issues; hence, new analysis methods and tools must be developed to evaluate new phenomena and aid the designer in making critical design decisions. An even greater challenge is to determine the most effective sequence in which issues should be considered and design decisions made, so as to minimize iterations.

With the transition from microelectronics to nanoelectronics along "More Moore" and "More than Moore," inevitably the paradigm shifts in the design of silicon systems. This affects all levels of the design process, and requires enormous effort toward new methodologies and tools.

DT must enable the creation of highly complex yet cost-efficient silicon system solutions, while exploiting all available opportunities afforded by nanoelectronics. For innovative applications to become affordable, daunting EDA challenges must be overcome. Shrinking of silicon devices and related fabrication processes has been the foundation for ever more powerful integrated silicon solutions that permeate daily life. Delivery of such silicon solutions has relied on the availability of EDA and design technologies that smoothly transform specification data into manufacturing-ready layout data, and perform necessary verifications at different levels of abstraction. However, the continued availability of such design technologies can no longer be taken for granted.

Cost and time-to-market of new SoCs requires DT that spans all parts of a complex design process which consists of two main elements: the implementation and the verification.

Regardless of the sequence in which issues will be considered and design decisions will be made, thermal management of the electronic systems is required to ensure their functionality. Thermal management has become increasingly challenging with the trend

toward miniaturization and the demand for integrating greater capabilities into an advanced electronic device.

As a consequence, thermal management cannot be treated as an afterthought anymore: it must be an integral part of the system design.