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Modelling, Control and Management of Thermal Effects in Circuits of the Future

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Preliminary THERMINATOR Roadmap

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3 References

IPCA – THERMINATOR Consortium Agreement,
D8.4.1 "First Release of Market Survey"

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Remark

In addition to the THERMINATOR consortium, the content of this document is considerably complemented with projected data and statistics coming from reference organizations, mainly from **ITRS** (**I**nternational **T**echnology **R**oadmap for **S**emiconductors).

As the majority of the partners are members of ITRS to refer to such documents was the most effective way to not duplicate unnecessarily the effort and to be sure to not break any confidentiality, as the matter is quite sensitive.

1 THERMINATOR Roadmap: Objective

The objective of this deliverable is to provide a document of the THERMINATOR roadmap covering the aspects of modelling, design and EDA, looking at the future.
This document will serve as guideline for the Consortium to be prepared for the new users requirements.
Roadmap will provide an outlook of needs and trends for future technologies, methodologies and tools and has been done based on the THERMINATOR experience which is wholesome in the different design domains and at all level of abstraction, the reader can easily refer to the different THEMINATOR WPs, if this has not been done by the author it is to not heavy the reading.
THERMINATOR activity has sorted or proposed a solution for many of the current thermal issues but the investigations have also set the path for future developments and research activities.

2 THERMINATOR Roadmapping Committee

The road mapping effort spans the entire duration of the project, the THERMINATOR Board Committee has nominated the Road mapping Committee. This Committee includes representative of the partners organisation involved in the task as stated in milestone MS841. The Exploitation Manager drives the activity of the committee. In spite of the vacancy of the role of the Exploitation Manager the activities have been carried on by the partners, the late nomination of the manager has permitted a coordination of the works and the organic collection of the outcomes inside this report.

3 THERMINATOR Roadmap: Introduction

For more than four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in the following Tables with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles roughly every 24 months).
The goal of the semiconductor industry is to be able to continue to scale the technology in overall performance. The performance of the components and the final chip can be measured in many different ways; higher speed, higher density, lower power, more functionality, etc.
Traditionally, dimensional scaling had been adequate to bring about these aforementioned performance merits but it is no longer so. Processing modules, tools, material properties, etc., are presenting difficult challenges to continue scaling.
Scaling may also lead to an effective increase of the stress factors. First, the current density is increasing and this increase impacts interconnect reliability. Second, voltages are often scaled down more slowly than dimensions, leading to increased electric fields that impact insulator reliability. Third, scaling has led to increasing power dissipation that results in higher chip temperatures, larger temperature cycles, and increased thermal gradients, all of which impact multiple failure mechanisms. The temperature effects are further aggravated by the reduced thermal conductivity that accompanies the reduction in the dielectric constant of the dielectrics between metal lines.

3.1 Decreasing cost-per-function

The most significant trend is the decreasing cost-per-function, which has led to major improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics and the pervasiveness in everyday life.

Improvement Trends for ICs Enabled by Feature Scaling

TREND	IMPACT
Integration Level	Components/chip, Moore's Law
Cost	Cost per function
Speed	Microprocessor throughput
Power	Laptop and cell phone's battery life
Compactness	Small and light-weight products
Functionality	Nonvolatile memory, imager

All of these improvement trends, sometimes called "scaling trends", have been enabled by large R&D investments. In the last three decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for

Semiconductors (NTRS), which had 1992, 1994, and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of the Roadmap and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999.

3.2 Markets Drivers

Future semiconductor manufacturing and design technology capability is developed in response to economic drivers within the worldwide semiconductor industry. Today, introduction of new technology solutions is increasingly application-driven – i.e., *applications drive technology.* Computer microprocessors have been joined as drivers by mixed-signal systems, battery-powered mobile devices, wall-plugged consumer devices, and networking devices. In-house chip designs are replaced by system-on-chip (SoC) and system-in-package (SiP) designs that incorporate building blocks from multiple sources.

So far, microprocessors, memories, and logic devices strongly rely on silicon-based CMOS technologies. The downscaling of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. The essential functions on such a system-on-chip (SoC) are data storage and digital signal processing. However, many quantitative requirements, such as power consumption (both dynamic and leakage power), communications bandwidth and many functional requirements, such as analog and RF components, sensors and actuators and even embedded software functions, do not scale with Moore's Law.

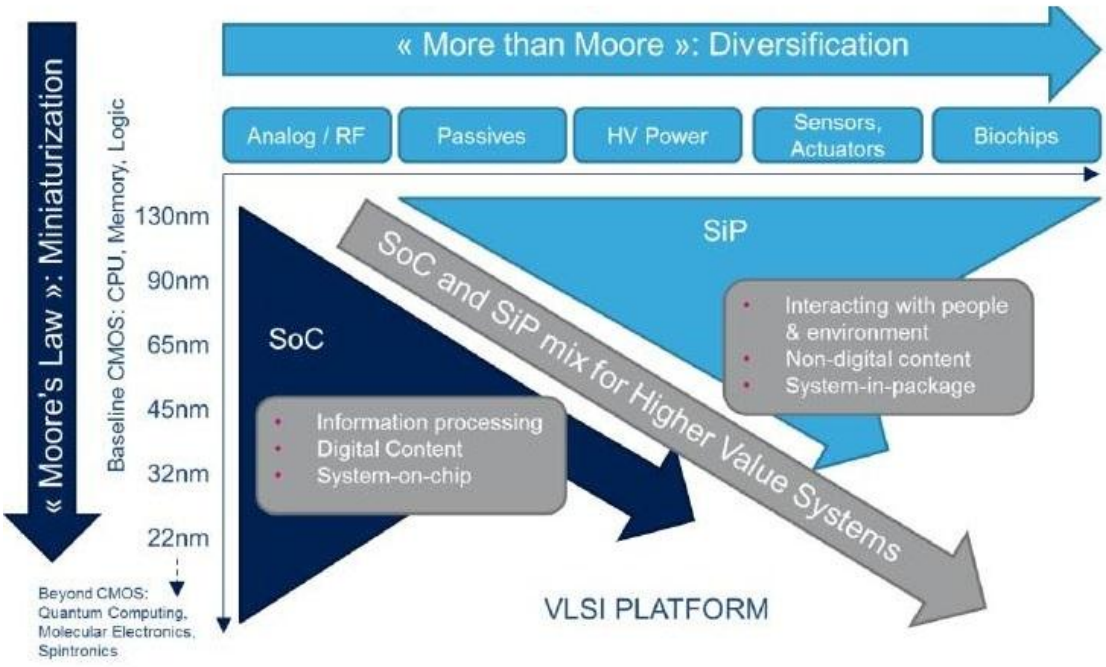

Fig. 1 Moore's Law and More than Moore.

This concept (see Fig. 1) has been established and pushed forward by ENIAC-JTI (European Technology Platform on Nanoelectronics) during 2005-2006 and refined, making a successfully fertilization, through ITRS and SIA.

3.3 "More Moore" vs. "Moore than Moore"

As a consequence, general consensus has been reached on the following peculiar definitions:

Scaling ("More Moore," Fig. 1 vertical axis)

Scaling is a continued shrinking of physical feature sizes of the *digital* functionalities (logic and memory storage) in order to improve *density* (cost per function reduction) and *performance* (speed, power).

Functional Diversification ("More than Moore", Fig. 1 horizontal axis)

Functional diversification is the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law", but provide additional value in different ways. The "More-than-Moore" approach allows for the ***non-digital*** **functionalities** to migrate from the system board-level into the package (SiP) or onto the chip (SoC).

It should be emphasized that "More-than-Moore" technologies do not constitute an alternative or even competitor to the digital trend as described by Moore's Law. In fact, it is the heterogeneous integration of digital and non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security and entertainment. Whereas "More Moore" may be viewed as the brain of an intelligent compact system, "More-than-Moore" refers to its capabilities to interact with the outside world and the users.

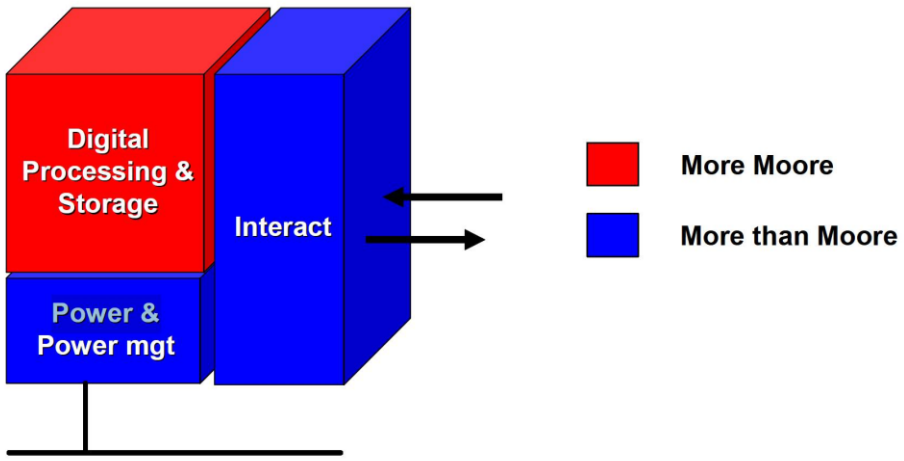

Fig. 2"More-than-Moore" devices complement the digital processing and storage elements of an integrated system in allowing the interaction with the outside world and in powering the system.

In order to identify relevant MtM devices and technologies to be roadmapped, one may start in looking for suitable markets and applications, derive then underlying functionalities and devices. A set of associated parameters and processes will be derived.

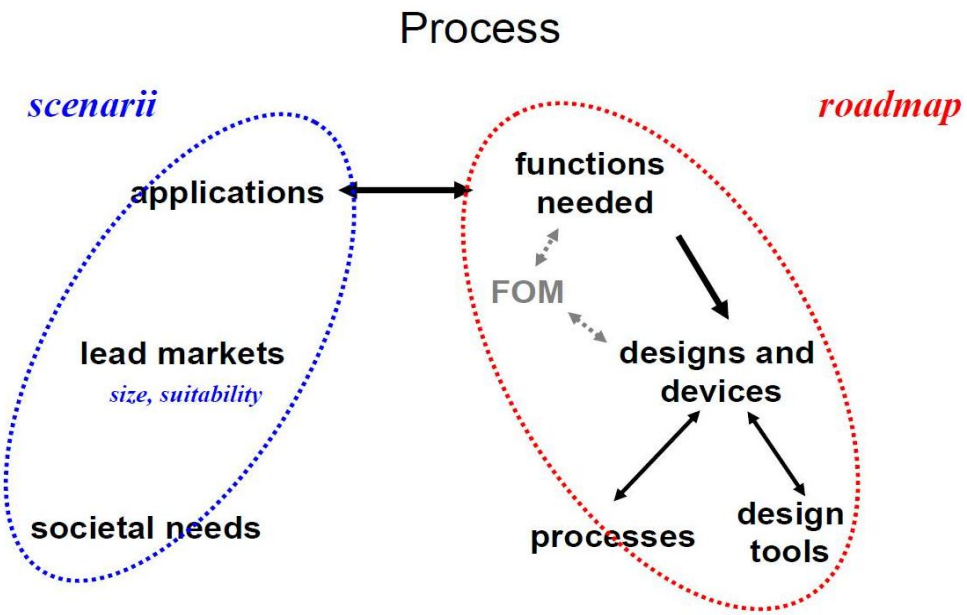

Fig. 3 From societal needs to markets.

Underlying the evolution of markets and applications, and therefore their economic potential, is their potential in addressing societal trends and challenges for the next decades. Societal trends can be grouped as health & wellness, transport & mobility, security & safety, energy & environment, communication and e-society (this latter term including infotainment). Many other names may be used but all cover more or less the same fields. These trends create significant opportunities in the markets of consumer electronics, automotive electronics, medical applications, communication, etc. Examples of applications linking societal trends and markets are given in the figure 4 below:

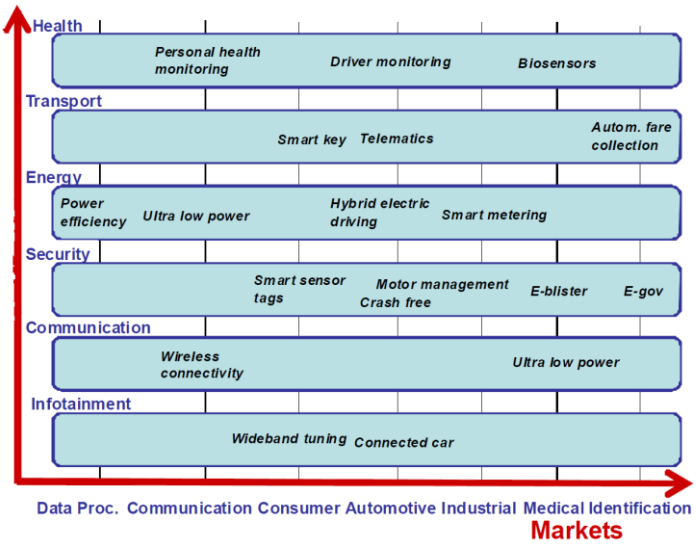

Fig. 4 Examples of applications liking societal trends and market.

4 THERMINATOR Roadmap: Topics of Relevance

As said in the initial remark, in addition to the THERMINATOR consortium the content of this document is valuably complemented with projected data and statistics coming from reference organizations, mainly from **ITRS**.
This Roadmap has been written in the spirit of defining what industry needs to develop in order to stay on Moore's Law and the other trends.
Within industry needs, the objectives of THERMINATOR project play a very important role. In fact, an unfortunate side effect of miniaturization and the continued scaling of CMOS technology is the ever increasing device power density with increasing difficulties in managing temperature. Moreover, neglecting *thermal* information during design may imply excessive over-design, due to the extremely conservative constraints that designers may pose in order to guarantee correct circuit operation under all possible running conditions. For these reasons the primary scientific and technical objective of the THERMINATOR project is to develop innovative design technologies for modeling, controlling, compensating and managing temperature in semiconductor circuits and systems to be manufactured with the most advanced processes and technologies (WP3-WP4). For what concern the power discrete devices (WP5) thermal modeling issues and estimation aspects are particularly important for high-voltage switching applications, where thermal effects have a huge impact.
Another important trend is the further increasing demand for *co-simulation* in various respects, including electro, *thermal* and mechanical effects, length scales from transistors through chips and packages to fabrication equipment, and covering not only performance but also **variability, reliability and reliability under variability**.
Co–simulation is also the MUST DO in the next future roadmap of SMART Power devices such as IPEM and the THERMINATOR experience is already influencing projects such as SMAC **Error! Reference source not found.**.
In the following sections of this report the need of "thermal awareness" will be highlighted in most of the items.

Key Lithography-related Characteristics by Product

Year of Production	***2011***	***2012***	***2013***	***2014***	***2015***	***2016***	***2017***	***2018***
DRAM ½ Pitch (nm) (contacted)	***36***	***32***	***28***	***25***	***23***	***20***	***17.9***	***15.9***
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	***30***	***32***	***27***	***24***	***21***	***18.9***	***16.9***	***15***
MPU Printed Gate Length (nm)	***35***	***31***	***28***	***25***	***22***	***19.8***	***17.7***	***15.7***
MPU Physical Gate Length (nm)	***24***	***22***	***20***	***18***	***17***	***15.3***	***14***	***12.8***
ASIC/Low Operating Power Printed Gate Length (nm)	***41***	***35***	***31***	***25***	***22***	***19.8***	***17.7***	***15.7***
ASIC/Low Operating Power Physical Gate Length (nm)	***26***	***24***	***21***	***19.4***	***17.6***	***16***	***14.5***	***13.1***
Flash ½ Pitch (nm) (un-contacted Poly)(f)	***22***	***20***	***18***	***17***	***15***	***14.2***	***13***	***11.9***

Notes for Table*: The technology requirements are intended to indicate current best estimates of introduction timing for specific technology requirements*

4.1 Power Supply and Power Dissipation

Total power dissipation will be limited more by system level cooling and test constraints than packaging.

Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
DRAM ½ Pitch (nm) (contacted)	36	32	28	25	23	20	17.9	15.9
Flash ½ Pitch (nm) (un-contacted Poly)(f)	22	20	18	17	15	14.2	13	11.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	38	32	27	24	21	18.9	16.9	15
MPU Physical Gate Length (nm)	24	22	20	18	17	15.3	14	12.8
Power Supply Voltage (V)								
Vdd (high-performance)	0.9	0.87	0.85	0.82	0.80	0.77	0.75	0.73
V_{dd} (Low Operating Power, high V_{dd} transistors)	0.93	0.90	0.87	0.84	0.81	0.78	0.75	0.72
Allowable Maximum Power								
High-performance with heat sink (W)	161	158	149	152	143	130	130	136
Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation	260	260	260	260	260	260	260	260
Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation	0.52	0.51	0.48	0.49	0.46	0.42	0.42	0.44
Cost-performance (W)	161	158	149	152	143	130	130	136
Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation	140	140	140	140	140	140	140	140
Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation	1.13	1.11	1.10	1.17	1.19	1.07	1.12	1.19
Battery (W)—(low-cost/hand-held)	3	3	3	3	3	3	3	3

4.2 Cost of manufacturing

Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
DRAM ½ Pitch (nm) (contacted)	36	32	28	25	23	20	17.9	15.9
Flash ½ Pitch (nm) (un-contacted Poly)(f)	22	20	18	17	15	14.2	13.0	11.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	38	32	27	24	21	18.9	16.9	15.0
MPU Physical Gate Length (nm)	22	20	18	17	15.3	14.0	12.8	11.7
Affordable Cost per Function ++								
DRAM cost/bit at (packaged microcents) at samples/introduction	0.66	0.46	0.33	0.23	0.16	0.12	0.082	0.058
DRAM cost/bit at (packaged microcents) at production §	0.24	0.17	0.12	0.08	0.06	0.04	0.030	0.021
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	5.50	3.89	2.75	1.94	1.38	0.97	0.688	0.486
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	3.33	2.35	1.66	1.18	0.83	0.59	0.416	0.294
High-performance MPU(microcents/transistor) (including on-chip SRAM) at production §§	3.04	2.15	1.52	1.08	0.76	0.54	0.380	0.269

4.3 High-Performance MPU/ASIC and Chip Size

Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
DRAM ½ Pitch (nm) (contacted)	36	32	28	25	23	20.0	17.9	15.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	38	32	27	24	21	18.9	16.9	15.0
MPU Physical Gate Length (nm)	24	22	20	18	17	15.3	14.0	12.8
Logic(Low-volume Microprocessor)High-performance‡								
Generation at Introduction	p13h	p13h	p16h	p16h	p16h	p19h	p19h	p19h
Functions per chip at introduction (million transistors)	8,848	8,848	17,696	17,696	17,696	35,391	35,391	8,848
Chip size at introduction (mm^2)	520	368	520	413	328	520	413	328
*Generation at production ***	p11h	p11h	p13h	p13h	p13h	p16h	p16h	p16h
Functions per chip at production (million transistors)	4,424	4,424	8,848	8,848	8,848	17,696	17,696	17,696
Chip size at production (mm^2) §§	260	184	260	206	164	260	206	164
HighperformanceMPUMtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	1,701	2,406	3,403	4,287	5,402	6,806"	8,575	10,804
ASIC								
ASIC usable Mtransistors/cm^2 (auto layout)	1,701	2,406	3,403	4,287	5,402	6,806	8,575	10,804
ASIC max chip size at production (mm^2) (maximum lithographic field size)	858	858	858	858	858	858	858	858
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	14,599	20,646	29,198	36,787	46,348	58,395	73,573	92,697

4.4 Lithographic-Field and Wafer-Size

Year of Production *Lithography Field Size*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
Maximum Lithography Field Size—area (mm^2)	858	858	858	858	858	858	858	858
Maximum Lithography Field Size—length (mm)	33	33	33	33	33	33	33	33
Maximum Lithography Field Size—width (mm)	26	26	26	26	26	26	26	26
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)								
Bulk or epitaxial or SOI wafer	300	300	300	300	300	300 or 450	300 or 450	300 or 450

4.5 Performance of Packaged Chips: Number of Pads and Pins

Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
DRAM ½ Pitch (nm) (contacted)	22	20	18	17	15	14.2	13.0	11.9
Flash ½ Pitch (nm) (un-contacted Poly)(f)	36	32	28	25	23	20.0	17.9	15.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	38	32	27	24	21	18.9	16.9	15.0
MPU Physical Gate Length (nm)	35	31	28	25	22	19.8	17.7	15.7
Number of Chip I/Os (Number of Total Chip Pads)—Maximum								
Total pads—MPU unchanged	"3,072"	"3,072"	"3,072"	"3,072"	"3,072"	"3,072"	"3,072"	"3,072"
Signal I/O—MPU (% of total pads)	33.3%	33.3%	33.3%	33.3%	33.3%	33.3%	33.3%	33.3%
Power and ground pads—MPU (% of total pads)	66.7%	66.7%	66.7%	66.7%	66.7%	66.7%	66.7%	66.7%
IS: Total pads—ASIC High Performance unchanged	"4,800"	"5,000"	"5,400"	"5,400"	"5,600"	"6,000"	"6,000"	"6,200"
Signal I/O pads—ASIC high-performance (% of total pads)	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%
Power and ground pads—ASIC high-performance (% of total pads)	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%
Number of Total Package Pins—Maximum [1]								
Microprocessor/controller, cost-performance	720-3061	720–3367	800–3704	800-4075	880–4482	880–4930	960-5423	960–5966
Microprocessor/controller, high-performance	5094	5348	5616	5896	6191	6501	6826	7167
ASIC (high-performance)	5094	5348	5616	5896	6191	6501	6826	7167

4.6 Performance and Package Chips: Frequency On-chip Wiring Levels

Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
DRAM ½ Pitch (nm) (contacted)	36	32	28	25	23	20.0	17.9	15.9
Flash ½ Pitch (nm) (un-contacted Poly)(f)	22	20	18	17	15	14.2	13.0	11.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	38	32	27	24	21	18.9	16.9	15.0
MPU Physical Gate Length (nm)	24	22	20	18	17	15.3	14.0	12.8
Chip Frequency (GHz)								
On-chip local clock [1]	3.744	3.894	4.050	4.211	4.380	4.555	4.737	4.927
Maximum number wiring levels [3] [**]	12	12	13	13	13	13	14	14

4.7 System Drivers

As said above, the assumption that technological advances are deployed in all semiconductor products, independent of the specifics of key product classes, is no longer valid. Today, introduction of new technology solutions is increasingly application-driven – i.e., *applications drive technology*. Computer microprocessors have been joined as drivers by mixed-signal systems, battery-powered mobile devices, wall-plugged consumer devices, and networking devices. One more driver must be considered: the consumer stationary driver that represents a high-performance version of the increasingly important consumer electronics and digital TV market.

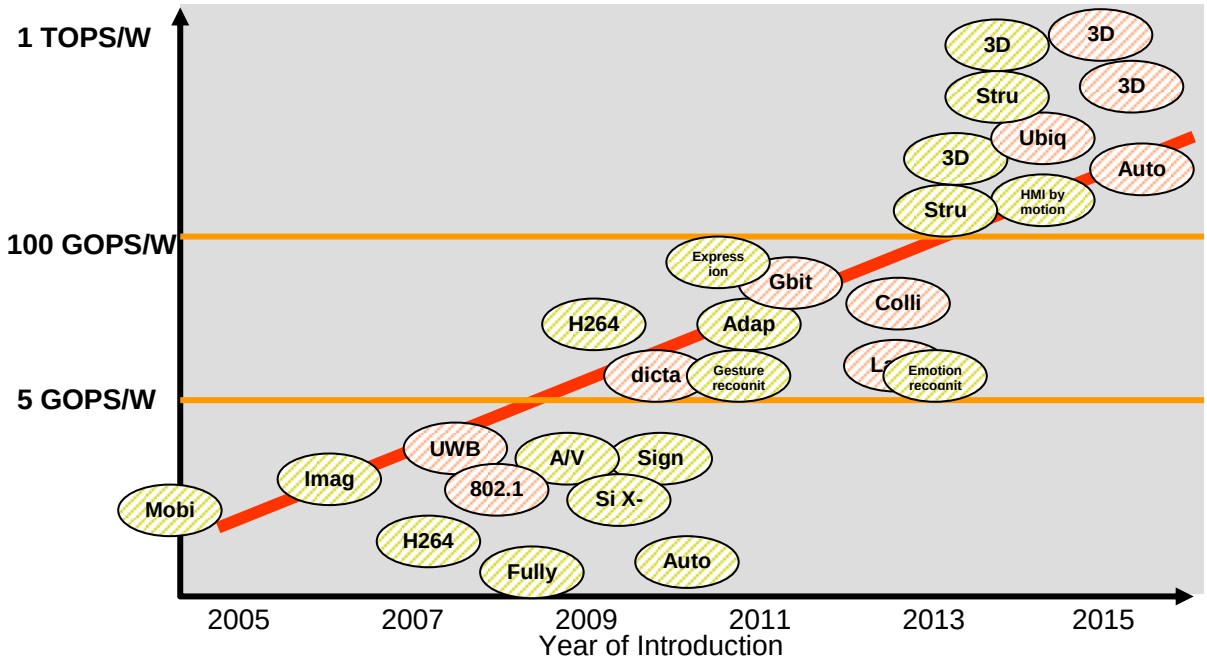

Fig. 5 Application rush [source STMicroelectronics].

4.7.1 Key Drivers

- **Power consumption: a first-class constraint**
  - Both for portable and non-portable applications
- **Highly parallel architectures**
  - Increasing number of "small" processing unit
- **System-On-Chip design techniques**
  - The System Drivers continues to evolve to include market-driven drivers that reflect the demands of a 21st-century roadmap. These driver segments include *Networking*, *Consumer stationary*, *Consumer mobile*, *Office / MPU*.

The long-term goal is to match system-level and chip-level requirements on a driver basis.

Major Product Market Segments and Impact on System Drivers.

Market Drivers	***SoC***	***Analog/MS***	***MPU***
	I. Portable/consumer		
1. Size/weight ratio: peak in 2004 2. Battery life: peak in 2004 3. Function: 2×/2 years 4. Time-to-market: ASAP	Low power paramount Need SoC integration (DSP, MPU, I/O cores, etc.)	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
	II. Medical		
1. Cost: slight downward pressure (~1/2 every 5 years) 2. Time-to-market: >12 months 3. Function: new on-chip functions 4. Form factor often not important 5. Durability/safety 6. Conservation/ ecology	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SoC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
	III. Networking and communications		
1. Bandwidth: 4×/3–4 years 2. Reliability 3. Time-to-market: ASAP 4. Power: W/m^3 of system	Large gate counts High reliability More reprogrammability to accommodate custom functions	Migrating on-chip for MUX/DEMUX circuitry MEMS for optical switching.	MPU cores, FPGA cores and some specialized functions
	IV. Defense		
1. Cost: not prime concern 2. Time-to-market: >12 months 3. Function: mostly on SW to ride technology curve 4. Form factor may be important 5. High durability/safety	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
	V. Office		
1. Speed: 2×/2 years 2. Memory density: 2×/2 years 3. Power: flat to decreasing, driven by cost and W/m^3 4. Form factor: shrinking size 5. Reliability	Large gate counts; high speed Drives demand for digital functionality Primarily SoC integration of custom off-the-shelf MPU and I/O cores	Minimal on-chip analog; simple A/D and D/A Video i/f for automated camera monitoring, video conferencing Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-position resolution	MPU cores and some specialized functions Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
VI. Automotive			
1. Functionality 2. Ruggedness (external environment, noise) 3. Reliability and safety 4. Cost	Mainly entertainment systems Mainly ASSP, but increasing SoC for high end using standard HW platforms with RTOS kernel, embedded software	Cost-driven on-chip A/D and D/A for sensor and actuators Signal processing shifting to DSP for voice, visual Physical measurement ("communicating sensors" for proximity, motion, positioning); MEMS for sensors	

SoC-CP Design Productivity Trends

The SoC Consumer Portable (SoC-CP) Driver increasingly represents SoC designs; it spans portable and wireless applications such as smart media-enabled telephones, tablets and digital cameras, as well as other processing purposes such as high-performance computing and enterprise applications. The SoC-CP driver is based on a model created by the Japan Semiconductor Technology Roadmap Design Group.

- Its typical application area is electronic equipment categorized as "Portable/Mobile Consumer Platforms", as this application area will make rapid progress in the foreseeable future across semiconductor technology generations.
- Typical requirements for this type of SoC ("Portable/Mobile Consumer Platforms") dictate a rapid increase in processing capability, despite an upper bound constraint on power to maintain battery lifetime. Processing power increases by 1000× in the next ten years, even as dynamic power consumption does not change significantly.
- Lifecycles of "Portable/Mobile Consumer Platform" products are and will continue to be short. Hence, design effort cannot be increased, and must remain at current levels for the foreseeable future.

Year of Production	***2011***	***2012***	***2013***	***2014***	***2015***	***2016***	***2017***	***2018***
Design block reuse [1] % of all logic	**54%**	**58%**	**62%**	**66%**	**70%**	**74%**	**78%**	**82%**
Requirement: Productivity for new designs (normalized to 2007)	**1.00**	**1.22**	**1.60**	**2.02**	**2.50**	**3.08**	**3.72**	**4.48**
Requirement: Productivity for reused designs (normalized productivity for new designs at 2007)	**1.00**	**1.22**	**1.60**	**2.02**	**2.50**	**3.08**	**3.72**	**4.48**

SoC-CP Driver Trends

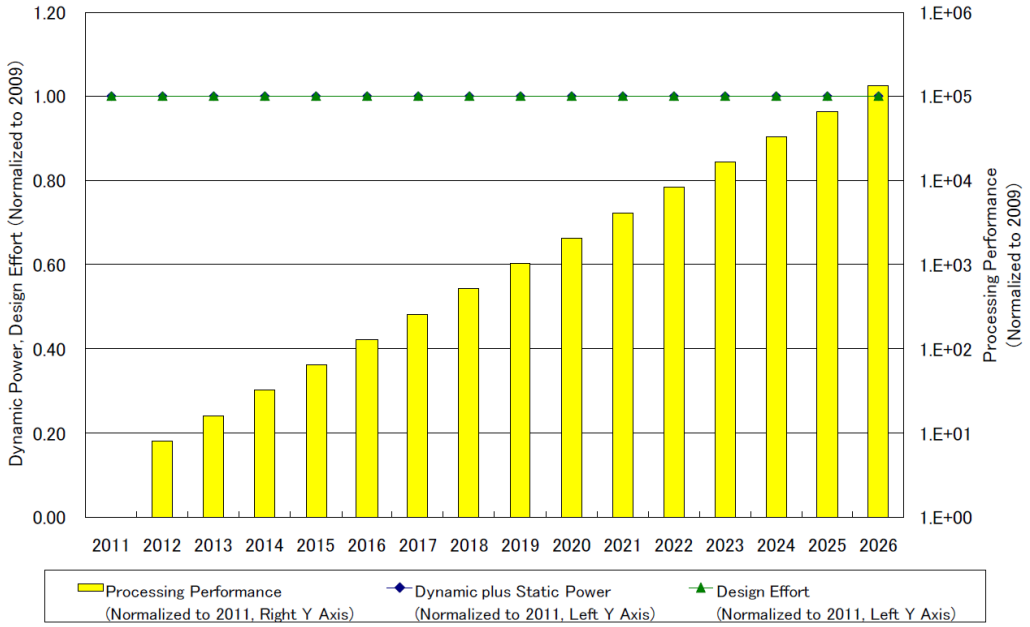

Fig. 6 Several Trends for the SOC Consumer Portable Driver.

SoC CONSUMER STATIONARY (SoC-CS) DRIVER

The SoC Consumer Stationary (SoC-CS) Driver represents SoC designs over a wide variety of applications in digital consumer electronic equipment, such as high-end game machines; these are assumed to be typically used in a tethered (non-mobile) environment. Key aspects of the model are as follows.

- Processing performance is the most important differentiator.

- Functions will be implemented and realized mainly by software. Thus, high processing power is required, and this SoC will have many Data Processing Engines (DPEs).
- In comparison with the SoC Consumer Portable driver, this driver has worse performance to power ratio, but superior functional flexibility to support adding or modifying functions.
- Because it is easy to add or modify functions, the lifecycle of SoC Consumer Stationary designs is relatively long, and as a result the application area is wide.

SoC CONSUMER STATIONARY PERFORMANCE TRENDS

The SoC Consumer Stationary driver's processing performance can be assumed proportional to the product of device performance and the number of DPEs on the SoC. Fig. 6 shows SoC Consumer Stationary processing performance trends. Required processing performance grows rapidly, by approximately 250x over the next fifteen years. Key potential solutions to achieve the required performance include various design technologies (particularly in the logical, circuit and physical design stages) to maximize circuit performance. Automated design methodologies such as high-level synthesis are of course important as well.

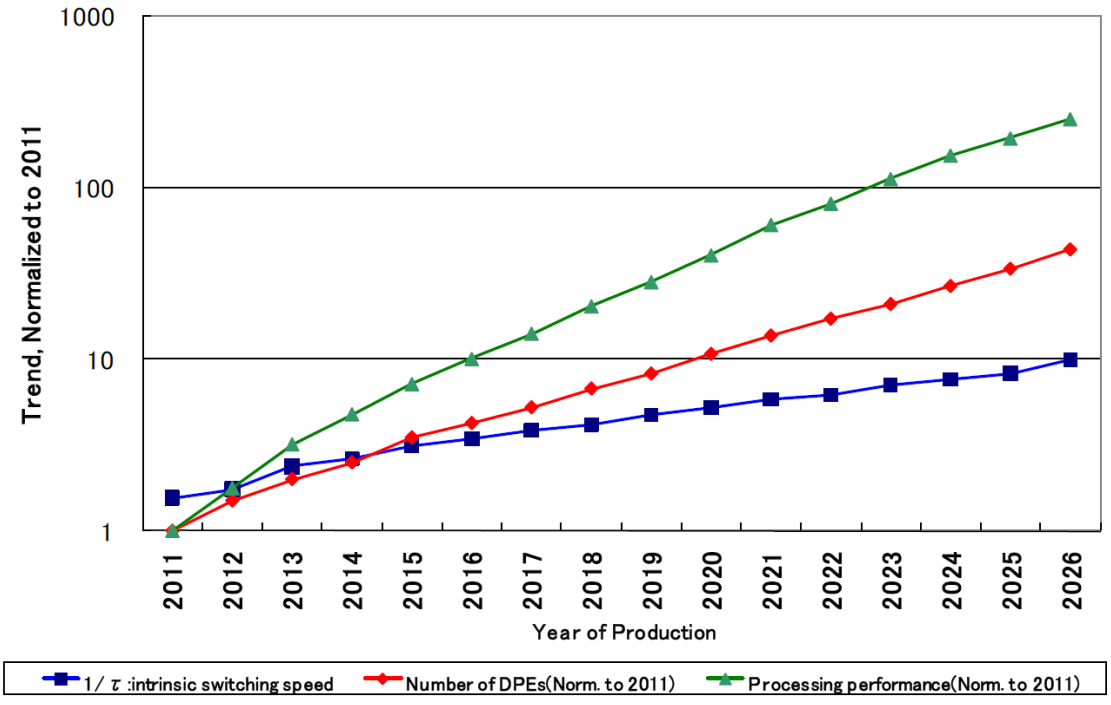

Fig. 7 SoC Consumer Stationary Performance Trends .

SoC CONSUMER STATIONARY POWER CONSUMPTION TRENDS

An explosion in power consumption will be a critical consideration for the design of future SoC Consumer Stationary chips. Fig. 7 shows the trend for total chip power, decomposed into switching and leakage power, across logic and memory. The analysis is based on transistor performance, interconnect performance parameters and the design complexity trends. We note the following.

- Unlike the SoC Consumer Portable Driver, the SoC Consumer Stationary Driver is generally free from battery life issues; however, the rapid increase in power consumption will result in critical chip packaging and cooling issues.
- Leakage power will be much greater than the calculated value shown in Fig. 7, due to variability and temperature effects.
- Power consumption per DPE will decrease according to trends for supply voltage and insulator dielectric constant. However, this will be outweighed by the increase in number of DPEs per chip.

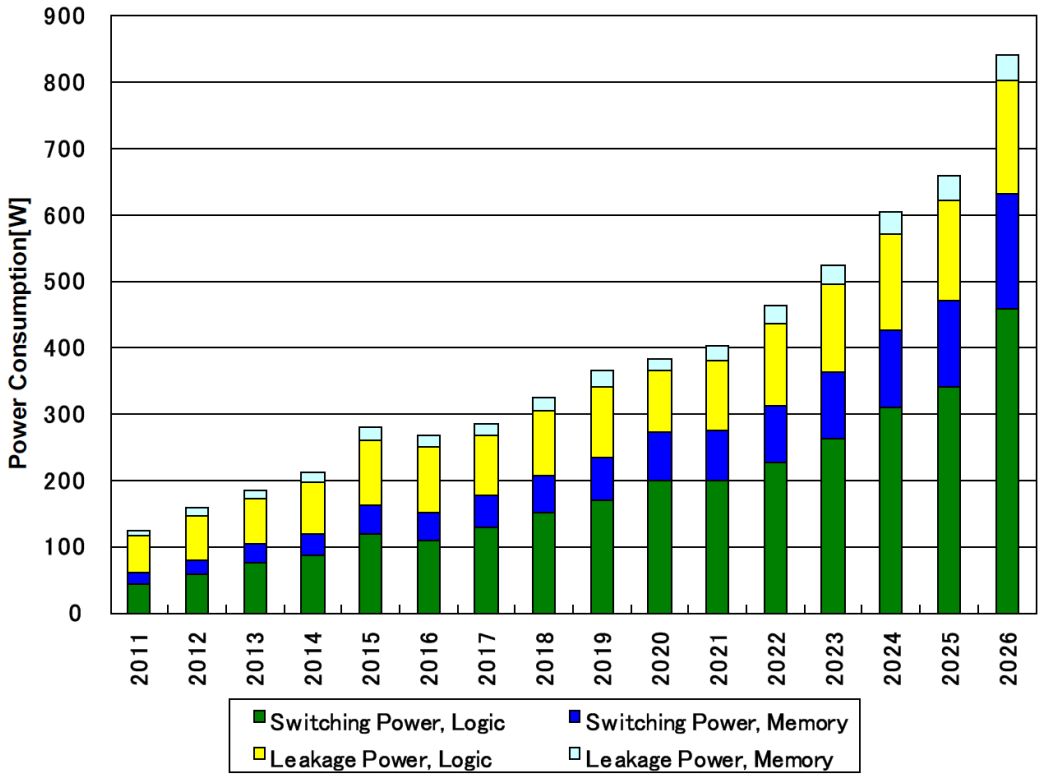

Fig. 8 SoC Consumer Stationary Power Consumption Trends.

Clearly, the trend in Fig. 7 highlights a pressing need to develop new solutions, beyond those already embedded in the technology roadmaps, so that actual power consumption remains within acceptable limits.

4.8 Design

The main message remains: cost (of design) is the greatest threat to continuation of the semiconductor roadmap. Cost determines whether differentiating value is best achieved in software or in hardware, on a programmable commodity platform, or on a new IC. Manufacturing non-recurring engineering (NRE) costs are on the order of millions of dollars (mask set + probe card); design NRE costs routinely reach tens of millions of dollars, with design shortfalls being responsible for silicon re-spins that multiply manufacturing NRE. Rapid technology change shortens product life cycles and makes time-to-market a critical issue for semiconductor customers. Manufacturing cycle times are measured in weeks, with low uncertainty. Design and verification cycle times are measured in months or years and this implies a high uncertainty.
ITRS have noted a **design productivity gap**: the numbers of available transistors growing faster than the ability to meaningfully design them. This gap impacts IC product value, placing at risk foundry amortization, return on investment (ROI) for supplier industries, and indeed the entire semiconductor investment cycle. Yet, investment in process technology continues to dominate investment in design technology. The DT (Design Technology) roadmap enables control of design costs.

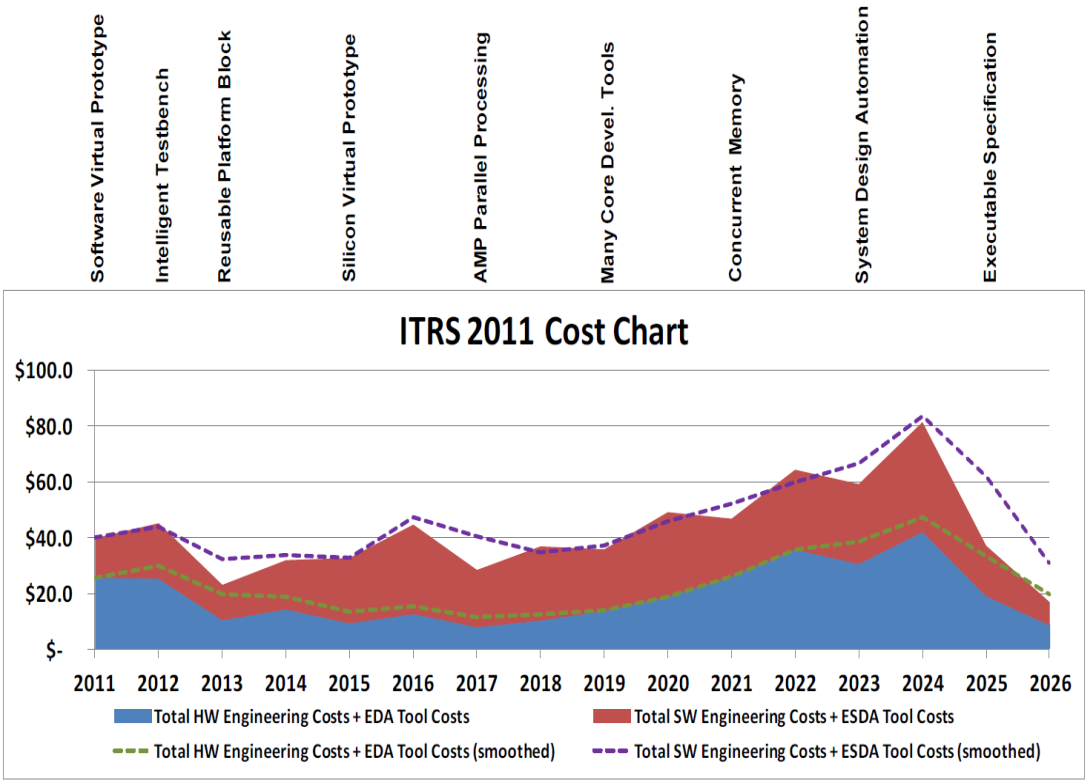

Fig. 9 ITRS 2011 Cost chart.

Table Overall Design Technology Challenges.

Challenges ≥ 22 nm	*Summary of Issues*
Design productivity	System-level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation Verification: executable specification, ESL formal verification, intelligent test bench, coverage-based verification Logic/circuit/physical: analog circuit synthesis, multi-objective optimization" Logic/circuit/physical: SiP and 3D (TSV-based) planning and implementation flows Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	Logic/circuit/physical: dynamic and static, system- and circuit-level power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Reliability	Logic/circuit/physical: MTTF-aware design, BISR, soft-error correction
Interference	Logic/circuit/physical: signal integrity analysis, EMI analysis, thermal analysis
Challenges <22 nm	*Summary of Issues*
Design productivity	Verification: complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage Tools specific for SOI and non-static logic, and emerging devices Cost-driven design flow
Power consumption	Logic/circuit/physical: SOI power management Logic/circuit/physical : Reliability and resilience- and temperature-constrained 3D physical implementation flows
Manufacturability	Uncontrollable threshold voltage variability Advanced analog/mixed signal DFT (digital, structural, radio), “statistical” and yield-improvement DFT Thermal BIST, system-level BIST
Reliability	Autonomic computing, robust design, SW reliability and resilience
Interference	Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.)

ATE—automatic test equipment BISR—built-in self repair BIST—built-in self test DFT—design for testability
EMI—electromagnetic interference ESL—Electronic System-level Design HW/SW—hardware/software
MTTF—mean time to failure SOI—silicon on insulator

4.9 Interconnect, SoC integration

The function of an interconnecting or wiring system is to distribute clock and other signals and to provide power/ground, to and among, the various circuit/system functions on a chip. The fundamental development requirement for interconnect is to meet the high-bandwidth low-power signalling needs without introducing performance bottlenecks as scaling continues.
One of the grand challenges for interconnect is the result of the rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity. These create integration, cost, and reliability challenges.
Another of the grand challenges is the variability associated with line edge roughness, trench and via depth and profile, etch bias, thinning due to cleaning and CMP as well as size effects.
Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.
Highlighting and differentiating the five key challenges in the near term (> 16 nm) and long term (< 16 nm) it's possible to say: in the near term, the most difficult challenge for interconnects is the introduction of new materials that meet the wire conductivity requirements and reduce dielectric permittivity; in the long term, the impact of size effects on interconnect structures must be mitigated.
Future effective κ requirements preclude the use of a trench etch stop for dual damascene structures. Dimensional control is a key challenge for present and future interconnect technology generations and the resulting difficult challenge for etch is to form precise trench and via structures in low-κ dielectric material to reduce variability in RC. The dominant architecture, damascene, requires tight control of pattern, etch and planarization. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. These dimensional control requirements place new demands on high throughput imaging metrology for measurement of high aspect ratio structures. New metrology techniques are also needed for in-line monitoring of adhesion and defects. Larger wafers and the need to limit test wafers will drive the adoption of more in situ process control techniques. Dimensional control, a challenge now, will become even more critical as new materials, such as porous low-κ dielectrics and ALD metals, play a role at the tighter pitches and higher aspect ratios (A/R) of intermediate and global levels.

Table Interconnect Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Material Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Manufacturable Integration Engineering manufacturable interconnect structures, processes and new materials*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Reliability Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.

Metrology Three-dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Cost & Yield for Manufacturability Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Difficult Challenges < 16 nm	*Summary of Issues*
Material Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity
Metrology Three-dimensional control of interconnect features (with its associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Process Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Complexity in Integration Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbates thermomechanical effects. Novel/active devices may be incorporated into the interconnection.
Practical Approach for 3D Identify solutions which address 3D structures and other packaging issues*	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

4.10 Modelling and Simulation

This is intended to further promote the usefulness of Modelling and Simulation to improve the physical understanding in semiconductor technology and to reduce development times and costs.

Technology Modelling and Simulation covers the region of the semiconductor modelling world called extended TCAD, and it is one of the few enabling methodologies that can reduce development cycle times and costs. Extended TCAD covers the following topical areas: 1) *Equipment/feature scale modelling*—hierarchy of models that allows the simulation of the local influence of the equipment (except lithography) on each point of the wafer, especially in deposition, etching and CMP processes, starting from the equipment geometry and settings; 2) *Lithography modelling*—modelling of the imaging of the mask by the lithography equipment, the photoresist characteristics and processing; 3) *Front end process modelling*—the simulation of the physical effects of manufacturing steps used to build transistors up to metallization, but excluding lithography; 4) *Device modelling*—hierarchy of physically based models for the operational description of active devices; 5*) Interconnect and integrated passives modelling*—the operational response (mechanical, electro-magnetic, and thermal properties) of back-end architectures; 6) *Circuit element modelling*—compact models for active, passive, and parasitic circuit components, and new circuit elements based on new device structures; 7) *Package simulation*—electrical, mechanical, and thermal modelling of chip packages; 8) *Materials modelling*—simulation tools that predict the physical properties of materials and, in some cases, the subsequent electrical properties; 9) *Reliability modelling*—the modelling of reliability and related effects on process, device and circuit level; 10) *Modelling for design robustness, manufacturing and yield*—the development of additional models and software to enable the use of TCAD to study the impact of inevitable process variations and dopant fluctuations on IC performance and in turn design parameters, manufacturability and the percentage of ICs that are within specifications; 11) *Numerical methods*—all algorithms needed to implement the models developed in any of the other sections, including grid generators, surface-advancement techniques, (parallel) solvers for systems of (partial) differential equations, and optimization routines. As shown in Fig. 9, these areas can be grouped into equipment, feature and IC-scale. Items 8 to 11 are unique because they in fact cross-cut almost all other topics in Modelling and Simulation. Material and reliability issues are becoming more and more important in all processes as well as for active devices and interconnect. Design robustness, manufacturing and yield are affected by all areas simulated. Numerical algorithms are shared by most of the areas in simulation.

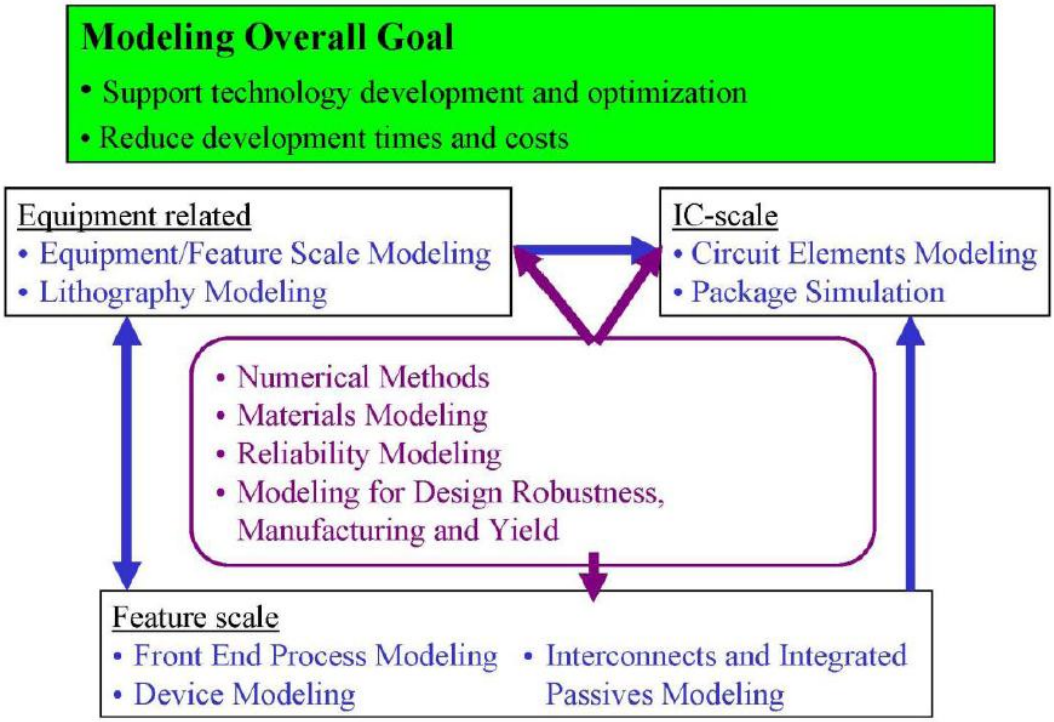

Fig. 10 Extended TCAD areas.

Concerning the short-term challenges:
Lithography simulation including EUV—Various tricks have been introduced to extend the applicability of optical lithography to even smaller dimensions, with substantial support from lithography simulation. The further technological development also requires large additional improvements in the area of lithography simulation, among others because the number of available resolution enhancement techniques increases.
Front-end process modelling for nanometer structures—This is the key challenge for the prediction of result from device fabrication. It overlaps to some extent with the challenge "Ultimate nanoscale CMOS simulation capability," which also includes materials and device simulation. Most important and challenging in the area of front-end process modelling is the modelling of ultra-shallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing and diffusion of dopants, and especially on activation and deactivation
Integrated modelling of equipment, materials, feature scale processes, and influences on devices—Variations of the results of a process step caused by the fabrication process and equipment used are key issues for manufacturability and yield of a technology. This refers especially to variations between neighbouring devices or non-homogeneities across the wafer or between different wafers, and to drifts of process results between maintenance of equipment, for example, due to coating of chamber walls.
Nanoscale device simulation capability: Methods, models and algorithms—A fundamental question of the microelectronics industry continues to be what are the ultimate limits of CMOS technology and devices. The key requirement to deal with this challenge is predictive simulation of materials, processes, and device behaviour including reliability.

Electrical-thermal-mechanical- modelling for interconnections and packaging—Performance and reliability of integrated circuits is increasingly affected by interconnects and packaging. Electrical, thermal, and mechanical properties highly interact with each other and must therefore be simulated together. Reliability issues requiring modelling include electromigration, stress voiding, integrity and adhesion of thin films, surface roughness, package fracture, and corrosion. Through Silicon Vias and thin stacked dies request new or largely extended simulation tools. Size effects (microstructure, surfaces) and variability of thinned wafers are important issues to be simulated. The capability to withstand the heat produced in the IC and to transport it off the chip is getting a top-level concern with further increasing densities.

Table Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 14 nm	*Summary of Issues*
Lithography simulation including EUV	Complementary lithography Simulation of defect inspection and characterization influences/defect printing. Mask optimization including defect repair or compensation Simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including EMF and resist effects, and extensions for inverse lithography Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects Predictive and separable resist models (e.g., mesoscale models) including line-edge roughness, accurate profiles, topcoat and substrate (under layer) interactions, etch resistance, adhesion, mechanical stability, leaching, swelling or slimming, and time-dependent effects in in single and multiple exposure Resist model parameter calibration methodology (including kinetic transport and stochastic parameters) Fast, predictive simulation of ebeam mask making (single-beam and multibeam) including short and long range proximity corrections Simulation of directed self-assembly of sublithography patterns Modeling lifetime effects of equipment and masks, including lens and mirror heating effects Predictive coupled deposition-lithography-etch simulation (incl. double patterning, self-aligned patterning) Modeling metrology equipment and data extraction for enhancing model calibration accuracy Modeling of pellicle effects and pellicle defects simulation (incl. double patterning, self-aligned patterning)
Front-end process modeling for nanometer structures	Coupled diffusion/(de)activation/damage/stress models and parameters including low-temperature, SPER, millisecond and microwave processes in Si-based substrate, that is, Si, SiGe, Ge-on-Si, III/V-on-Si (esp. InGaAs-on-Ge-on-Si), SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers. Accurate models for Stress-Induced Defects Implantation models for ions needed for new materials Models for alternative implantation methods: Plasma doping (e.g. for FinFETs), cluster implantation, cyro or hot implants (incl. self-annealing) Diffusion in advanced gate stacks Predictive segregation and dose loss models Modeling of interface and dopant passivation by hydrogen or halogens Modeling of epitaxially grown layers: Shape, morphology, stress, defects, doping, diffusion, activation Modeling the impact of front-end processing-induced damage to devices on their leakage, noise and reliability behavior during operation
Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-□ metal gate); reaction mechanisms (reaction paths and (by-) products, rates ...) , and simplified but physical models for complex chemistry and plasma reaction Linked equipment/feature scale models (including high-□ metal gate integration, flows for RIE processes, damage prediction) Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling Spin-on-dielectrics (stress, porosity, dishing, viscosity, …) for high aspect ratio fills, evolution during transformation and densification Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern de-pendent effects) Pattern/microloading effects in radiative annealing or plasma processing Propagation of process variations into circuit block simulation Simulation of wafer polishing, grinding and thinning

Table Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 14 nm	*Summary of Issues*
	Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulations
Nanoscale device simulation capability: Methods, models and algorithms	General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra Efficient models and tools for analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS Models (incl. material models) to investigate new memory devices like redox resistive memories, PCM/PRAM, etc. Models for gate stacks with ultra-thin/high-k dielectrics for all channel materials addressed above w.r.t. electrical permittivity, built-in charges, influence on work function by interface interaction with metals, reliability, tunneling currents and carrier transport Modeling of salicide/silicon contact resistance and engineering (e.g. Fermi-level deepening to reduce Schottky barrier height) Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure , dopant and material variations in order to assess the impact of variations on statistics of device performance Physical models for novel channel materials, e.g., p-type Ge and compound III/V (esp. n-type InGaAs-on-Ge-on-Si) channels …: Band structure, defects/traps... Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation. Coupling between atomistic process and continuum or atomistic device simulation Reliability modeling for ultimate CMOS and new memory devices Commercial device simulators (software) for STT and redox resistive memories Physical models for (mechanical) stress induced device performance for advanced architectures (esp. Fin-FET) and/or novel materials
Electrical-thermal-mechanical-modeling for interconnect and packaging	Model thermal-mechanical, thermodynamic and electrical properties of low □, high □, and conductors for efficient on-chip and off-chip incl. SiP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension Thermal modeling for 3D ICs and assessment of modeling and CAD tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stresses, expansion, keep out regions …). Size effects (microstructure, surfaces, ...) and variability of thinned wafers Signal integrity modeling for 3D ICs Identify effects and apply/extend models which influence reliability of interconnects/packages incl. 3D integration (e.g., stress voiding, electromigration, fracture initiation, dielectric breakdown, piezoelectric effects) Physical models and simulation tools to predict adhesion and fracture toughness on interconnect-relevant interfaces (homogeneous and heterogeneous), packages and die interfaces Dynamic simulation of mechanical problems of flexible substrates and packages Models for electron transport in ultra fine patterned interconnects Simulation tools for die, package and board that allow for coherent co-design
Circuit element and system modeling for high frequency (up to 300 GHz) applications	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package: - possibly consisting of different technologies, - covering and combining different modeling and simulation levels as well as different simulation domains - including manufacturability Introduction of new model features including non-quasi-static effects, substrate noise and coupling, high-frequency RT and 1/f noise, temperature and stress layout dependence and parasitic coupling Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently Scalable active component models for circuit simulation of new multigate MOSFET like double gate FDSOI, FinFET … Scalable passive component models [2] for compact circuit simulation, including interconnect, transmission lines, …

Table Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 14 nm	*Summary of Issues*
	Scalable circuit models [2] for More-than-Moore devices including switches, filters, accelerometers, … Compact models for new memory devices, such as PCM, and standardization of models for III/V (esp. In-GaAs-on-Ge-on-SI) devices Computer-efficient assessment of building block/circuit-level using process/device/circuit simulation, including process variations
Difficult Challenges < 14 nm	*Summary of Issues*
Modeling of chemical, thermo mechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: 1) Layer stacks for gates, junctions and channels: Predictive modeling of dielectric constant, bulk polarization charge, ferroelectric/-magnetic properties, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, transport properties, reliability, breakdown, and leakage currents including band structure, phonon coupling, tunneling from process/materials and structure conditions 2) Models for novel integrations in 3D interconnections including data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties 3) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following:
Nano-scale modeling for Emerging Research Devices including Emerging Research Materials	Ab initio modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping and doping by chemical functionalization, quantum dots, atomic electronics, multiferroic materials and structures, materials for non-charge-based Beyond-CMOS devices) Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport …). Modeling impact of geometry (esp. edge effects / edge roughness), interfaces and bias on transport for carbon-based nanoelectronics (carbon nanotubes and monolayer/bilayer graphene structures)
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, fast and efficient optical interconnect models of larger domains Physical design tools for integrated electrical/optical systems
NGL simulation	Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects & impact on LER); heating and charging effects), including impact on device characteristics (e.g. due to local crystal dam-age by electron scattering or charging effects) Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

4.11 Assembly and Packaging: System Level Integration – SiP

Predictions that Moore's Law has reached its limits have been heard for years and have proven to be premature. We are now nearing the basic physical limits to CMOS scaling and the continuation of the price-elastic growth of the industry cannot continue based on Moore's law scaling alone. This will require "More than Moore" through the tighter integration of system level components at the package level. In the past scaling geometries enabled improved performance, less power, smaller size and lower cost. Today scaling alone does not ensure improvement of all four items.

System on Chip (SoC) and System in Package (SiP) technologies provide a path for continued improvement in performance, power, cost and size at the system level without relying upon conventional CMOS scaling alone. System in Package (SiP) technology is rapidly evolved from specialty technology used in a narrow set of applications to a high volume technology with wide ranging impact on electronics markets. The broadest adoption of SiP to date has been for stacked memory/logic devices and small modules (used to integrate mixed signal devices and passives) for mobile phone applications. Both these applications are driving high volume and a very cost competitive market with a broad base of suppliers. Numerous concepts for three dimensional (3D) SiP packaging are now emerging driven largely by the demands of portable consumer products.

SiP has evolved as an alternative approach to System on Chip (SoC) for electronics integration because this technology provides advantages over SoC in many market segments. In particular SiP provides more integration flexibility, faster time to market, lower R&D cost, lower NRE cost, and lower product cost than SoC for many applications. SiP is not a replacement for high level, single chip, and silicon integration but should be viewed as complementary to SoC. For some very high volume applications SoC will be the preferred approach. Some complex SiP products will contain SoC components.

As with most emerging markets, there remain a number of critical infrastructure issues to be resolved to improve time to market, cost structure, reliability, and performance. These include the need for low cost, higher density substrates, high speed co-design and simulation tools for electrical and mechanical design and analysis, wafer level packaging, lower cost assembly equipment, and improved materials.

The market demand for increased performance, smaller size, lower power and lower cost cannot be met with conventional packaging and interconnect technologies. There are limitations in interconnect density, thermal management, bandwidth and signal integrity that cannot be addressed with conventional technology. System in Package technology is perhaps the most important technology to address these limitations

The overall performance, cost, size, and functionally of a SiP will be limited by both on-chip interconnects of the individual microchips as well as by off-chip interconnects. Complexity, power dissipation, and size are driven by on-chip interconnects. At the off-chip level, lack of high input/output bandwidth and inability to deliver hundreds of amperes of supply current has limited performance below the "intrinsic limits" of each generation of technology.

Inferior thermal dissipation imposes the most serious bottleneck for the realization of ultimate performance SiP. Not only does the thermal dissipation technology dictate the chip junction temperature and subsequently its performance, but the size and cost of the thermal technology will limit the packing density, size, cost, and performance of SiP. Thermal dissipation is also the key limiter to 3D stacking of microprocessors and other high power density integrated circuits.

Even though IO bandwidth is often better than for single chip packages, inadequate chip input/output (I/O) bandwidth is the second most serious challenge to the realization of

ultimate performance. Low-density electrical signal I/Os limit the aggregate off-chip bandwidth while losses due to the organic substrate, cross-talk, and impedance mismatches are exacerbated as off-chip bandwidth per channel increases and signal noise budget decreases. The impact of inadequate number of power and ground I/Os on the on-chip IR drop on the power distribution network, on-chip simultaneous switching noise, and signaling integrity will increase with each technology generation unless scaled accordingly. Moreover, the inductance of chip I/O interconnects and the on-chip power distribution network will require large decoupling capacitors on the silicon and the SiP substrate. Perhaps the greatest issue is the inability of the small transistor to drive the off-chip impedance at high speed. SiP technologies can address these limitations but much development work remains to be done.

Definition of SiP

System in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled in a single unit that provides multiple functions associated with a system or sub-system. A SiP may optionally contain passives, MEMS, optical components and other packages and devices.

SiP vs. SoC Comparison

The benefits of "more than Moore" can be realized through both SoC and SiP technology. Each approach has specific advantages and both will be used in the future. The pros and cons for each architecture are outlined in Table below.

Comparison of SoC and SiP architecture Market and Financial Issues		
Item	SiP	SoC
Relative NRE cost	1X	4-10X
Time to Market	3 –6 months	6 –24 months
Relative Unit Cost	1X	0.2 – 0.8X

Technical Features	
SiP	SoC
Pros	
Different front-end technologies; GaAs, InP, Si, SiGe, etc.	Better yields at maturity (this depends upon complexity)
Different device generations	Greater miniaturization
Re-use of common devices	Improved performance
Reduced size vs. conventional packaging	Lower cost in volume
Active & passive devices can be embedded	CAD systems automate interconnect design
Individual components can be upgraded	Higher interconnect density
Better yields for smaller chip sets	Higher reliability (not true for very large die)
Individual chips can be redesigned cheaper	Simple logistics
Noise & crosstalk can be isolated better	
Faster time to market	
SiP	SoC
Cons	
More complex assembly	Difficult to change
More complex procurement & logistics	Single source
Power density for stacked die may be too high	Product capabilities limited by chip

	technology selected
Design Tools may not be adequate	Yields limited in very complex, large chips
High NRE cost	

Market Trends

SiP has rapidly penetrated most major market segments: consumer electronics, mobile, automotive, computing, networking, communications, medical electronics, etc. The benefits of SiP are for different market segments but the share some common elements. Time to market, size, power requirements and cost have resulted in the strongest initial penetration in mobile communications. The unit shipments are increasing at approximately 10% per year and this is forecast to continue.

4.11.1 Simulation Tool Requirements

SiP Electrical Simulation Tools Requirements

With increasing frequency, and performance, it is necessary that chip, package and board should be co-designed to optimize the performance, increase the density and reduce the overall product cost.

Having separate tools for chip, package and board, today's design methodologies are not consistent and therefore leading to higher design cycle time. In every design, the tool should be intelligent enough that can optimize the design at all levels. In such unified tool environment, the design flow should be consistent and efficient to reduce the design cycle time. For complex and high performance designs, it is necessary that the electrical modeling tools should be integrated with the physical design tools, so that the performance can be predicted while it is being co-designed.

Very often, the material and design rules from different suppliers are different and result in non-consistent characteristics of the components. Thus, it is important that a consistent material data base be generated and integrated with the co-design tools so that correct performance can be predicted.

The signal integrity tools are the critical analysis tools for predicting the performance for the given design. With the requirements of higher density and lower cost, the electrical tools can provide guidelines for selecting material and providing design trade-offs. Thus the integration of electrical modeling tools with the physical design tools is very important. Today we see several electrical modeling tools, each having unique capabilities, but lacking their integration to the co-design environment. Therefore, there is need to integrate the EM tools that can predict both the signal and power performance at the system level.

Every designer uses the tools to do electrical modeling in different way. What is right or wrong? The proper methodologies need to be developed and validated with measurements. During the system design cycle, signal integrity (SI) analysis is needed at different stages of the design:

- Early stage SI where the system is defined and components are selected
- Pre-layout SI where the design rules are generated to start the design
- Post-layout SI where the signal integrity analysis is performed on the entire designed system. Accuracy of the models becomes critical.

In the analog-digital mixed designs, the density at the chip or package level may cause crosstalk noise from digital to analog. The modeling tools should be capable of doing that analysis and help correct the design accordingly.
Current tools cannot handle large complexity of the model. As a result the models are simplified and therefore suffer poor accuracy. To handle the complex models, advanced computers and large memory amounts are needed. The fast and efficient algorithms for EM tools need to be developed or optimized so that they can solve the complex problems in less time with less memory.

SiP Mechanical Simulation Tools Requirements

SiP presents new challenges for mechanical properties. The incorporation of different devices and materials which present varying heat load, unmatched CTE, different thermal conductivity and a variety of elastic properties results in a complex structure. These structures have dynamic response to mechanical stimuli which may come from changing temperature; vibration in the environment, externally applied forces, etc. Simulation tools that can predict SiP package mechanical behavior are essential to determine if the design requirements are met before fabricating a SiP. The requirements for these simulation tools include:

- Static stress simulation for SiP complex structures
- Dynamic stress simulation for SiP solder reflow undergoing power on-off cycles
- Mechanical properties of materials used in the SiP structures
- Interfacial adhesion properties.

Thermal Simulation Tools Requirements

SiP solutions will combine chips with different power density very close to each other and therefore these chips will heat each other. For good thermal design the power maps of all heat sources are needed in order to predict hotspots. Simulation tools should be able to read in power maps of active devices as well as trace layout details of interconnects to calculate additional resistive heating in substrates and other interconnect structures, where very fine and dense wiring might occur. As this often cannot be modeled in detail, a two-step procedure should be incorporated in the tools.
First calculation of substrate thermal conductivity and resistive heating for selectable substrate patterns before adding the chips. To do that, simulation tools should be able to read in substrate layout data. After adding the chips with their power maps, locally distributed trace heating and thermal conductivity, the complete heat generation pattern is there and hot spots can be identified. However, that is only the first step.
Next is to optimize thermal design. Simulations should have the capability to shift heat sources around on a plane or in a stack in order to minimize peak temperatures. That requires parametric modeling and interlinking to optimization tools, open interfaces to external optimization tools. Depending on technology, active and passive components have specifications of lifetime or failure critical temperature. Simulation capabilities needed include:

- Simulation capabilities for advanced hot spot cooling solutions are needed, e.g. for thermo-electric cooling, spray cooling, phase change, etc.

- Time and temperature dependent modeling of diffusion and electro-migration is needed, especially with progressively smaller dimensions of features. Thin layers may disappear in processes.

- Multi-physics coupling like electro-thermal, thermo-electric, and thermo-mechanical should be as easy and fast as possible because most processes, stresses and failures are temperature dependent.

Lifetime Models and Acceleration Factors

Time to market is a parameter that determines success or failure in the consumer dominated electronics market today. The short product life cycles, cost sensitive markets and the requirement for timely market introduction limit the time available for product development. The product life/reliability must therefore be determined during the design cycle rather than through the traditional method of building prototypes and extensive testing. The use of lifetime models with appropriate acceleration factors defined will be required to meet these cost and time to market requirements. The parameters modeled may be product specific but will include some or all of the following:

- Mechanical shock
- Mechanical vibration
- High temperature storage
- Thermal cycle bias voltage stress
- High humidity bias voltage stress
- Bending
- Pull strength of bond wire or other joints
- Power cycling.

5 EDA Roadmap – Design Technologies

In the past, Design Automation advancements have been following process integration capabilities and have lost an overall vision of their strategic priorities. The consequence of this is that many developments have been conducted based on individual initiatives without a global understanding of the problem complexity.
More recently, various organizations (and in particular, European ones) involved in standardization and roadmapping, such as ITRS, ENIAC JTI, CATRENE, ARTEMIS JTI, have started using a more strategic approach, in which the EDA requirements are not driven just by technology scaling, but also by other key drivers such as different application domains.
From the following description we can understand how is pressing the need to enhance existing EDA solutions with "thermal aware" tools which will enable designers to address temperature issues during their daily activity.

5.1 Introduction

Design technology enables the *specification, concept engineering, architectural exploration, implementation* and *verification* of microelectronics-based systems. It includes design flows, *tools*, *libraries, IP, manufacturing process characterizations,* and *methodologies*. Design technology is the key link between technology and the world of applications, transforming ideas and requirements of the electronic systems designer into manufacturable and testable representations, by increasing design productivity, reducing the development costs and time to market and ensuring the achievement of the requirements of safety and reliability.
For instance, if ICT is considered one of the key drivers for the economic and social growth, it is through the design of new semiconductor components and their introduction on the market that the impact of ICT is realized. However with the increasing complexity of targeted applications, design capabilities and design cost are becoming the limiting factors for the future technological development, as indicated by the design gap, which is widening between what technology offers, and what design can use.

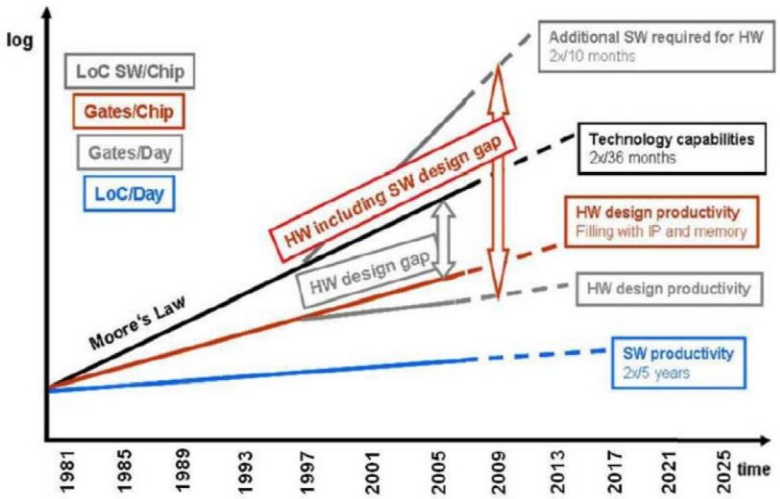

Fig. 11 Hardware and Software Design Gaps versus Time.

The requirements that applications are putting on Design technology are constantly increasing due to the increasing complexity of systems to be integrated, the growing weight of parasitic and statistical effects coming from deep submicron technologies, the inclusion of heterogeneous functions, and the trend to System-in-Package integration, requiring 3D stacking, and the increasing demand for energy reduction and for better reliability.

Relevance for Europe

5.2 Competitive value

Quoting ITRS: "*The process of designing and implementing a chip requires a large collection of techniques, or tools, and an effective methodology by which a designer's input predictably leads to a manufacturable product. ….*" While EDA industry is active in developing and improving tools for the most general design problems, the definition of the methodology and the exploration of new tools is left to leading edge system and semiconductor companies, with the support of Small and Medium Enterprises and Academia. Large scale cooperation among all actors is needed to standardize solutions and to spread the benefits throughout all the design community. The importance that European semiconductor and system companies are giving to Design Technology is also demonstrated by the support given since several years to a quite extensive initiative to define a European EDA Roadmap.
The proper use of Design Technology to reduce the development time of new products has also a significant economic impact on semiconductor industry and on the system industry depending on the availability of dedicated solutions, as shown in the graph below.

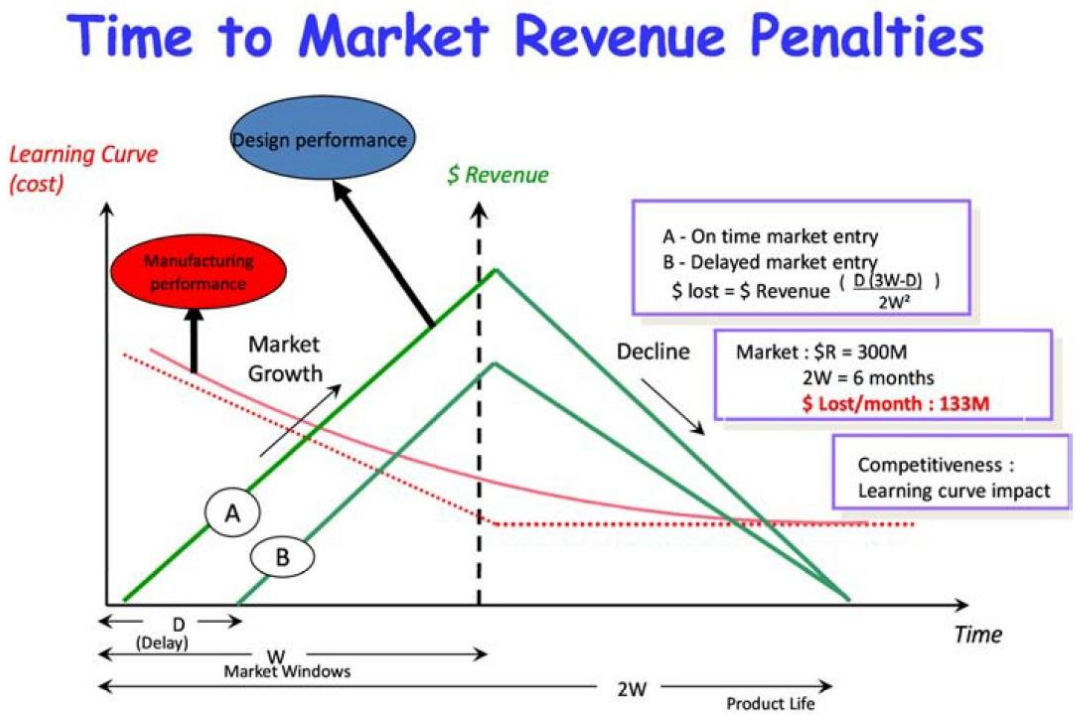

Fig. 12 Time to Market Revenue Penalties.

Societal Benefits

Design technology has an indirect social impact, by enabling critical applications in fields of social relevance, like Health, Security and Transport. *"Over the period 1995-2004, ICT drove half of all productivity gains in the EU, mainly through efficiency gains in the ICT sector and investment in ICT."* The impact of ICT has been particularly evident in specific high tech sectors, which are among the strong points of Europe, like Automotive, Telecom and Security, or of high growth potential like Health and services for Aging Population. All these sectors are critically dependent of dedicated design solutions, capable to integrate also non logical functions (like sensors) and are strongly demanding in specific performances, like reliability and low power consumption that require a tight integration between architectural design and technology. Properly applied design methods and tools will allow increasing the reliability of semiconductor devices, and reducing the costs of the final products making them available to the wider market. As an example we can quote the reduction in casualties made possible by the widespread adoption of safety features in the car industry (ABS, airbag, EPS,..), which has been enabled by the reduction of costs and the increase in device reliability related to the continuous developments in silicon and design technologies.
Development of innovative devices and of specific tools is a field where the entry barrier is quite low, and where innovative SME's can easily find a space. Tight cooperation with user allows for keeping European leadership/employment in key areas.

5.3 Grand Challenges

5.3.1 Competitive Situation

Large EDA companies are providing standard tools essentially for logic synthesis and layout optimization and initiatives exist to try to move design at higher abstraction levels. The most critical issues to be covered are:

- Capture and verification of specifications
- Tools and methodologies to handle multi-core design, taking into account both hardware and software and operating systems
- Tools to verify hardware dependent software
- Standard languages for high level design
- Open standards for IP exchange and interfacing
- Tools and flows to interface design cores coming from different sources and to handle communications among them
- Tools and models to perform basic design evaluation for performances and power dissipation at the highest abstraction levels.

Among these the main achievement that the projects should target is the establishment of a standard language for the high level design. A non-exhaustive list of required innovation is:

- Standardized description language
- Flows and tools for model generation at high abstraction levels
- Tools able to handle at the same level hardware and software
- Tools for the formal verification of the design at different abstraction levels
- Tools for generating interfaces among heterogeneous IPs
- Definition of an OPEN standard ecosystem.

5.3.2 Managing Diversity

Diversity management aims at the development of design technologies to enable the design of complex system-in-package incorporating heterogeneous devices and functions.
The drive towards higher integration levels for semiconductor components, coming from considerations of cost, form-factor, connection speed/overhead, and reliability, has pushed towards the tighter integration also of heterogeneous non-logic functions, like power, communication (RF or optical) and sensors. System integration in package and 3D stacking of different devices are becoming mandatory to achieve the desired targets in terms of size and performances and to interface non-logic functions to data processing devices, when cost and reliability considerations limit the full integration of heterogeneous functions on a single chip, even if technically feasible. The total combination must be designed as a single system and tools and methodology are lacking. At the moment three main challenges exist:

- Standardized modelling tools also for non-logic components compatible with the design of the system at higher abstraction levels
- An integrated design environments for PCB, package and chip design
- Tools taking into account parasitic effects like heat generation and propagation, related to the close proximity of components in the package and an efficient A/MS simulation capability on large scale.

Specific tools exist for board design and package design, but they are not integrated with chip design, and nothing is available for System-in-Package integrated design. Support for non-purely logical functions is also poor and limited to RF design and analogue/mixed mode design, with severe limitations for complex devices. The most important bottlenecks are:

- Missing standards for bare-die-IP (e.g. interfaces electrical and mechanical)
- Models of bare die IP and their integration into system simulation
- 3D floor-planning, place and route
- 3D-parasitic extraction methods (concerning stacked dies and/or bond wires)
- Standardized design rule description (3D) on package level (enabling die and package DRC)
- Test approaches on die and system level, especially for analogue and RF, with links to testing equipment.

The lack of a 3D design-flow for heterogeneous applications prevents the broad application of SiP and stacking technologies in domains e.g. as medical and automation.

A non-exhaustive list of expected achievements is:

- Initiation of standardization process for bare die IP's
- EDA compatible design kits for sensors, actuators and other heterogeneous system components
- Creation of models for non-electrical components and interfaces for SiP design
- Creation of intermediate, digital/mixed analog and RF levels of abstraction for EDA improvement and making most use of existing levels for verification, validation, testability and repair
- Development of a platform that enables the delivery of reusable IPs for microsystems and other heterogeneous systems and is compatible to existing EDA environments
- Creation of a design flow for Heterogeneous functions
- Technologies for chip, package and board co-design with multi-scale simulation tools (SMAC **Error! Reference source not found.**)
- Technologies for implementation of heterogeneous SiP and 3D-stacks (3D parasitic extraction, 3D-DRC)
- Testing approaches for non-logic functions
- Test strategy for SiP and 3D integration, considering also the interface to testing equipment.

5.3.3 Design for Reliability and Yield

In this field, the aim is the development of design technologies to compensate the effect of parameter variability, parasitics and aging effect on yield and reliability of semiconductor devices.
Following CMOS scaling to deep submicron regions, intrinsic device reliability of transistors cannot be any longer guaranteed due to the increase in electric fields and local power densities, and the large number of elements involved. At the same time, critical applications in the field of Automotive and Aerospace, Security and Health require very high levels of reliability, often for limited production volumes. Yield, which is determined by the device functionality at time zero over the entire range of application, and reliability, which is understood as the extrapolation of this functionality over lifetime, are becoming closely related and cannot be any longer guaranteed by process and design only. Testability, yield and reliability must be inserted by design, starting from the architectural level, and going down to cover parameter spread in the line and parasitic and reliability effects at device level. Therefore for models and procedures is required to migrate reliability modelling from transistor level up to system/architectural level. At the moment further progress is needed in moving to compact model-based simulation flows and to cover analog and mixed-signal circuits in the presence of parametric degradations. Tools and flows should cover the interactions among components (EMC, thermal management) and allow interfacing reliability issues among the blocks that form the complete system. New design approaches must be developed to increase and verify device testability, also for non-logic functions, interfacing testing equipment.

Part of the work has been done within THERMINATOR as it easy to see from the outcomes of WP5, WP4 , WP3 and WP6 and in the results on the TSV activities . This has been the path to start co-simulation works in SMAC **Error! Reference source not found.**.
Europe is quite innovative in the Design Technology and EDA area. Some of these EDA companies have achieved unique breakthroughs. They are focusing on supplementary solutions to large EDA tools in the area of design support in face of varying parameters, changing technologies, and parasitic effects. More approaches are available throughout Europe in academia, which are not covered by the mainstream tools from the big USA based EDA companies. These efforts should be strengthened in order to meet the special European needs (heterogeneous system integration and safety relevant applications) and to keep some independence of the large mainly US-based EDA companies.

A non-exhaustive list of main expected achievements:

- Methods to extract independent, uniform distributions out of device characterization data e.g. for Monte Carlo simulations
- Faster simulations to handle complex circuits and large number of influencing parameters as well as methods to handle non-uniform distributions
- Methods to transfer variability and reliability information over different levels of abstraction (MANON)
- Tools and flows to handle simultaneously in the design optimization both process variability and lifetime related parametric degradation
- Design and testing approaches for failure detection, localization and repair during application (and tools to verify them) (WP3-WP6)
- Design and testing tools for fast and efficient yield learning.

5.4 Timeframes

All three grand challenges need to be met in parallel, since all elements are required to design reliable new applications. A detailed analysis of the requirements of Design Technology is given in the European EDA Roadmap, periodically updated with the support of CATRENE organization. An indicative roadmap of some major tools and flows, from ITRS, is reported here below.

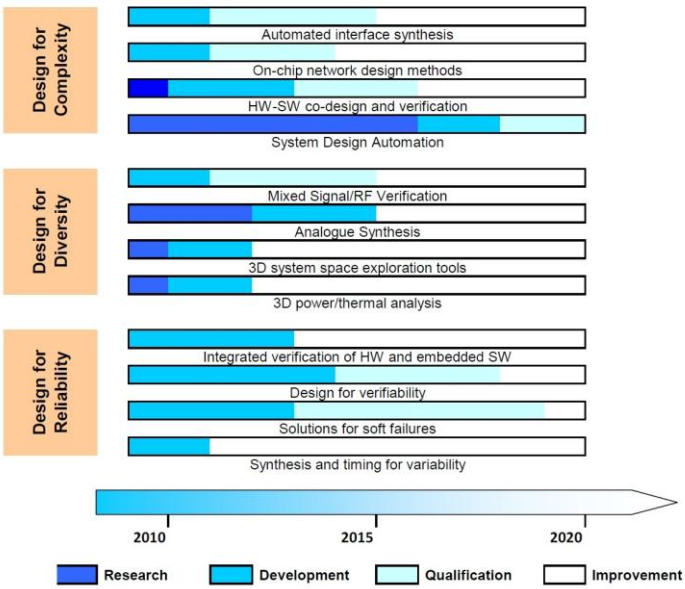

Fig. 13 Major tools and flows roadmap.

5.5 Synergies with Other Domains

Possible synergy areas with other priorities are (not exhaustive):

- Design for Safety and Reliability with application projects in "Automotive and Transport" and "Health and Aging Society"
- Design for complexity includes tools for reducing power dissipation, which is essential for "Communications" and "Health and Aging Society"
- Design for diversity includes sensor integration 3D and SiP design, essential for "Communications", "Automotive and Transport" and "Health and Aging Society"
- Failure analysis and reliability procedures related to high temperature, high current/voltage operation will also be an issue for Sub-programme: "Automotive and Transport" and "Energy Efficiency"
- TCAD and modelling of device reliability and variability will be synergic to "Silicon Processes and Integration"
- Design for diversity implies strong cooperation with "equipment, Materials and manufacturing" especially on package modelling
- Testing development, especially for 3D and heterogeneous components requires synergy with testing equipment development, manufacturing especially on package modelling.

6 Reference glossary

6.1 Moore's Law

An historical observation by Gordon Moore, stating that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Scaling ("More Moore")

a. *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.

b. *Equivalent Scaling* which occurs in conjunction with, and also enables, continued Geometrical Scaling, refers to 3-dimensional device structure ("Design Factor") Improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

6.2 Functional Diversification ("More than Moore")

Functional Diversification refers to the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board level into a particular package-level (SiP) or chip-level (SoC) implementation. In addition, the increasingly intimate integration of complex embedded software into SoCs and SiPs means that software might also need to become a fabric under consideration that directly affects performance scaling. The objective of "More-than-Moore" is to extend the use of the silicon-based technology developed in the microelectronics industry to provide new, non-digital functionalities. It often leverages the scaling capabilities derived from the "More Moore" developments to incorporate digital and non-digital functionality into compact systems.

7 Conclusion

Thermal issues have come to the forefront, and thermally aware design techniques are likely to play a major role in the future. While improved heat sink technologies are available, economic considerations restrict them from being widely deployed until and unless they become more cost-effective. Low power design is helpful in controlling on-chip temperatures, but is already widely utilized, and new thermal-specific approaches are necessary. In short, the onus on thermal management is moving from the package designer toward the chip designer.

Thermal analysis is important in ensuring the accuracy of timing, noise, and reliability analyses during chip design. The thermal properties of integrated systems can be studied at different levels. However, an essential prerequisite to addressing thermal issues is the ability to model heat transfer paths of a chip with its surrounding environment, and to analyze the entire thermal system, including effects that are not entirely within the chip.

The cost of the cooling solution is a nonlinear function of the chip power dissipation: the initial rise is gentle, but beyond the point of convective cooling, the costs rise steeply. This knee point is a function of cooling system complexity.

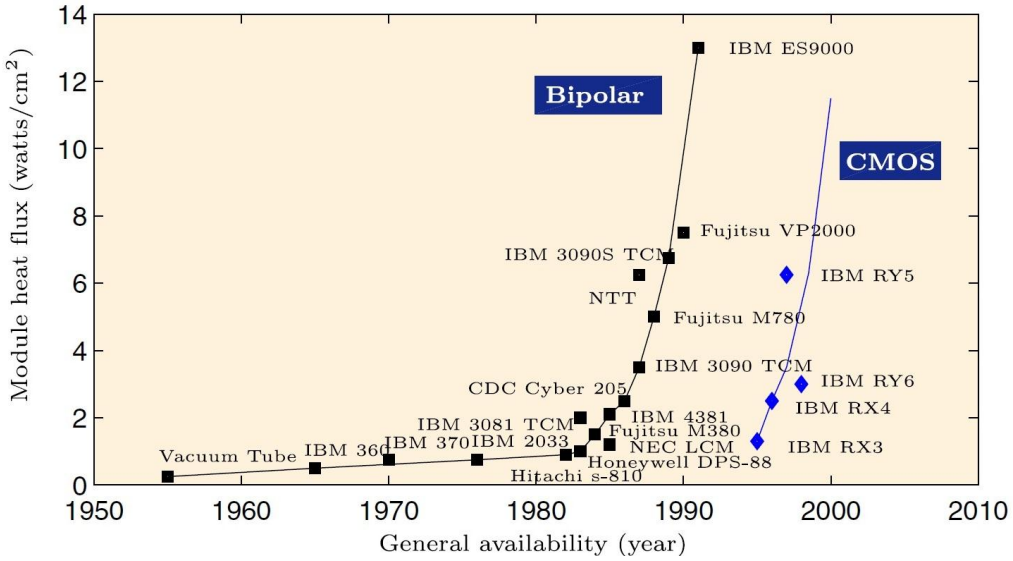

Fig. 14 Trends for the heat flux for state-of-the-art systems over the years.

There have been numerous improvements even in air-cooled technologies and improved thermal interface materials in the recent past, which have progressively shifted the knee of the cooling so that the heat fluxes that are currently obtained by air cooling could only be achieved by liquid cooling in the 1980s. However, even these improvements cannot keep up with the capability of Moore's law to integrate more functionality on a chip. Indeed, while it is possible to pack more transistors on a chip today, only a fraction of them can actually be used to full potential, because of power and thermal limitations. More advanced solutions using, for example microfluidic channels and microrefrigeration, have been proposed, these are not cost-effective enough for widespread use today.

What said demonstrates that temperature must be an important consideration in the design of nanoscale integrated circuits. Thermally conscious design need has come about with the advent of 3D integration, which makes the on-chip problem particularly acute. Unlike 2D circuits, where all transistors are placed in a single plane, with several layers of interconnect

above, 3D circuits stack tiers of such 2D structures, one above the other. 3D structures may be built by stacking tiers of dies above each other, where the separation between tiers equals the thickness of the bulk substrate, which is of the order of several hundreds of microns. Advances in industrial, government and academic research laboratories have demonstrated 3D designs with inter-tier separations of the order of a few microns, enabling short connections between tiers, accentuating the advantages of short vertical interconnections in these 3D structures. With these technological advances, 3D technologies provide a roadmap for allowing increased levels of integration within the same footprint, in a direction that is orthogonal to Moore's law. Moreover, 3D technologies provide the ability to locate critical blocks close to each other, e.g., by placing memory units in close proximity to processors by placing them one above the other. These, and other, advantages make 3D a promising technology for the near future.

In conclusion, *temperatures affect the properties and performance of a circuit*. In terms of delay, the performance of transistors and the resistance of interconnect wires can be affected; in terms of power dissipation, there is a strong relationship, with potential feedback, between temperature and leakage power; in terms of reliability, the lifetime of both devices and interconnects all depend critically on the operating temperature of the circuit. These are all critical factors in ensuring circuit performance, and the complexity of these problems makes it essential to build efficient and scalable CAD solutions for on-chip thermal analysis.