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Modelling, Control and Management of Thermal Effects in Circuits of the Future

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Second and Final release of market survey document

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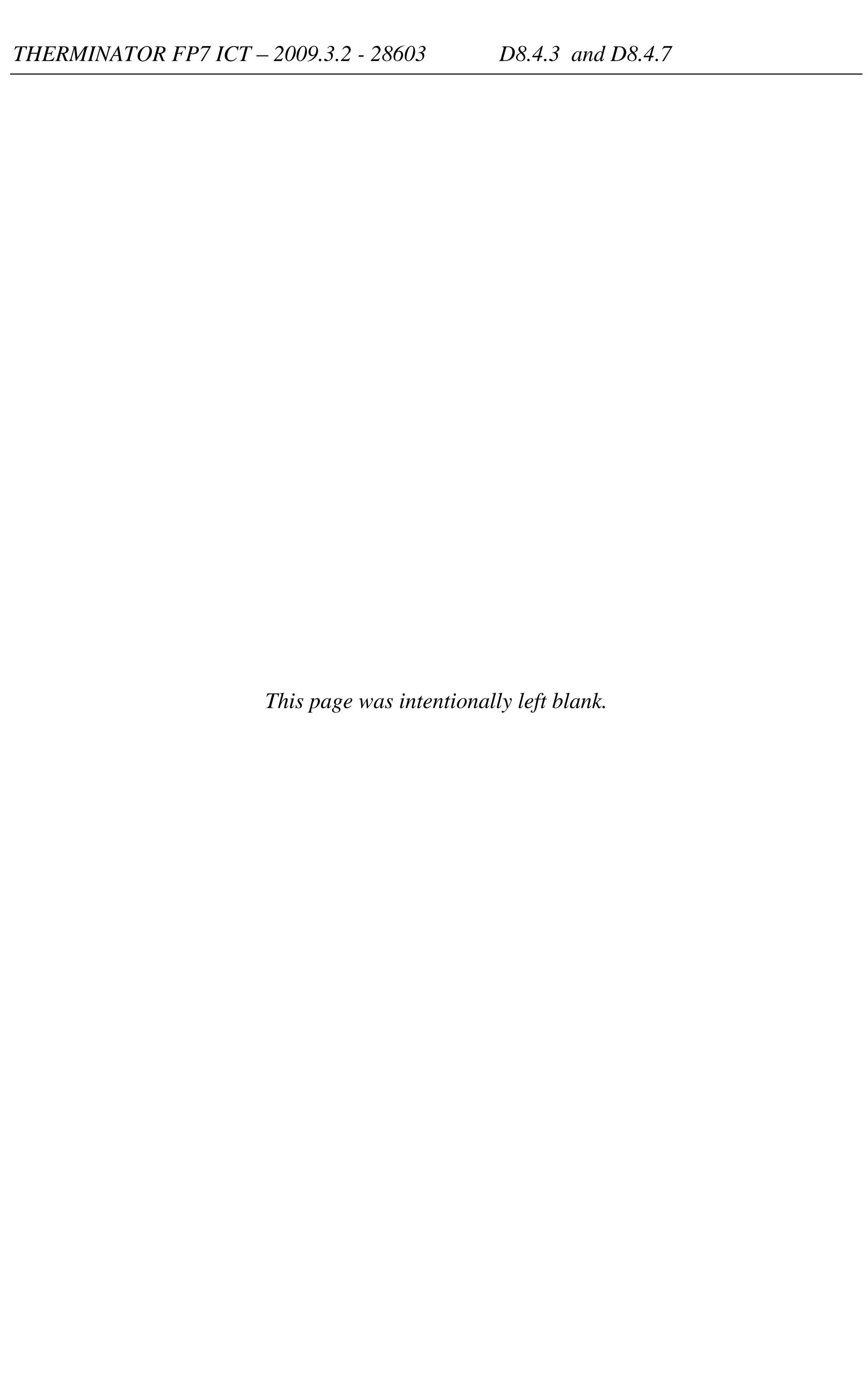
References

[1] **IPCA – THERMINATOR Consortium Agreement**,

[2] **D8.4.1 First release of Market Survey.**



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1 Remarks

This document brings together both the second (D8.4.3) and the final (D8.4.7) report on market survey activities and it is because the exploitation manager joined the project in its final step.

Moreover, this document is to be considered the completion of the document D8.4.1 (First release of market survey) in which research and commercial tools were presented available for thermal modelling and analysis and it became apparent that none of the commercially available tools had the wished features; features addressed by the developments of THERMINATOR project. In this document the strategies are presented that will be followed by industrial partners to launch on the market products developed using what has been produced in THERMINATOR project.

2 NXP

The activities of NXP in the THERMINATOR project addressed electro-thermal modelling of various electronic devices and designs relevant for the present and future product portfolios of NXP. Examples include RF-power amplifiers for wireless communications, ICs for near-field communication (NFC) in identification applications, and discrete packaged components. Electro-thermal models are essential in modern circuit design; inaccurate tools will result in costly re-spins and product delays. On the other hand, the tools developed in THERMINATOR can be used to investigate the root causes of self-heating in current technologies and mitigate limitations from thermal effects on the overall performance in future products.

In summary, NXP worked on the following thermal models, verification activities, simulation methodologies, and optimisation techniques within THERMINATOR:

- Electro-thermal model for silicon RF-LDMOST (laterally diffused metal-oxide-semiconductor transistor) and GaN-HEMT (gallium-nitride high–electron-mobility transistor) technologies in WP2.
- Electro-thermal modelling and simulation on circuit level, using the FHG thermal solver, for identification applications in WP4.
- Study on the impact of thermal variation and circuit optimisation together with MUN in WP4.
- Electro-thermal simulations with BME in WP4.
- Modelling the effect of thermal distribution in the crystal on the electrical performance for discrete devices in WP6.
- Integration of the electro-thermal models for RF-power amplifiers developed in WP2, into (existing) design flows in WP7.
- Reuse and modification of electro-thermal models, developed for RF-power amplifiers, for other types of device, namely SOI-LDMOS and GaN Schottky diodes, in WP7.
- TCAD models for heater elements and diodes for temperature sensing developed with SNPS-CH in WP7.

- Electro-thermal models for packages (SOD123W, SOD882, SOT23, SOT89, and SOT1061) for discrete devices in WP7 together with BME.
- Electro-thermal modelling of test chips for identification applications, designed for the first time in 40 nm, together with FHG in WP7.
- Yield optimisation simulation for power-on-reset (POR) together with MUN in WP7.

Simulation and design activities in NXP are predominantly based upon using tools available from EDA vendors. For this reason, the implementation of solutions and methodologies for thermal-aware design, developed within THERMINATOR, will focus on integration into existing design tools and flows from EDA vendors. An advantage of the approach followed is that the models can be made available to external NXP customers with a limited amount of extra effort. More specifically, integration of the electro-thermal models for RF-power technologies (RF-LDMOS and GaN-HEMT) developed by NXP-NL in THERMINATOR was demonstrated in WP7. These models are used by the internal NXP design community. These models can be combined with models for packages and bond wires into models for dedicated products, and can be made available to external customers when needed. The models developed for other types of device, based on reuse and modification of the modelling approach developed for RF-power amplifiers, will be introduced in NXP internal design activities. Examples of the other types of device include devices used in WP7, *e.g.*, SOI-LDMOS and GaN-Schottky diodes, although electro-thermal modelling of poly-resistances and bipolar transistors in BiCMOS technologies is also on the roadmap of NXP-NL.

NXP-D2 recognises the increasing need for thermal-aware design. Their role within the THERMINATOR project was to provide measurement data from a dedicated test chip. The data was used by the project partners involved in the tool development, such as MUN and SNPS-CH, for verification, validation, and benchmarking. In the application areas of contactless chip cards and identification products, which is the business focus of NXP-D2, the tools and models of the THERMINATOR project will be very useful in the design of optimised power systems. Contactless cards require advanced power design: long-range operation implies low power capability as the operating power of the contactless device is drawn from the RF field. On the other

hand, in the near-field and proximity operation modes, the device has to cope with the strong field, which generates high power in the antenna and hence in the RF interface within the chip. The means and tools developed in THERMINATOR will be applied to optimise the thermal design of such analog interfaces by modelling and simulating the thermal power in the silicon. As the form factor of contactless products covers a wide range – cards, tags, labels, *etc.* – the impact of the package needs to be taken into account. NXP will adopt the results from THERMINATOR for this purpose in order to estimate the thermal behaviour in the early design phase, thus saving cost and reducing time-to-market.

NXP-D is a leading supplier of discrete small-signal semiconductor devices. Their portfolio contains more than 3000 products, covering a wide range from products for commodity applications to more specialised products for ESD protection. The on-going trend for discrete small-signal devices is to enhance their electrical performance in smaller packages, resulting in an improved power-handling capability per PCB area. For this reason, the tools developed by NXP-D and its THERMINATOR partners focussed on a better understanding of self-heating at board level. The thermal models for TCAD can be used in commercial tools, and will be used for future device optimisation. The thermal models for packages, developed within THERMINATOR, can be integrated into any commercial circuit simulator. These package models will be combined with electro-thermal circuit models of small-signal devices to study limitations on performance from electro-thermal behaviour. If applicable, the models can easily be made available to external customers in a later stage, since the models are already included in commercial tools for internal use.

3 OFFIS

3.1 Device Ageing Analysis Models and Tools

In the recent past the analysis of long-term degradation and ageing effects started to become a topic of high interest because recent semiconductor technologies require meaningful statements regarding the reliability of circuits especially under harsh environmental conditions. For this reason, efforts have been made to include an analysis into state-of-the-art simulation tools. The HSIMplus MOS Reliability Analysis (MOSRA) [1] adds ageing effects to industry-standard BSIM3 and BSIM4 models that can be used in analogue circuit simulation tools such as Synopsys HSPICE or CustomSim. These circuit-level simulation tools perform slow transient simulations and estimate the degradation on a device-by-device level.

The degradation models and their integration into a long-term thermal-aware estimation flow as they have been developed within the THERMINATOR project and with the features described in the D6.2.x deliverables are unique at the addressed level of abstraction. Recently no commercial tools are available for a long-term prediction of NBTI (Negative Bias Temperature Instability) effects with the scope of multiple years of degradation. Further, the implemented degradation models represent the state-of-the-art understanding of the NBTI degradation effect and consider healing during relaxation phases of low utilization.

[1] MOS Device Aging Analysis with HSPICE and CustomSim, White Paper, August 2011, Synopsys
http://www.synopsys.com/Tools/Verification/AMSVerification/CircuitSimulation/HSPICE/Documents/mosra-wp.pdf

4 ST

In the near past, ICT drove half of all productivity gains in the EU, mainly through efficiency gains in the ICT sector and investment in ICT.

Design Technology has an indirect impact by enabling critical applications in field of social relevance, like Health, Security and Transport and in specific high tech sectors, which are among the strong points of Europe, like Automotive, Telecom and Security, or of high growth potential like Health and Services for Aging Population.
All these sectors are critical dependent of dedicated design solutions, capable to integrate also non logical functions (like sensors) and are strongly demanding in specific performances, like reliability and low power consumption that require a tight integration between architectural design and technology; moreover low power design is helpful in controlling on-chip temperatures, but is already widely utilized, and new thermal-specific approaches are necessary. ***New design methods and tools - and what developed within THERMINATOR project fully reflect the above - properly applied, will also allow increasing the reliability of semiconductor devices, and reducing the costs of the final products making them available to a wider market***.
Neglecting thermal information during design may imply excessive over-design, due to the extremely conservative constraints that designers may pose in order to guarantee correct circuit operation under all possible running conditions. For these reasons the primary scientific and technical objective of the THERMINATOR project has been to develop innovative design technologies for modelling, controlling, compensating and managing temperature in semiconductor circuits and systems to be manufactured with the most advanced processes and technologies (WP3-WP4). For what concern the power discrete devices (WP5) thermal modelling issues and estimation aspects are particularly important for high-voltage switching applications, where thermal effects have a huge impact.
Thermal-specific approaches are also a MUST DO in the next future roadmap of SMART Power devices.
All the above considerations perfectly fit inside the ST new strategic plan announced in December 2012.

ST is addressing a $140 billion market (**source WSTS**) through the strategy shown in the following:

Fig. 1 Leadership in

Fig. 2 Large attractive markets where ST leads or will lead

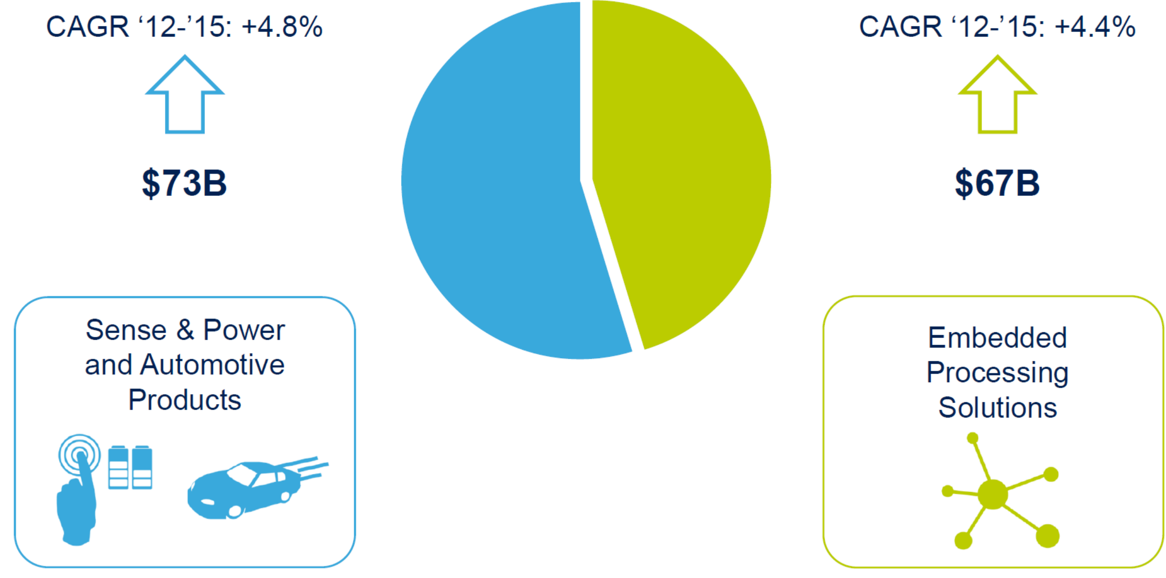
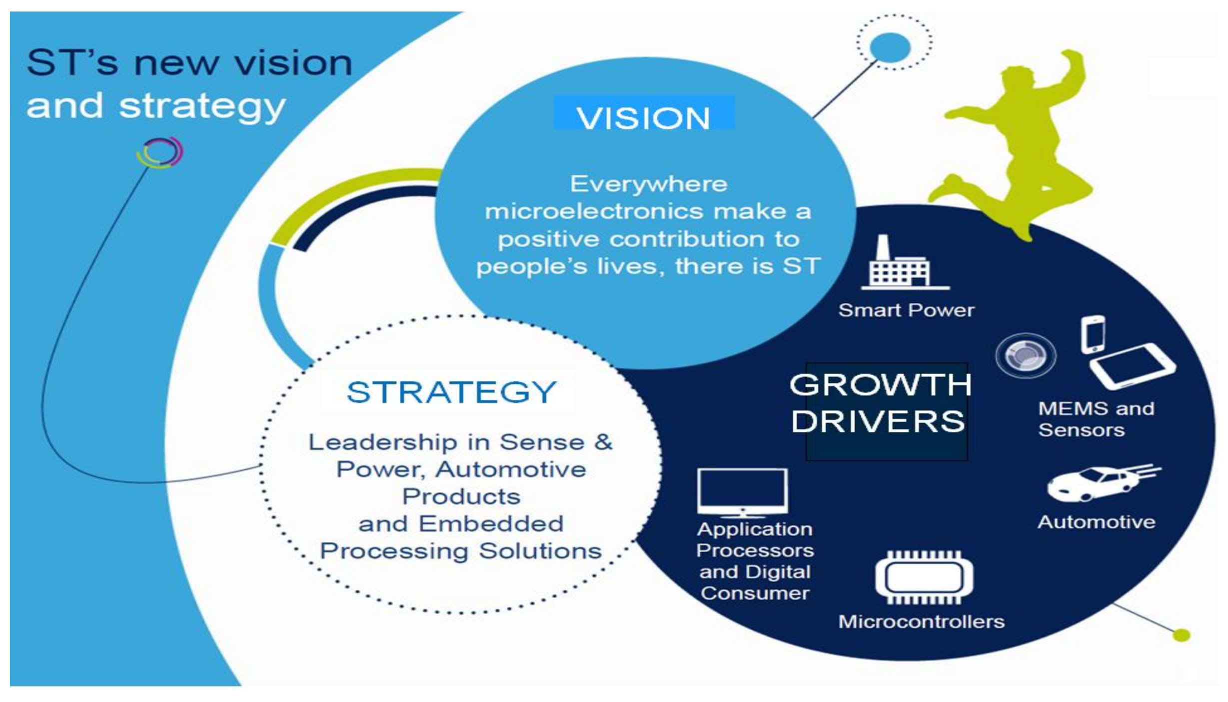


Fig. 3 More focused product portfolio

In conclusion what developed within THERMINATOR project is mandatory to design new products that will enable ST to achieve its goals under the new vision and strategy shown in Fig. 4.

Fig. 4 ST's new vision and strategy



5 Synopsys EDA Tools for Power Optimization

5.1 Power Compiler Overview

Power Compiler™ automatically minimizes power consumption at the RTL and gate level. Power Compiler performs automatic clock gating to reduce the power consumption. Driven by the design constraints, it performs simultaneous optimization for timing, power and area. With power intent defined by UPF (Unified Power Format), it automatically inserts power management cells such as isolation, level-shifter, retention registers, power gates and always-on cells as needed. It also supports multi-threshold libraries for optimal leakage power optimization. Power Compiler is seamlessly integrated with the synthesis design flow and shares the same GUI, commands, constraints and libraries with the Design Compiler® and IC Compiler® tools.

5.2 Power Compiler Features

Power Compiler provides fully automated and complete power synthesis:

- Single-pass multi-voltage optimization
- Automated implementation of advanced low-power methodologies
- Advanced clock-gating for optimal dynamic power savings
- Concurrent synthesis optimization for performance, area, leakage and test
- Fine-grain control over leakage optimization.

Power Compiler™ also offers concurrent multi-scenario synthesis, or multi-corner and multi-mode (MCMM) optimization.

5.3 PrimeRail (In-Design Rail Analysis for Place-and-Route) Overview

PrimeRail is the rail analysis technology foundation for IC Compiler In-Design Rail Analysis™. Invoked directly from IC Compiler, In-Design Rail Analysis utilizes embedded PrimeRail analysis and fixing guidance technology to enable designers to easily perform power network verification throughout physical implementation. By identifying and fixing voltage-drop and electromigration issues earlier in the flow,

designers can eliminate costly iterations late in the design process. Built on industry gold standard PrimeTime® SI and StarRC™ signoff technologies, PrimeRail offers high-accuracy, full-chip SoC static and dynamic rail analysis to accelerate design closure.

5.4 IC Compiler In-Design Rail Analysis

Working in concert with IC Compiler’s Power Network Synthesis (PNS) and In-Design Physical Verification™ capabilities, In-Design Rail Analysis provides designers with the most comprehensive power network design and verification solution. Traditional approaches to power network design consist of separate implementation and verification steps, often performed by different engineers using many tools and environments in a complex flow. With leading-edge SoC designs, this approach often results in multiple iterations between physical implementation and signoff, adding significant risk to project schedules.

In-Design Rail Analysis works in tandem with IC Compiler Power PNS capability to enable designers to efficiently implement optimize and refine power networks, significantly reducing overdesign. In addition, In-Design Physical Verification helps ensure that power networks are design-rule clean as refinements and fixes are implemented. IC Compiler’s ecosystem of PNS, In-Design Rail Analysis and In-Design Physical Verification today offers the fastest and most comprehensive solution for power network design.

Features

- Integrated IC Compiler In-Design Rail Analysis environment
- Integrated with Galaxy™
- Comprehensive dynamic and static rail analysis
- Full-chip SoC capabilities

5.5 Overview IC Compiler

Comprehensive Place and Route System

Overview

IC Compiler is an integral part of the Synopsys Galaxy™ Implementation Platform that delivers a comprehensive design solution, including synthesis, physical implementation, low-power design, and design for manufacturability. IC Compiler is a single, convergent, chip-level physical implementation tool that includes flat and hierarchical design planning, placement and optimization, clock tree synthesis, routing, manufacturability, and low-power capabilities that enable designers to implement today's high-performance, complex designs on schedule.

Features

- Multicore support for higher throughput for designs in mainstream silicon technologies
- High performance for advanced silicon technologies
- Power-aware placement technology groups registers to reduce dynamic power
- Support for complex clock gating in clock tree synthesis
- Low-power, SI-aware CTS
- Signal electromigration analysis and repair significantly improves design reliability
- In-Design static rail and EM analysis with PrimeRail and IC Compiler improves designer productivity
- Manufacturing Awareness
- Complete support for advanced design rules
- Soft rule support
- Cell and route-based yield optimizations
- Critical Area Analysis (CAA)
- Optimization of critical areas through wire-spreading/widening during global route, track assignment and detailed routing
- Automated, timing driven multi-pattern via selection
- Timing-driven metal fill
- Staggered metal fill
- Litho-friendly routing
- Automated lithography hotspot fixing

- Faster In-design flow with IC Validator DRC/LVS signoff technology for accurate metal fill and automated DRC fixing
- Design Planning
- Concurrent hierarchical design
- Complete design planning solution for hierarchical and flat designs
- Early analysis and feasibility exploration capabilities
- Multi-Million instance design capacity
- Complete multi-voltage flow with MTCMOS support
- Power network analysis (PNA), Power network synthesis (PNS), and power-pad synthesis capabilities
- Easier handling of complex P/G structures using template-based PNS

6 WiCkeD from MunEDA

MunEDA offers within its EDA software tool suite WiCkeD numerous and powerful tools for intensive circuit analysis, modeling and model generation, sizing and optimization and IP porting. WiCkeD supports all kind of custom IC design based on nominal process, PVT corner and statistical process variation data. MunEDA WiCkeD tools can be configured and licensed by the customer based on the specific and individual needs of the underlying design projects. MunEDA WiCkeD offers both, interactive design analysis and diagnosis tools and fully-automatic sizing and optimization tools. Both complement the designer in its familiar manual or tool-supported design flow.

With WiCkeD the designer can analyze the influence of temperature variations and thermal behavior of integrated circuits based on the applied process technology. For this reason different tools and methodologies are available in WiCkeD:
- BAS - Basic and Sensitivity Analysis: Analysis of device sensitivities depending on temperature variation
- SCG - Parameter Screening: influence and impact analysis of thermal parameters on device level
- WCO - Worst Case Operation: identification of worst case temperature corners for a given circuit analysis and sizing problem
- MCA - Monte-Carlo-Analysis: Enhanced Monte-Carlo Analysis based on worst-case temperature corners for real-predictable circuit yield

The application of such tools and methodologies has been shown with the pre-selected industrial circuit examples of the project partners ST and NXP in WP4.