"Definition of MAC protocols supporting FDM/OFDM operation"

Update of D4.2

D4.5

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Abstract:

This document is an update to Deliverable D4.2. In that sense, it aims at verifying the alignment of the ACCORDANCE FPGA system developed in WP3 with the ACCORDANCE MAC protocol specifications provided in D4.2. In addition, it looks into ways of implementing the MAC control messaging in the aforementioned system, in anticipation of the relevant work to be conducted in the framework of T6.2.

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1. Referred Documents

[1] "Definition of MAC protocols supporting FDM/OFDM operation", Deliverable D4.2, ACCORDANCE, FP7 – ICT– GA 248654.

[2] "MAC layer requirements for the ACCORDANCE Network", Deliverable D4.1, ACCORDANCE, FP7 – ICT– GA 248654.

[3] "Design and implementation of FPGA modules", Deliverable D3.5, ACCORDANCE, FP7 – ICT– GA 248654.

[4] "Definition and evaluation of algorithms for dynamic bandwidth allocation in ACCORDANCE", Deliverable D4.3, ACCORDANCE, FP7 – ICT– GA 248654.

[5] IEEE Std 802.3ah, 2004.

[6] IEEE Std 802.3av, 2009.

[7] "Gigabit-capable passive optical networks (G-PON): Transmission convergence layer specification," 2004, ITU-T Rec. G.984.3.

[8] "10-Gigabit-capable passive optical networks (XG-PON): Transmission convergence (TC) specifications", 2010, ITU-T Rec. G.987.3.

[9] K. Kanonakis, I. Tomkos, "MAC Framework and Algorithms for Dynamic Subcarrier Assignment in OFDMA-PONs", IEEE Symposium on Computers and Communications (ISCC'11), June 28 – July 2011, Corfu, Greece.

[10] K. Kanonakis, E. Giacoumidis and I. Tomkos, "Physical Layer Aware MAC Schemes for Dynamic Subcarrier Assignment in OFDMA-PON Networks", IEEE/OSA Journal of Lightwave Technology, 2012.

2. Executive Summary

In Deliverable D4.2 [1] care was taken to provide a detailed description of the ACCORDANCE MAC protocol, based on the definitions of D4.1 [2] and the architectural aspects of ACCORDANCE from WP2. D4.2 thus provides a detailed list of all the control messages, their fields and the message exchanges that need to take place between the OLT and the ONUs to achieve all ACCORDANCE functionalities. The same document also suggested ways of migrating from existing TDMA-PON protocols to the ACCORDANCE MAC with minimal modifications. Therefore, D4.2 is a comprehensive document that contains all required ACCORDANCE MAC definitions.

The current deliverable (D4.5) was originally intended as an update of D4.2. At the same time, work in ACCORDANCE WP3 progressed resulting in the development of a complete FPGA system able to demonstrate OFDMA-PON operation. For this reason it was decided to use D4.5 as the bridge between the theoretical definition of the ACCORDANCE MAC in D4.2 and the actual FPGA implementation that will be employed for its realization (as documented in D3.5 [3]). Therefore, in the present document we provide a look at the ACCORDANCE FPGA system from a strictly MAC point of view and verify its alignment to the specifications of D4.2. Furthermore, one of the goals of the document is to prepare the ground for the work that has to take place in the course of Task 6.2 (FPGA board preparation). In that respect, we also identify solutions for implementing the MAC control messaging in order to finally host a selection of the MAC algorithms (taken from [4]) for the final ACCORDANCE experimental validation.

Concluding, this document should only be considered as a supplement to D4.2 and has to be read in conjunction with the latter document to obtain a clear understanding of the ACCORDANCE MAC operation.

3. Overview of the ACCORDANCE MAC FPGA System

3.1 Introduction

For the final experimental evaluation of the ACCORDANCE MAC functionality a custom MAC protocol has been defined and will be implemented, by means of a synergy between the already developed (in WP3) FPGA modules and code that will be produced in the framework of WP6 to customize operation according to the exact ACCORDANCE requirements. In that respect, care has been taken (via a continuous interaction between WP3 and WP4 participants) to make the developed FPGA system capable of demonstrating all the basic and innovative features described in D4.2. Those for example include the hybrid OFDMA/TDMA way of operation for the dynamic bandwidth assignment, as well as the concept of adaptive subcarrier modulation per ONU proposed by ACCORDANCE.

At the same time, it was also decided to implement the minimum set of modules necessary (i.e. not an entire protocol stack) for the purposes of the project, taking into account that they are intended for an experimental prototype rather than a commercial product. Having said that, it was deemed more beneficial to avoid modifying any of the existing TDMA protocols (although, of course, the exact ways for achieving this have also been explained in D4.2) but rather design a more lightweight, hybrid MAC, borrowing elements from both (10G-)EPON [5], [6] and (X)GPON [7], [8].

In the sections below we briefly present (from a MAC point of view) the FPGA system developed within the course of ACCORDANCE WP3 and discuss how each of the concepts presented in deliverable D4.2 have been translated into actual functionalities in the aforementioned system.

3.2 The Overall FPGA System

Figure 1 depicts the generic ACCORDANCE FPGA system (applies for both the OLT and the ONUs) as described in D3.5. As shown in the figure, a basic building block of the system is the “MAC Layer & Subcarrier Management” module, which performs the routing between the external 10G Ethernet interfaces and the subcarriers of the OFDMA physical layer. This module is also responsible for creating the control and information flows as will be explained below.

The whole system, along with the MAC module is controlled by an embedded Leon-3 processor via an AHB & APB system. During the course of Task 6.2 (FPGA board preparation), the latter processor will be augmented with specially developed code that will make it interact with the MAC module to enable all required functionalities. This code will hence be in charge of preparing the necessary control messages and forwarding them (via specific functions that will be defined) to the MAC module that will, in turn, implement them. Therefore, the complete ACCORDANCE MAC should be considered as a combination of the FPGA MAC modules along with the respective code on the embedded processor.

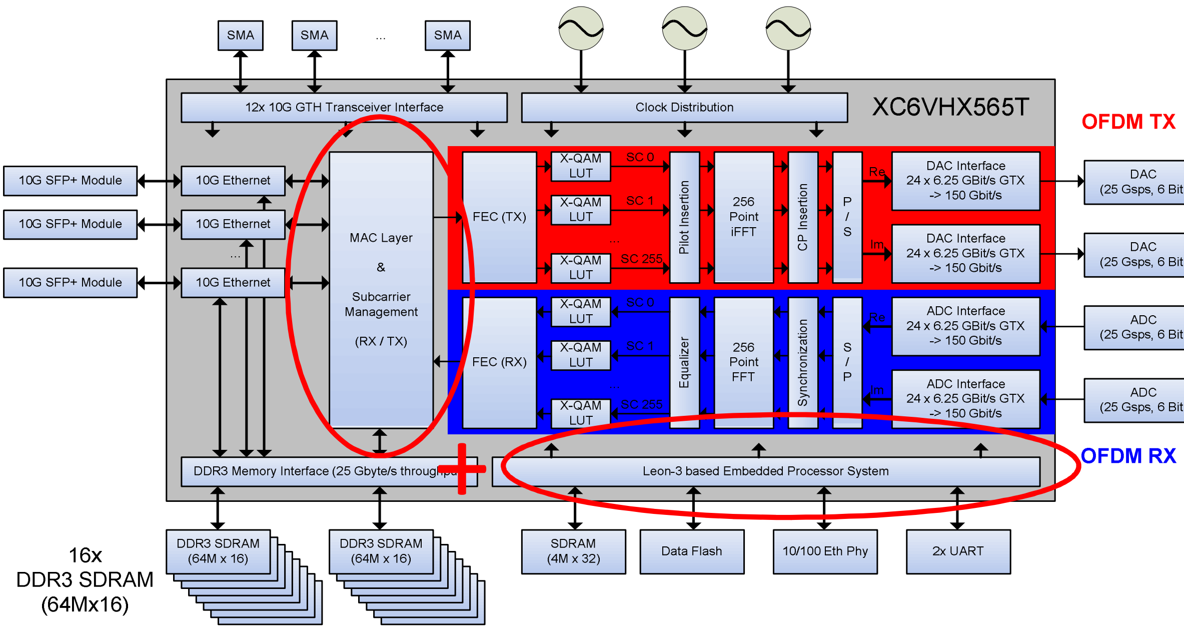

Figure 1: The ACCORDANCE FPGA system (from D3.5) and location of the MAC functionality.

3.3 CONTROL AND PAYLOAD DATA CHANNELS

3.3.1 Introduction

As mentioned in 3.1, the MAC FPGA module performs the preparation of the ACCORDANCE frames, which basically include control information and also encapsulate data packets (e.g. Ethernet frames). In that respect, an approach similar to GPON is adopted, whereby each frame includes PHY-related and control data at the beginning followed by the actual payload data. Figure 2 shows the overall structure of the ACCORDANCE (downstream and upstream) frames. As it can be seen from the figure, each frame has a fixed duration of 105.6μs (similarly to GPON).

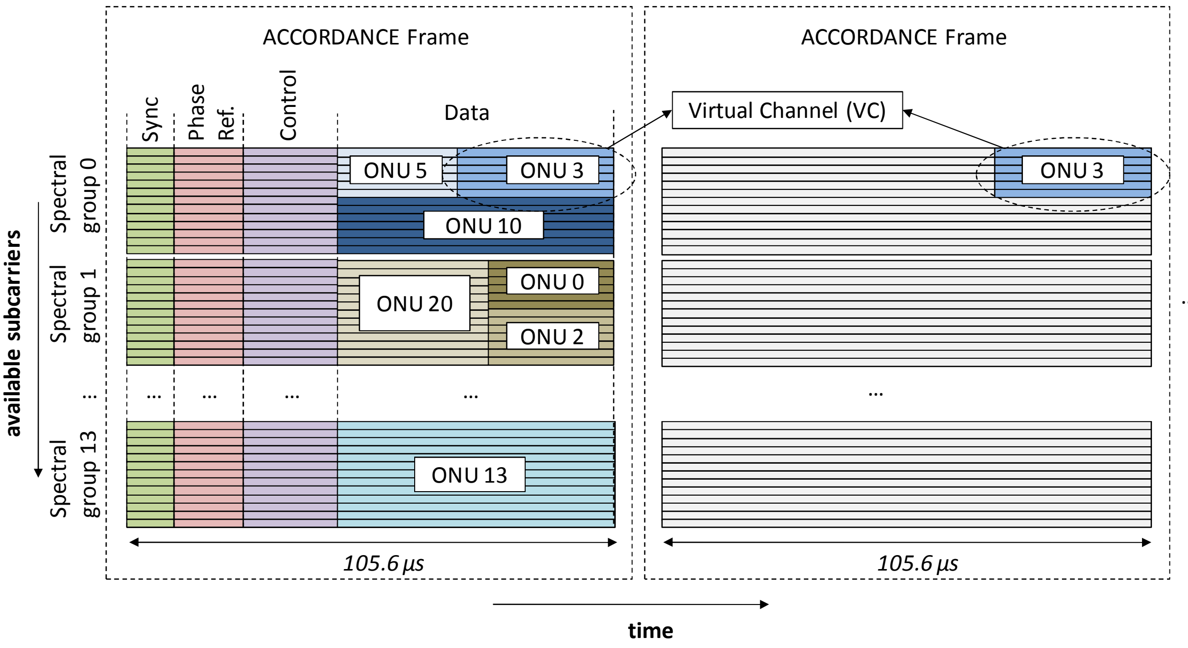

Figure 2: ACCORDANCE frame structure and the notion of the ACCORDANCE Virtual Channels (VC).

In the vertical (frequency) dimension, the frame consists of a number of subcarriers. Although in total there are 256 subcarriers available, spread in 16 *spectral groups* of 16 subcarriers each, not all of them are usable: Two of the spectral groups (the outer ones) are not used due to being very close to the Nyquist frequency, while in each of the rest groups two subcarriers are used as pilots and the central ones are left unmodulated to avoid DC offsets. As a result, and since in the current document we are only interested in the MAC layer, only the 182 (=14x13) effective subcarriers are shown. The latter are the only subcarriers that should be taken into account during the bandwidth allocation process performed via the MAC layer.

In the (horizontal) time dimension, the overall frame duration of 105.6 μs is split into 8250 OFDM symbols of 12.8 ns each. Furthermore, each symbol consists of 320 samples from the OLT perspective and 40 from the ONU one (the symbol duration should be the same for both, while the sampling rates of the OLT and the ONUs are 25 GSps and 3.125 GSps respectively). Note also that a cyclic suffix, employed to facilitate FFT operation, occupies 25% of the duration of each symbol.

3.3.2 The ACCORDANCE Frame Blocks

Moreover, as also shown in Figure 2, each ACCORDANCE frame is broken down in four discrete blocks:

- *Synchronization block*: Consists of 10 symbols and contains training symbols that allow the ONU receivers to perform coarse time and frequency synchronization.

- *Phase reference block*: Consists of 16 symbols and is used for phase estimation of each subcarrier.

- *Control block*: Consists of 32 symbols. In line with D4.5 descriptions, the control channel uses a robust modulation scheme (DBPSK) to avoid losing important control information. In the same direction, it was chosen to use a ½ FEC for the control data. As indicated in the figure, the same control information is sent in all spectral groups. In that respect, the available control bandwidth is limited to the bitrate that can be transmitted (using the parameters described above) using 13 subcarriers only. After performing the respective calculations, this bitrate equals approximately 2 Mbps, while the control block in each frame occupies 26 Bytes.

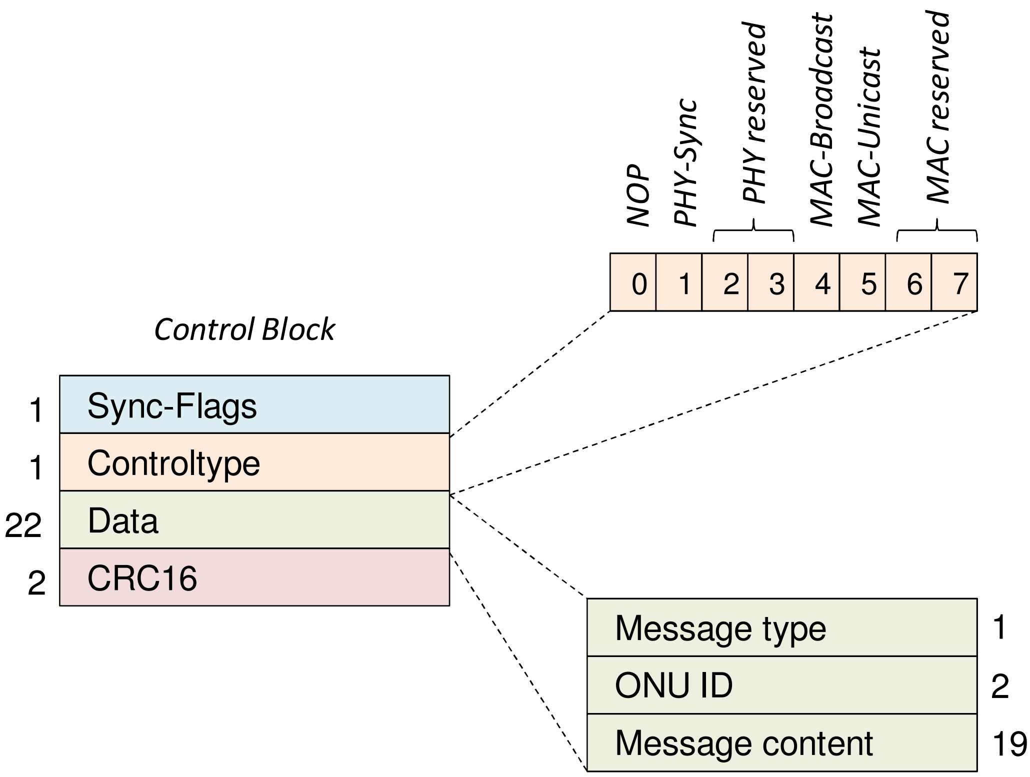

Figure 3: Detailed view of the ACCORDANCE frame control block structure and proposed usage of the data bytes available.

The structure of the control block is shown in Figure 3. It can be seen there that Byte 0 is devoted to PHY-layer synchronization, while bits 4-7 of Byte 1 are used by the MAC. In particular, bits 4 and 5 indicate whether the control message is broadcast or unicast, while bits 6 and 7 are reserved to be used at will. Taking out the last two bytes used for a 16-bit CRC, there are 22 Bytes available for each control message. In the figure we suggest a possible structure of the control messages, whereby the first byte is used for discriminating among the various message types, the next 2 Bytes denote the ONU and the remaining 19 Bytes can be used for carrying the actual message.

- *Data block*: Consists of 8192 symbols. In contrast to the previous block, the data block subcarriers can be modulated using any m-QAM format. Moreover, the data block is shared among the different ONUs as shown in the figure. In contrast to the control block, a Reed-Solomon FEC algorithm is employed.

Each ONU is allocated a set of adjacent subcarriers for a number of symbols ranging from 1 up to 8192. This is obviously in line with the *rectangular* bandwidth assignment proposed in D4.2, with the only restriction being that each ONU can only get subcarriers assigned in one spectral group. Therefore, the maximum number of subcarriers that can be used per ONU is limited to 13. However, this is not considered to be an issue, since it has already been shown in [4], [9], [10] that even from a QoS point of view it is beneficial to keep the maximum number of subcarriers per ONU limited to around 16 for a total number of 256 subcarriers (a ratio quite similar to the one in the ACCORDANCE system under discussion).

Note that the series of rectangles assigned to each ONUs in consecutive ACCORDANCE frames form a transmission pipe, called *Virtual Channel (VC)* (the VC for ONU 3 is depicted in Figure 2). The OLT informs the ONU via control messages (that will be elaborated below) about the exact shape of its rectangle in the upcoming frame and then the ONU can transmit in a continuous manner using this VC. Note that, unless instructed otherwise via a new message, the ONU will assume the same subcarrier/timeslot allocation in all upcoming frames.

The payload of the ONU (e.g. Ethernet frames) is encapsulated in the so-called ACCORDANCE *VC packets* as shown in Figure 4. Since a continuous bit stream has to be transmitted through the VC, it is necessary to send pad (zero) bits in between the transmitted VC packets. The packets are identified with the help of a predefined 4-byte pattern ("magic number"), while their header also includes their exact length (maximum packet size is 64 kBytes) and their payload type (e.g. Ethernet, CPRI…). It can be seen in the figure that there are two options for the payload transmission: In the first one, each Ethernet frame (or any other packet type supported) is placed in a separate VC packet. In other words, whenever a new Ethernet frame is available, it is encapsulated in a VC packet and sent via the VC. This guarantees minimum delay, however it may imply a significant additional overhead due to the VC packet header (8 bytes), especially for small frames (e.g. 64 Bytes). The alternative option would be to perform an assembly of several Ethernet frames and group them in a single VC packet to reduce the associated overhead. However, care has to be taken when implementing the assembly algorithm to avoid excessive delays for some of the encapsulated Ethernet frames.

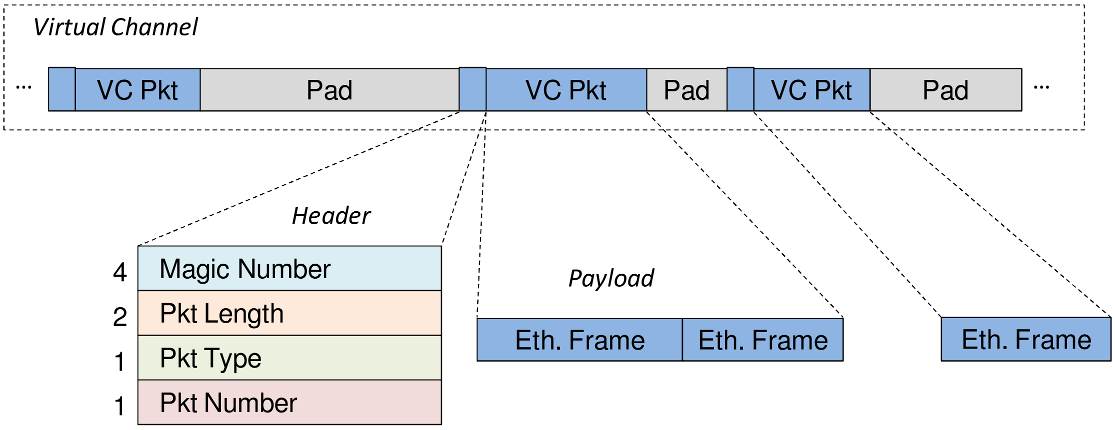

Figure 4: Detailed view of an ACCORDANCE Virtual Channel and the VC packet structure.

Depending on the modulation format used (note that, as defined in D4.2, a different modulation format can be used by each ONU depending on their transmission performance) and based on the aforementioned parameters, the *aggregate* bitrates shown in Table 1 are available for transmitting payload data (i.e. taking out the cyclic suffix and FEC overheads, as well as the pilot and zero subcarriers). In this table it is assumed that all ONUs employ the same format.

Table 1: Aggregate payload capacity for different modulation formats.

Modulation Format	Aggregate Payload Capacity (Gbps)
DBPSK	14.2
DQPSK	28.4
8-QAM	42.5
16-QAM	56.7
32-QAM	70.9
64-QAM	85.1
128-QAM	99.2
256-QAM	113.4

4. Implementation of the ACCORDANCE MAC

4.1 Introduction

Taking into account the nature of the control and data streams in the ACCORDANCE FPGA system, as discussed above, in this section we elaborate on how the control and payload data of ACCORDANCE can be transmitted in the best possible way.

4.2 Options for the Control Channel

Two different options were identified for implementing the necessary MAC protocol functionalities:

- In the first case, we would modify/enhance the EPON MPCP control message set following the detailed instructions provided already in D4.2 and use the *data block* of the ACCORDANCE frame for transmitting those messages (just like normal data frames). This option provides the maximum possible flexibility, since it in essence allows implementing a full MAC protocol suite if needed. However, since the control information should be available to all ONUs (e.g. for broadcast messages), it implies that the data block of *at least one* of the 13 available subcarriers *per spectral segment* in all downstream ACCORDANCE frames should be reserved for this purpose. It is obvious that this leads to a significant waste of bandwidth.

- Since, as shown already in Figure 2 (and explained in detail in Section 3.3.2), a control block has already been reserved in each ACCORDANCE frame (the same control information is sent in all spectral groups), it makes sense from a utilization point of view to take advantage of it for hosting the required control messages. The only potential drawback of this method is that, as discussed above, the maximum possible control message size in each frame is 24 Bytes, thus limiting the possible message contents. However, by having a closer look at the message definitions provided in D4.2, it is clear that all required message types can be hosted in the aforementioned number of Bytes.

As mentioned in the introduction, the first option seems preferable for the preparation of the MAC to be used in the final experimental validation of ACCORDANCE, since it is considered as adequate enough for demonstrating all MAC functionality. However, the preceding discussion actually refers to the *downstream* direction, since in that case the same control block is broadcast to all ONUs. The same approach cannot be followed for the upstream, where frames are formed by adding the signals sent by the various ONUs. The reason is that this would require some form of coordination between ONUs for sharing in a TDMA manner the upstream control block across consecutive frames, thus increasing the overall MAC complexity.

Hence, for transmitting the required *upstream* MAC messages, the most feasible option seems to be the use of the VCs allocated to each ONU and the encapsulation of those messages in normal Ethernet frames. As in the case of EPON, the *Length/Type* could be employed to distinguish them from payload frames while the *Opcode* field could indicate the different control message types.

Of course, for the purposes of the final ACCORDANCE experiments another possible solution, still using the ACCORDANCE frame control blocks would be to decide on a fixed TDMA sharing of upstream control blocks among the ONUs. For example, if 2 ONUs are connected, the one of them could use the control block of odd frames and the other the control block of even frames.

In Section 4.3 below we discuss how each the key required control messages could be implemented in the framework of the ACCORDANCE experimental testbed.

4.3 Implementation of Control Messages

4.3.1 Introduction

As mentioned in section 4.2 above, control messages in the ACCORDANCE validation testbed will mainly be implemented by using the control block of the ACCORDANCE downstream frames and, most probably, special purpose payload frames in the upstream direction. In either case, the preparation of the control messages as well as the actions taken upon their reception will be handled by the code developed for the FPGA embedded processor.

Below we elaborate further on how each of the key messages defined in D4.2 could be hosted in the ACCORDANCE experimental system. This should be considered as an initial discussion on the control messaging implementation, as the actual work will be performed in T6.2. In that respect, several other options will also be considered and the most appropriate ones (from both the functionality and complexity point of views) will be chosen. Moreover, additional messages may need to be implemented in the course of the aforementioned activities.

4.3.2 Registration

In D4.2 a comprehensive list of fields (e.g. operating wavelengths, laser tuning time etc) has been defined as necessary to be communicated during the ONU registration/activation phase. This is true in the case of a real system. However for the purposes of the ACCORDANCE experimental validation it is obvious that the aforementioned information is already known, so only a simple handshake mechanism is needed, consisting of the following messages:

Upstream

Register request: This message contains no actual contents and is transmitted by an ONU to the OLT upon its connection.

Register acknowledgement: This message also contains no actual contents and is transmitted by an ONU to the OLT upon to acknowledge receipt of the corresponding downstream REGISTER message (see below).

Downstream

Register: This message is sent from the OLT to an ONU after a *REGISTER_REQ* message has been received. In the context of the ACCORDANCE experiments, the additional information that needs to be sent within such a message is the modulation format to be used by the ONU. According to D4.2, 1 Byte is enough for this purpose.

4.3.3 Bandwidth assignment

Upstream

Report: In case a queue status reporting approach is followed by the implemented DBA algorithms, it will be required to include an upstream message containing the amount of bytes stored in the ONU buffer. The exact details of such a message are to be further elaborated if needed in Task 6.2 (FPGA board preparation).

Downstream

Grant: This message is sent from the OLT to an ONU for the creation of a transmission pipe. As described in D4.2, due to the rectangular shape of the allocations, it is only required to include the low/high subcarrier indices (with less than 256 subcarriers available, 1 Byte is enough for the two aforementioned fields) and the start/stop time within the upcoming frames. The latter are specified in symbols and, given that there are 8192 symbols per frame, 2 Bytes are enough for each of the start/stop time fields. Therefore, 8 Bytes are needed per grant, making it even possible to host two grants per downstream control block if needed (the reserved bits of the Controltype field – see Figure 3 – could be used to indicate this case).

Rx Configuration: In ACCORDANCE (in contrast to common TDMA-PONs), it is also necessary to perform *downstream* bandwidth allocation (ONUs do not receive all downstream subcarriers). Therefore, the *Rx Configuration* message (in a similar manner to *Gate*), is sent in advance by the OLT to an ONU to inform it about the subcarrier range and timeslots they should receive. The field lengths are identical to what was described above for the *Gate* messages.

4.3.4 Adaptive subcarrier modulation

As described in D4.2, during the registration process of each ONU, the OLT needs to identify the most appropriate modulation format to be used by each ONU. The mechanism for achieving this has been described already in D4.2. The associated messages are the following:

<u>Upstream</u>

Remote error indication: This is a message sent by the ONU to the OLT, reporting the number of BIP errors it has counted during the indicated by the OLT (see below) BER interval. The exact number of bytes required for this message will be defined during Task 6.2 (FPGA board preparation).

<u>Downstream</u>

BER interval: This message is sent from the OLT to an ONU and requests from it to monitor errors within the specified interval. Again, the exact number of bytes for this message will be defined in Task 6.2.

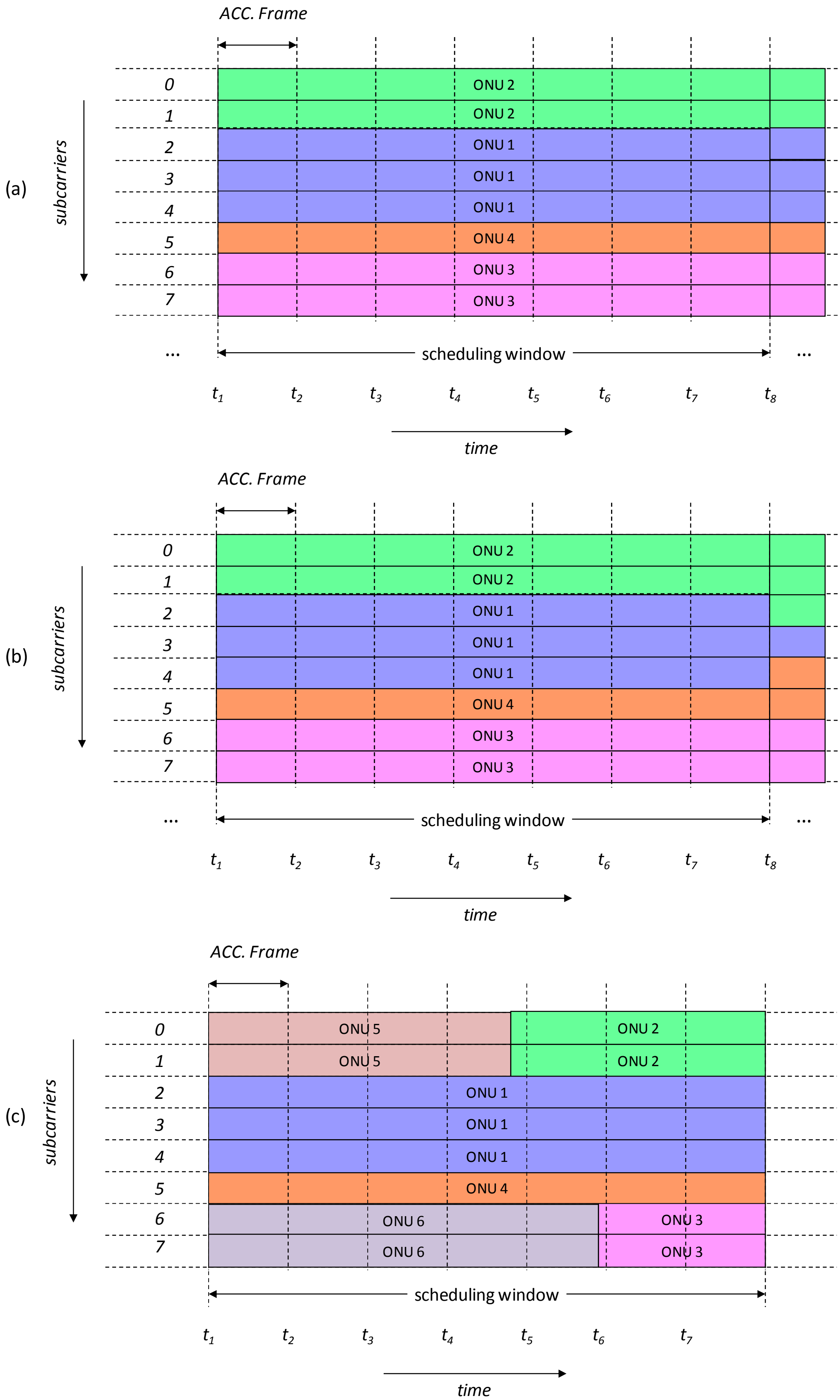

Figure 5: Examples of (a) FSCA, (b) DSCA and (c) RDSCA operation.

4.4 Options for the Payload Channels

As described above, the way the payload data block is implemented provides significant flexibility for bandwidth allocation among ONUs. In particular, it allows implementing in essence all the key types of subcarrier allocation described in D4.2, namely:

- *Fixed Subcarrier Assignment (FSCA)*: Each ONU is allocated, upon their registration, a fixed number of 1 to 13 subcarriers for the whole duration of each frame. This is the least flexible approach; however it serves well as an initial test case to verify the experimental setup.

- *Dynamic Subcarrier Assignment (DSCA)*: The ONU is allocated a fixed number of subcarriers (again, from 1 up to 13), but only for the next scheduling window. The duration of the scheduling window could range from 1 to several tens of frames. However, a very small time window will be very challenging from a processing point of view (given also the expected latency in the communication between the embedded processor, the MAC module and the PHY layer). On the other hand, a very large window will cause an unwanted increase in packet delay. In D4.2, an indicative window of few ms is suggested (compare this also to the 2 ms window suggested in the majority of the EPON literature). In any case though, during the experiments to be performed in the framework of Task 6.2, it is expected that the optimal trade-off will be identified.

- *Rectangular Dynamic Subcarrier Assignment (RDSCA)*: According to D4.2, the RDSCA mode implies that the ONU is allocated a fixed number of subcarriers for a limited number of timeslots within the next scheduling window. Given the MAC implementation as described above, it is obvious that, unless the scheduling window duration equals 1 ACCORDANCE frame, RDSA can only be realized via the transmission of multiple control messages per scheduling window, rendering it somehow impractical.

Figure 5 shows an example of upstream bandwidth assignment using the FSCA, DSCA and RDSCA modes. In this example, the scheduling window equals 7 ACCORDANCE frames. For simplicity we show only the payload data block of each frame and only 8 subcarriers. The time instants $t_1 - t_8$ indicate the arrivals of control messages from the OLT to the ONUs, assigning VCs according to the required bandwidth allocation for each ONU. It is assumed that those messages arrive before the upcoming frame, and that the new VCs are valid from that frame on. Below we describe the control messages required in each case to achieve the allocations shown in the figure:

FSCA [Figure 5 (a)]:

time t_1:

- Control message to ONU 2, allocating subcarriers 0-1 for symbols 0-8191.
- Control message to ONU 1, allocating subcarriers 2-4 for symbols 0-8191.
- Control message to ONU 4, allocating subcarrier 5 for symbols 0-8191.
- Control message to ONU 3, allocating subcarriers 6-7 for symbols 0-8191.

DSCA [Figure 5 (b)]:

time t_1:

- Control message to ONU 2, allocating subcarriers 0-1 for symbols 0-8191.
- Control message to ONU 1, allocating subcarriers 2-4 for symbols 0-8191.
- Control message to ONU 4, allocating subcarrier 5 for symbols 0-8191.
- Control message to ONU 3, allocating subcarriers 6-7 for symbols 0-8191.

time t_8:

- Control message to ONU 2, allocating subcarriers 0-2 for symbols 0-8191.
- Control message to ONU 1, allocating subcarrier 3 for symbols 0-8191.
- Control message to ONU 4, allocating subcarriers 4-5 for symbols 0-8191.
- Control message to ONU 3, allocating subcarriers 6-7 for symbols 0-8191.

DSCA [Figure 5 (c)]:

time t_1:

- Control message to ONU 5, allocating subcarriers 0-1 for symbols 0-8191.
- Control message to ONU 1, allocating subcarriers 2-4 for symbols 0-8191.
- Control message to ONU 4, allocating subcarrier 5 for symbols 0-8191.
- Control message to ONU 6, allocating subcarriers 6-7 for symbols 0-8191.

time t_4:

- Control message to ONU 5, allocating subcarriers 0-1 for symbols 0-6999.
- Control message to ONU 2, allocating subcarriers 0-1 for symbols 7000-8191.

time t_5:

- Control message to ONU 5, allocating zero subcarriers/symbols.
- Control message to ONU 2, allocating subcarriers 0-1 for symbols 0-8191.
- Control message to ONU 6, allocating subcarriers 6-7 for symbols 0-7499.
- Control message to ONU 3, allocating subcarriers 6-7 for symbols 7500-8191.

time t_6:

- Control message to ONU 6, allocating zero subcarriers/symbols.
- Control message to ONU 3, allocating subcarriers 6-7 for symbols 0-8191.

It is obvious that in the FSCA case, control messages for bandwidth allocation only need to be sent once per ONU, while in DSCA they may be needed at maximum once per scheduling window. On the contrary, RDSCA implies a significantly larger amount of messages (in the ACCORDANCE frame timescale), in order to achieve the required sub-frame granularity.

5. Abbreviations

ACCORDANCE	A Converged Copper-Optical-Radio OFDMA-based Access Network with high Capacity and flExibility
ADC	Analog to Digital Converter
BE	Best Effort
BER	Beat Error Ratio
DAC	Digital to Analog Converter
DBA	Dynamic Bandwidth Assignment
DBPSK	Differential Binary Phase Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
DSCA	Dynamic Subcarrier Assignment
EPON	Ethernet PON
FDM	Frequency Division Multiplexing
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FSCA	Fixed Subcarrier Assignment
GPON	Gigabit PON
MAC	Medium Access Control
MPCP	Multi Point Control Protocol
OFDM	Orthogonal Frequency Division Multiplexing
OFDMA	Orthogonal Frequency Division Multiple Access
OLT	Optical Line Termination
ONU	Optical Network Unit
PON	Passive Optical Network
QAM	Quadrature Amplitude Modulation
QoS	Quality of Service
RDSCA	Rectangular DSCA
TDMA	Time Division Multiple Access

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