WiserBAN

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Siemens Audiologische Technik GmbH	DE-SAT	DE
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WiserBAN

Smart miniature low-power wireless microsystem for Body Area Networks

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Revision History

Version	Date	Changed page(s)	Cause of change	Partner
V0	Feb14 2012		Creation	CSEM
V1			Pre-final version	SORIN
V2	March 28, 2012		Reviewed version, unified D1.2 vs D1.3	CSEM
V3	April 9, 2012		Final review	CSEM

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Contents

Executive Summary

D1.2 is a deliverable from WP1 which is the workpackage that focuses on the selection and description of the platform applications which will be enabled by the WiserBAN BAN radio modules, on the derivation of the associated platform requirements, and on the definition of the radio system architecture.

In particular, D1.2 concerns Task 1.2 Platform architectures: the main objective of this task is to specify the requirements for the WiserBAN platform, based on the use cases derived in Task 1.1. In addition, other important requirements which are not directly related to the analysed applications may be considered here in order to maintain the generic character of the platform.

This formal deliverable "D1.2 Final platform specification and architecture" is the result of the evolution of the internal deliverable "IR1.2 Target radio platform and specification" that has evolved along the specification process up to be able to be delivered externally:
- The platform specification is derived from the use cases requirements and parameters that have been described in deliverable "D1.1 Report about WiserBAN platform applications". Details comments are associated to each particular demand in Annex 11. User point of view is described in the "IR1.1 (M4) Target platform specification and architecture" document and a more detailed designer point of view is described in this document.
- This document can be seen as a top-level PLATFORM specification. Detailed specifications for different sub-parts are associated to different specific documents to allow a distribution of specification work and update of those documents during the design.

1 Introduction

This formal deliverable "**D1.2 Final platform specification and architecture**" is the result of the evolution of the internal deliverable "**IR1.2 Target radio platform and specification**" that has evolved along the specification process up to be able to be delivered externally. As master specification of the platform, this document may still evolve to precise some points that have been considered unclear or to add some discovered points during the rest of the project.

The platform specification is derived from the use cases requirements and parameters that have been described in deliverable "**D1.1 Report about WiserBAN platform applications**". Details comments are associated to each particular demand in Annex 11. User point of view is described in the "**IR1.1 (M4) Target platform specification and architecture**" document and a more detailed designer point of view is described in this document.

This document can be seen as a **top-level PLATFORM specification**. Detailed specifications for different sub-parts are associated to different specific documents to allow a distribution of specification work and update of those documents during the design. This document is a readable, standalone and synthetic concatenation of the following sub-documents used the design teams on an internal basis:

- IR1.3 Target radio System-on-Chip architecture and specifications (CSEM), evolving to the D1.3 Final radio system architecture and specification.
- IM2.1 Target RF specifications (CSEM).
- IM2.2 RF_IF_MEMS Target Specs (CSEM).
- IM2.3 LF MEMS and Oscillator target specs (CSEM).
- IR3.2 Intermediate report on smart antenna-to-radio interface for the active tunable antenna (VTT).
- IR3.2 Intermediate report on smart antenna-to-radio interface for the active tunable antenna (VTT).
- IR4.1 Reconfigurable baseband and protocol draft architecture description (CEA).
- IR5.1 3D SiP platform architecture proposal (TUB).
- D6.1 Implementation of wearable and implantable BAN demonstrators (DE-SAT & SORIN)

Note that in case of inconsistency between those documents and this top-level specification, the correct values are the ones presented in the sub-part specification document listed above.

2 Platform hardware architecture

2.1 From scenarios to demonstrators

For sake of clarification, the following terminology is used when discussing about the demonstrators:

- **Scenarios (or use-cases), established in WP1**: Deliverable "**D1.1 Report about WiserBAN platform applications**" sketched several scenarios, among which four principal scenarios related to the four industrial end-users: Audio case (SAT), Insulin pump case (DEBIOTECH), Cardiac implant case (SORIN), cochlear implant (MEDEL).

- **Demonstrator Platforms, to be realized in WP6**: According to the DoW, there are two demonstrator platforms, namely the "**Wearable BAN demonstrator**" and the "**Implanted BAN demonstrator**". The former concentrates inputs related to the SAT and the DEBIOTECH scenarios, the later towards the SORIN and the MEDEL scenario. The Demonstrator Platforms collects the technology bricks from WP2 to WP5 and assembles them into prototypes for validating and demonstrating the WiserBAN concepts.

At this stage, the precise architectural break-down of the demonstrator platforms needs yet to be defined, under the lead of the industrial end-user partners. For the sake of channelizing the discussions, the following table shows the relation between the two Demonstrator Platforms and the four principal end-user-driven Scenarios (or use-cases).

The color codes are the following:

Blue is for the Wearable Demonstrator platform:

- **Dark blue** for the principal items of the demonstrator: this targets a full demonstration based on the complete set of building bricks from WiserBAN (SoC/SiP, antenna, protocol) jointly with other end-user components (housing, other chips, power-management, applicative software, etc).

- **Light blue** for secondary items of the demonstrator: this concerns only a "limited" validation with only selected building bricks:

Purple is for the Implanted Demonstrator platform:

- **Dark purple** for the principal items of the demonstrator: this targets a full demonstration based on the complete set of building bricks from WiserBAN (SoC/SiP, antenna, protocol) jointly with other end-user components (housing, other chips, power-management, applicative software, etc).

- **Light purple** for secondary items of the demonstrator: this concerns only a "limited" validation with only selected building bricks.

Demo. Platform	Scenario (use-case)	BAN node type	Platform			
			SiP	Antenna	Available Supplies[2]	Used interface
Wearable BAN demo	Audio Case (SAT)	Behind-The-Ear Hearing Instrument	3D	VTT active	Zinc-air + Voltage step-up	I2S, GPIO
		In-The-Ear Hearing Instrument[3]	3D	CEA Active		
		Remote Control [1]	MicroSD card, see line at bottom of table			
	Insulin Pump Case (DEBIOTECH)	Insulin Pump[4]	2D	Debiotech	Zinc-air + 2.3V	UART, GPIO
		Remote Control [1]	MicroSD card, see line at bottom of table			
Implanted BAN demo	Cardiac Implant Case (SORIN)	Cardiac Pump	2D	Sorin	Lithium + Voltage step-down	SPI
		Remote Control [1]	MicroSD card, see line at bottom of table			
	Cochlear Implant Case (MEDEL)	Cochlear Implant [5]	2D	CSEM	Li-ion + Voltage step-down	I2, SPI
		Remote Control [1]	MicroSD card, see line at bottom of table			
Both demo platforms	MicroSD card	Remote control for several Scenarios [1]	2D	CEA LETI passive	2.0-3.6V + on-SiP LDO	SPI

Table 1: Demo. platforms vs SiP type, antenna, supply and IOs. C.f. text above for color code.

Notes:

1. The remote control node is the same for all scenarios and demonstrators
2. The SiP necessitates a 1.2V±10% supply for its core and a max. 3.6V supply for its digital IOs. The voltage of this IOs voltage supply depends on the voltage supply of the circuitry connected to these digital IOs (e.g. 1.8 is the M95M01 EEPROM min. voltage supply).
3. The In-The-Ear platform case is redundant with the Behind-The-Ear demonstration platform for its functionality: its study is then limited to its dedicated antenna and propagation environment.
4. The budget link associated to the Insulin Pump is less constrained than the others. The product, with especially an embedded antenna, already exists: its study is then more theoretical and concentrated on the improvement in term of functionality and current consumption.

The Cochlear Implant platform case is redundant with the Behind-The-Ear demonstration platform for its functionality aspects: its study is then limited to its dedicated antenna and propagation environment.

2.2 3D SiP

The 3D SiP try to reduce as much as possible the overall volume of the SiP.

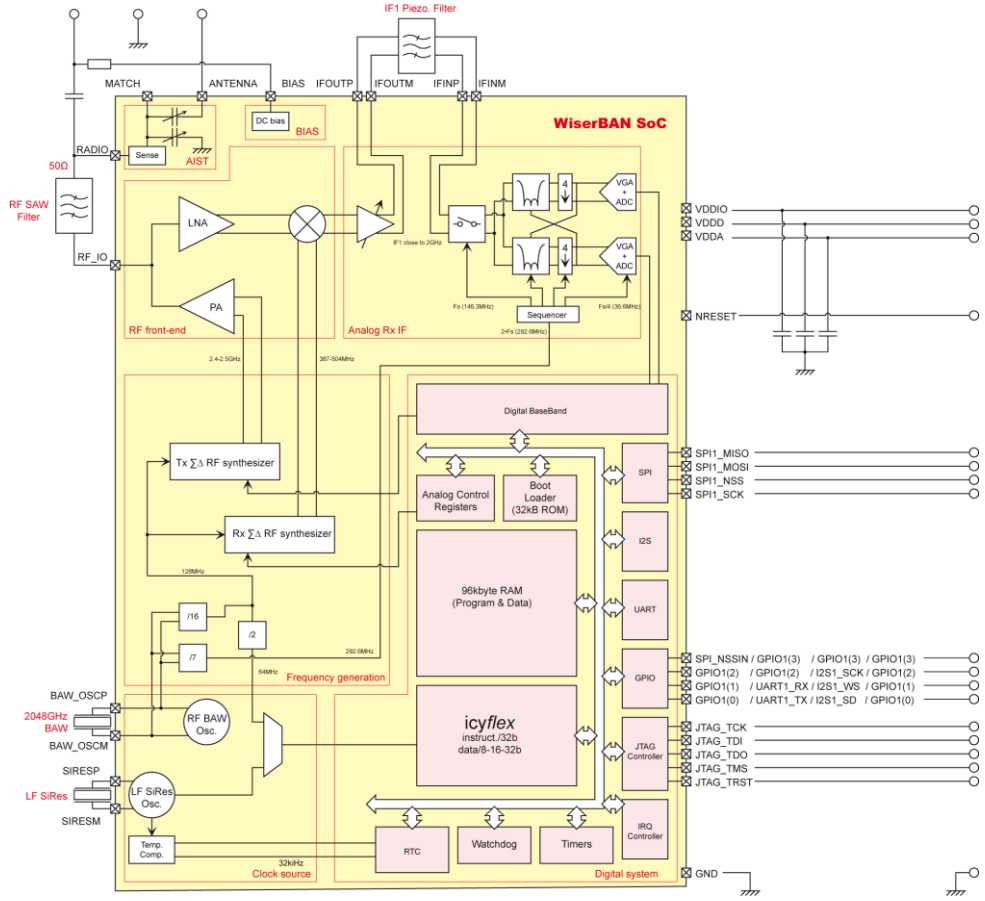
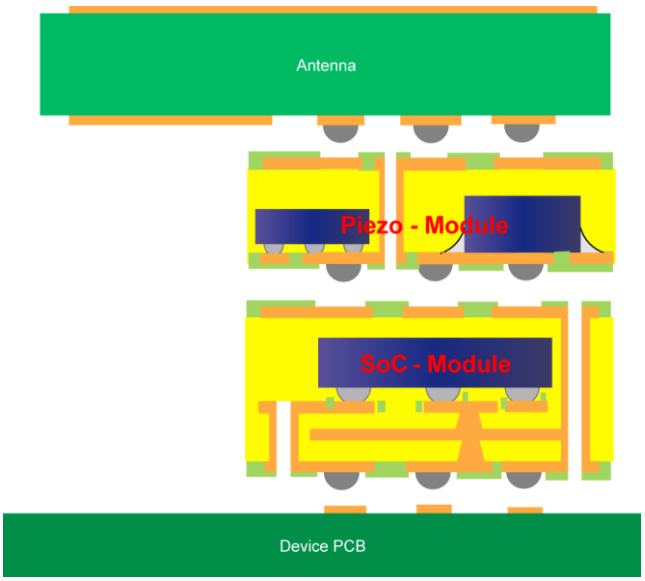


Figure 1: 3D SiP Schematic



3.0 x 3.0 x 1.0 mm^3
(approximation tbc)

(2+4) x copper layers

2x 50µm FR4 bottom interlayer

Ø100µm via
Ø150µm via pad

100µm min. isolation and min. trace width

Figure 2: 3D SiP layers stacking principle

2.3 2D SiP

The 2D SiP try to reduce as much as possible the thickness of the SiP.

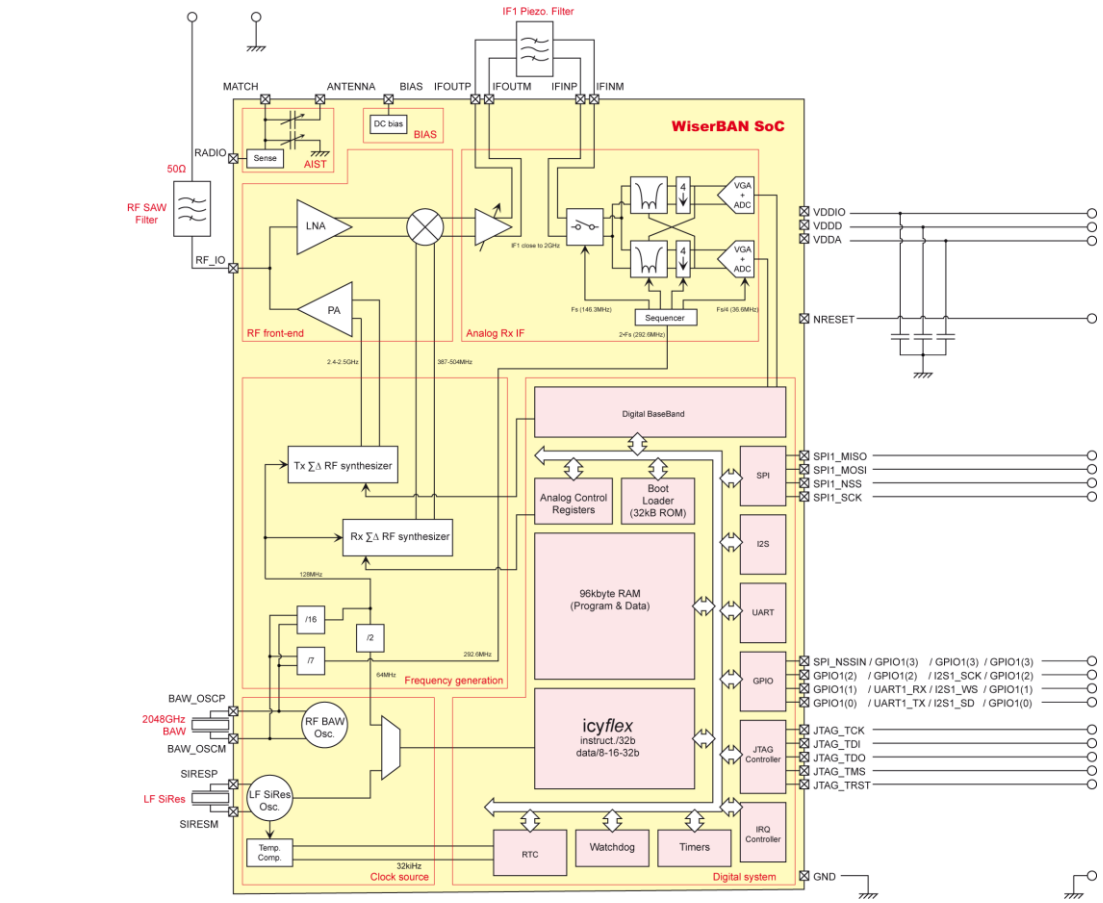
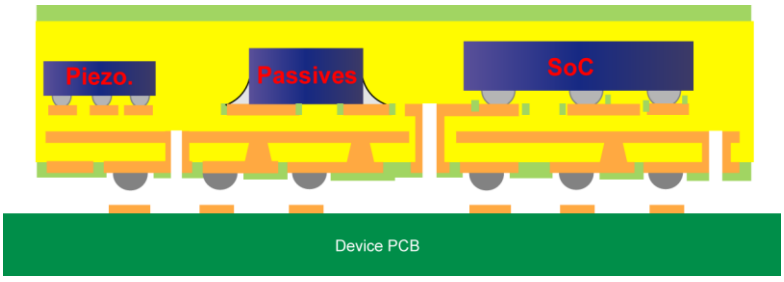


Figure 3: 2D SiP Schematic



5.0 x 3.5 x 0.8mm^3
(approximation tbc)

3x copper layers

2x 50µm FR4
interlayer

Ø100µm via
Ø150µm via pad

100µm isolation and
min. trace width

Figure 4: 2D SiP layers stacking principle

2.4 microSD SiP

The microSD SiP embed a complete RF modem including the antennain a microSD card.

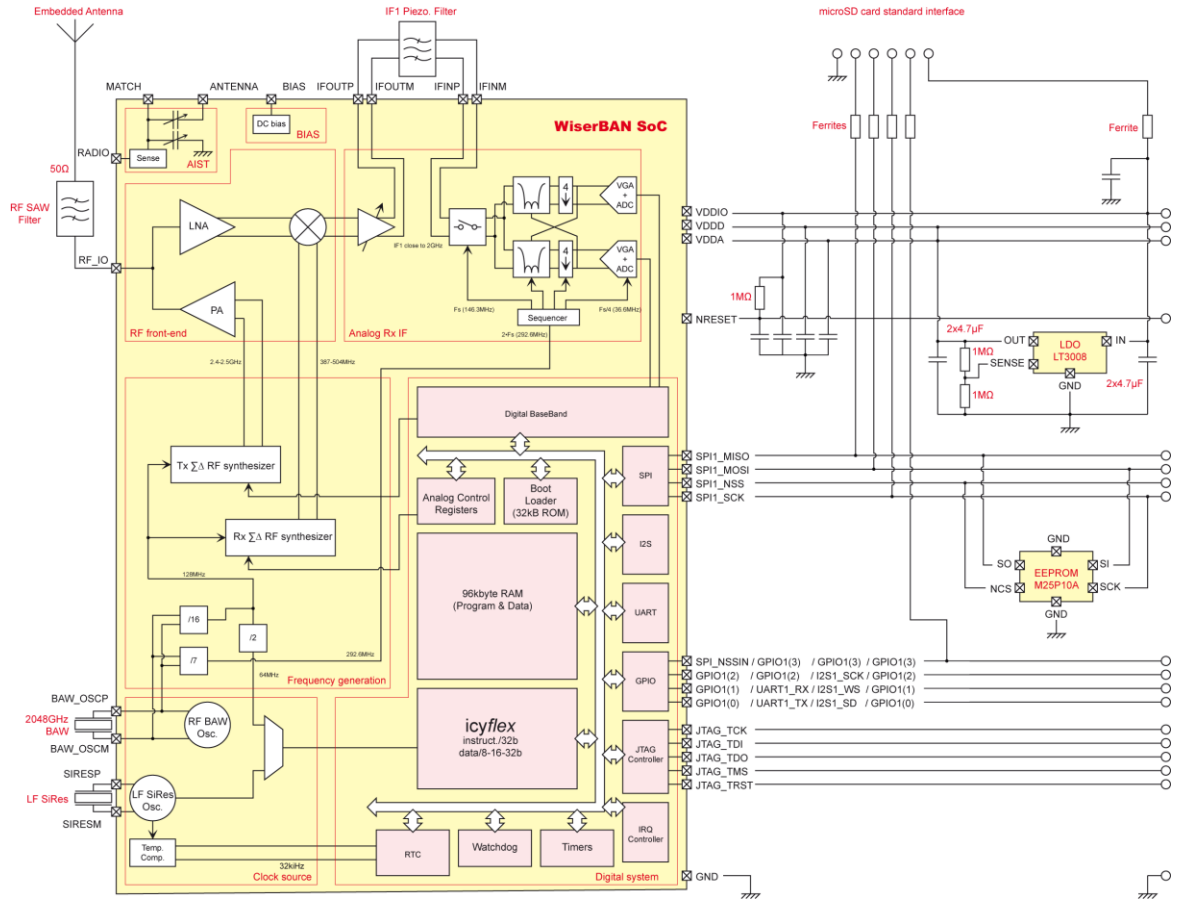
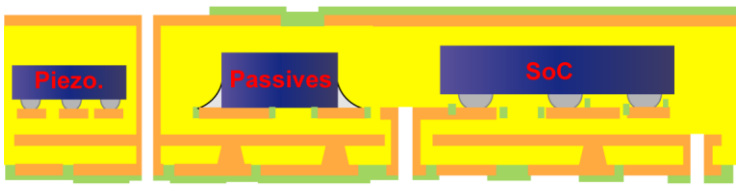


Figure 5: microSD SiP schematic



22.0 x 11.0 x 1.0mm^3

4x copper layers

2x 50µm FR4 interlayer

Ø100µm via
Ø150µm via pad

100µm isolation and min. trace width

Figure 6: microSD SiP layers stacking principle

The microSD card SiP supports the common SiP interface (described in section2.5) on one side for test and programming purpose together with a SPI interface to the SOC, mechanically and electrically compatible with standard microSD card SPI interface. Once programmed, the common SiP interface can be masked with a sticker for insulation.

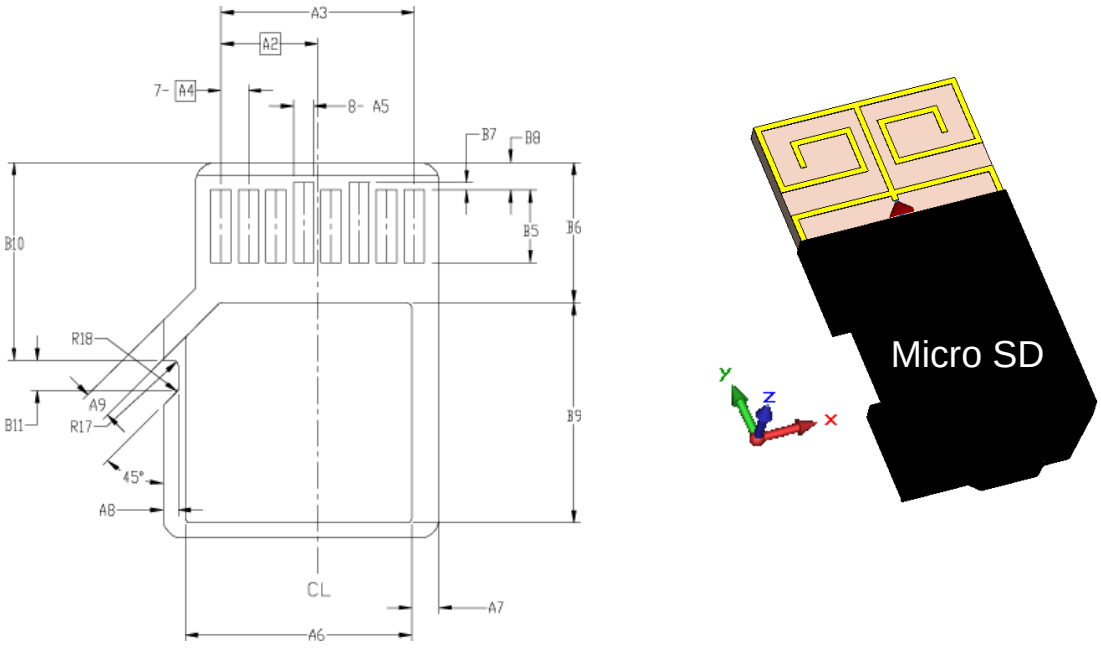


Figure 7: microSD card mechanical description

The microSD card SiP embeds an antenna in the 11x7mm extension from the standard mechanical format (c.f. section 2.7.4 and annex 10). The host microSD cardholder necessitates then an opening in order to place this antenna extension out of the host case (e.g. smartphone).

2.5 SiP IOs

2.5.1 Common interface

The electrical interfaces are described in the table below:

Name	I/O	Description
VDDA	supply	Core analog positive voltage supply (1.2V±10%) (1)
VDDD	supply	Core digital positive voltage supply (1.2V±10%) (1)
VDDIO	supply	Digital interface positive voltage supply (<3.6V)
GND	supply	Ground of the platform and negative voltage supply
RADIO	analog	Antenna port for 2D SiP, unused for other SiP
NRESET	in	Platform reset, active low, pull-down by default
JTAG_TCK	in	JTAG Test ClocK
JTAG_TDI	in	JTAG Test Data Input
JTAG_TDO	out	JTAG Test Data Output
JTAG_TMS	in	JTAG test Mode Select
JTAG_TRST	in	JTAG Test ReSeT, actif low
SPI1_NSS	in	SPI Not Slave Select of external used by bootloader
SPI1_SCK	in-out	SPI Serial Clock
SPI1_MOSI	in-out	SPI Master-Out Slave-In
SPI1_MISO	in-out	SPI Master-In Slave-out
GPIO1(3)	in-out	General Purpose Input-Output, with multiplexed functionalities as described in the table below
GPIO1(2)		
GPIO1(1)		
GPIO1(0)		

Table 1: List of supply and ports of the SiP.

1. Present on microSD card SiP interface but an implemented voltage regulator elaborates the VDDA and VDDD from VDDIO inside of microSD card SiP (become then output instead of input).

Different serial communication interfaces are multiplexed on the GPIO as describe in the table below:

IO	**SPI (**11)	**UART** (10)	**I2S** (01)	**GPIO**[2](00)
GPIO1(3)	SPI1_NSSIN[1]	GPIO1(3)		
GPIO1(2)	GPIO1(2)		I2S1_SCK	GPIO1(2)
GPIO1(1)	GPIO1(1)	UART1_RX	I2S1_WS	GPIO1(1)
GPIO1(0)	GPIO1(0)	UART1_TX	I2S1_SD	GPIO1(0)

Table 2: description of multiplexed serial interface on GPIOs.

1. The SPI1_NSSIN is used for SPI interface when SoC in slave mode.

2. GPIO is the «by default» functionality of the pad, each pad can be configured independently.

To facilitate the test of different SiP and use a common programming tool, they are all sharing a common interface with same “bottom” PCB footprint that is described below:

SiP Common Pinning bottom view

	A	B	C	D	E	F
6	**GND**	JTAG_TRST	JTAG_TDI	ANTENNA	**GND**	**GND**
5	IFOUTM	JTAG_TMS	JTAG_TDO	JTAG_TCK	**VDDA**	**GND**
4	IFOUTP	**VDDIO**			**VDDA**	**GND**
3	NRESET	**VDDA**			**VDDD**	SPI1_MISO
2	**GND**	**GND**	GPIO1(0)	GPIO1(2)	SPI1_NSS	SPI1_SCK
1		**GND**	GPIO1(1)	GPIO1(3)	SPI1_MOSI	**GND**

SiP Common Pinning top view

	F	E	D	C	B	A
6	**GND**	**GND**	ANTENNA	JTAG_TDI	JTAG_TRST	**GND**
5	**GND**	**VDDA**	JTAG_TCK	JTAG_TDO	JTAG_TMS	IFOUTM
4	**GND**	**VDDA**			**VDDIO**	IFOUTP
3	SPI1_MISO	**VDDD**			**VDDA**	NRESET
2	SPI1_SCK	SPI1_NSS	GPIO1(2)	GPIO1(0)	**GND**	**GND**
1	**GND**	SPI1_MOSI	GPIO1(3)	GPIO1(1)	**GND**	

Table 3: SiP common interface pinning.

2.5.2 microSD SiP specific interface

An additional interface part described below is added only on microSD card (in operation, a sticker to insulate the common interface may be needed):

Figure 8: microSD card SPI mode compatible interface (NSS on GPIO&(3)).

2.5.3 RF interfaces and 3D SiP specific antenna interface

2.5.3.1 For the 2D SiP

The RF interface is implemented as RADIO footprint pad on the “bottom” common interface described in preceding section 2.5.1. This is a 50Ω connection to an out-of-SiP antenna.

2.5.3.2 For the 3DSiP

There are two possible active antennas described in section 2.7.2 and 2.7.3 that are mounted on “top” of SiP, i.e. at opposite side of “bottom” common interface described in preceding section 2.5.1. Because the two considered antennas are using different tuning scheme, they are connected to two different nodes of the SoC, the unused connection needing to remain unconnected on antenna side. A common physical bottom SiP interface is described below inFigure 9 below:

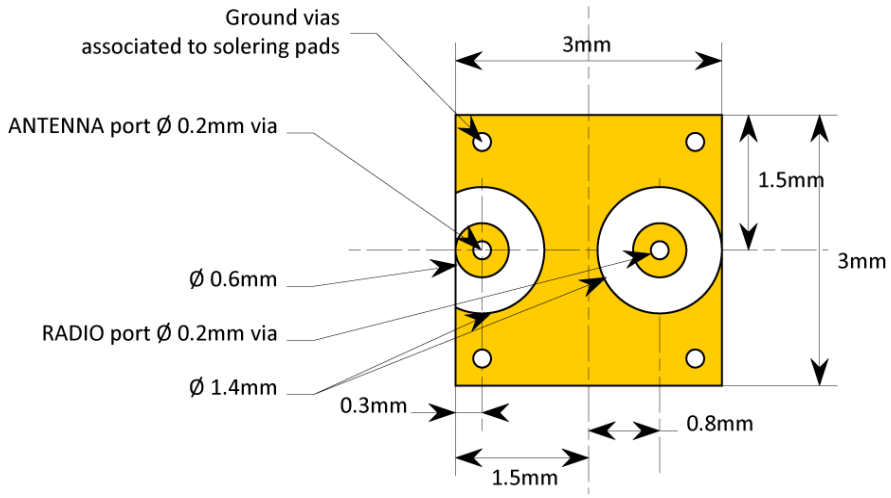


Figure 9: top 3D SiP interface to active antennas.

Note that attention has been paid to not miniaturize too much the RF interface in order to facilitate the testing (of SiP as well as antennas), for example with RF connector described in annexes 11.

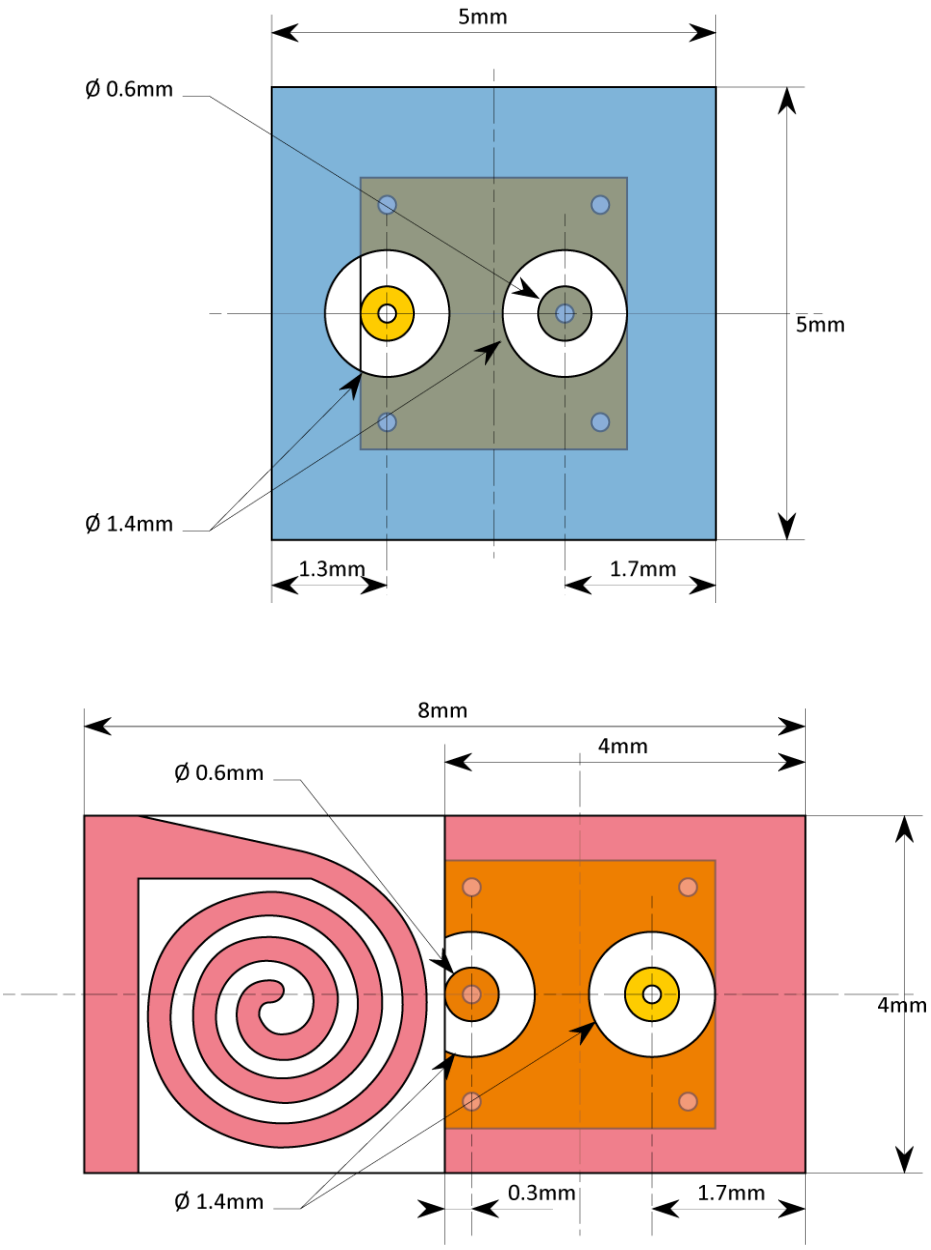


Figure 10: example of antenna superposition with antenna bottom footprint.

2.5.3.3 For the microSD SiP

The RADIO pad of the “bottom” common interface described in preceding section 2.5.1 remained unconnected because the antenna is embedded into the SiP as described in the section 2.7.4. There is then no RF signal at SiP interface.

2.6 Generic design specifications

2.6.1 Temperature

Because the targeted applications are Body-Area-Network, the temperature range should be limited to commercial grade, i.e. **0°C to 60°C** range. But we also want to enlarge the possible application of the platform to Wireless-Sensor-Network type of applications. For this reason and even if exceptions are always possible to not overstress the design, we are targeting the industrial grade, i.e. the **-40°C to 85°C** range.

2.6.2 Voltage supplies

The 65nm CMOS core voltage is fixed to 1.2V±10%, i.e. in the **1.08V to 1.32V** range. This voltage range is well aligned with the voltage provided by Zinc-air type of battery. When possible (to not overstress the design), it is interesting to **note min. 0.9V compliance** for possible enlargement to alkaline cell type of supply. This voltage can be further referred as “low-voltage” or “SoC core” supply.

On one hand, the 65nm CMOS thick gate transistors for digital IOs can handle up to 3.3V+10%. On the other hand, for large choice of EEPROM (or sensor, controller, etc), it is interesting to maintain the IOs voltage above 2.7V (even if the chosen one for the microSD card is 1.8V compatible). The voltage range, also well aligned with primary lithium cell (i.e. Li-SOCl2 or Li-MnO2) is then **2.7V to 3.6V**. This voltage can be further referred as “high-voltage” or “SoC IOs” supply.

2.6.3 Leakages

Because of important leakage variations with respect to temperature and technological cases, we only consider typical cases at 25°C for leakages calculations.

For long-autonomy scenarios (e.g. cardiac implant), the current consumption in standby may outbalance the active current consumption because of very low activity duty cycling to achieve multi-years of autonomy. For such applications a standby current in the order of 1µA is typically needed. The 65nm CMOS technology has been chosen for best active current performances and miniaturization but it can, certainly in this first integration, induce higher leakage current because of non-optimized digital library and memory. A special mode with a complete platform supply disconnection controlled by an external controller would be needed to reduce the leakage current.

However, to anticipate the use of low-leakages libraries and SRAM, it is important to maintain the leakages of the designed analog blocs at a low level.

2.7 Antennas

2.7.1 Overview

Several antennas are considered depending on the physical dimensions of the demonstrator.

All considered antennas are small and then induce close to isotropic radiation pattern, not considering their environment.

For the tiniest antenna cases, because of the associated low bandwidth, impedance-tuning schemes have to be considered in order to re-align the optimum frequency and, in general, optimize the antenna efficiency.

The precise specifications of the different antennas are described in the "**IR3.2 Intermediate report on smart antenna-to-radio interface for the active tunable antenna**" document from which the formal deliverables of the project Documents D3.2 and D3.3 will be derived.

2.7.2 Active L-antenna to be mounted on 3D SiP

The active tuning scheme is implemented in the SoC, placed between the RF front-end SAW filter and the antenna. It involves digitally tunable serial capacitor and a sensing mechanism controlled via a SPI-like interface by the on-chip controller (i.e. software algorithm).

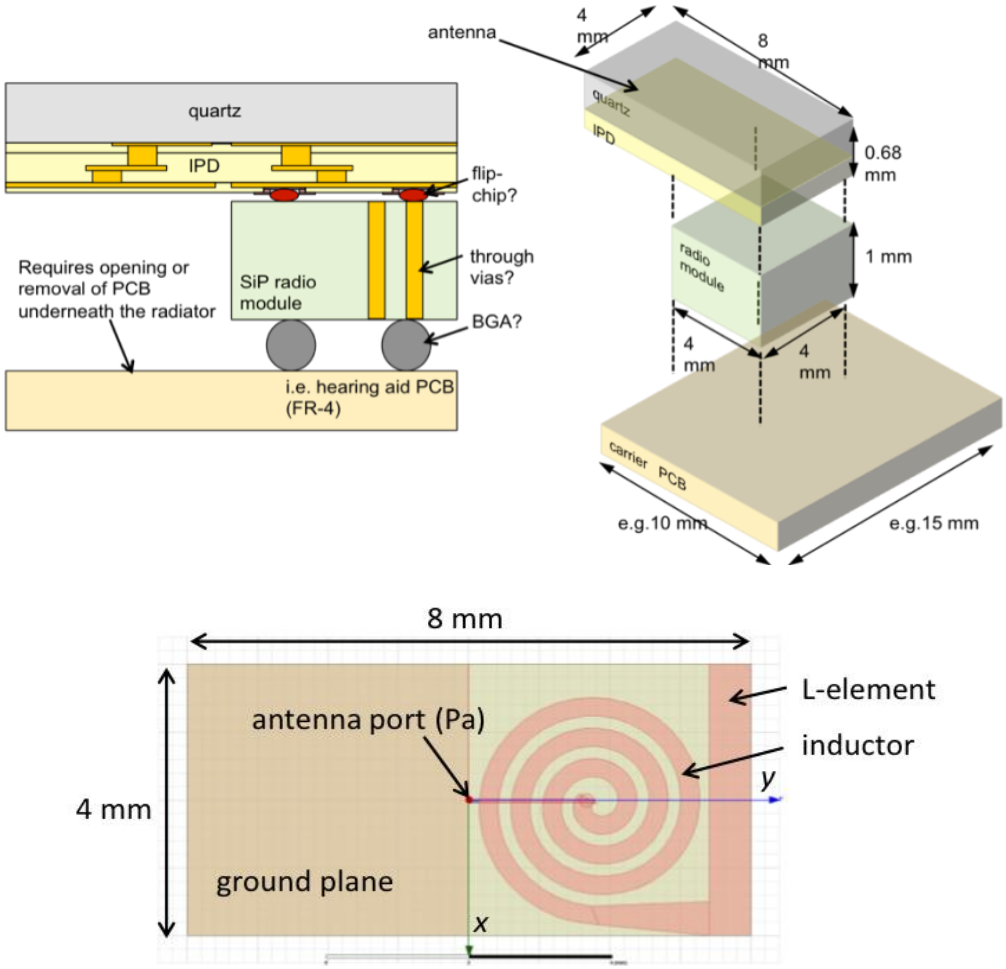


Figure 11: Active L-antenna

Typical specification are at 25°C, voltage supply=1.2V, unless otherwise noted.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Antenna Frequency		2400		2484	MHz
Antenna Bandwidth	50Ω matched, -10dB |s11|		10		MHz
Antenna Gain	50Ω matched, including losses	-12	-10	-8	dBi
Antenna size			8.0 x 4.0		mm^2
Antenna height			0.7		mm

Table 4: Active L-antenna specifications

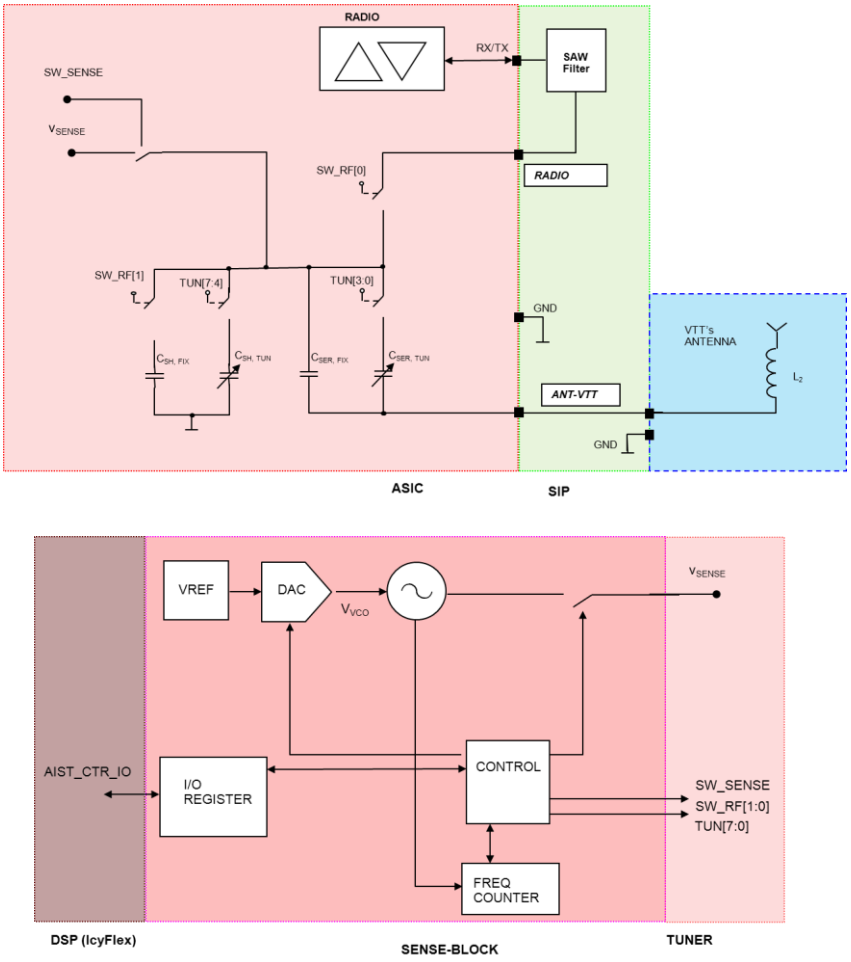


Figure 12: Antenna tunable matching network and impedance sensing

Typical specification are at 25°C, voltage supply=1.2V, unless otherwise noted.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Voltage supply		1.08	1.2	1.32	V
Fixed capacitance	Shunt capacitor (C_{SH})		0.41		pF
Tuning step			0.10		pF
Max. capacitance			5.60		pF
Fixed capacitance	Serial capacitor (C_{SER})		1.05		pF
Tuning step			0.21		pF
Max. capacitance			4.20		pF
Capacitor Q value			270		
RF switch Ron				1	Ω
Sensing active current			1		mA
Sensing leakages (2)	Including tuned capacitors			1	nA

Table 5: Active L-antenna specifications

Note that the active tuning scheme is described in the “IR3.2 Intermediate report on smart antenna-to-radio interface for the active tunable antenna” Document.

2.7.3 Agile slotted-dipole antenna to be mounted on 3D SiP

This antenna is the tinier antenna.

The agility scheme involves a discrete varactor, such as the one described in the annex 8, implemented directly on the antenna and an associated DC biasing voltage introduced via the antenna feed interface.

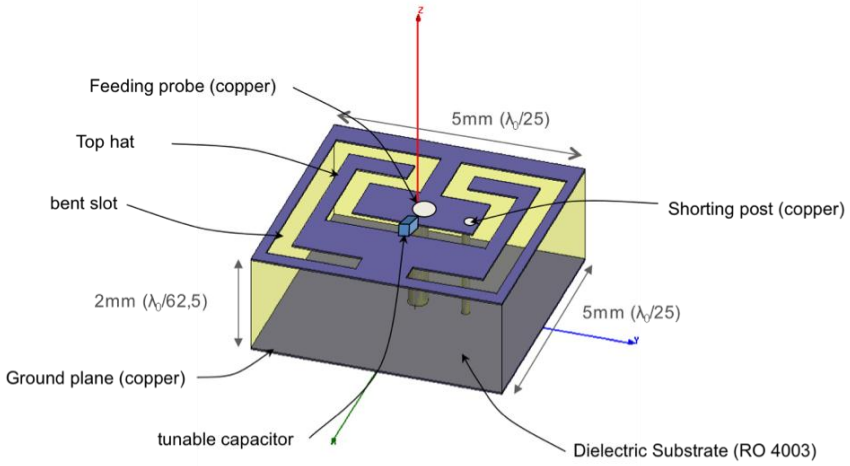


Figure 13: Agile slotted-dipole antenna

Typical specification are at 25°C, voltage supply=1.2V, unless otherwise noted.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Antenna Frequency (1)		2400		2484	MHz
Antenna Bandwidth	50Ω matched, -10dB |s11|		10		MHz
Total efficiency	Without considering ground plane extension in antenna integration and the human body effect		1		%
Antenna Gain	50Ω matched, included losses and without considering human body effects		-17.7		dBi
Tuning active current	1µA DC leakages at RF port			10	µA
Voltage control	Estimation from simulation results and varactor datasheet (by step of 0.02V)	1		2	V
Antenna size Antenna height			5.0 x 5.0 2		mm^2 mm

Table 6: Agile slotted-dipole antenna specifications

2.7.4 Passive microSDantenna

The preliminary design of the passive antenna is a folded T-shaped monopole antenna as shown in the figure 4. It is designed to be integrated on 11 x 7 x 1 mm^3 micro SD extension.

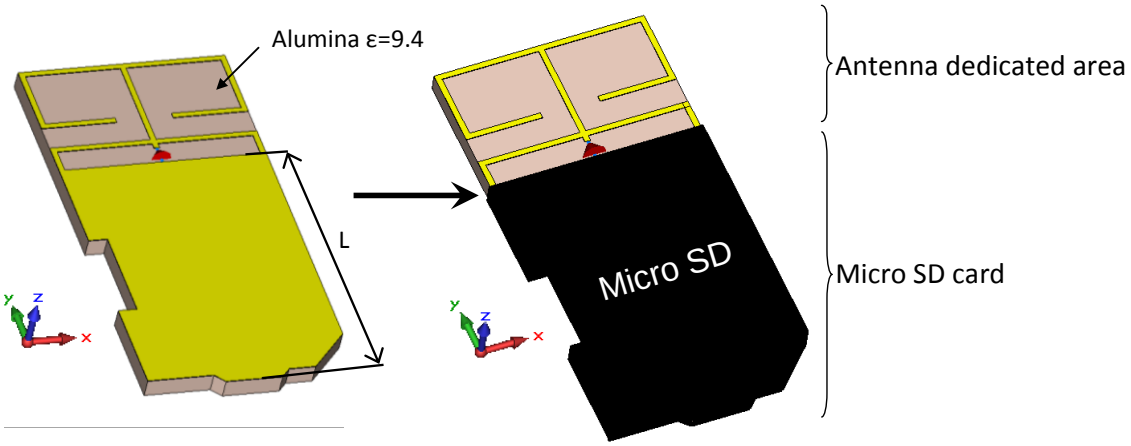


Figure 14: Preliminary design of the passive antenna

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Antenna Frequency (1)		2400		2484	MHz
Antenna Bandwidth	50 Ω matched, -10dB |s11|		35		MHz
Antenna Gain	50 Ω matched, including losses For L=15mm (micro SD card length) For L=3mm		0 -4		dBi
Total efficiency	For L=15mm For L=3mm		63 25		%
Antenna size Antenna height			11.0 x 7.0 1		mm^2 mm

Table 7: Passive antenna specifications

The results presented in this table do not consider the Micro-SD antenna insertion into the remote control

2.7.5 Passive antenna for cochlear implant

This antenna is large but need to be extremely flat because implanted between the skull and the skin. The very special environment needs to be taken into account in order to maximize the RF power radiated to the outside of the body.

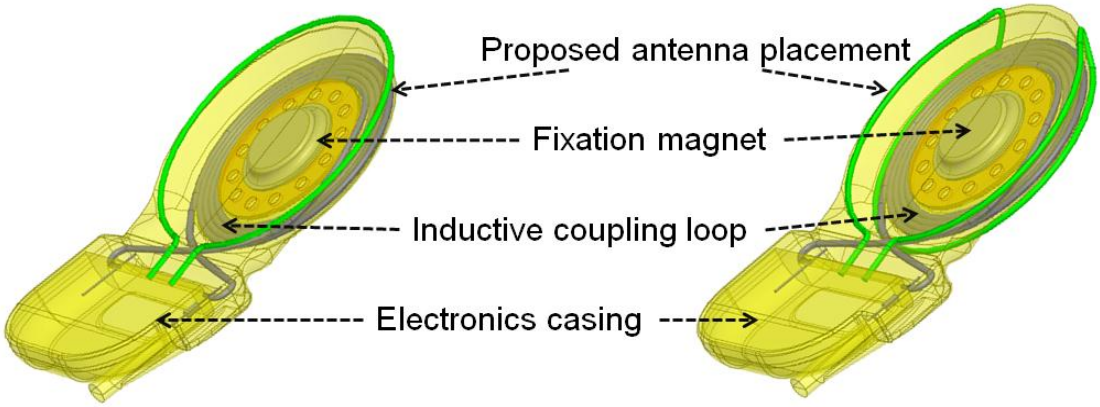


Figure 15: Passive cochlear implant antenna

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Antenna Frequency		2400		2484	MHz
Antenna Bandwidth	50Ω matched, -10dB |s11|		210		MHz
Antenna Gain	50Ω matched, including losses		-0.1		dBi
Antenna size Antenna height			28 x 28 3.8		mm^2 mm

Table 8: Passive cochlear implant antenna specifications

Because the antenna alone impedance is quite low, a matching network is necessary between the SoC with a 50Ω interface and the antenna. To obtain a wide enough bandwidth, a ∏ network is proposed as described in the Figure 16 below:

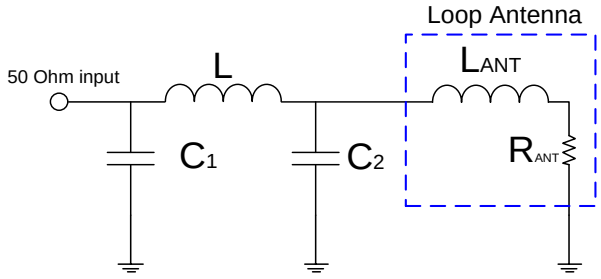


Figure 16: Proposed ∏ impedance matching network

2.7.6 Antenna for cardiac implant

This antenna is the bigger antenna but need to be installed outside the cardiac implant titanium package, inside the connector's head. The very special environment with metal parts needs to be taken into account in order to maximize the RF power radiated to the outside of the body. Because of compatibility with MICS standard (402-405 MHz) this antenna is dual band. However, in WiserBAN, only the 2.4-2.5 GHz band will be used and is specified here.

This antenna is not developed in WiserBAN project: existing design isreused. Antenna characteristics are given below for information.

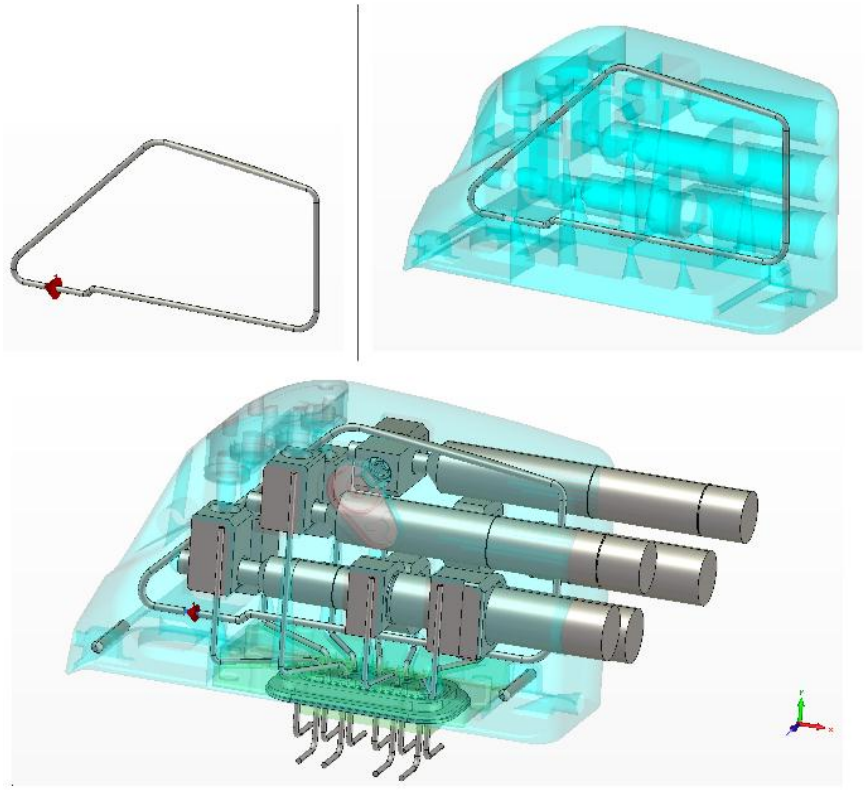


Figure 17: Cardiac implant passive antenna

Picture shows loop antenna (top left), loop antenna in plastic molding (top right) and complete assembly including cardiac probes metal inserts (bottom).

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Antenna Frequency		2400		2500	MHz
Antenna Bandwidth	50 Ω matched, -10dB |s11|		40		MHz
Antenna Gain	50 Ω matched, including losses	-6.6		+2.7	dBi
Antenna size			10 x 4		mm^2
Antenna height			<1		mm

Table 9: Cardiac implant passive antenna specifications

2.8 Piezoelectric components

2.8.1 Overview

The precise specifications of the different piezoelectric components are described in the "**IM2.2 Internal Milestone: RF, IF MEMS Target specifications**" and "**IM2.3 Internal Milestone: LF MEMS and oscillator target specifications**" documents from which the D2.2 and D2.3 prototypes as deliverables of the project will be derived.

2.8.2 RF front-end filter

The front-end filter is a SAW filter realizing a filtering between the antenna and the transceiver. In transmission, this filter reduces the output level of harmonics at multiples of the RF frequency. In reception, more importantly, it reduces the level of out-of-band interferer reducing the probability of jamming and then improving the quality of service. This filtering is especially important because the low current consumption is obtained with linearity tradeoff in the receiver chain that may make the receiver more sensitive to strong interferers.

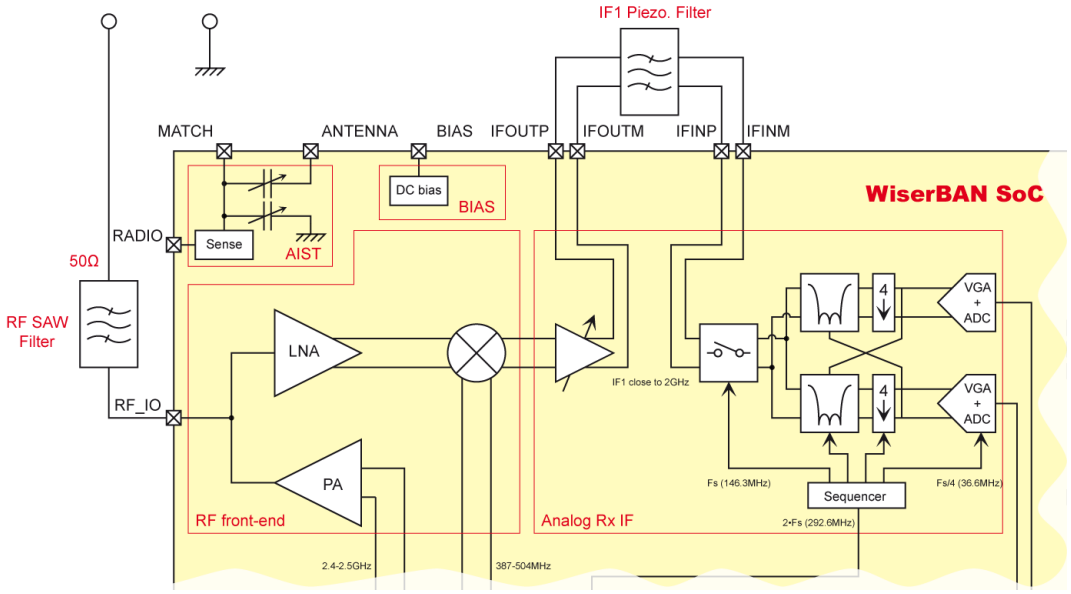


Figure 18: transceiver signal paths

Two different filters are required to cover the full range of applications. One standard filter will cover the 2.4 to 2.4835 GHz ISM band while the other one will cover the 2.483 to 2.5 GHz

2.8.2.1 2.4 – 2.4835 GHz RF Front end filter

This filter (EPCOS reference E369A) is intended to reject the out of band strong interferers especially from the 1.8 GHz and 2.5 GHz bands.

	Specifications E369A			
Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
Operating temperature range	0	-	60	°C
Center Frequency	-	2441.75	-	MHz
Passband Width	83.5	-	-	MHz
Max Insertion Loss over 83.5 MHz band @ Fc	-	2.2	2.8	dB
Relative attenuation				
880 - 960 MHz	40	43.5	-	dB
960 - 1800 MHz	34	42	-	dB
2110 - 2170 MHz	40	47	-	dB
2700 - 2800 MHz	35	39	-	dB
3600 - 5000 MHz	28	44	-	dB
Amplitude Ripple over 83.5 MHz band @ Fc	-	1.0	2.0	dB
Input V.S.W.R. over Passband	-	1.5	2.0	
Output V.S.W.R. over Passband	-	1.5	2.0	
Source Impedance (single - no external matching)	-	50	-	Ω
Load Impedance (single - no external matching)	-	50	-	Ω
Package size	DSSP 0.95 x 0.6 mm (CBT06A)			
Package height	0.2 mm + 0.085 mm (bumps)			

Pinout configuration :

Input : 1

Output : 4

To be grounded : 2, 3, 5, 6

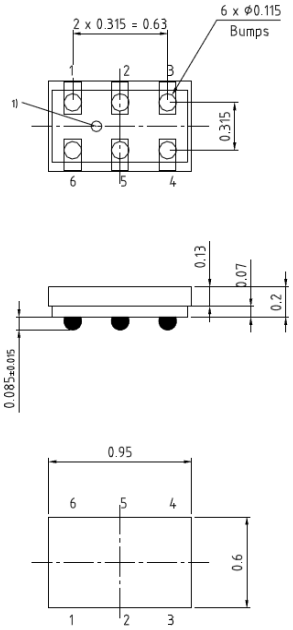


Table 10: 2.4-2.4835GHz RF Saw Filter specification

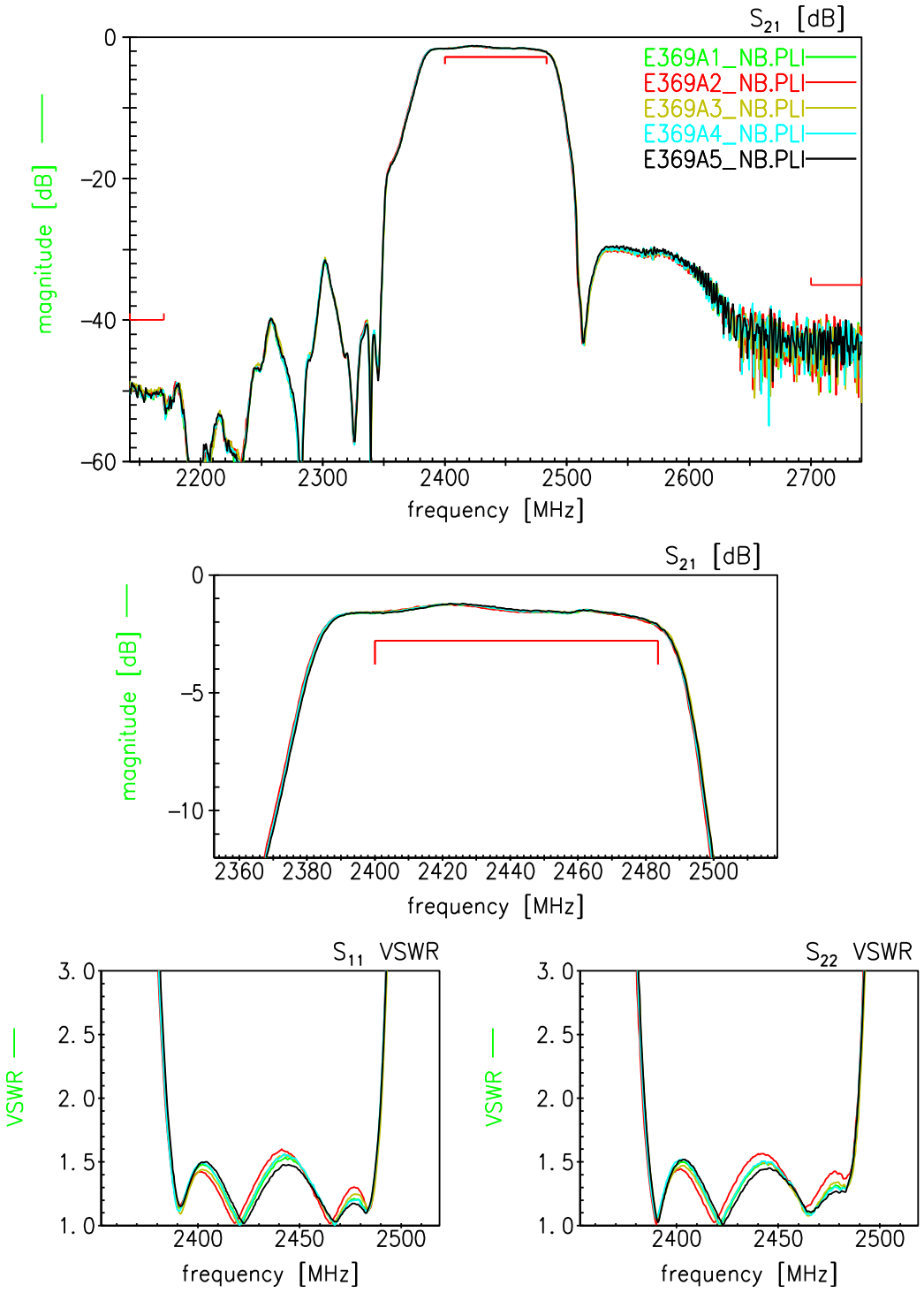


Figure 19: 2.4-2.4835GHz RF Saw Filter measurement results at 25°C

Note that the 2.4835-2.5GHz band is not covered even if the associated losses should be limited and should make the wiserband system functional over the 2.4835-2.5GHz band.

2.8.2.2 2.4835-2. 5GHz RF front-end filter

The 2.4835-2.5GHz is an alternate frequency band of operation, not considered in the project proposal. The first usage of this band is the downlink of the Globalstar satellite modile phone service. A secondary usage, presently in discussion, may be Low Power Active Medical Implant operation.

If this dedicated band is targeted, a dedicated optimized filter should be designed, i.e. rejecting as much as possible the interferers in the crowded ISM 2.4-2.4835GHz band. Such a RF front-end filter could be defined as below:

This filter is intended to reject the out of band strong interferers especially from the 1.8 GHz, 2.4 GHz and 2.5 GHz bands.

	Specifications proposal			
Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
Operating temperature range	0	-	60	°C
Center Frequency	-	2491.75	-	MHz
Passband Width	16.5	-	-	MHz
Max Insertion Loss over 16.5 MHz band @ Fc	-	2.0	2.8	dB
Relative attenuation				
880 - 960 MHz	40	-	-	dB
960 - 2110 MHz	38	-	-	dB
2110 - 2400 MHz	35	-	-	dB
2400 - 2440 MHz	27	-	-	dB
2440 - 2450 MHz	18	-	-	dB
2535 - 2545 MHz	18	-	-	dB
2545 - 2560 MHz	25	-	-	dB
2560 - 3600 MHz	35	-	-	dB
3600 - 5000 MHz	28	-	-	dB
Amplitude Ripple over 16.5 MHz band @ Fc	-	-	1.0	dB
Input V.S.W.R. over Passband	-	-	2.2	
Output V.S.W.R. over Passband	-	-	2.2	
Source Impedance (single - no external matching)	-	50	-	Ω
Load Impedance (single - no external matching)	-	50	-	Ω
Package size **Package height**	DSSP 0.95 x 0.6 mm (CBT06A) 0.2 mm + 0.085 mm (bumps)			

Table 11: 2.4835-2.5GHz RF Saw Filter specification

The pinout configuration and mechanical are the same as for E369A (c.f. preceding section 2.8.2.1).

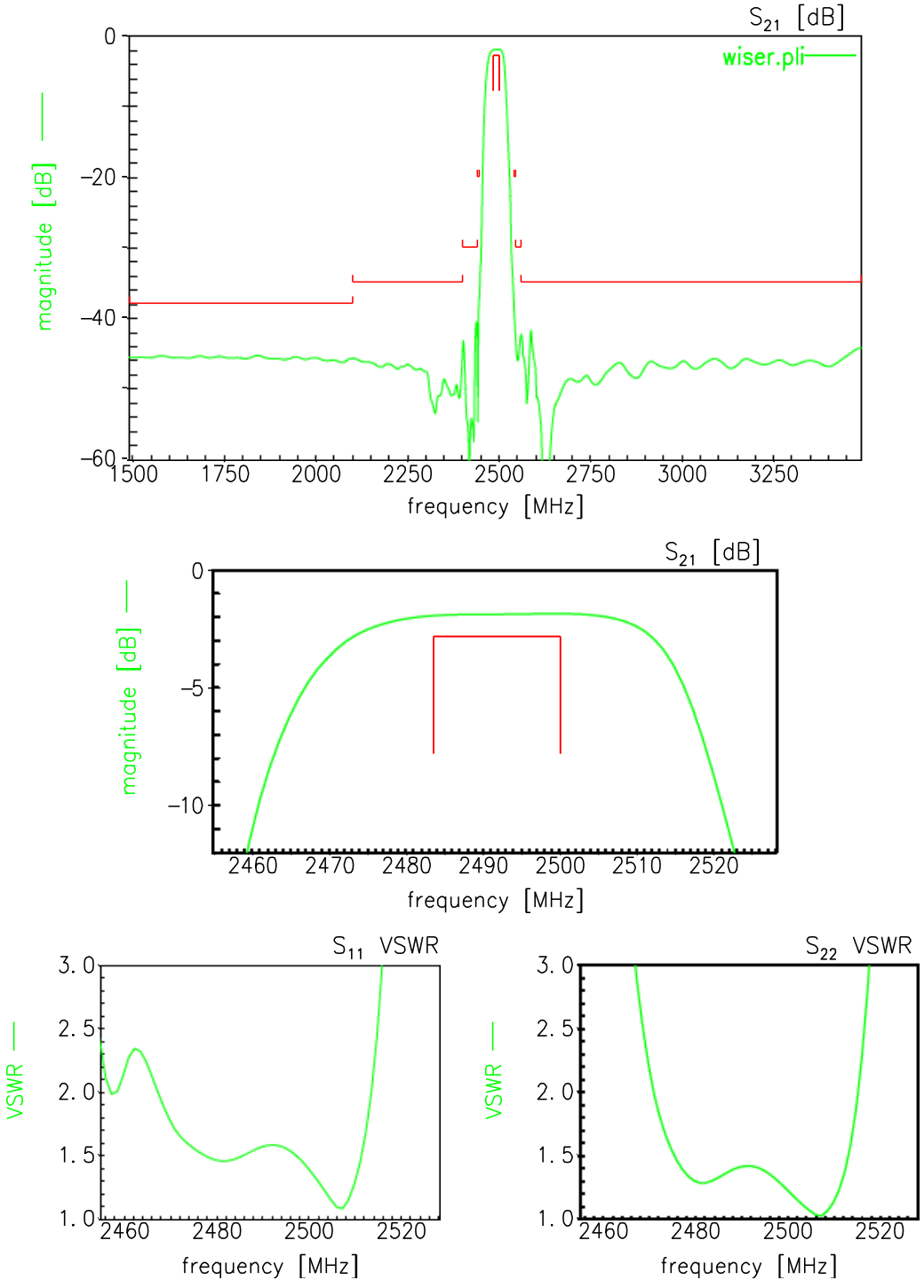


Figure 20: 2.4835-2.5GHz RF Saw Filter specification and simulated behavior

2.8.3 IF1 filter

Two IF1 filters are considered at the beginning of the project. One can consider the BAW filter as a better choice for the current consumption. But this is a risky solution because involving a less mature technology than SAW filter that can be considered as a fold-back solution. The two solutions could be reduced to one choice for the realization of the demonstrators, once the IF1-Filters are evaluated after the first test-chip silicon characterization.

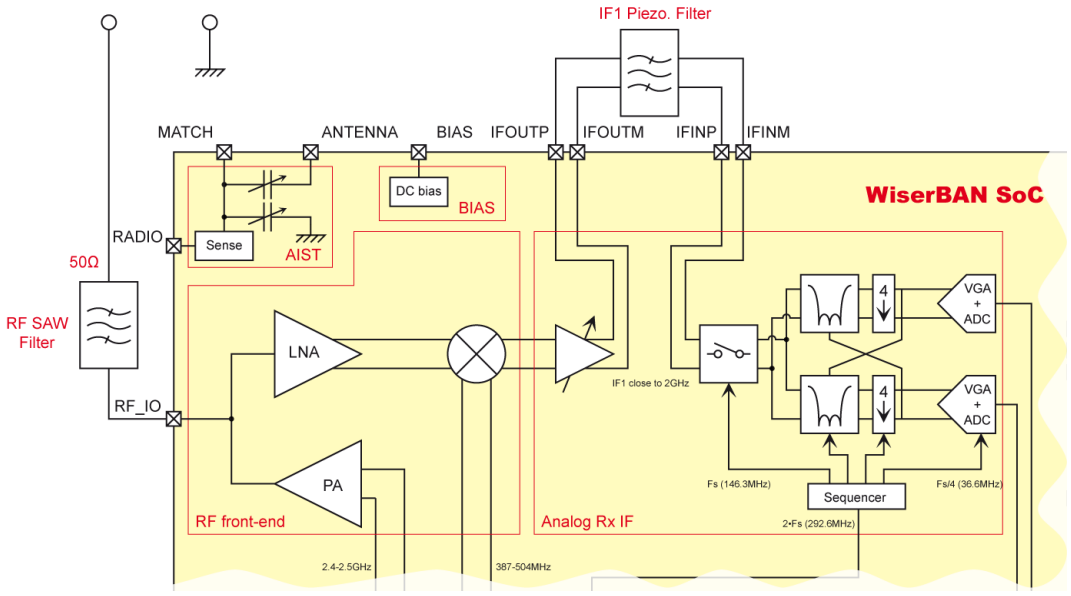


Figure 21: transceiver signal paths

2.8.3.1 BAW IF1 filter

This is a 2 GHz narrow-band filter designed together with a dedicated on-chip interface implemented in the SoC.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
BAW IF filter size					
Width		1.03	1.09	1.15	mm
Length		1.14	1.20	1.26	mm
Height	+85µm bump height			250	µm
BandWidth	Measured at 3 dB		10		MHz
Impedance			1.5		kΩ

Table 12: BAW IF1 filter specifications

The IF1 filter is an out-of-chip piezoelectric passive filter with a narrow bandwidth intended to filter out in-band interferers, especially at multiples of the sub-sampling frequency. An important characteristic of this filter is to present a high impedance above which allow slow drive current.

2.8.3.2 SAW IF1 filter

The IF1 filter (EPCOS reference E370A) is an out-of-chip piezoelectric passive filter with a narrow bandwidth intended to filter out in-band interferers, especially at multiples of the sub-sampling frequency.

	Specification E370A			
Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
Operating temperature range	**0**	**-**	**60**	**°C**
Center Frequency	**-**	**2002.29**	**-**	**MHz**
Passband Width	**5.0**	**-**	**-**	**MHz**
Max Insertion Loss over 5MHz band @ Fc	**-**	**1.8**	**3.0**	**dB**
Relative attenuation				
0.1 - 1942.5 MHz	**23**	**44**	**-**	**dB**
1942.4 - 1952.4 MHz	**30**	**40**	**-**	**dB**
1952.4 - 1966.0 MHz	**23**	**29**	**-**	**dB**
2038.0 - 2088.7 MHz	**23**	**27.5**	**-**	**dB**
2088.7 - 2098.7 MHz	**44**	**50**	**-**	**dB**
2098.5 - 5000.0 MHz	**23**	**43**	**-**	**dB**
Amplitude Ripple over 5MHz band @ Fc	**-**	**0.1**	**0.5**	**dB**
Phase Variation over 5MHz band @ Fc	**-**	**1.5**	**10**	**deg**
Group Delay Variation over 5MHz band @ Fc	**-**	**5.6**	**20**	**ns**
Input V.S.W.R. over 5MHz band @ Fc	**-**	**1.15**	**1.4**	
Output V.S.W.R. over 5MHz band @ Fc	**-**	**1.25**	**1.5**	
Source Impedance (differential)		**200**		**Ω**
Load Impedance (differential)		**200**		**Ω**
Package size	**DSSP 0.9 x 0.65 mm**			
Package height	**0.2 mm + 0.085 mm (bumps)**			

Pinout configuration :

Input : 1, 8

Output : 4, 5

To be grounded : 2, 3, 6, 7

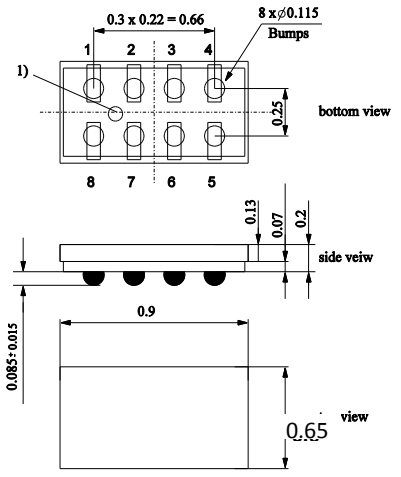


Table 13: SAW IF1 filter specifications

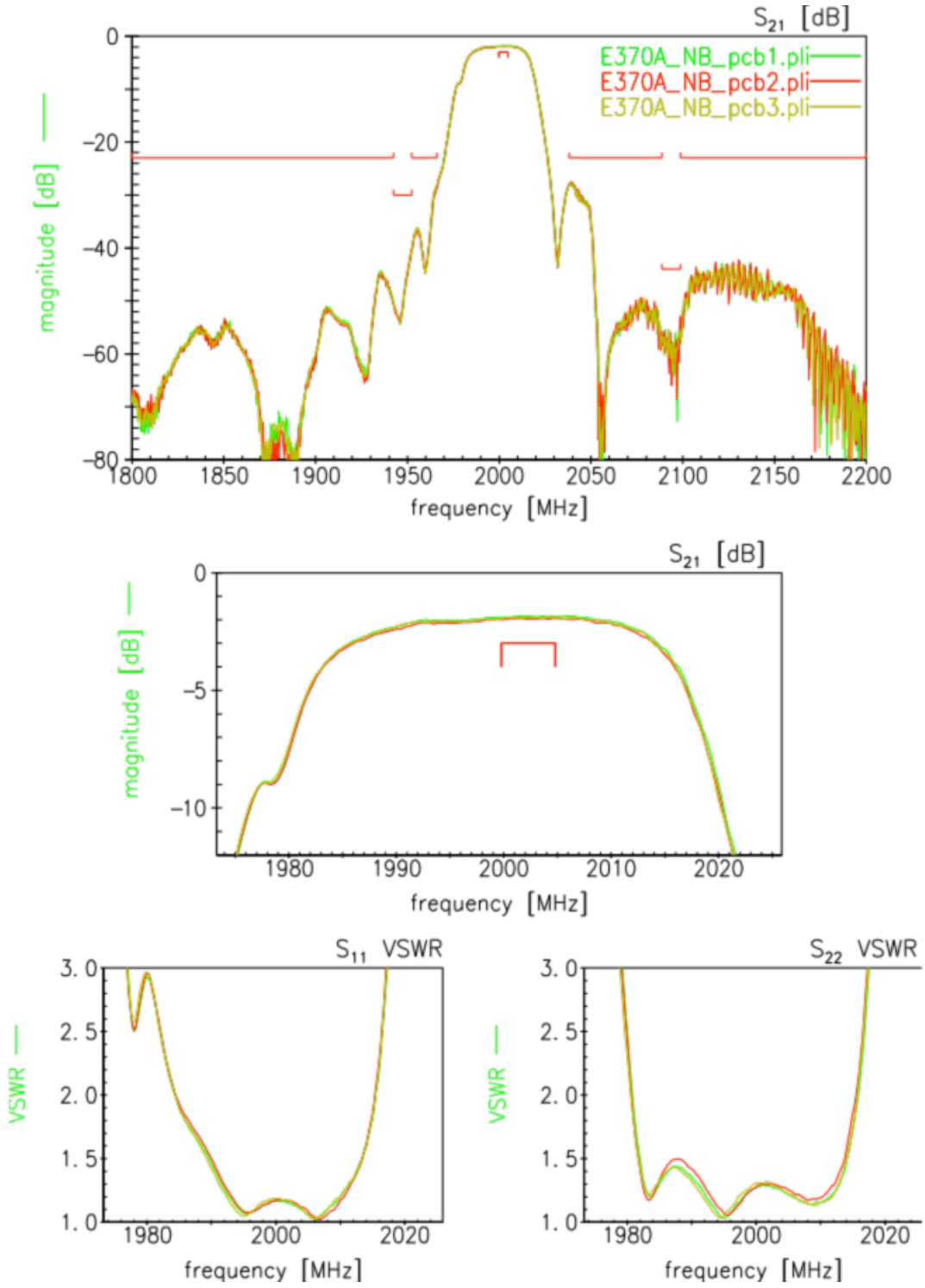


Table 14: SAW IF1 filter specificationsand measurement results at 25°C

2.8.4 BAW resonator

This BAW resonator (EPCOS reference E349C) is used, in conjunction with a dedicated on-chip oscillator, to provide a high frequency low-phase-noise reference to the transceiver. The associated relative low-current consumption and unique fast settling time is a key characteristic for the transceiver architecture and the associated low-current consumption.

Two mechanical versions are considered: the first one corresponds to its implementation in a standard (SAW filter) package whereas the second one is a Chip-Scale-packaging, optimized in size.

Parameter	Test conditions, comments	Min	Typ	Max	Unit
$(f_s+f_p)/2$	f_s, f_p series and parallel resonance		2048		MHz
Qs			1500		
Qp			1500		
k^2 (C_m/C_0)			6		%
C_0	(140Ω @ f_s)		0.5		pF
C_m			30		fF
R_m			1.1		Ω
R_0			0.4		Ω
Initial frequency				± 400	ppm
Temperature coeff. α β $\Delta T_0 = -\alpha/2\beta$				 ±0.6 -30 ±10	 ppm/°C ppb/°C^2 °C
Frequency drift over -40 to 85°C over 0 to 50°C		 -150 -40		 +3 +3	 ppm ppm
Package size Package height	First version		1400 x 1100 450		µm µm
Package size Package height	Second version		800 x 600 200 + 85 (bump)		µm µm

Table 15: BAW resonator specifications

Pinout configuration :

Inputs : 3 and 4
(any of them can be grounded)

Not connected : 1, 2, 5
(any or all of them can be grounded)

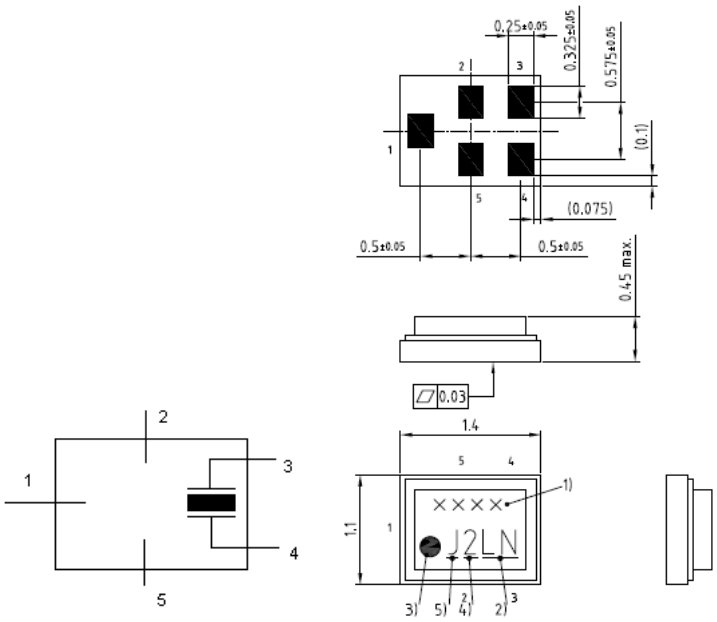


Figure 22: BAW resonator mechanical description

An important feature of this component necessary to provide a low-noise frequency reference is that it is potentially tinier than classical AT-cut quartz crystals.

2.8.5 LF resonator

This low-frequency silicon resonator is used in conjunction with an on-chip oscillator to provide an ultra-low power and precise frequency reference for long-term time scheduling (Real-Time-Clock).

Parameter	Test conditions, comments	Min	Typ	Max	Unit
$(f_s+f_p)/2$	f_s, f_p series and parallel resonance (1)	0.5		1	MHz
FoM	$Q \times k^2$		30		
C_0				2	pF
Initial frequency	Not critical (2)				ppm
Temperature coeff. α	(3)		-30		ppm/°C
Package size Package height	First version		2100 x 1230 500		µm µm
Package size Package height	Second version		660 x 660 150 + 85 (bump)		µm µm

Table 16: LF Silicon Resonator specifications

Notes:

1. A 32kiHz is flexibly formed from any resonance frequency at the given range.
2. Not critical: correction factors to be used within the oscillator IC will be determined by calibration measurements.
3. It is not desirable to have a TCF of smaller magnitude since the LF MEMS resonator has a role of a temperature sensor as well.
4. Any parasitic resonance should have FoM<2.

Both BAW resonator and LF silicon resonator have too wide production tolerances and temperature drift. But using the fact that they are uncorrelated, both frequencies can be compensated at system level using calibrations.

An important characteristic of this component necessary to provide a low frequency reference is that it is potentially tinier than classical fork quartz crystals (e.g. 32kiHz wristwatch crystal).

2.9 Radio System-on-Chip

The Radio SoC specification is the objective of deliverable D1.3. For sake of easy reading, a summary is provided in this section.

2.9.1 Overview

The radio SoC integrates the 2.45GHz radio transceiver and the controller that handles the software part of the radio communication protocol.

The precise specification is described in the "**D1.3 Final radio system architecture and specification**" document.

2.9.2 Transceiver

Typical specification are at 25°C, voltage supply=1.2V, unless otherwise noted.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Voltage supply	Core analog and digital	1.08	1.2	1.32	V
Temperature	Operating	-40	25	85	°C
RF frequency (1)		2400		2500	MHz
PeakDatarate (2)				2000	kbit/s
Modulation index (3)	2-FSK	0.3	0.5		
Channel bandwidth (4)	-3dB			2	MHz
Sensitivity	1‰ BER, for 2Mbit/s MSK		-87		dBm
Rejection Adjacent channel (5) Alternate channel (5) Intermodulation (5)	 ±5MHz for 2Mbit/s MSK ±10MHz for 2Mbit/s MSK Adjacent & alternate		 0 -30 0		 dB dB dB
Transmitted power (6)	2Mbit/s MSK		-2	0	dBm
Turnaround time	Rx to Tx or opposite		10		µs
RF&analog current Receiver (2) Transmitter (3)	 Steady state Steady state		 7.5 7.5		 mA mA
Digital current Receiver Transmitter			 200 100		 µA µA
Startup overhead (7)	Rx or Tx		0.25		µC
Leakage			50		nA
SoC dimensions		2.3 x 2.0 x 0.25			mm^3

Table 17: transceiver specifications

Notes:

1. The RF frequency range is limited by RF the front-end filter and IF1 filter frequencies for maximum performances (e.g. interferer rejection). Other frequency ranges in the vicinity, such as

2360MHz to 2400MHz for 802.15.4j or 24835MHz to 2500MHz for 802.15.6 are also possible but require different piezoelectric components.

2. The peakdatarate can be digitally tuned to integer fractions of the maximum raw datarate in order to increase the budget link. But note that the sensitivity improvement is not linear because it is also depending on the channel bandwidth. Note also that the effective datarate is affected by the protocol overhead (preamble, sync. word, address, CRC, etc).

3. Thanks to the modulation through the RF synthesizer in transmission, the modulation index is only limited by the digital settings.

4. There is no real interest to lower the channel bandwidth below this minimum because it has to handle the reference frequencies misalignment. Thanks to $\Sigma\Delta$ RF synthesis, the channel center frequencies can be freely fixed.

5. The rejections are defined as the energy of interferer over the sensitivity plus 3dB at which the BER is 1‰. For intermodulation, both adjacent and alternates are at same level and only one of them is modulated.

6. At 2.4GHz, there is a 40dB free-space path loss associated to the first 1m-communication range with 0dBi antennas. The $1/d^2$ radiated energy density adds 6|20dB free-space propagation losses every factor of 2|10 in distance.

7. This startup overhead is a very important specification because of the preferred duty cycling scheme for average current reduction: for intermittent communication, the ultra-low-power receiver has an average current consumption directly proportional to this value and to the RF channel sampling frequency. For continuous streaming of information, the average current is proportional to the average datarate only if this overhead can be neglected versus the transceiver steady-state current multiplied by the packet duration. The shorter is this packet duration, the shorter are the latency and the easier is the associated supply noise filtering. Note that to minimize this overhead, the different sub-blocks are powered on “just in time” depending on their different startup time inducing a non-constant current profile as described in the Figure 23 below:

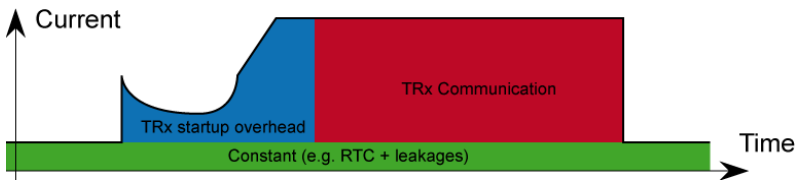


Figure 23: standby, radio start-up and active currents

2.9.3 Controller

The controller is a 32bit RISC general-purpose controller with additional DSP-oriented instruction set using two MAC engine.

Typical specification are at 25°C, voltage supply=1.2V, unless otherwise noted.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Voltage supply		1.08	1.2	1.32	V
IO voltage range (1)		1.8		3.6	V
Temperature	Operating	-40	25	85	°C
Clock frequency		0.1		32	MHz
Memory	Program + Data memory		96		kByte
SoC wakeup time					
Power-up	96kB SPI-loading at 5Mbit/s		1		s
From sleep (2)	Using GPIO based IRQ or Timer		10		µs
Active current					
CPU			50		µA/MHz
Sleep	RTC running, 25°C		12		µA
Leakages (3)					
Digital			2		µA
RAM	Typical case 25°C		9		µA
RTC current			1		µA

Table 18: transceiver specifications

Notes:

1. Depends in practice of voltage supply of components that are outside of the SoC, e.g. nvRAM used for the boot (c.f. section 2.10).

2. The sleep state is triggered by a µController instruction. The wake-up is triggered by an event (typ. a RTC IRQ). During the sleep state, the major part of the digital system is unclocked to minimize the current consumption. Of course, also to minimize the current consumption, the BAW oscillator is preferably switched off and then the only available digital clock is coming from the Silicon resonator oscillator, typically limited to 100kHz. The BAW oscillator starts up very quickly, i.e. in less than one cycle of the 100kHz clock that limits the frequency switching time: an instructionwakes up the BAW oscillator and another instruction is necessary to switch the digital frequency.

3. Without RAM and digital libraries optimized for low leakage.

2.9.4 Digital peripherals

In addition with the transceiver with its digital baseband several digital peripherals of the controller have been implemented:

- **ReQuest Controller** manages the interrupt triggered by other peripherals.
- **GPIOs** are general purpose digital Input-Output with push-pull output, selectable pull-up, input with Schmidt trigger.
- **SPI** with a dedicated NSSOUT pin for selection of nvRAM used by bootloader.
- **I2S** multiplexed on GPIO pin as secondary functionality.
- **UART** multiplexed on GPIO pins as third functionality.
- **JTAG** interface for debug and possible interface for external nvRAM.
- **4x Timers and Watchdog**, mainly to generate interrupts.
- **RTC**, mainly for Real Time counting whatever is the state of the system, e.g during sleep mode.

2.9.5 Oscillator and clocks

Oscillator and clocks
Two oscillators are integrated:

- An ultra-low-power low-frequency oscillator based on silicon resonator for time precision (c.f. chapter 2.8.5). An associated 32.768kHz derived clock is used for long-term scheduling (RTC) and tuning of the BAW resonator.
- A low-power high-frequency oscillator based on a BAW resonator (c.f. chapter 2.8.4). The derived clocks are used by the transceiver as low phase noise frequency reference and by the controller as high-frequency clock source.

Typical specification are at 25°C, voltage supply=1.2V, unless otherwise noted.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Voltage supply		1.08	1.2	1.32	V
Temperature	Operating	-40	25	85	°C
Si resonator osc.					
Frequency (1)		0.5		1	MHz
Startup time			50		ms
Startup current			0.1		µC
Active current			1		µA
Leakages			0.01		nA
BAW resonator osc.					
Frequency (2)			2048		MHz
Startup time			20		µs
Startup current			0.12		µC
Active current			500		µA
Leakages			5		nA
RTC precision (3)	32kiHz, 0°C to +70°C		±60		ppm

Table 19: oscillators specifications

Notes:

1. This frequency is divided by fractional ratio to provide a compensated 32.768kHz frequency.
2. This frequency is divided by fixed integer ratio to provide lower clock frequencies (typ. 32MHz) to the controller.
3. This Real Time Clock frequency is derived by division of Si resonator LF frequency. The division factor is programmable in order to implement a compensation scheme using both resonator frequencies and multiple temperature calibrations.

Compared to more classical frequency references based on bulkier quartz crystal, both oscillators are less accurate. We rely on a calibration scheme using the relative non-correlation of specific drifts to obtain state of the art frequency precision.

The BAW frequency reference has less temperature drift than the Silicon resonator frequency reference that have a monotonic temperature drift. The relative measurement of the low-frequency reference using the high-frequency reference provides then a temperature measurement that can be used to compensate both frequency references.

The equations **(1)** and **(2)** describes the temperature dependence with polynomial approximation:

$$f_{BAW}(t) = f_{BAW}(25°C) + \alpha_{BAW} \cdot (t - 25°C) + \beta_{BAW} \cdot (t - 25°C)^2 + \gamma_{BAW} \cdot (t - 25°C)^3 \quad \textbf{(1)}$$

$$f_{LF} = f_{LF}(25°C) + \alpha_{LF} \cdot (t - 25°C) + \beta_{LF} \cdot (t - 25°C)^2 + \gamma_{LF} \cdot (t - 25°C)^3 \quad \textbf{(2)}$$

$$\alpha_{BAW} << \alpha_{LF} \quad \textbf{(3)}$$

The Figure 24 below compares the BAW and LF frequency deviations with standard quartz crystal frequency deviations and illustrates a first-order temperature compensation of the BAW frequency:

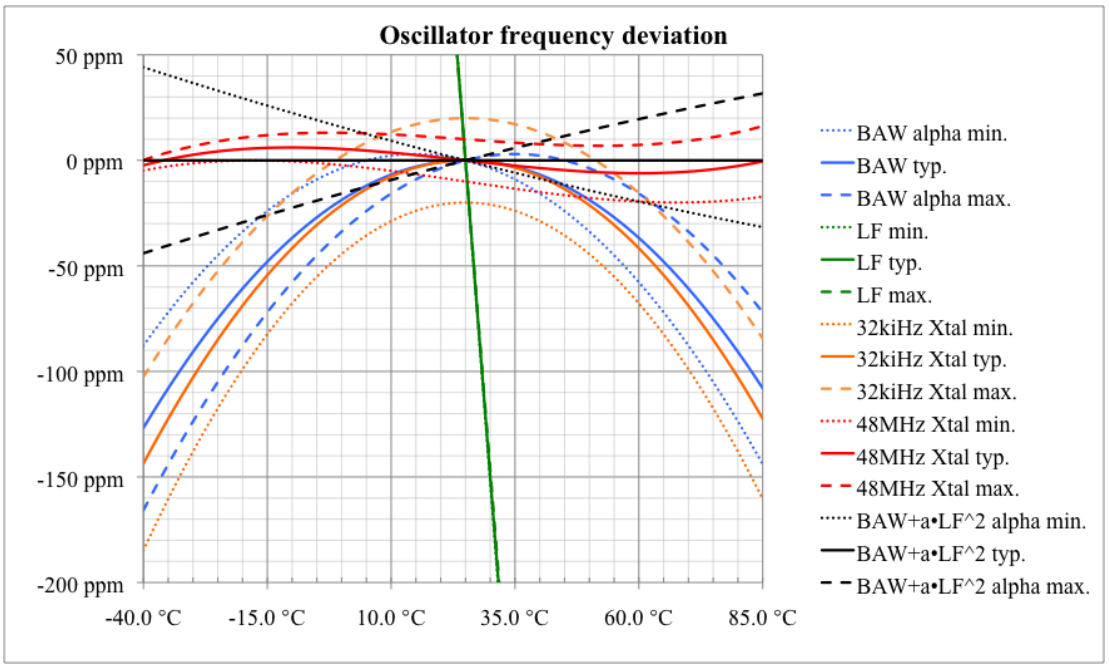


Figure 24: example of oscillator frequency temperature deviations

2.10 nvRAM

The 65nm that is used for the SoC implementation does not allow the implementation of non-volatile memory. An off-chip backup memory such as an EEPROM or Flash, with SPI interface for is then needed. It is used by the ROM-implemented boot program that loads the program after each reset. It can also be used by the embedded software to store long-term settings such as calibrations, ID's, etc.

A possible off-the-shelf component is the 1Mbit EEPROM described in the Annex 1. Using this component fixes the specifications listed in the table below:

Typical specification are at 25°C, voltage supply=2.7V, unless otherwise noted.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Supply voltage		1.8	2.7	5.5	V
Temperature		-40		85	°C
Supply current					
Write	5MHz			5	mA
Read				4.4	mA
Standby				3.3	µA
1Mbit read					
Time	5MHz		0.2		s
Current	5MHz, integrated		880		µC

Table 20: off-chip non-volatile memory specifications

The typical voltage supply has been chosen at 2.7V for maximum compatibility with large choice of memories (and possibly micro-controller): lowering this voltage will lower the dynamic current but also the maximum speed. At first order, the integrated current seems constant.

Note that the emulation of such a SPI memory, for example by a controller external to the WiserBAN System, allows to possibly suppressing this component from the platform.

2.11 Power management

2.11.1 Overview

The WiserBAN project does not cover the integration of complex power management functionalities such as adiabatic voltage conversions, dynamic voltage scaling, bulk biasing, etc. Moreover, such power management would need to be generic enough to cover all the demonstration cases.

Nevertheless, a minimum has to be implemented in the platform in order to provide a voltage supplies compatibles with the SoC specifications. The platform needs two different voltages, one to supply the SoC core around 1.2V and another over 2.7V to supply the EEPROM and the associated SoC digital IOs.

Depending on the demonstrators, the primary batteries are either Zinc-air or Lithium types. The batteries voltages should be compatible with one of the voltage needed for the platform. The other voltage needs to be elaborated by a buck or boost adiabatic voltage converter for maximum power efficiency. A buck converter is needed in the case of lithium type of primary battery to provide the 1.2V for the SoC cor. A boost is needed in the case of Zinc-air type of primary battery to provide the 2.7V for the EEPROM and associated SoC digital IOs.

Note also that if the platform environment associated to a given demonstrator can provide both voltage supplies, the DC-DC converter can be eliminated from the platform.

During MRI examinations, the SOC device will be applied a strong DC magnetic field in addition to an RF magnetic field. The DC field drives inductors cores into saturation making them ineffective. For this reason, medical implanted devices must either use inductorless DC-DC converters or provide a specific MRI operating mode in which no inductors are used during the examination. This inductorless mode can be implemented by a parallel LDO voltage regulator that may be useful anyway for reduced current consumption in standby mode. In this mode, the simple linear regulation instead of adiabatic conversion increase the current consumption reported on the battery.

2.11.2 Battery model

The battery behavior is critical, especially for tiny batteries associated with important serial resistance at end of life. A static DC model, with only one equivalent resistance is presumably not sufficient to properly model the impact of current pulses on the battery. For this reason a dynamic model, described in the Figure 25 below, is proposed.

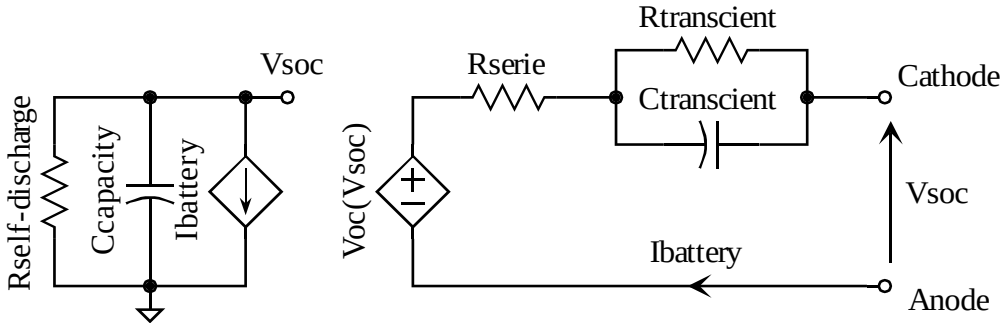


Figure 25: dynamic model of battery

Typical specification are at 25°C, unless otherwise noted.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Low-voltage battery					
V_{oc}		1.08		1.25	V
Capacity			160		mA
$R_{self\text{-}discharge}$			0.02		MΩ
R_{serie}		0.5		4	Ω
$R_{transcient}$		2		16	Ω
$C_{transcient}$		66		461	µF
High-voltage battery					
V_{oc}		2.90		3.6	V
Capacity			240		mA
$R_{self\text{-}discharge}$			10		MΩ
R_{serie}		2		16	Ω
$R_{transcient}$		8		64	Ω
$C_{transcient}$		34		240	µF

Table 21: Batteries example of specification (to be confirmed, likely by measurement)

Extended model explanation can be founded in Annex 9.

2.11.3 1.08V to 1.32V primary voltage supply case

This case allows a direct connection of the battery to the core voltage of the SoC.

The IOs (and EEPROM) supply needs to be elaborated by DC-DC voltage up-conversion.

Possible off-the-shelf components are the tiny inductive boost converters described in the Annexes 2 and 3. The feedback resistive network fixes the output voltage that can be chosen to the minimum supply voltage of the EEPROM (e.g. 2.7V). This boost converter can shutdown by the SoC's controller for minimum current consumption in standby mode.

The ripple produced by such a DC-DC voltage converter should not be a problem for the supplied digital functionalities.

The associated passive component, i.e. inductor and capacitors need to be carefully chosen according to a volume-performance tradeoff.

The platform can also benefit from an already "high-voltage" supply existing in the system carrying the platform.

2.11.4 2.7V to 3.63V primary voltage supply case

This case allows a direct connection of the battery to the IOs (and EEPROM) voltage. The core voltage needs to be provided by means of a DC-DC voltage conversion for maximum power efficiency.

Possible off-the-shelf components are the tiny inductive buck converters described in the Annexes 4 and 5.

The output ripple produced by such a DC_DC voltage converter can be a problem for the core analog functionalities, especially the RF font-end and RF frequency synthesizer: an additional voltage regulator is then required in order to supply the SoC core with a sufficiently clean voltage. Possible off-the-shelf components are the tiny Low-Dropout voltage regulators described in the Annexes 6 and 7.

The associated passive component, i.e. inductor and capacitors need to be carefully chosen according to a volume-performance tradeoff.

Note that the external inductive converters have a quiescent current that is incompatible with the current consumption required for long autonomy type of applications. Then a complete supply disconnection controlled by an external controller would be needed.

Note also that an extreme miniaturization and/or minimum standby current research would lead to avoid the DC-DC conversion and only use a simple voltage regulation. The platform can also benefit from an already "low-voltage" supply existing in the system carrying the platform (with careful attention to the associated supply noise).

2.11.5 Radio SoC voltage reference

Different on-chip functionalities might need a fixed voltage reference. To avoid the design effort, silicon area, current consumption and calibration needed by such an integrated functionality, it has been decided to use the external supply voltage as reference. Two different cases need then to be differentiated depending on what is the externally regulated voltage we can rely on as reference (c.f. preceding sections 2.11.3 and 2.11.4):

- When there is a 1.2V LDO or voltage step-down in the platform, this 1.2V voltage supply canbe used to derive an on-chip ±2% reference voltage.
- When there is a voltage step-up in the platform to supply external chips (e.g. nvRAM), the associated voltage can be used to derive an on-chip ±2‰ reference voltage.

2.11.6 Power-on-Reset and EEPROM programming

At power-on, when the supply is provided to the radio SoC, the digital states are unknown and even some glitches could appears at radio SoC IOs: it is then a priori important to maintain the platform reset active up to the point where the supply voltage is correctly established.

In fact, the platform reset is directly the radio SoC reset and is also used to access to the on-platform EEPROM (e.g. for programming) being assured that there is no concurrent access from the radio SoC.

3 Platform Software architecture

3.1 Overview

The precise specification of the software architecture is described in the "**IR4.1 Reconfigurable baseband and protocol draft architecture description**" document that is a WiserBAN internal living document that is intended to be updated along the specification process up the point it will be provided externally as "**D4.1 BAN upper layers, baseband and DSP architecture specification**".

In order to distribute the software programming but also to facilitate the reuse and secure the software design, a modular structure of the software is mandatory. The associated modules can be differentiated in:

- "Application-specific Layer" for software specific to the demonstrators.
- "Protocol Upper Layer" for hardware-independent part of the radio protocol stack.
- "Hardware Abstraction Layer" if the associated software is hardware-dependant.

A Scheduler sequences the different tasks according to their priority and a hardware-based interrupt controller allows fast event handling according also to event priority.

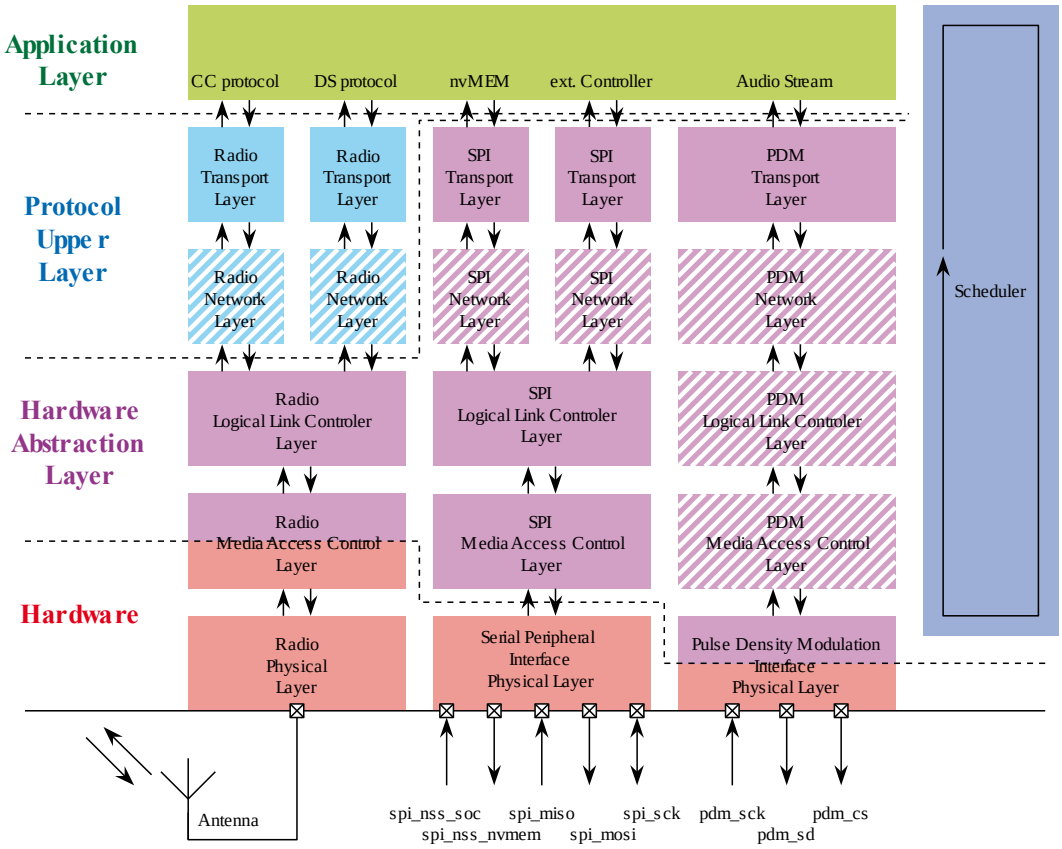


Figure 26: Software architecture

Note that we aim to follow “Programming by Contract” philosophy meaning that each piece of code should be documented with preconditions (input variable and constant type and range, needed resources, state, needed time or processor cycles for execution, etc), invariant (constants, released resources, invariant stat, etc), post-conditions (output type and range, unreleased resources, etc).

3.2 Boot

After each reset release, the on-chip memory is loaded from the external non-volatile memory (i.e. EEPROM). A ROM-based boot program realizes this RAM loading using the SPI peripheral with specific digital settings. A checksum is then calculated before running the application program in RAM.

3.3 Hardware Abstraction layer

Or specific platform drivers.

This routine ensemble aggregates all software functionalities that are specific to the hardware implementation in order to facilitate the software reuse but also to facilitate the work of “high-level” programmers by providing “standard” software interfaces. The induced modularity facilitates also the software bench and then secure the overall software.

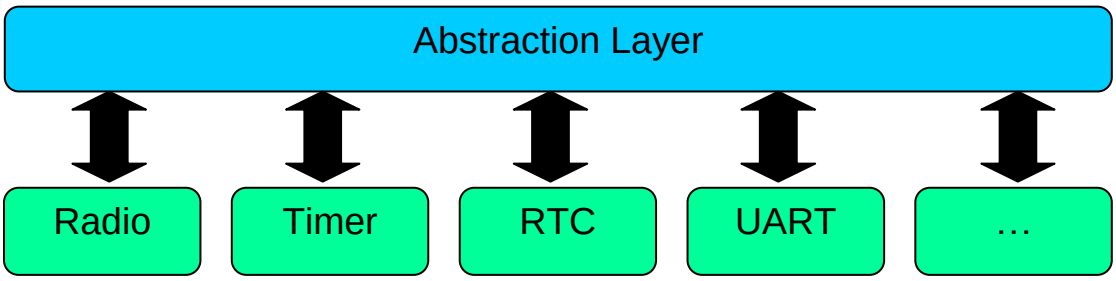


Figure 27: Abstraction Layer

3.4 Radio Protocol stack

3.4.1 Overview

The physical layer, that manages the raw datarate (i.e. air-interface datarate, equivalent to peak datarate in absence of Direct Sequence Spread Spectrum and channel coding, modulation and demodulation type, index, pulse shaping, carrier frequencies, etc), is implemented in hardware and configured and controlled by HAL routines.

The covered modulation and frame format are the standard Bluetooth Low Energy and 802.15.4-2006. An additional 2Mbit/s proprietary mode is derived from the 802.15.4-2006 by removing the spreading coding and decoding. All modes implement hardware-based CRC.

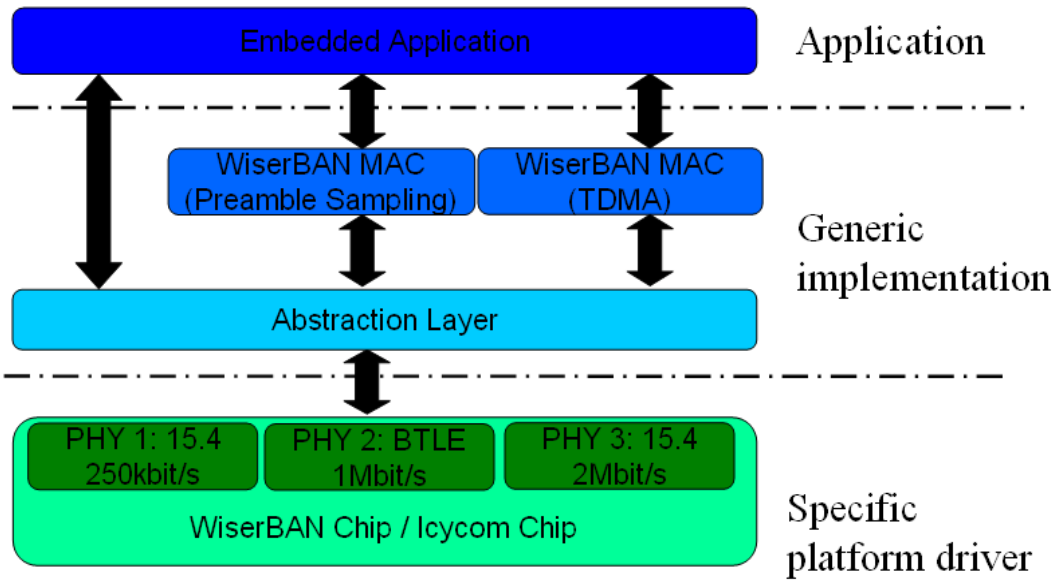


Figure 28: Software implementation architecture

3.4.2 Media Access Control layer

The Media Access Control part of the Data Link layer, that manages when and at what condition the transmitter (e.g. Listen-Before-Talk scheme) and the receiver (e.g. radio channel sampling) runs, is partly implemented in hardware, partly implemented in software using HAL routine calls for handling the hardware.

The MAC layer is responsible for:

- the association and disassociation of devices to the network (network formation)
- the maintenance of the network
- the management of the access to the radio channel

The WiserBAN network will be managed by a device, denoted as WiserBAN Coordinator. The Coordinator will be the Remote Control (RC), when it is present, and it could be substituted by whatever a device in the network, in case of absence of the RC (or simply removal of the RC from the body).

The Coordinator is in charge of:

- forming the network
- maintaining the network
- maintaining synchronization (i.e., sending SYNCH frames)
- managing the access to the channel (i.e., defining the superframe structure, allocating Time Slots (TS), etc.).

The procedure for the formation of the WiserBAN network is based on the association procedure specified in the IEEE 802.15.4/Zigbee standard.

1. Association Request → the node wishing to join the network will send to the Coordinator an *Association Request Frame*, containing the MAC address of the device.

2. Association Response → the MAC address of the device wishing to join the network is visualized on the screen of the RC. The user checks if the MAC address is correct (i.e., it is the same he/she knows) and, in this case, the Coordinator sends the *Association Response Frame*, otherwise the request is ignored. The *Association Response Frame* will contain the BAN ID and the network address selected by the Coordinator, which will be used for addressing such device in the WiserBAN network.

Once the Coordinator will receive all the association requests coming from the devices to be included in the network, it will send a broadcast packet, called *BAN Notification Frame*, informing the nodes about: the channel used by the network, the default value of the superframe duration and the list of nodes present in the network, including their network addresses and Node ID. In this way each node will know the addresses of the other nodes and could send directly data to its destination, without passing through the Coordinator.

At this point all devices and the Coordinator will enter in the **Operating mode**.

To establish and maintain the superframe, similarly to what IEEE 802.15.4 and 802.15.6 standards propose, the Coordinator periodically broadcasts a beacon packet, containing useful management information.

The period between two consecutive beacons defines a superframe (SF) structure. The SF will have an active portion and an inactive part; during the latter, nodes can go into a sleeping state, in order to reduce the power consumption. The duration of the SF (denoted hereafter as T_s) and of its active part (T_a) should be set depending on the application requirements.

Adapting 802.15.4, 802.15.6, and BATMAC SF proposals, we can identify several parts to divide the SF into :

- Beacon portion, reserved for the transmission of the beacon by the Coordinator;
- Indicators portion, where nodes have reserved mini-slots to send an acknowledgement (ACK) to the Coordinator in case the beacon has been successfully received;
- Contention Free Period (CFP), where the access is TDMA based: a certain number of time slots (TS) is allocated;
- Contention Access Period (CAP), where the access to the channel is performed according to a CSMA/CA or a Slotted ALOHA algorithm;
- Acknowledgement (ACK) Period, where mini-slots are assigned to the nodes to communicate if the transactions in the SF were successful or not;

- Inactive portion, where nodes go to the sleep state.

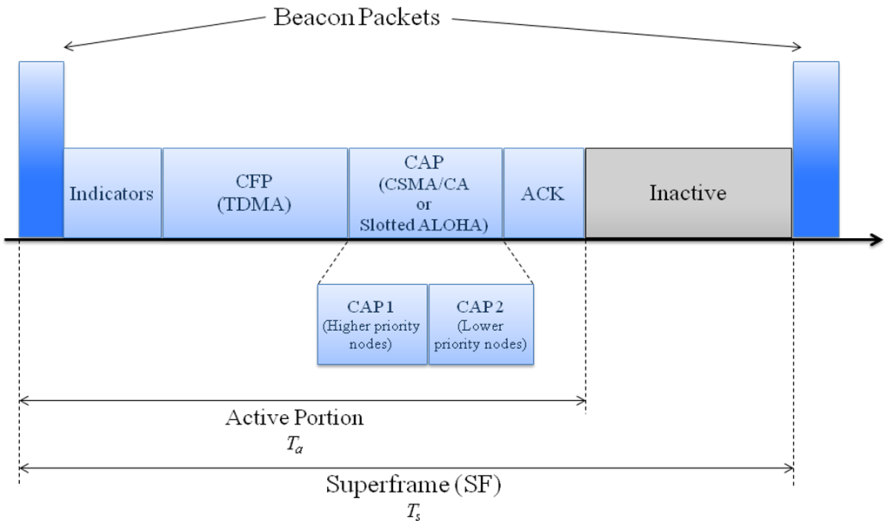


Figure 29: Structure of the proposed superframe.

The duration of the TSs in the CFP will be set such that they could contain the data packet and, in case an ACK is requested, the turn-around-time and the ACK packet.

The CAP should come after the CFP (and not before it as it is specified in 802.15.4) for several reasons, such as:

- If an emergency packet failed in the CFP, it potentially could be retransmitted in the CAP;
- The CFP should directly follow the indicator period in order to consider the channel coherent.

The CAP should always be present in a SF, at least to handle slot requests. If no other traffic needs to be managed in it, the duration of the CAP will be set to its minimum.

When the Remote Control is in the range of the other network devices it will always act as WiserBAN Coordinator. When, instead, it is out of the range (i.e., it cannot reach the devices), whatever a node in the network will take the role of Coordinator. In particular, such a node will be the first node having a packet to be transmitted after the disconnection of the RC.

A device wishing to send data to another device will send a burst of preambles addressing both, the Coordinator and the destination device. If no ACK from the Coordinator is received, the source node sends another burst of preambles to be sure the Coordinator is no longer connected to the network. In such case the device will start sending beacons and forming the superframe according to its new role of Coordinator. On the other hand, the RC will continue sending synchronization frames, without receiving any data from the network: if the RC does not receive data from whatever a node in the network for a given interval of time (timeout to be set properly), it will stop sending synchronization packets and it will sense the channel periodically to understand if there are packets on the channel. In case the RC returns in the range of the network and it will receive some packets from the network

nodes, it will transmit a *Coordinator Request Frame* to the network devices, to take again the role of Coordinator.

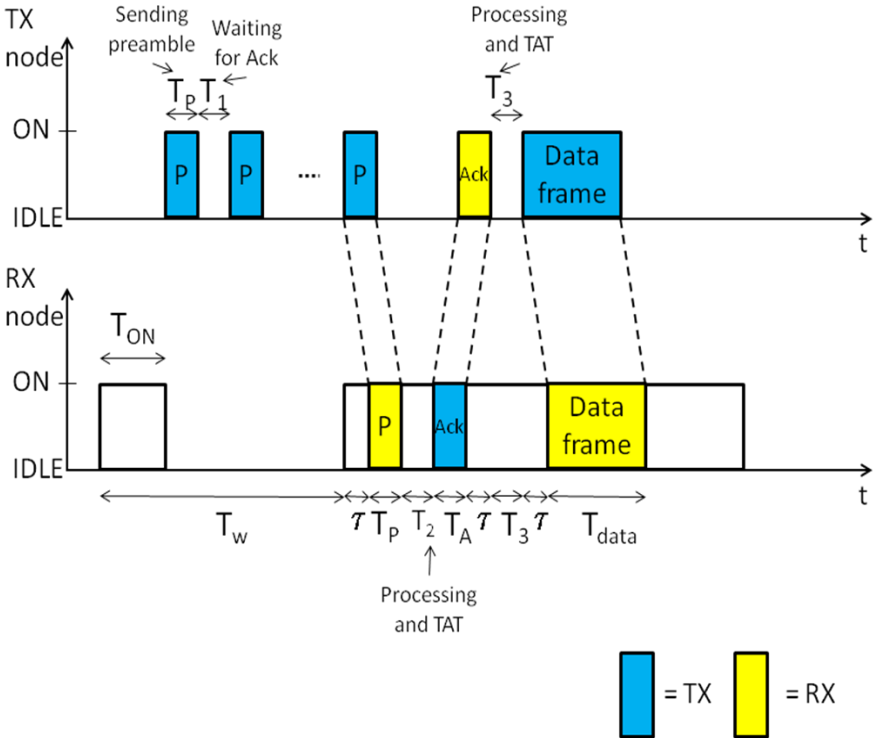


Figure 30: Wake up mechanism in case of direct transmission of the data.

3.4.3 Logical Link Control layer

The Logical Link Control part of the Data Link layer, that manages the frame (i.e. synchronization, error checking, acknowledgement, etc), is partly implemented in software, partly implemented in software in HAL routine.

Half-duplex asked.

The Logical Link Control (LLC) sublayer provides an interface between upper sublayers (e.g. Application layer) and the MAC data communication protocol sublayer. The LLC provides flow control of data to MAC sublayer, Buffer management mechanisms, Quality of service and Traffic (Bandwidth) such as permanent traffic set up when the connection is established or switched traffic Set up and released on demand via a procedure.

A connection (an LLC flow) must be established before any packets are sent. Each flow category is defined by associated traffic, priority and QoS parameters. Each Flow has its own packet queue and its associated priority. This scheme permits to a higher flow priority to used bandwidth to a lower flow priority (e.g. emergency data used bandwidth to monitoring data).

Several profiles should be defined with the following parameters:

- Priority Level

- Type of Flows
- Devices Address
- Packet rate
- Acknowledgement policy
- Transmission and retransmission policy i.e. the selected periods for transmission and retransmission, the number of retransmission allowed,
- Loss Rate acceptable
- Time to Live i.e. time before discarding the data

4 Radio Communication

4.1 Communication range

4.1.1 Overview

The communication distance is a critical specification that depends on the transceiver link budget, the antenna gain (or loss) as well as propagation losses:

- The transceiver budget link depends on output power and sensitivity but this sensitivity depends also on datarate. A good approximation fixes the transceiver budget link (as well as the consumed power per transmitted bit) inversely proportional to the datarate. This is then a convenient way to increase an insufficient communication range at the cost of increased power consumption.
- The antenna gain (and associated losses) depends a lot on chosen antenna that tends strongly to depend on its associated volume. An important point is also the sensitivity of this antenna gain related to close environment variation. Frequency agility and/or resonance frequency tuning may then help a lot to stabilize the antenna performances.
- The propagation losses are certainly the more variable point that impacts the communication range.

The equation **(4)** below calculates the margin in dB that need to be positive:

$$Margin = \underbrace{Pout - Sensitivity}_{Transceiver\ \ Budget\ \ Link} + G_{Tx\ \ Antenna} - A_{Propagation\ \ Losses} + G_{Rx\ \ Antenna} \qquad \textbf{(4)}$$

An order of magnitude could be 90dB for the transceiver 2Mbit/s budget link, -10dBi for both antennas and 60dB for propagation losses.

An exact transceiver budget link is specified in the chapter 2.9.2. Antennas gains (and associated losses) are specified in the chapter2.7. Demonstrator-specific propagation studies are summarized in following chapter 2.1.

The precise studies of the different propagation losses associated to demonstrator cases are described in the "**D3.1 Final report on the antenna-human body interactions, around-the-body propagation**" document.

4.2 Communication latencies versus current tradeoff

4.2.1 Control-commands communication principle

The approach described in this chapter is only a principle description to explain the current-latency tradeoff for control-command type of communications. Different other protocol principles could be used (e.g. TDMA) but other scheme should induce similar tradeoffs.

We assume a double constraint on receiver node side: its current consumption needs to be minimized while guaranteeing a given maximum reaction time.

For intermittent type of control-commands communication, the average receiver current consumption is fixed by the receiver startup overhead multiplied by the receiver RF channel sampling frequency as illustrated in the Rx current profile of Figure 31 below and described in the equation (5) below:

$$\underbrace{\bar{I}_{RxCC}}_{mA} = \frac{\overbrace{C_{TRxOverhead}}^{mC}}{\underbrace{T_{RxCC}}_{ms}} \qquad (5)$$

Order of magnitude could be 0.25µC for transceiver startup overhead. 50ms of RF channel sampling period induces an average receiver current of 5µA.

For such a scheme, the transmitter needs to repeat its packet to transmit in order to cover the associated receiver RF channel sampling period to assure that the receiver will catch its transmission. The scheme is illustrated in the Figure 31 below:

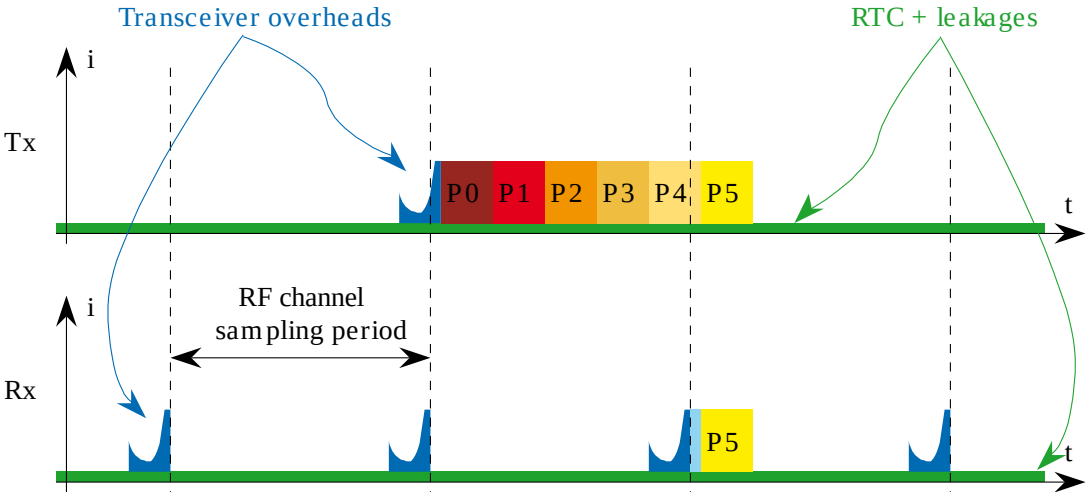


Figure 31: Rx and Tx current profiles during control-command communication

The average transmitter current consumption is then fixed by the transceiver startup overhead increased by the RF channel sampling period and two times the length of the control-command packet to as described in the equation (6) below:

$$\underbrace{\bar{I}_{TxCC}}_{mA} = \left[\overbrace{C_{TRxOverhead}}^{mC} + \underbrace{\hat{I}_{TxCC}}_{mA} \times \underbrace{T_{RxCC}}_{ms} + 2 \times \frac{\overbrace{L_{packet\,DS}}^{bit}}{\underbrace{\hat{D}_{CC}}_{kbit/s}} \right] \times \frac{1}{\underbrace{T_{TxCC}}_{ms}} \quad (6)$$

Order of magnitude could be 0.25µC for transceiver startup overhead and 9.5mA peak transmitter current and 50ms of receiver RF channel sampling and packet of 1kbit transmitted at 2Mbit/s. 10 control-commands per hour in average induces an average transmitter current of 1.35µA.

The receiver RF channel sampling period fixes the minimum guaranteed latency associated to the control communication. There is then a tunable tradeoff between latency (and transmitter current consumption) and receiver current consumption as described in the equation (7) below.

$$\left. \begin{array}{l} \underbrace{\hat{T}_{Latency\,CC}}_{ms} = \underbrace{T_{RxCC}}_{ms} + 2 \times \frac{\overbrace{L_{packet\,CC}}^{bit}}{\underbrace{\hat{D}_{CC}}_{kbit/s}} \\ \underbrace{\bar{I}_{TRxCC}}_{} = \frac{\overbrace{C_{TRxOverhead}}^{mC}}{T_{--}} \end{array} \right\} \Rightarrow \hat{T}_{Latency\,CC} = 2 \times \underbrace{\frac{L_{packet\,CC}}{\hat{D}_{CC}}}_{PacketDuration} + \frac{C_{TRxOverhead}}{\bar{I}_{TRxCC}} \quad (7)$$

Order of magnitude could be 0.25µC for overhead, 5µA for average Rx current. For 1kbit packet length and 2Mbit/s peak datarate, the resulting latency is 50.5ms.

This tradeoff depends in practice very little on the peak datarate.

4.2.2 Data-streaming type of communication principle

The approach described in this chapter is only a principle description to explain the current-latency tradeoff for data-streaming type of communication. Different other protocol principles could be used (e.g. together with FHSS) but the tradeoff should remain similar.

We assume a similar constraint on both side of the communication link for the current consumption minimization.

For data-streaming type of communication, once fixed the maximum datarate depending on the needed transceiver budget link, the transceiver average current depends mainly on the needed average datarate, if the transceiver startup overhead can be neglected as illustrated in the Figure 32 below and described in the equation (8) below:

$$\underbrace{\bar{I}_{TRxDS}}_{mA} = \left(\underbrace{C_{TRxOverhead}}_{mC} + \underbrace{\hat{I}_{TRxDS}}_{mA} \times \frac{\overbrace{L_{packetDS}}^{bit}}{\underbrace{\hat{D}_{DS}}_{kbit/s}} \right) \times \frac{1}{\underbrace{T_{TRxDS}}_{ms}} \quad (8)$$

$$= \underbrace{\frac{C_{TRxOverhead}}{T_{RxDS}}}_{OverheadCurrent} + \underbrace{\frac{\hat{I}_{TRxDS}}{\hat{D}_{DS}}}_{IntegratedCurrentPerBit} \times \underbrace{\frac{L_{packetDS}}{T_{TRxDS}}}_{\bar{D}_{DS}}$$

Order of magnitude could be 0.25µC for transceiver startup overhead and 5ms for packet period and 9.5mA for peak current and 2Mbit/s for peak datarate. 200kbit/s (i.e. 1kbit packet length) induce an average current consumption of 1mA.

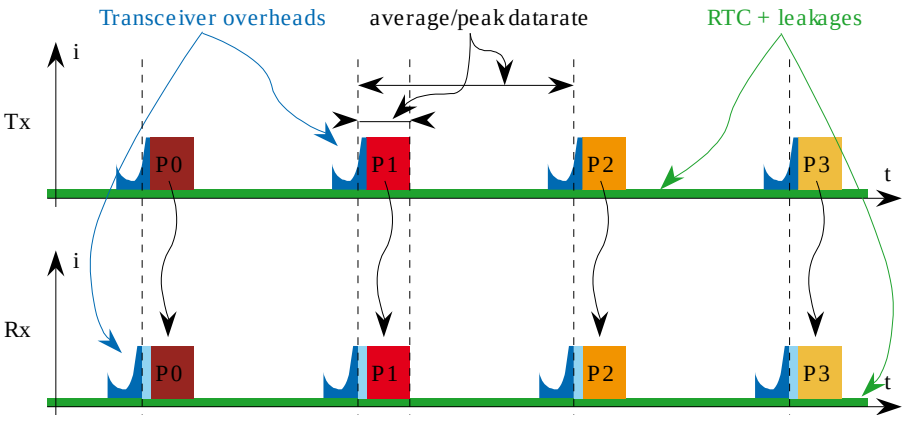


Figure 32: Rx and Tx current profiles during data-streaming communication

The overall overhead impact is inversely proportional with the packet length that fixes also the protocol-induced latency. There is then a tradeoff between current consumption and protocol-induced latency as described in the equation (9) below:

$$\left.\begin{array}{l} \underbrace{\overline{D}_{DS}}_{kbit/s} = \frac{\overbrace{L_{packet\,DS}}^{bit}}{\underbrace{T_{TRx\,DS}}_{ms}} \\ \underbrace{T_{Latency\,DS}}_{ms} = T_{TRx\,DS} + \frac{L_{packet\,DS}}{\underbrace{\hat{D}_{DS}}_{kbit/s}} \\ \underbrace{\overline{I}_{TRx\,DS}}_{mA} = \frac{\overbrace{C_{TRxOverhead}}^{mC}}{T_{TRx\,DS}} + \underbrace{\hat{I}_{TRx\,DS}}_{mA} \times \frac{L_{packet\,DS}}{T_{TRx\,DS} \times \hat{D}_{DS}} \end{array}\right\} \Rightarrow \hat{T}_{Latency\,DS} = \underbrace{\frac{L_{packet\,DS}}{\hat{D}_{DS}}}_{PacketDuration} + \underbrace{\frac{1}{\overline{I}_{TRx\,DS}} \times \underbrace{\left(C_{TRxOverhead} + \hat{I}_{TRx\,DS} \times \frac{L_{packet\,DS}}{\hat{D}_{DS}} \right)}_{PacketIntegratedCurrent}}_{T_{TRx\,DS}} \quad (9)$$

Order of magnitude could be 0.25µC for overhead, 1mA for average Rx current, 9.5mA for peak TRx current. For 1kbit packet length and 2Mbit/s peak datarate, the resulting latency is 5.5ms with 5ms for transceiver activity period, i.e. 200kbit/s average datarate.

A more important overhead than the transceiver startup overhead may come from packet overhead, i.e. needed preamble, node address, CRC, etc. Order of magnitude could be 24bit for the preamble and packet Start-of-Frame, 16bit for the address and 16bit for CRC. The additional associated overhead at 2Mbit/s and 9.5mA peak current is 0.266µC, i.e. same order of magnitude as the transceiver startup overhead.

Note also that the overhead coming from software processing of packets is not taken into account because considered negligible.

Depending on streamed data, another source-coding latency is in practice much more important: on the transmitter side, this is by principle the delay to acquire the raw signal to compress. And the more raw signal is acquired, the more efficient tends to be the compression by the use of auto-correlation extraction (e.g. typ. 20ms for max. speech compression). On receiver side, this is the same thing by principle (so this double the delay). Of course, the more efficient is the compression, the lower average datarate is needed and, proportionally, the lower is the average current on both side of the communication. There is then a tradeoff between current consumption and source-coding induced latency.

This tradeoff can also be impacted by the needed processing power and associated current consumption: the more efficient is the compression algorithm, the more processing power it tends to require. A priori, there is then an optimum algorithm that can be found by constrained optimization but the choice of it may need in practice a lot of trial-and-errors. Note that this is further complicated by the fact that the source-coding algorithm may be strongly asymmetrical (compression-decompression) in term of needed processing power. We can also be limited by the maximum processing power available.

4.2.3 Other important aspects

4.2.3.1 Timing precision

For simplicity of explanation, the above description of communication principles assumes no possible synchronization at long-term (e.g. for control-command communication described principle) and perfect synchronization at short-term (e.g. for data-streaming communication described principle). On one hand, possible synchronization may help to save energy by avoiding transmitting or receiving when not necessary. The energy saving is in practice related to the precision of the long-term time reference (i.e. frequency and jitter). On the other hand, even at short-term, the synchronization cannot be perfect and a time margin needs to be added that can be interpreted as a timing overhead (e.g. in blue on the Figure 31 and Figure 32). This overhead is also related to the precision of the short-term time reference (i.e. frequency and jitter linked to phase noise).

4.2.3.2 Network asymmetry

If particular nodes of the network can consume more energy than the common implanted or wearable nodes, e.g. a base station or a central data sink node with more important or rechargeable battery, some asymmetry can be implemented in the protocol to dissymmetry also the energy consumption in order to maximize the autonomy, especially for control-command type of communication.

4.2.3.3 Standby modes

In addition to the active communication-induced current consumption, several other consumptions such as the consumption related to the time reference, the dynamic consumption of the controller or the leakages need to be taken into account for the autonomy calculations. Overall current minimization may then imply to define several standby modes depending on re-startup time and associated energy.

In general, the less current the mode consumes, the more time it needs to get back into normal active mode when all functionalities can be used.

An example of functional modes is given in the table below:

Modes	Test conditions, comments	Min.	Typ.	Max	Unit
Normal					
Current	Duty-cycled communication		1	10	mA
Sleep	Triggered by sleep instruction				
Current (1)	RTC running, 25°C		12		µA
Sleep to Normal	After timer IRQ,		1		cycle
Normal to sleep	After “sleep” instruction		1		cycle
Off					
Current (1)	Drawn from1.2V supply		12		µA
Off to Normal (2)	64kByte loading from EEPROM		0.5		s
Normal to Off	1kByte load to EEPROM		8		ms

Table 22: Modes specifications

1. This current does not take into account possible quiescent or leakage current induced by off-chip components, especially the DC-DC buck converter if needed.

2. This Off to normal transition that needs a RAM reloading from off-chip EEPROM does not only take time but current (c.f. chapter 2.10).

List of Tables

List of Figures

Glossary

FMEA **F**ailure **M**ode &**E**ffect **A**nalysis

BAW **B**ulk **A**coustic **W**ave

SAW **S**urface **A**coustic **W**ave

RTC **R**eal **T**ime **C**lock

HAL **H**ardware **A**bstraction **L**ayer

List of reference documents

[1] D1.1 Report about WiserBAN platform applications

[2] D1.2 Final platform specification and architecture

[3] IR1.1 (M4) Target platform specification and architecture

[4] System-in-Package Specification

[5] IR1.3 Target radio System-on-Chip architecture and specifications

[6] IR4.1 Reconfigurable baseband and protocol draft architecture description

[7] Antenna Specification

[8] Piezo Components Specification

[9] IR5.1 3D SiP platform architecture proposal

[10] IR3.2 Intermediate report on smart antenna-to-radio interface for the active tunable antenna

[11] IM2.2 Internal Milestone: RF, IF MEMS Target specifications

[12] IM2.3 Internal Milestone: LF MEMS and oscillator target specifications

[13] IR1.2 Target radio Platform architecture and specifications

[14] IR4.1 Reconfigurable baseband and protocol draft architecture description

[15] D4.1 BAN upper layers, baseband and DSP architecture specification

[16] IR3.1 Intermediate report on the antenna-human body interaction, around-the-body propagation

[17] IR1.1 (M4) Target platform specification and architecture

[18] "Accurate Electrical Battery Model Capable of Predicting Runtime and I–V Performance", Min Chen and Gabriel A. Rincón-Mora, IEEE transactions on energy conversion, vol. 21, no. 2, june 2006

Annexes 1: EEPROM

M95M01-R
M95M01-W

1 Mbit serial SPI bus EEPROM
with high speed clock

Features

- Compatible with SPI bus serial interface (Positive Clock SPI modes)
- Schmitt trigger inputs for enhanced noise margin
- Single supply voltage: 1.8 V to 5.5 V
- High speed
  - 5 MHz clock rate
  - 5 ms Write time
- Status Register
- Hardware Protection of the Status Register
- Byte and Page Write (up to 256 bytes)
- Self-timed programming cycle
- Adjustable size read-only EEPROM area
- Enhanced ESD Protection
- More than 1 000 000 Write cycles
- More than 40-year data retention
- Packages
  - ECOPACK® (RoHS compliant)

SO8N (MN)
150 mils width

SO8W (MW)
208 mils width

WLCSP (CS)

July 2009 Doc ID 13264 Rev 7 1/41

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Annexes 2: Boost DC-DC converter

LINEAR TECHNOLOGY

LTC3526L-2/LTC3526LB-2

550mA 2MHz Synchronous Step-Up DC/DC Converters in 2mm × 2mm DFN

FEATURES

- **Delivers 3.3V at 100mA from a Single Alkaline/ NiMH Cell or 3.3V at 200mA from Two Cells**
- **V_{IN} Start-Up Voltage: 680mV**
- **1.5V to 5.25V V_{OUT} Range**
- **Up to 94% Efficiency**
- **Output Disconnect**
- **2MHz Fixed Frequency Operation**
- **$V_{IN} > V_{OUT}$ Operation**
- **Integrated Soft-Start**
- Current Mode Control with Internal Compensation
- Burst Mode® Operation with 9µA I_Q (LTC3526L-2)
- Low Noise PWM Operation (LTC3526LB-2)
- Internal Synchronous Rectifier
- Logic Controlled Shutdown (I_Q < 1µA)
- Anti-Ring Control
- Low Profile (2mm × 2mm × 0.75mm) 6-Lead DFN Package

APPLICATIONS

- Medical Instruments
- Noise Canceling Headphones
- Wireless Mice
- Bluetooth Headsets

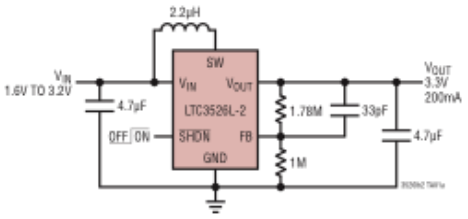
DESCRIPTION

The LTC®3526L-2/LTC3526LB-2 are synchronous, fixed frequency step-up DC/DC converters with output disconnect. Synchronous rectification enables high efficiency in the low profile 2mm × 2mm DFN package. Battery life in single AA/AAA powered products is extended further with a 680mV start-up voltage and operation down to 500mV once started.

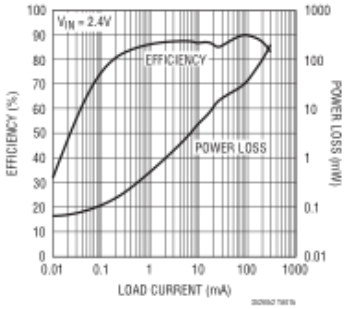
A switching frequency of 2MHz minimizes solution footprint by allowing the use of tiny, low profile inductors and ceramic capacitors. The current mode PWM design is internally compensated, reducing external parts count. The LTC3526L-2 features Burst Mode operation at light load conditions allowing it to maintain high efficiency over a wide range of load. The LTC3526LB-2 features fixed frequency operation for low noise applications. Anti-ring circuitry reduces EMI by damping the inductor in discontinuous mode. Additional features include a low shutdown current of under 1µA and thermal shutdown.

The LTC3526L-2/LTC3526LB-2 are housed in a 2mm × 2mm × 0.75mm DFN package.

TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current



3526l2f

LINEAR TECHNOLOGY

1

Annexes 3: Boost DC-DC converter

SEMTECH

SC122

Low Voltage Synchronous Boost Converter

POWER MANAGEMENT

Features

- Input voltage — 0.7V to 1.6V
- Minimum start-up voltage — 0.85V
- Output voltage fixed at 3.3V
- Peak input current limit — 350mA typically
- Output current 95mA at V_{IN} = 1.6V, 50mA at V_{IN} = 0.9V
- Efficiency up to 80%
- Internal synchronous rectifier
- Switching frequency — 1.2MHz
- Power save (voltage hysteretic) control
- Anti-ringing circuit
- Operating supply current (measured at OUT) — 40µA
- No forward conduction path during shutdown
- MLPD-UT-6 1.5 × 2.0 × 0.6 (mm) package
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- Electric toothbrushes
- Personal medical products
- Single-cell alkaline, NiCd, or NiMH applications

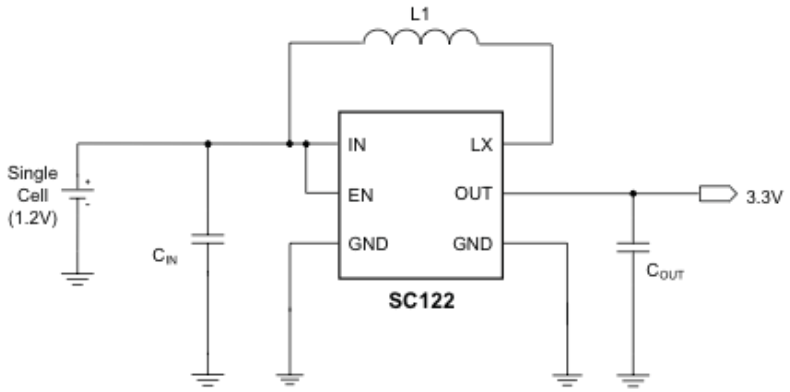
Description

The SC122 is a high efficiency, low noise, synchronous step-up DC-DC converter. It produces a fixed 3.3V output from a single cell alkaline or NiMH battery. It features an internal 1.2A switch and synchronous rectifier to achieve high efficiency and to eliminate the need for an external Schottky diode.

The SC122 operates exclusively in voltage-hysteretic power save mode (PSAVE) for high efficiency under light load conditions. It features anti-ringing circuitry for reduced EMI in noise sensitive applications. While disabled, the output remains in a high impedance state to preserve the charge on the output capacitor. This permits ultra-low idle quiescent currents in applications in which the SC122 can be periodically enabled by an external controller to recharge the output capacitor.

Low quiescent current is obtained despite a high 1.2MHz operating frequency. Small external components and the space saving MLPD-UT-6, 1.5×2.0×0.6 (mm) package, make this device an excellent choice for small handheld applications that require the longest possible battery life.

Typical Application Circuit



This project is funded by the European Commission under the 7th Research Framework Programme.

Annexes 4: Buck DC-DC converter

National Semiconductor

October 28, 2008

LM3677
3MHz, 600mA Miniature Step-Down DC-DC Converter for Ultra Low Voltage Circuits

General Description

The LM3677 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Li-Ion cell battery and input voltage rails from 2.7V to 5.5V. It provides up to 600 mA load current over the entire input voltage range. The LM3677 is configured to different fixed voltage output options as well as an adjustable output voltage version range from 1.2V to 3.3V.

The device offers superior features and performance for mobile phones and similar portable applications with complex power management systems. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system control. During PWM mode operation, the device operates at a fixed frequency of 3 MHz (typ). PWM mode drives loads from ~ 80 mA to 600 mA max. Hysteretic PFM mode extends the battery life by reducing the quiescent current to 16 µA (typ.) during light load and standby operation. Internal synchronous rectification provides high efficiency. In shutdown mode (Enable pin pulled down), the device turns off and reduces battery consumption to 0.01 µA (typ.).

The LM3677 is available in a lead-free (NOPB) 5-bump micro SMD package and 6-pin LLP package. A switching frequency of 3 MHz (typ.) allows use of tiny surface-mount components. Only three external surface-mount components, an inductor and two ceramic capacitors, are required.

Features

- 16 µA typical quiescent current
- 600 mA maximum load capability
- 3 MHz PWM fixed switching frequency (typ.)
- Automatic PFM/PWM mode switching
- Available in 5-bump micro SMD package and 6-pin LLP package
- Internal synchronous rectification for high efficiency
- Internal soft start
- 0.01 µA typical shutdown current
- Operates from a single Li-Ion cell battery
- Only three tiny surface-mount external components required (solution size less than 20 mm²)
- Current overload and thermal shutdown protection

Applications

- Mobile Phones
- PDAs
- MP3 Players
- W-LAN
- Portable Instruments
- Digital Still Cameras
- Portable Hard Disk Drives

Typical Application Circuits

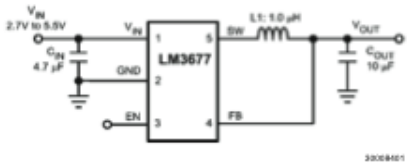


FIGURE 1. Typical Application Circuit

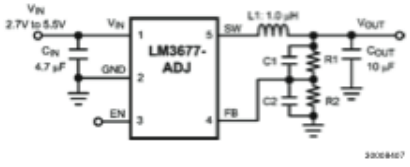
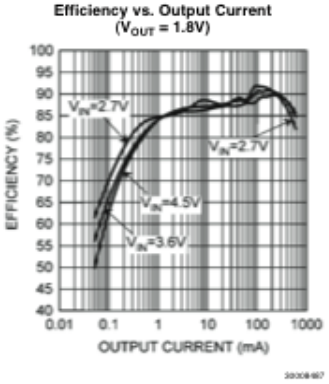


FIGURE 2. Typical Application Circuit - ADJ. Version



LM3677 3MHz, 600mA Miniature Step-Down DC-DC Converter for Ultra Low Voltage Circuits

Annexes 5: Buck DC-DC converter

SEMTECH

SC191
Low Supply Ripple Synchronous Buck Conversion Regulator

POWER MANAGEMENT

Description

The SC191 is a synchronous step-down converter with integrated power devices and an integrated front-end LDO regulator to minimize input supply ripple. If supply ripple is not a concern, the front-end LDO regulator can be bypassed externally to maximize efficiency.

The internal MOSFET switches provide peak current greater than 550mA to achieve a DC output of at least 330mA over the rated input voltage range, making the SC191 ideal for single-cell Li-ion battery applications as well as fixed 3.3V and 5V fixed input applications. The output is a fixed 1.2V - ideal for low-voltage microprocessors. Other voltage options are available (consult the factory for details).

Additional features include internal soft-start to limit in-rush current, over-current protection, over-temperature protection, and over-voltage protection.

The 1MHz switching frequency allows the use of small surface mount capacitors and inductors, and no other external compensation components are needed. The device is available in a low profile (0.8mm max height) 2.3mm x 2.3mm MLPD 8-lead package, minimizing area without compromising performance.

Features

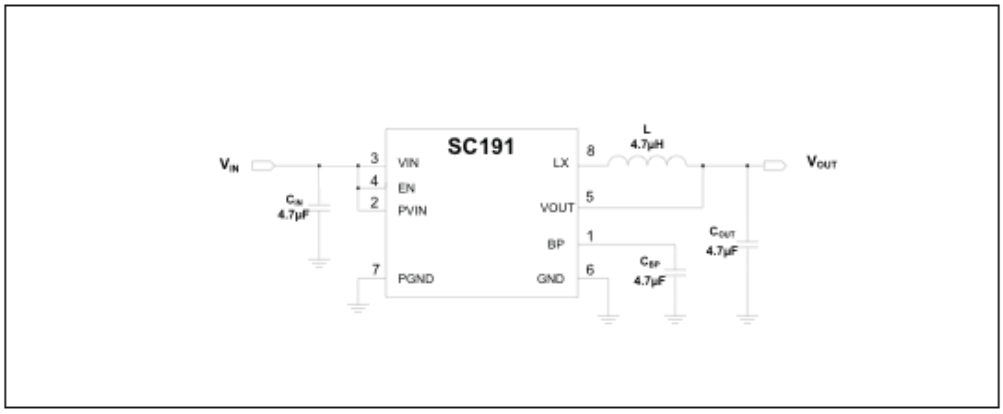
- Less than 1mV Supply Ripple
- 2.7V to 5.5V Input Range
- 330mA Guaranteed Output Current
- Fixed Frequency 1MHz Operation
- No Schottky Diode Required
- Over-Current Protection
- Over-Voltage Protection
- Over-Temperature Protection
- Soft-Start
- No External Compensation Required
- MLPD-8, 2.3mm x 2.3mm Package
- WEEE and RoHS Compliant

Applications

- Cell Phones
- Cordless Phones
- Notebook and Subnotebook Computers
- PDAs and Mobile Communicators
- WLAN Peripherals
- Wireless Modules
- 1 Li-Ion or 3 NiMH/NiCd Powered Devices

Patent Pending

Typical Application Circuit



This project is funded by the European Commission under the 7th Research Framework Programme.

Annexes 6: Low-voltage LDO

MICREL®

MIC5232

10mA Ultra-Low Quiescent Current µCap LDO

General Description

The MIC5232 is an ultra-low quiescent current, low-dropout linear regulator that is capable of operating from a single-cell lithium ion battery. Consuming only 1.8µA of quiescent current while operating, the MIC5232 is ideal for stand-by applications like powering real-time clocks or memory in battery operated electronics.

The MIC5232 is capable of providing 10mA of output current and has low output noise, providing a small, efficient solution ideal for any keep-alive application. Including reverse current protection, keeping reverse leakage ($V_{OUT} > V_{IN}$) down to 20nA.

The MIC5232 is a µCap design, operating with very small ceramic output capacitors for stability, reducing required board space and component cost.

The MIC5232 is available in fixed output voltages in the miniature 6-pin 2mm x 2mm MLF® package and thin SOT-23-5 package with an operating junction temperature range of -40°C to 125°C.

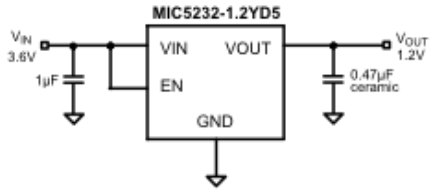
Features

- Input voltage range: 2.7V to 7.0V
- Ultra-low Iq: Only 1.8µA operating current
- Stable with 0.47µF ceramic output capacitor
- Low dropout voltage of 100mV @ 10mA
- Reverse Battery Protection
- High output accuracy:
  - ±2.0% initial accuracy
  - ±3.0% over temperature
- Logic-Level Enable Input
- Miniature 6-pin 2mm x 2mm MLF® package
- Lead-Free Thin SOT-23-5 Package
- Tight Load and Line Regulation

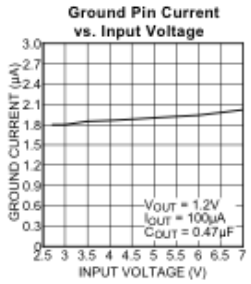
Applications

- Real-Time Clock Power Supply
- Stand-by Power Supply
- SRAM Memory Back-up Supply
- Cellular Telephones and Notebook Computers

Typical Application



1.5 Real-Time Clock Back-up Supply



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September 2008 M9999-090508-C

Annexes 7: Low-voltage LDO

LINEAR TECHNOLOGY

LT3009 Series

3µA I_Q, 20mA Low Dropout Linear Regulators

FEATURES

- **Ultralow Quiescent Current: 3µA**
- **Input Voltage Range: 1.6V to 20V**
- **Output Current: 20mA**
- **Dropout Voltage: 280mV**
- **Adjustable Output (V_{ADJ} = $V_{OUT(MIN)}$ = 600mV)**
- **Fixed Output Voltages: 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V**
- Output Tolerance: ±2% Over Load, Line and Temperature
- Stable with Low ESR, Ceramic Output Capacitors (1µF minimum)
- Shutdown Current: <1µA
- Current Limit Protection
- Reverse-Battery Protection
- Thermal Limit Protection
- 8-Lead SC70 and 2mm × 2mm DFN Packages

APPLICATIONS

- Low Current Battery-Powered Systems
- Keep-Alive Power Supplies
- Remote Monitoring
  - Utility Meters
  - Hotel Door Locks

DESCRIPTION

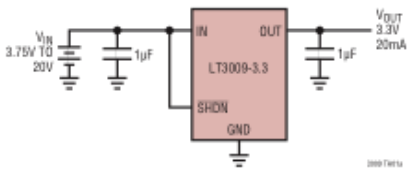
The LT®3009 Series are micropower, low dropout voltage (LDO) linear regulators. The devices supply 20mA output current with a dropout voltage of 280mV. No-load quiescent current is 3µA. Ground pin current remains at less than 5% of output current as load increases. In shutdown, quiescent current is less than 1µA.

The LT3009 regulators optimize stability and transient response with low ESR ceramic capacitors, requiring a minimum of only 1µF. The regulators do not require the addition of ESR as is common with other regulators. Internal protection circuitry includes current limiting, thermal limiting, reverse-battery protection and reverse-current protection.

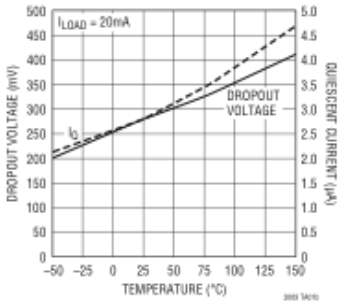
The LT3009 Series are ideal for applications that require moderate output drive capability coupled with ultralow standby power consumption. The device is available in fixed output voltages of 1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5V, and as an adjustable device with an output voltage range down to the 600mV reference. The LT3009 is available in the 6-lead DFN and 8-lead SC70 packages.

TYPICAL APPLICATION

3.3V, 20mA Supply with Shutdown



Dropout Voltage/Quiescent Current



This project is funded by the European Commission under the 7th Research Framework Programme.

Annexes 8: Varactor

MA46H120 Series

GaAs Constant Gamma Flip-Chip Varactor Diode Rev. V3

Features

- Constant Gamma for Linear Tuning
- Low Parasitic Capacitance
- High Q
- Silicon Nitride Passivation
- Polyimide Scratch Protection
- Surface Mount Configuration

Description

M/A-COM Technology Solutions' MA46H120 series is a gallium arsenide flip chip hyperabrupt varactor diode. These devices are fabricated on OMCVD epitaxial wafers using a process designed for high device uniformity and extremely low parasitics. The MA46H120 diodes are fully passivated with silicon nitride and have an additional layer of polyimide for scratch protection. The protective coatings prevent damage to the junction during automated or manual handling. The flip chip configuration is suitable for pick and place insertion.

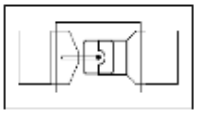
Absolute Maximum Ratings [1,2]

Operating Temperature	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Power Dissipation	100 mW
Mounting Temperature	+235°C for 10 seconds

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. M/A-COM does not recommend sustained operation near these survivability limits.

Chip Layout

Front View (Circuit Side)



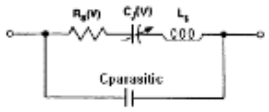
Back View (Operator Side)

Ordering Information

Part Number	Package
MA46H120-W	Whole Wafer
MA46H120	Gel Pack
MAVR-000120-12030W	Waffle Pack

Schematic

FLIPCHIP TUNING VARACTOR EQUIVALENT CIRCUIT



Electrical Specifications @ T_A = +25 °C

Breakdown Voltage @ I_R = 10μA, V_R = 20 V Minimum
Reverse Leakage Current @ V_R =14V, I_R = 100 nA Maximum

	C_T (pF) f=1MHz, V_R=0V			C_T (pF) f=1MHz, V_R=4V			C_T (pF) f=1MHz, V_R=10V			Q Factor f=50MHz, V_R=4V			Gamma V_R=2-12V		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
MA46H120		1.1		0.30		0.40	0.14		0.20	3000			0.9		1.1

* Specifications are subject to change without prior notification

1

• **North America** Tel: 800.366.2266 / Fax: 978.366.2266
• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298
Visit www.macom.com for additional data sheets and product information.

Annexes 9:Battery dynamic model

Batteries may have quite different behavior with dynamic current (i.e. pulse currents) than at DC. Depending on the use cases, a dynamic electrical model may then be mandatory. Such a model is used, inspired by the publication "Accurate Electrical Battery Model Capable of Predicting Runtime and I–V Performance", Min Chen and Gabriel A. Rincón-Mora, IEEE transactions on energy conversion, vol. 21, no. 2, june 2006.

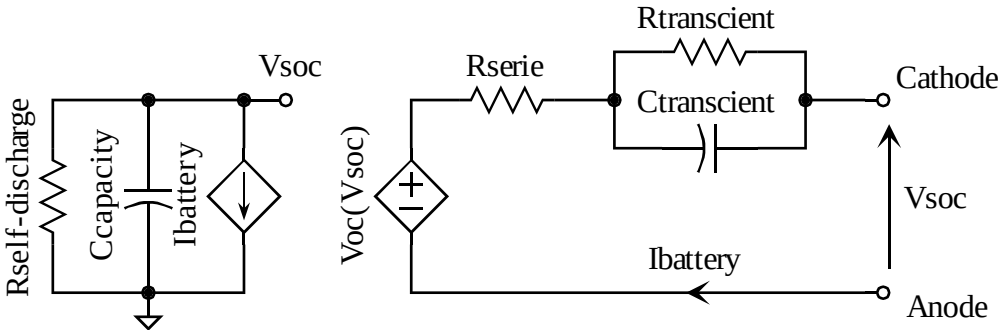


Figure 33: dynamic model of battery

The State-Of-Charge of the battery is modelized by a capacity loaded at the begin-of-life by the standard capacity given in mAH multiplied by the begin-of-life open-circuit voltage:

$$\left.\begin{aligned}\frac{1}{2}C_{capacity}V_{SOC}(0)^2 = Capacity_{mAH}\cdot 3.6E6\cdot V_{OC}(100\%)\\ V_{SOC}(0) = V_{OC}(100\%)\end{aligned}\right\} \quad \textbf{(10)}$$

$$\Rightarrow C_{capacity} = \frac{7.2E6\cdot Capacity_{mAH}}{V_{OC}(100\%)}$$

The fully charged battery voltage is taken as the maximum voltage across the Ccapacity as well as the maximum Voc(Vsoc). This maximum voltage and the minimum usable voltage define the usable capacity.

The Rself-discharge is fixed by the battery leakage.The Rserie is linked to the instantaneous voltage drop and the sum of Rserie and R transient is linked to the DC voltage drop. The Ctransient is linked, with Rtransient, to the time constant extracted from the battery voltage transient associated with a current pulse.

Note that several parallel RC can be added to the model to precise the dynamic behavior.

Note also that the temperature-dependent behavior is not taken into account.

Typical specification are at 25°C, unless otherwise noted.

Parameter	Test conditions, comments	Min.	Typ.	Max	Unit
Low-voltage battery					
V_{oc}		1.08		1.25	V
Capacity			160		mAh
$R_{self\text{-}discharge}$			0.02		MΩ
R_{serie}		0.5		4	Ω
$R_{transcient}$		2		16	Ω
$C_{transcient}$		66		461	µF

Table 23: Example of batteries specifications

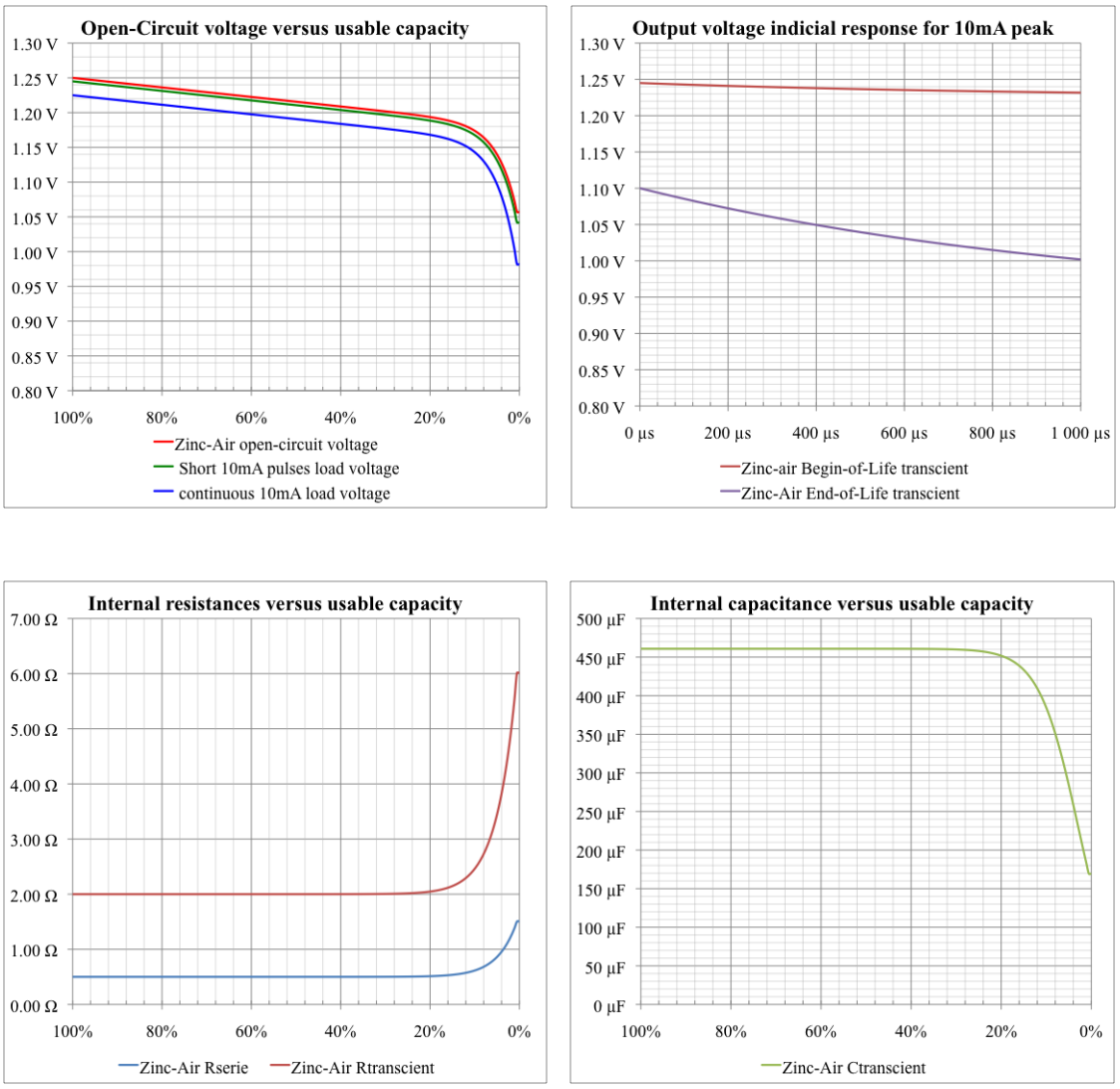


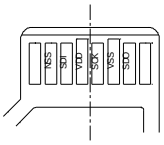
Figure 34: Example of dynamic model results

Annexes 10: microSD card mechanical drawing

	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.



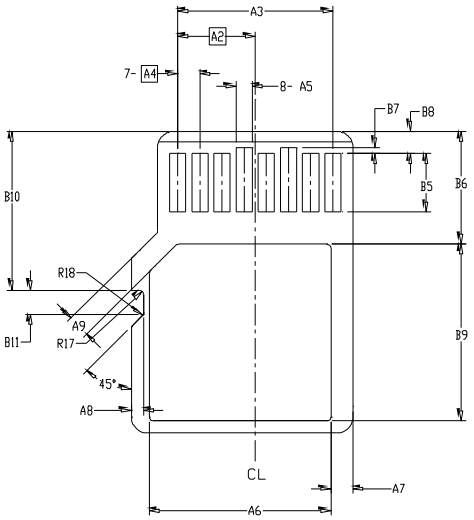


Figure E-2 : Mechanical Description: Bottom View

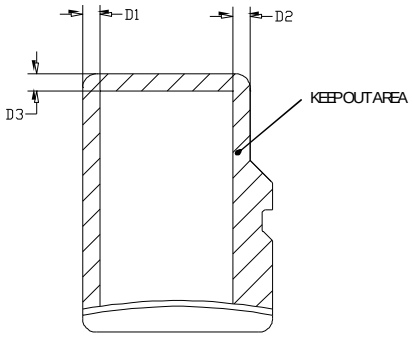


Figure E-4 : Mechanical Description: KeepOut Area

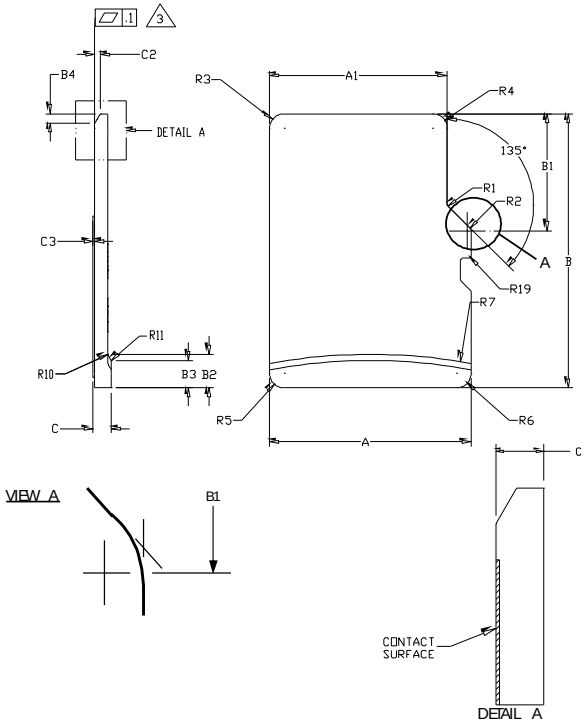


Figure E-1 : Mechanical Description: Top View

Figure 35: microSD card mechanical definition

Annexes 11:Compression coax board-to-board STAX®

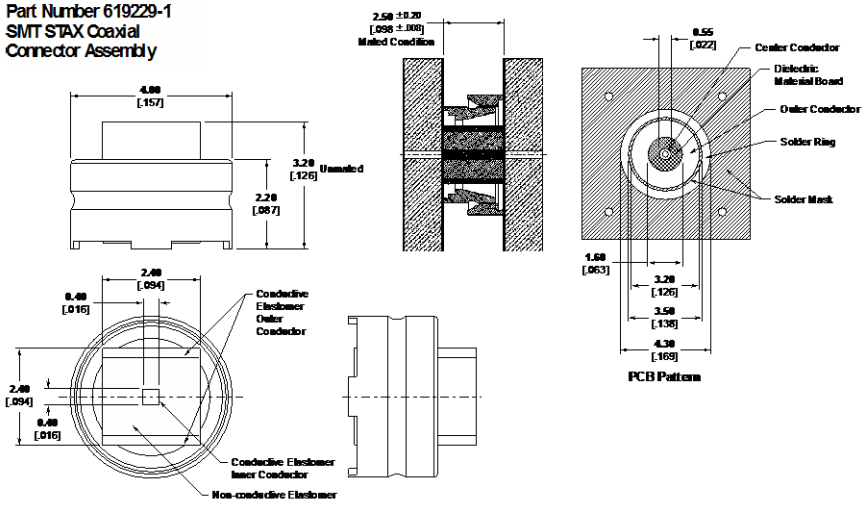
Tyco Electronics

RF Coax Connectors

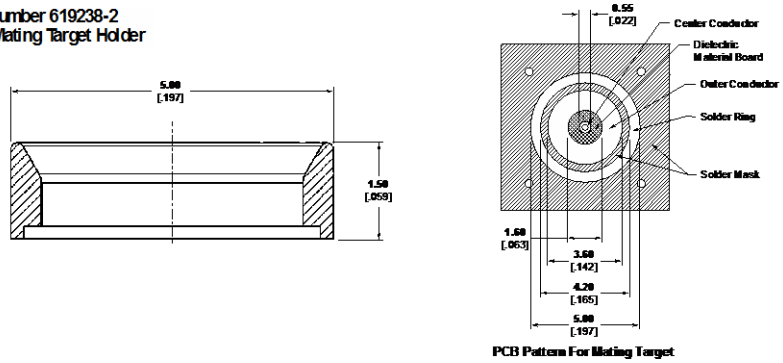
STAX Coax Connectors (Continued)

Description	Part Number
STAX SMT Coax Connector Assembly: Consists of STAX Coax elastomer in round SMT holder	619229-1
Mating SMT Target Holder: Controls alignment between PCBs	619238-2
STAX Coax RF Elastomer only: Used with customer furnished holder	1442004-1

Part Number 619229-1
SMT STAX Coaxial Connector Assembly



Part Number 619238-2
SMT Mating Target Holder



Note: Part Numbers are RoHS compliant except: ♦ Indicates non-RoHS compliant.

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Catalog 1307191
Revised 3-07

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Dimensions are in millimeters and inches unless otherwise specified. Values in brackets are standard equivalents.

Dimensions are shown for reference purposes only. Specifications subject to change.

USA: 1-800-522-6752
Canada: 1-905-470-4425
Mexico: 01-800-733-8926
C. America: 52-55-1106-0803

South America: 55-11-2103-6000
Hong Kong: 852-2735-1628
Japan: 81-44-844-8013
UK: 44-8706-080-208

Annexes 12: Comments on D1.1 demands

Items have been sorted and grouped in the following categories:

- Transmission
- Supply
- Interface
- Quality and Reliability

Comments have been added

1 Transmission

This section groups all the items relating to channel, data rate, latency, networking, range and compatibility. Channel

1.1.1 Channel requirements

Reference	Requirement	Status
R 1	2.5GHz band support	5

The 2.4GHz to 2.4835GHz ISM is covered but the upward extension to 2.5GHz, for the 802.15.6, or the downward extension to 2.36GHz, for the 802.15.4j, would need different passives: An alternate RF front-end SAW filter has been designed by EPCOS in order to cover the 2.4835-2.5GHz band and the rest of the system (RF synthesizer, etc) as been specified to cover this band extension. This is not the case for the downward extension (even if not specified, he RF synthesizers should be able to address down to 2.36GHz).

R 2	Extension to 2.5GHz	3

C.f. above remark for the R 1

R 3	Tunable modulation index	3

On Tx side, thanks to the modulation by dynamic digital programming of the RFsynthesizer, the modulation index is very precise and will be easily made programmable. The limit is in fact more on the maximum raw symbol rate limited by the synthesizer close loop bandwidth. On The Rx side, constraints upon bandwidth may limit the maximum modulation index for maximum symbol rates.

R 4	Extension to 2.5GHz	3(medical monitoring)

C.f. above remark for the R 1 in same chapter.

Table 24 Channel requirements

1.1.2 Channel parameters

Reference	Description	Min	Typ	Max	Unit	Status
P 1	Channel width	0.1		1	MHz	5

Thanks to ∑Δ RF frequency synthesis, the center frequency can be tuned very precisely and freely to whatever frequency needed. The receiver bandwidth (e.g. -3dB) needs to be fixed taking into account the signal bandwidth (depending on raw symbol rate, modulation index and pulse shaping) and the Rx-Tx relative reference frequency uncertainty. The BAW frequency uncertainty is quite important (e.g. ±400ppm max. initial frequency tolerance) and a calibration scheme needs to be implemented in order to narrow the overall uncertainty. The selectivity, e.g. adjacent channel and far interferer rejection specification is based on Bluetooth Low Energy and 802.15.4 2006 specifications.

P 2	Frequency range		2.4	2.5	GHz	5

C.f. above remark for the R 1 in chapter 1.1.1.

Table 25 Channel parameters

1.2 Data rate

1.2.1 Data rate requirements

Reference	Requirement	Status
R 5	Peak data rate >2kB/s, in small bursts	5

The specified peak datarate is 2Mbit/s. Any peak datarate reduction improves the sensitivity. But too low peak datarate may be impractical because of relative frequency reference imprecision. Any average datarate reduction can be implemented with reduction of average current consumption.

R 6	Tunable data rate	3 (Eb tradeoffs)

On transmitter side, it is quite simple to scale down the peak datarate by integer division factor (possibly with the addition of an interpolation filter in digital domain). On receiver side, it should be also quite simple to implement the same scheme in digital domain (possibly with a decimation filter). The difficulty may be to implement the same scaling for the channel prior to analog to digital conversion. So by principle it should be quite easy to implement a datarate scale down over a decade but maybe at the cost of reduced channel filtering performances. Note that the narrowing of the channel filter is limited by the obtain RF frequency precision. Regarding this aspect, an Automatic Frequency Control may be considered for Data Streaming type of communication. Some limited Direct Sequence Spread Spectrum scheme, such as what is used in 802.15.4 2006 can also be considered. In practice, there is no AFC implemented and the raw modulation schemes that are considered are the 2Mbit/s MSK and the 1Mbit/s GFSK. Note that duty cycling the transceiver activity

Reference	Requirement	Status
	reduces the peak data rate to an average data rate by reducing approximately by the same amount the current consumption: by principle any average data rate lower than the peak data rate can be configured.	

Table 26 Data rate requirements

1.2.2 Data rate parameters

Reference	Description	Min	Typ	Max	Unit	Status
P 3	Data rate		1		MBit/s	3
C.f. above remark for the R 5 and R 6 in chapter 1.2.1.						
P 4	Data rate		1		kBit/s	3
C.f. above remark for the R 5 and R 6 in chapter 1.2.1: this data rate is too low to gain on sensitivity linearly because of relative frequency imprecision.						
P 5	Data rate		100		kBit/s	3
C.f. above remark for the R 5 and R 6 in chapter 1.2.1.						
P 6	Data rate		30		kBit/s	3
C.f. above remark for the R 5 and R 6 in chapter 1.2.1: this data rate is too low to gain on sensitivity linearly because of relative frequency imprecision.						
P 7	Data rate		5		kBit/s	3
C.f. above remark for the R 5 and R 6 in chapter 1.2.1: this data rate is too low to gain on sensitivity linearly because of relative frequency imprecision.						
P 8	Data rate		5		kBit/s	3
C.f. above remark for the R 5 and R 6 in chapter 1.2.1: this data rate is too low to gain on sensitivity linearly because of relative frequency imprecision.						
P 9	Useful data rate (non-streaming)	2			kBit/s	5
C.f. above remark for the R 5 and R 6 in chapter 1.2.1: this data rate is too low to gain on sensitivity linearly because of relative frequency imprecision.						
P 10	Data rate	30	200	1000	kBit/s	5
C.f. above remark for the R 5 and R 6 in chapter 1.2.1: lower data rate is too low to gain on sensitivity linearly because of relative frequency imprecision.						

Reference	Description	Min	Typ	Max	Unit	Status
P 11	Data rate	3			kbit	5

C.f. above remark for the R 5 and R 6 in chapter 1.2.1: this datarate is too low to gain on sensitivity linearly because of relative frequency imprecision.

P 12	Data rate (payload)	200			kbit	5

C.f. above remark for the R 5 and R 6 in chapter 1.2.1.

P 13	Data rate (payload)	1.2			Mbit	5

C.f. above remark for the R 5 and R 6 in chapter 1.2.1.

P 14	Data rate	20			kbit	5

C.f. above remark for the R 5 and R 6 in chapter 1.2.1: this datarate is too low to gain on sensitivity linearly because of relative frequency imprecision.

P 15	Data rate (payload)	300			kbit	5

C.f. above remark for the R 5 and R 6 in chapter 1.2.1.

P 16	Data rate	10			kbit	2

C.f. above remark for the R 5 and R 6 in chapter 1.2.1: this datarate is too low to gain on sensitivity linearly because of relative frequency imprecision.

P 17	Data rate	20		2000	kbit/s	5

C.f. above remark for the R 5 and R 6 in chapter 1.2.1: lower datarate is too low to gain on sensitivity linearly because of relative frequency imprecision.

P 18	Data rate	10		1000	Kbit	4

C.f. above remark for the R 5 and R 6 in chapter 1.2.1: lower datarate is too low to gain on sensitivity linearly because of relative frequency imprecision.

P 19	Data rate	1000			kbit/s	5

C.f. above remark for the R 5 and R 6 in chapter 1.2.1.

P 20	Data rate	1000			Kbit/s	2

C.f. above remark for the R 5 and R 6 in chapter 1.2.1.

P 21	Data rate	20		2000	kbit/s	5

C.f. above remark for the R 5 and R 6 in chapter 1.2.1: lower datarate is too low to gain on sensitivity linearly because of relative frequency imprecision.

Table 27 Data rate parameters

1.3 Latency and delays

1.3.1 Latency and delays requirements

Reference	Requirement	Status
R 7	Latency <1s to initiate communication, then <50ms	3

C.f. above remark for the R 5 and R 6 in chapter 1.2.1. For extremely long latencies, wake up from Off mode can be considered in order to limit the leakages.

R 8	Tolerance to long latencies (several tens of ms) by the MCU controlling the WiserBAN radio sub-system	5

This is inherent to Control-Command type of communication described in chapter 4.2.1.

Table 28 Latency and delays requirements

1.3.2 Latency and delays parameters

Reference	Description	Min	Typ	Max	Unit	Status
P 22	Latency			500	ms	3

Any average data rate reduction can be implemented with reduction of average current consumption with tradeoff on latency. This max. latency should be covered without problem.

P 23	Delay			300	ms	3

C.f. P 22 in same chapter.

P 24	Latency			300	ms	3

C.f. P 22 in same chapter.

P 25	Latency			500	ms	3

C.f. P 22 in same chapter.

P 26	Delay			15	ms	3

Any average data rate reduction can be implemented with reduction of average current consumption with tradeoff on latency. This latency should be covered without problem except source coding (e.g. audio compression & decompression).

P 27	Latency			250	ms	3

C.f. P 22 of same chapter

Reference	Description	Min	Typ	Max	Unit	Status
P 28	Delay			25	ms	3

C.f. P 26 of same chapter

P 29	Latency			200	ms	3

C.f. P 22 of same chapter

P 30	Latency			200	ms	3

C.f. P 22 of same chapter

P 31	Delay			5	ms	3

Any average datarate reduction can be implemented with reduction of average current consumption with tradeoff on latency. This latency is not a problem for the communication itself but will be hard to comply with in case of source coding.

P 32	Latency (link established)			50	ms	4

C.f. P 22 of same chapter

P 33	Wake-up time		100		µs	3

From sleep mode, tough but aligned with one of the more constrain specification of the platform.

P 34	Latency	1	2	4	ms	5

C.f. P 31 in same chapter.

P 35	Wake up time		20		µs	5

From sleep mode, tough but aligned with one of the more constrain specification of the platform. If number not reached in practice, it could be possible to run the BAW oscillator continuously to reach the number.

P 36	Latency			100	ms	5

C.f. P 22 of same chapter

P 37	Wake-up time		100		µs	1

C.f P 33 in same chapter

P 38	Latency (without			1	ms	5

Reference	Description	Min	Typ	Max	Unit	Status
	compression)					

Any average datarate reduction can be implemented with reduction of average current consumption with tradeoff on latency. This latency is not a problem for the communication only.

P 39	Timing Jitter (bilateral CI case)			+/-50	µs	5

Should not be a problem because number much lower than the data rate itself.

P 39	Wake-up time		100		ms	0

No problem except if needs to be waked up from Off state: in this case only extremely short software can be compliant (because of on-chip RAM reload from EEPROM).

P 40	Latency (without compression)			1	ms	5

Any average data rate reduction can be implemented with reduction of average current consumption with tradeoff on latency. This latency is not a problem for the communication only.

P 41	Timing Jitter (bilateral CI case)			+/-50	µs	5

C.f. P 39 of same chapter.

P 42	Latency			1	ms	5

C.f. P 38 of same chapter.

P 43	Timing Jitter (trigger)			+/-50	µs	5

Specification imprecise but assumed to be the same as P 39 of same chapter.

P 44	Wake-up time		100		µs	0

C.f. P 33 of same chapter.

P 45	Latency (activation)			1	ms	0

C.f. P 38 of same chapter.

P 46				+/-50	µs	5

Reference	Description	Min	Typ	Max	Unit	Status
Specification not comprehensible.						
P 47				50	µs	5
Specification not comprehensible.						
P 48	Timing Jitter	0.5			m	5
For synchronizing of sound processing: basically not a problem this specification has to consider tradeoff on current consumption.						
P 49	Wake-up time					
Specification not comprehensible.						
P 50	Latency (without compression)			1	ms	5
C.f. P 38 of same chapter.						
P 51	Timing jitter			+/-50µs		5
C.f. P 44 of same chapter.						
P 52	Wake-up time		100		µs	0
C.f. P 33 of same chapter.						
P 53	Latency			100	ms	1
C.f. P 22 of same chapter.						
P 54	Wake-up time		100		µs	0
C.f. P 33 of same chapter.						
P 55	Latency			200	ms	1
C.f. P 22 of same chapter.						
P 56	Wake-up time		100		µs	1
C.f. P 33 of same chapter.						
P 57	Latency			250	ms	1
C.f. P 22 of same chapter.						
P 58	Set-up time			3	s	5
Not a problem.						

Reference	Description	Min	Typ	Max	Unit	Status
P 59	Latency			100	ms	3
C.f. P 22 of same chapter.						
P 60	Wake-up time		100		µs	3
C.f. P 33 of same chapter.						
P 61	Latency			200	ms	1
C.f. P 22 of same chapter.						
P 62	Wake-up time		100		µs	1
C.f. P 33 of same chapter.						

Table 29 Latency and delays parameters

1.4 Networking

1.4.1 Networking requirements

Reference	Requirement	Status
R 9	Bidirectional radio link	5
With Half-Duplex link.		
R 10	2 and 3 nodes BAN (works with 2 HI only or with additional remote)	5
Star-shape multi-node protocol foreseen.		
R 11	Bidirectional radio link	5
C.f. R 9 of same chapter.		
R 12	Listen before talk	0
Taken into account (the “CA” in CSMA-CA means “Collision Avoidance” which is in practice a mechanism similar to the “Listen Before Talk”).		
R 13	Preferred topology Star, Remote is in the center	2
C.f. R 10		
R 14	Channel management	5
Any type of slow frequency hopping , listen before talk, etc can be implemented in		

Reference	Requirement	Status

software.

R 15	Bluetooth (audio profile) and Bluetooth LE compatibility mode	5

The Bluetooth audio profile will not be covered: it would overstress the design with particularly important impact on current consumption (but everything will be attempt to make possible the interaction at hardware level even if not fully compliant).

R 16	Bidirectional radio link (half duplex)	5

C.f. R 9 of same chapter.

R 17	Bidirectional radio link (TX power management, acknowledge)	5

C.f. R 9 of same chapter.

R 18	Bluetooth audio profile	5

C.f. R 15 of same chapter.

R 19	Bidirectional radio link (TX power management, acknowledge)	5

C.f. R 9 of same chapter and R 20 of chapter 3.1.1.

R 21	Bidirectional radio link (half duplex)	5

C.f. R 9 of same chapter.

R 22	Bidirectional radio link (full duplex)	5

C.f. R 9 of same chapter.

R 23	Bidirectional radio link (wake up)	5

According to response time /current consumption tradeoff.

R 24	Bidirectional radio link	5 (meshed network)

C.f. R 9 of same chapter.

R 25	Listen before talk	5 (CSMA-CA)

C.f. R 12 of same chapter.

Reference	Requirement	Status
R 26	Bluetooth LP compatible	5t
Targeted for PHY layer but complete software-based protocol stack may be out-of-project.		
R 27	802.15.4-2006 compatible	5
Targeted for PHY layer but complete software-based protocol stack may be out-of-project.		
R 28	Bidirectional radio link	4
C.f. R 9 of same chapter.		
R 29	Coexistence	5
Specification needs to be stated.		
R 30	Compatibility with existing communication standards	4
C.f. R 25 and R 26.		
R 31	Bidirectional radio link	5 (reliable links)
C.f. R 9 of same chapter.		
R 32	Listen before talk	3
C.f. R 12 of same chapter.		
R 33	Bluetooth le compatible	5
C.f. R 26 of same chapter.		
R 34	802.15.4-2006 compatible	3
C.f. R 27 of same chapter.		
R 35	Channel management	4
C.f. R 14 of same chapter.		
R 36	Bidirectional radio link	5
C.f. R 9 of same chapter.		
R 37	Bluetooth LE compatible	5
C.f. R 26 of same chapter.		

Table 30 Networking requirements

1.4.2 Networking parameters

Reference	Description	Min	Typ	Max	Unit	Status
P 63	Number of devices		6			5

Reference	Description	Min	Typ	Max	Unit	Status

Taken into account.

Table 31 Networking parameters

1.5 Link range

1.5.1 Link range requirements

Reference	Requirement	Status
R 38	Range 2 to 5m	5

C.f. chapter 4.1.

Table 32 Link range requirements

1.5.2 Link range parameters

Reference	Description	Min	Typ	Max	Unit	Status
P 64	Range		3m			3

C.f. chapter 4.1.

P 65	Range		1m			3

C.f. chapter 4.1.

P 66	Range		10m			3

C.f. chapter 4.1.

P 67	Range		1m			3

C.f. chapter 4.1.

P 68	Range HI-to-HI		0,3m			3

C.f. chapter 4.1.

P 69	Range Remote-to-HI		1m			3

C.f. chapter 4.1.

P 70	Range		0,3m			3

C.f. chapter 4.1.

Reference	Description	Min	Typ	Max	Unit	Status
P 71	Range	2	3	10	m	5

C.f. chapter 4.1.

P 72	Distance range	3			m	4

C.f. chapter 4.1.

P 73	Distance range	5			m	4

C.f. chapter 4.1.

P 74	Distance range	5			m	4

P 75	Distance range	5			m	4

C.f. chapter 4.1.

P 76	Distance range	0.5			m	5

C.f. chapter 4.1.

P 77	Distance range	3			m	4

C.f. chapter 4.1.

P 78	Distance range		3	10	m	5

C.f. chapter 4.1.

P 79	Distance range	3			m	4

C.f. chapter 4.1.

Table 33 Link range parameters

1.6 Electromagnetic compatibility

1.6.1 Electromagnetic compatibility requirements

Reference	Requirement	Status
R 39	Worldwide regulatory compliance	5

As far as it remain in 2.4GHz to 2.483GHz ISM band: compliance with 802.15.6 and 802.15.4j

Reference	Requirement	Status
may ask for different modulation not covered		
R 40	Worldwide regulatory compliance	5
C.f. R 39 of same chapter.		
R 41	Interoperability with other protocols & perturbators	5
Specification needs to be stated.		
R 42	Immunity to MRI	5
Specification needs to be stated.		
R 43	Can survive 200 V/m at 2.45 GHz	5
Depends on the antenna gain, not impossible but need to be checked: it would be interesting to precise the specification especially the test setup.		

Table 34 Electromagnetic compatibility requirements

1.6.2 Electromagnetic compatibility parameters

None.

2 Supply

This section groups the items related to the supply voltage and the power consumption

2.1 Supply requirements

Reference	Requirement	Status
R 44	Supply voltage range <1.8 to >2.3V	2
C.f. chapter 2.6.2.		
R 45	Autonomy at least 9 days @ <120J/day	5
Depends on tradeoff explained in previous chapters… and battery capacity.		

Table 35 Supply requirements

2.2 Supply parameters

Reference	Description	Min	Typ	Max	Unit	Status

Reference	Description	Min	Typ	Max	Unit	Status
P 80	Standby current			<200	nA	5

Impossible with existing memory and digital gate libraries, except with complete supply disconnection.

P 81	Peak current			20	mA	4

Taken into account.

P 82	Power consumption active		1	10mW	mW	5

Targeted but depends on tradeoffs explained in previous chapters

P 83	Power consumption idle		1	3	μ W	5

C.f. P 80 of same chapter.

P 84	Power consumption sniff mode		1	3	μ W	4

Possible for analog only, c.f. P 80 of same chapter for digital.

P 85	Standby current (sniff mode, RSSI, no RF)			5	µW	5

C.f. P 84 of same chapter.

P 86	Standby current (sniff mode, RSSI, RF noise present)			50	µW	5

Possible but depends on tradoff described in previous chapters

P 87	Standby current (sniff mode, RSSI, no RF)			5	µW	5

C.f. P 84 of same chapter.

P 88	Standby current (sniff mode, RSSI, RF noise present)			50	µW	5

C.f. P 86 of same chapter.

Reference	Description	Min	Typ	Max	Unit	Status
P 89	Standby current (sniff mode, RSSI, no RF)			5	µW	5

C.f. P 84 of same chapter.

P 90	Standby current (sniff mode, RSSI, RF noise present)			50	µW	5

C.f. P 86 of same chapter.

P 91	Operating power consumption			1	mW	5

C.f. P 86 of same chapter.

P 92				5	µW	5

?

P 93				50	µW	5

?

P 94	Operating power consumption			100	µW	4

C.f. P 86 of same chapter.

P 95	Standby current (sniff mode, RSSI, no RF)					

?

P 96	Standby current (sniff mode, RSSI, RF noise present)					

?

P 97	Operating current consumption			0.5	mW	5

C.f. P 86 of same chapter.

Reference	Description	Min	Typ	Max	Unit	Status
P 98	Standby current (sniff mode, RSSI, no RF)			5	µW	5

C.f. P 84 of same chapter.

P 99	Standby current (sniff mode, RSSI, RF noise present)			50	µW	5

C.f. P 86 of same chapter.

P 100	Tx consumption		10		mA	3

Targeted below for max. datarate.

P 101	Rx consumption		10		mA	3

Targeted below for max. datarate.

P 102	Standby current			5	µA	5

C.f. P 84 of same chapter.

P 103	Tx consumption			10	mA	3

C.f. P 100 of same chapter.

P 104	Rx consumption			10	mA	3

C.f. P 101 of same chapter.

P 105	Standby current (sniff mode, RSSI, no RF)			2	µA	4

C.f. P 84 of same chapter.

2.3

Reference	Description	Min	Typ	Max	Unit	Status
P 106	Standby current current (sniff mode, RSSI, RF noise present)			20	µA	5

C.f. P 84 of same chapter.

P 107	Tx consumption		10		mA	3

C.f. P 100 of same chapter.

P 108	Rx consumption		10		mA	3

C.f. P 101 of same chapter.

P 109	Standby current			5	µA	5

C.f. P 84 of same chapter.

Table 36 Supply parameters

3 Interface

This section groups all the items relating to the interface aspects on the RF side, on the application side and on the mechanical side.

3.1 RF interface

3.1.1 RF interface requirements

Reference	Requirement	Status
R 46	Adaptive antenna matching	1

Specified for antennas described in chapter 2.7.2 chapter 0.

R 47	Adaptive antenna matching	5

C.f. R 46 of same chapter.

R 48	TX power management	2

There is very little current saving by reducing the Tx power below the targeted one because of overhead such as the BAW oscillator and RF synthesizer consumption. So we did not

Reference	Requirement	Status
consider any tuning on RF power (but it's possible).		
R 49	TX power management	5
C.f. R 48 of same chapter.		
R 50	TX power management	3
C.f. R 48 of same chapter.		
R 51	TX power management	5
C.f. R 48 of same chapter.		
R 52	TX power management	5
C.f. R 48 of same chapter.		
R 53	TX power management	0
C.f. R 48 of same chapter.		
R 54	Adaptive antenna matching	3
C.f. R 46 of same chapter.		
R 55	Programmable pulse shaping	3
Taken into account.		
R 56	Tunable RF output power	3
C.f. R 48 of same chapter.		
R 57	Tunable RF output power	3
C.f. R 48 of same chapter.		
R 58	Adaptive antenna matching	3
C.f. R 46 of same chapter.		
R 59	Tunable RF output power	3
C.f. R 48 of same chapter.		
R 60	Adaptive antenna matching	4
C.f. R 46 of same chapter.		

Reference	Requirement	Status
R 61	TX power management	3

C.f. R 48 of same chapter.

R 62	Adaptive antenna matching	3

C.f. R 46 of same chapter.

Table 37 RF interface requirements

3.1.2 RF interface parameters

Reference	Description	Min	Typ	Max	Unit	Status
P 110	Sensitivity	-102		-92	dBm	5

Max. considered for 1mbit/s and min considered for 100kbit/s.

P 111	Input impedance (antenna)		50		Ω	5

Taken into account.

P 112	RF interface impedance		50		Ω	5

C.f. P 111 of same chapter.

P 113	Output power		0		dBm	5

Taken into account.

P 114	Output power	-20		0	dBm	5

Taken into account , c.f. R 48 of same chapter if RF output power tuning is understood.

P 115	Output power		-10		dBm	5

C.f. R 48 of same chapter.

P 116	Input impedance		50		Ω	4

C.f. P 111 of same chapter.

P 117	RF interface impedance		50		Ω	5

C.f. P 111 of same chapter.

Reference	Description	Min	Typ	Max	Unit	Status
P 118	Output power		0		dBm	5

C.f. R 113 of same chapter.

Table 38 RF interface parameters

3.2 System and interface

3.2.1 System and interface requirements

Reference	Requirement	Status
R 63	I2C Interface	5

Not considered because we prefer SPI serial because of possible reuse of EEPROM interface: It's possible but it would add additional pins.

R 64	Low pin-count: interface <6 lines, serial	4

The SPI (SoC and EEPROM access) need 5pins and PDM 3 additional pins.

R 65	Low processing power requirement for the MCU controlling the WiserBAN radio sub-system	5

C.f. chapter 2.9.3.

R 66	Low memory footprint requirement for the MCU controlling the WiserBAN radio sub-system	5

All protocol intended to be integrated non-chip so a simple SPI interface should be enough to control the SoC and exchange data.

R 67	Device-wakeable Yes	5

Yes using on-chip RTC-based interrupt (if leakages ok).

R 68	Host-wakeable Yes	5

Yes through interrupt on an interface port (or supply disconnection).

R 69	Listen before talk (2.5GHz Band)	5

Taken into account.

R 70	Data integrity	5

A hardware CRC is planned. Further verification can be implemented in software.

Reference	Requirement	Status
R 71	I2S Interface (adapted)	5

Yes, confirmation needed that the “adapted” correspond to a PDM interface.

R 72	I2C Interface	5

C.f. R 63 of same chapter.

R 73	SPI Interface	0

Yes, in Master mode for interface to EEPROM and possibly on Slave mode for interface with off-chip controller.

R 74	FLASH/EEPROM	5

Yes but off-chip.

R 75	RAM	5

96kBytes partitionable into program and memory banks.

R 76	GPIO	3

All digital IOs can be configured as standards GPIOs.

R 77	Voltage regulator up to 7V input	2

The power management is implemented off-chip on the platform (to focus the SoC design on more challenging functionalities).

R 78	Peripheral logic level scalable	5

This is the SoC “high voltage”, c.f. chapter 2.6.2.

R 79	Encryption	1

Not considered in hardware but always possible in software.

R 80	Low duty cycle RX, wake up on RSSI (sniff mode)	5

Targeted, c.f. chapter 4.2.1.

R 81	Encryption	0

C.f. R 78 in same chapter.

Reference	Requirement	Status
R 82	Wake up: activation with RC	5

No, with RTC based on Low-Frequency silicon Resonator

R 83	Embedding of control data (RC functionality)	5

Specification not understood.

R 84	I2S Interface (adapted)	5

C.f. R 71 of same chapter.

R 85	I2S Interface (adapted)	5

C.f. R 71 of same chapter.

R 86	Wake up: activation with RC	5

C.f. R 82 of same chapter.

R 87	Data integrity	5

C.f. R 71 of same chapter.

R 88	Wake up: activation with Codeword (sniff mode)	5

C.f. R 80 of same chapter.

R 89	I2C Interface	5

C.f. R 63 of same chapter.

R 90	SPI Interface	0

C.f. R 73 of same chapter.

R 91	Encryption	5

C.f. R 78 in same chapter.

R 92	Encryption	3

C.f. R 78 in same chapter.

R 93	Wake up: activation	5

C.f. R 80 in same chapter.

Reference	Requirement	Status
R 94	I2C Interface	5

C.f. R 63 of same chapter.

R 95	SPI Interface	0

C.f. R 73 of same chapter.

R 96	Encryption	0

C.f. R 78 in same chapter.

R 97	Wake up: activation	5

C.f. R 80 in same chapter.

R 98	I2S Interface (adapted)	5

C.f. R 71 of same chapter.

R 99	Encryption	0

C.f. R 78 in same chapter.

R 100	Low duty cycle RX, wake up on RSSI (sniff mode)	5

C.f. R 80 of same chapter.

R 101	I2C Interface	5

C.f. R 63 of same chapter.

R 102	RSSI	5

Yes, mandatory for wakeup on RF.

R 103	AGC	5

Yes, implemented in hardware.

R 104	FEI | AFC	3

Yes, yet, a priori implemented in software for maximum flexibility (i.e. in physical layer).

R 105	Controller	5 (protocol and sensing)

Yes, low-power general purpose 32bit µC with additional instruction set dedicated to DSP (2 MAC I //).

R 106	SPI & PDM interface	5

Yes.

Reference	Requirement	Status
R 107	I2C interface	5
C.f. R 63 of same chapter.		
R 108	I2C interface	3
C.f. R 63 of same chapter.		
R 109	I2S interface	3
Yes.		
R 110	UART interface	3
Yes but multiplexed on existing digital IOs.		
R 111	JTAG interface	3
Yes, for test and debug purpose but multiplexed on the limited number of digital IOs.		
R 112	RF remote programming	3
A priori, should be feasible.		
R 113	Real Time Clock	5
Yes, with on-platform Low-Frequency silicon resonator.		
R 114	4 Hardware Timers with PWM	3
Yes.		
R 115	Clock outputs	3
Yes but multiplexed on the limited number of digital IOs.		
R 116	Regulated voltage outputs	3
No, c.f. R77 of same chapter.		
R 117	GPIO	5
C.f. R 76 of same chapter.		
R 118	Ultra-low-power comparators	3
Not presently, specification and use to be precised.		
R 119	Regulators	5 (RF & digital)
No, c.f. R77 of same chapter.		
R 120	Voltage step-up	3
No, c.f. R77 of same chapter.		
R 121	Voltage step-down	3
No, c.f. R77 of same chapter.		

Reference	Requirement	Status
R 122	Low-resolution ADC	3 (t° sensing & voltage monitoring)
No, c.f. R77 of same chapter, specification and use to be precised.		
R 123	Brown out	5 (POR)
No, c.f. R77 of same chapter.		
R 124	LED current sources	3
No, c.f. R77 of same chapter.		
R 125	RSSI	5
C.f. R 102 in the same chapter.		
R 126	Micro-Controller	5
C.f. R 105 in same chapter.		
R 127	SPI	5
C.f. R 73 of same chapter.		
R 128	UART interface	3
C.f. R 110 in same chapter.		
R 129	JTAG interface	3
C.f. R 111 in same chapter.		
R 130	Real Time Clock	5
C.f. R 113 in same chapter.		
R 131	High-resolution ADC	3
C.f. R 122 in same chapter.		
R 132	Brown out & Power-On-Reset	5
C.f. R 77 in same chapter.		
R 133	Encryption	4
C.f. R 78 in same chapter.		
R 134	Data integrity	4
C.f. R 71 of same chapter.		
R 135	Low duty cycle RX, wake up on RSSI (sniff mode)	4
C.f. R 80 of same chapter.		

Reference	Requirement	Status
R 136	I2C Interface	5

C.f. R 63 of same chapter.

R 137	integrated Controller	3

C.f. R 105 of same chapter.

R 138	SPI & PDM interface	3

C.f. R 106 of same chapter.

R 139	I²C interface	5

C.f. R 63 of same chapter.

R 140	UART interface	3

C.f. R 110 of same chapter.

R 141	JTAG interface	3

C.f. R 111 of same chapter.

R 142	RF remote programming	3

C.f. R 112 of same chapter.

R 143	Real Time Clock	3

C.f. R 113 of same chapter.

R 144	Voltage step-up	3

No, c.f. R77 of same chapter.

R 145	Voltage step-down	3

No, c.f. R77 of same chapter.

R 146	Low-resolution ADC	3

No, c.f. R77 of same chapter.

R 147	LED current sources	3

No, c.f. R77 of same chapter.

R 148	Privacy	4

Specification that need precision: if mean encryption, c.f. C.f. R 78 in same chapter.

Table 39 System and interface requirements

3.2.2 System and interface parameters

Reference	Description	Min	Typ	Max	Unit	Status

Reference	Description	Min	Typ	Max	Unit	Status
P 119	device protocol stack memory footprint (RAM)			5	kBytes	5

If by “device” it means the SoC, 5kBytes will not be enough to cover the complete protocol stacks.

P 120	device protocol stack memory footprint (ROM)			50	kBytes	5

C.f. P 110 in the same chapter: except the boot and possibly some small functions, the software will be placed in big majority in RAM for debug purposes.

P 121	Listen before talk		Yes			5

Taken into account.

P 122	SPI Interface		Yes			5

C.f. R 73 of chapter 3.2.1.

P 123	Memory	64	128	256	kBytes	5

C.f. chapter 2.9.3.

P 124	MCU clock	0.1		10	MHz	3

C.f. chapter 2.9.3.

P 125	MCU consumption		25		µA/MHz	3

C.f. chapter 2.9.3.

P 126	Memory		128		kBytes	5

C.f. chapter 2.9.3.

P 127	MCU clock		10		MHz	5

C.f. chapter 2.9.3.

P 128	Memory	64	128	256	kBytes	5

C.f. chapter 2.9.3.

Reference	Description	Min	Typ	Max	Unit	Status
P 129	MCU clock	0.1		10	MHz	3

C.f. chapter 2.9.3.

P 130	MCU consumption		25		µA/MHz	3

C.f. chapter 2.9.3.

Table 40 System and interface parameters

3.3 Mechanical interface

3.3.1 Mechanical interface requirements

Reference	Requirement	Status
R 149	Size < 25mm² x 1mm	5

Order of magnitude but TBC precisely.

R 150	Size < 150mm^2 x 1mm	4

C.f. R 149 in same chapter.

Table 41 Mechanical interface requirements

3.3.2 Mechanical interface parameters

None.

4 Quality and reliability

This section groups all the items related to the quality aspects

4.1 Quality and reliability requirements

Reference	Requirement	Status
R 151	Reliability (implanted)	5

Specification needing to be stated.

R 152	Link reliability	3

Specification needing to be stated.

R 153	QoS: sensitive to errors	4

Specification needing to be stated.

R 154	QoS: sensitive to latency	3

Specification needing to be stated.

Table 42 Quality and reliability requirements

4.2 Quality and reliability parameters

None.