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NANOTEC
Ecosystems Technology and Design for Nanoelectronics

Coordination Action
Information and Communication Technologies

Deliverable 6.6:
Workshop 4 Results Summarized and Recommendation Report

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Nanotec Project Partners

Partner	Please, give a short description (1-3 sentences) of partners contribution to this deliverable
Chalmers	Contributor
CNRS-LAAS	Contributor
ECN	Organised all the WS4 material in the project web site
EPFL	Responsible for this deliverable
ICN	Contributor
CNRS-IEMN	Contributor
ITE	Contributor
TU-Delft	Contributor
Tyndall	Contributor
VTT	Contributor

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1. About NANO-TEC

1.1. Context

Given the existence of the JU AENEAS and the room for the EU to fund Beyond CMOS research, a community with long-term research interests in nanoelectronics is needed. As the top level importance is to address the design issues in Beyond CMOS as well as to build a bridge between technologies and design or, better still from novel device concepts through technologies, systemability, to design for applications. The JU AENEAS covers the whole of nanoelectronics research, except the Beyond CMOS Domain. Beyond CMOS research is carried out mainly in academic and research organisations. Existing consortia is covering several domains including Beyond CMOS, which lacks visibility in the ERA and in the EU Framework program.

1.2. Objectives and Partners

The NANO-TEC project objective is to identify the next generation of (emerging) device concepts and technologies for ICT; and subsequently to build a joint technology-design community to coordinate research efforts in nano-electronics. NanoTec Project Partners are: Chalmers, CNRS-LAAS, ECN, EPFL, FZ Juelich, ICN, IEMN, ITE, NCSRD/IMEL, TU-Delft, Tyndall, VTT, leading European academic and R&D institutions.

1.3. Activities

The NANO-TEC project partners have organized four subsequent workshops with invited international experts for discussing Beyond CMOS devices, benchmarking and a SWOT analysis of new devices. In parallel, a state-of-the-art web platform for working groups was created for enabling discussion forms, meetings, communications and access to a dedicated information repository. Consequential reports on Emerging Nanoelectronics have been delivered as the result of the workshop discussions.

2. NANO-TEC Workshop 4 Program

Monday, November 5, 2012	
20.00	Welcome reception at Restaurante 1881, Museum of History of Catalunya, Plaza Pau Vila 3, Barcelona
Tuesday, November 6 2012	
08.30-09.00	Registration
09.00-09.10	Welcome address: Carles Cané, National Centre for Microelectronics, CSIC, Barcelona, and member of the GENESIS National Technology Platform
09.10- 09.40	Session 1: Introduction and summary of Workshop 1-3, Clivia Sotomayor Torres, Catalan Institute of Nanotechnology
09.40-10.55	Session 2: Nanoelectronics in EU Horizon 2020 and SRC views Dirk Beernaert, Nanoelectronics in EU Horizon 2020 Victor Zhirnov, SRC views on Nanoelectronics
10.55-11.15	Coffee break
11.15-11.55	Session 3: Technology and Design for devices with charge as state variable Mart Graef, Delft University of Technology, Guilhem Larrieu, CNRS-LAAS
11.55-12.35	Session 4: Technology and Design for devices with non charge state variables Jouni Ahopelto, VTT Technical Research Centre of Finland, Piotr Grabiec, ITE
12.35- 13.15	Session 5: Technology and Design of new computing Paradigms, Dag Winkler, Chalmes University, Sweden Georgios Fagas, University College Cork
13.15-14.30	Lunch
14.30- 15.30	Session 6: Neuromorphic computing as a new computing paradigm, Prof. Dr Simon Thorpe, CNRS
15.30-16.00	Coffee break
16.00-17.30	Parallel working groups in order to collect comments and further recommendations from the workshop participants. Working groups: Technology and Design for devices with charge as state variable Convenor: Mart Graef, Delft University of Technology, Rapporteur: Guilhem Larrieu, CNRS-LAAS

	Technology and Design for devices with non charge state variables Convenor: Jouni Ahopelto, VTT Technical Research Centre of Finland, Rapporteur: Piotr Grabiec, ITE Technology and Design of new computing Paradigms, Convenor: Dag Winkler, Chalmes University, Sweden Rapporteur: Georgios Fagas, University College Cork
20.00	Dinner
Wednesday, November 7, 2012	
09.00-09.45	Report back from the working groups by rapporteurs
09.45-10.45	Session 7: Topological insulators Prof. Dr. Laurens Molenkamp, University of Wuerzburg
10.45-11.15	Coffee Break
11.15-11.45	Session 8: Ecosystem technology Alain Cappy, CNRS, Thomas Swahn, Chalmers University of Technology
11.45-13.00	Session 9: Design-technology integration Panel Discussion: "Design Tools for Beyond CMOS technologies" Chair: Livio Baldi, Micron Technology Inc., Milan; Panelists: Wolfgang Rosenstiel, edacentrum GmbH and University of Tübingen Paolo Lugli, Technical University of Munich Sandip Tiwari, Cornell University, Ithaca Mustafa Badaroglu, IMEC, Leuven
13.00-14.00	Lunch
14.00-14.30	Wrapping up and concluding remarks Clivia Sotomayor Torres, Catalan Institute of Nanotechnology, Barcelona Wladek Grabinski, EPFL, Lausanne
14.30-15.00	Coffee break and end of workshop

3. Session 1: Introduction and summary of Workshop 1-3

Available as a separate document (see ref. 2)

4. Session 2: Micro & nano-electronics in Europe - Step by step to a bright future

Dirk Beernaert, European Commission, DG CONNECT - Adviser for Interdisciplinary and Integrating Activities

(see ref. 3)

Mr. Beernaert introduced EUROPE 2020 (EU2020) initiative as an EU strategy for smart (knowledge and innovation economy), sustainable (greener and competitive economy) and inclusive (high employment, knowledge people and social and territorial cohesion) growth. These elements of local European economics are needed more than ever!
Horizon 2020 (H2020) requires more innovation thru better articulation of the research and innovation, local VC support, involvements of the high-tech SMEs as well as non-traditional actors. H2020 will focus on the societal challenges including health, energy and transport. Having a simplified access for local companies, universities, institutes in all EU countries and beyond, with H2020 being a light, open, fast bottom-up experimentation. An integrated approach involving R&D&I in all KETs, exploring their combinations and interfaces (X-KET, multi-KET), addressing whole the value chain is essential.
The H2020 planning has secured the EU budget proposal of 80 B€ 8,5 % of MFF 2014+ (1083 B€ - 1.1% GNI), and Education and Cohesion Policy: 336B€ (of which large percentage includes innovation). H2020 is a single program going from ideas to the market consolidating FP7, CIP and EIT to focus on following priorities including societal challenges (Health & Ageing, Energy, Transport, Resource Efficiency, Climate Challenge), Industrial Leadership (Leadership in Enabling Technologies (ICT, Nanotechnology materials, Biotechnology, Production Technologies, and others), and Excellent Science (ERC, Marie Curie actions, FETs, Research infrastructures). Creating local European industrial leadership and competitive R&D frameworks in enabling (incl. KET - key enabling technologies) and industrial technologies is essential. The KET recommendations are major input to industrial and regional policy (smart specialisation), competition policy.
Role of the European Institute Technology (EIT) and Joint Research Centre (JRC) in Horizon 2020 has been highlighted by combining research, innovation and training in knowledge and innovation communities as well as providing a robust, evidence base for EU policies. There are following steps: First, adding value from technology diversification; Second: developing small, integrated and smarter components More Moore AND more than Moore; Third: (very) advanced nano-electronics as system enablers and solution providers (energy, functionality, system-technology interaction, and others) including hybridized silicon with molecular switches, ferromagnetic logic, spin devices and sensors in order to enable heterogeneous and morphic system architectures. Integrate-ability, system-ability and manufacturability of novel technology and reliability are key factors; Fourth: multi-disciplinary and system enabling concepts as transversal research and multi-disciplinary cooperation for systems 2020 and beyond. The key actions are integratability, systemability and manufacturability demanding an integrated European industrial strategy on the electronics components developments.
An 'aggressive' RD&I strategies have to go beyond business as usual. The trend of declining market shares have to be reversed. To remain and become a world leader in selected technological areas, Europe should focus on areas of strength. A bold and 'holistic' approach combining policy instruments to support full value chain (R&I&M; More Moore & More than Moore, 200-300-450 mm); complete innovation chain (All TRL's bridge valley of death); using reach critical mass (MS, Smart Specialisation, …); and benefiting on additional policy actions in line with KET approach (state aid, trade,.) to be explored.

One bold initiative: i.e. "airbus for electronics" would eventually bring together micro/nanoelectronics innovation and the application-pull of the system requirements. Such initiative would cover the full value chain from equipment and materials, manufacturing, to designers and system integrators – addressing manufacturing and lead markets, combining research and innovation. Pooling resources to respond to increasing costs of R&D&I –institutionalised PPP (JTI-type) with drastic simplification of the operational model.
Finally, Neelie Kroes (as of 24 May 2012) has been quoted: "Imagine if we built a whole electronics ecosystem right here. Building on the leading technology institutes, and our world-class equipment and materials industry. Connecting the electronics industry with the markets that demand their innovations — public and private, research and industry, small and large business. And connecting with those who can train and supply skilled labour… Are we prepared to set strategic alliances, build value chains in Europe, set R&D priorities and invest further downstream?"

Beyond Moore's Law: SRC Views on Nanoelectronics
Victor V. Zhirnov and Ralph K. Cavin; SRC

(see ref. 4)

Dr. Zhirnov introduced SRC as an industrial collaborative research initiative celebrating 30 Years R&D activities this year. The Semiconductor Research Corporation (SRC) was established in 1982 as a consortium of semiconductor companies to manage high priority university research defining new concepts of “pre-competitive research" and enabling shared R&D resources as well as enhancing interaction with government agencies to focus basic research. Global SRC collaboration model ultimately leading to: the National Technology Roadmap for Semiconductors, transformed into International Technology Roadmap for Semiconductors. It is important to note that ITRS Emerging Research Devices Chapter provides Potential/Risk assessments for the Beyond CMOS solutions. Current technical directions of SRC program entities are Global Research Collaboration (GRC): to address CMOS scaling and scaling independent challenges collectively aimed toward continuing the viability of the current industry; Focus Centre Research Program (FCRP): Addressing technical barriers faced by semiconductor industry to enable execution of ultimate-CMOS while developing linkages to beyond-CMOS; Nanoelectronic Research Initiative (NRI): identification of the next “switch” or “information element” enabling revolutionary new approaches that significantly increase functionality and expand system application space.
Dr. Zhirnov reviewed breakthrough technology challenges for next decades. From fundamental physics it seems likely that the scaling of MOSFET devices will end in the few nanometer regimes. Industry is working with universities to develop replacement technologies; Some brilliant ideas are emerging but there are no evident replacement technologies yet. Are there other models for information processing technologies that offer the promise to sustain Moore’s Law? The speaker suggested that inspiration can be derived from organic systems, i.e., at the intersection of chemistry, biology, and information processing
Dr. Zhirnov discussed a living cell as a general purpose processor. Single-cell living organisms, such as bacteria, have the formal attributes of a Turing Machine, i.e. a machine expressing a program. In fact, the cell can be thought of as von Neumann’s universal constructor, as the cell expresses the output of its information processing on the matter constituting the building blocks of the cell itself computer making computers. In addition, single-cell organisms have been shown to exhibit the ability to learn, the ability to communicate with each other, various complex social behaviour, etc. Experimental estimates of the information content of living cells were made based on microcalorimetric measurements (Experimental estimates are giving 10E11-10E13 bits). It has been concluded that the major consumption of energy during a cell’s reproduction cycle arises from the correct placement of molecules within the cell.
Subsequently In-Silicon versus In-Carbon logic hardware has been discussed. Many proteins in cells have as their primary function the transfer and processing of information are regarded as logic elements of the in-carbon processor. The proportions of components devoted to computational networks increases with

the complexity of the cell, and are absolutely dominant in humans. Proteins can alter their 3D structural shapes (conformation) in response to external stimuli; different conformations can represent different logic states. These nanomechanical changes form a state variable which are conformal. Different nanomechanical conformations of these protein devices are recognized by other elements of the in-carbon cell circuit by a process based on selective affinity of certain biomolecules with given conformational states (e.g. electrostatic attraction).
DNA-inspired memory was other important topic addressed by Dr. Zhirnov. The DNA volumetric memory density far exceeds (1000x) projected ultimate electronic memory densities. It has a potential for very low-energy memory access with the goal to demonstrate a miniaturized, on-chip integrated DNA storage.
In summary, developments of more complex and powerful information processing devices are mandatory. In the same time one has into account that a typical latency time from first publication to first production is more than a decade (about 12 years). Today there are many diffused nanoelectronic endeavours, but one need to drive investments toward most promising approaches. Due to limited global R&D resources, the cost of wrong decisions is high and as consequence it is necessary to develop mechanisms to focus research programs and to filter unlikely technologies, as an example the ITRS ERD provides Potential/Risk assessments for the Beyond CMOS solutions.

5. Session 3: Technology and Design for devices with charge as state variable

Mart Graef, Delft University of Technology,
Guilhem Larrieu, CNRS-LAAS

(see ref. 5)

The ecosystem technology and design-technology integration for Beyond CMOS can be classified into three main groups: Charge-based state variable (Graphene, Nanowire, Molecular Electronic), Non charge-based state variable (MEMS Spintronics) and New computing paradigms (Neuromorphics computing, Quantum computing). These categories have been carefully discussed at the NANO-TEC workshop and then summarized in series presentations, discussions, working group and rapporteur reports. To address recent issues of the scaling limitations of the MOSFET devices due to rapid reduction of the gate oxides thickness (dox) which leads to increased gate leakage; significant reduction of the device channel length (L) allowing only a fraction of the channel charge to be controlled by gate, subsequently threshold voltage (VT) shift, DIBL as well as increased inverse subthreshold slope (S) requires developments of new semiconductor technologies to allow low operation voltage/ low off current (power challenge). New targeted processing should be CMOS/Si platform compatible. Moreover charge-based state variable for beyond CMOS opens new channel architecture/material challenges. From the device architecture perspective new ultra-thin layer (graphene, molecules), 1D (nanowire) can be explored. The material science delivers such new materials as the graphene, molecule and compound semiconductors. Recent developments of the nano-wire-based (NW) transistors with Gate All Around (GAA) are showing their excellent electrostatic control of the gate over the channel. The NW transistors are implemented on single NW with narrow device diameter delivering high drive current (Ion) maintained thru its multi NW architecture. The NW-based transistors are available as horizontal or vertical technology integration. Advanced top-down NWs processing also allow its planar integration i.e. using Hf-based dielectric and TaN metal gates. This significantly improved scaling behaviour compared to planar fully depleted devices making GAA FET – the ultimately scaled devices. Bottom-up NWs processing is an alternative vertical integration allowing direct integration of III-V materials on Si platform. “Catalyst-free / self-catalysed” position-controlled growth and III-V heterostructures are possible. Nanowire density might not be

competitive with top-down in terms of the insulation, contacts, BEOL. High-electron-mobility transistor structures (InGaAs) are development as an alternative. Recent reports are showing greatly enhance the on-state current (Ion) and device transconductance (Gm) keeping good gate controllability. Other option are Junctionless nanowire transistors (JNT), the devices with no junctions and no doping concentration gradients (which are made of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off.). The JNT are offering low off current (Ioff) with bulk conduction i.e. less sensitive to surface roughness. Graphene is also drawing a lot of attention as a new semiconductor material. The graphene is a mono -layer material with very good mobility (up to 200 000 cm^2/Vs at room temperature in vacuum), high saturation velocity (4 x 105 m/s). At device level, it is observed that the mobility is dependent on host substrate as well as on the gate oxide used (charged impurity scattering largely degrade the mobility). Production quality graphene material layers are deposited using CVD which appears as the most promising technique because it is scalable, transferable, is rapidly developing the presence of defects in CVD graphene sheet lead to relatively low mobility values (103 cm^2/Vs). Electrical contacts arising some concerns; contacting graphene device is more difficult than Si device, where one order of magnitude in terms of the accuracy better than silicon is needed to have the graphene-metal ohmic contacts with contact resistance below 100 Ohm um. Also absence of a band gap makes it hard to turn off the graphene based transistors. Nevertheless, BiSFET, tunnel FET are predicted to have very low switching energies, but they have not been demonstrated experimentally. Graphene base transistors (BGT) in vertical structure are under research. More than Moore area should have a higher potential than logic for graphene transistor applications. Optoelectronics, where optical applications range from ITO replacement (absorption 2.3% per layer), through solar cells to lasers; NEMS, low mass and large Young's modulus are promising characteristics for high frequency NEMS as well as Spintronics, using large spin coherence lengths, pure spin currents and large resistance signal for spin-dependent transport in spin-based logic devices.

Molecular device or speaking more generally the molecular electronics offers natural nanometer scale, programmable functionalities activated by light, E-field and temperature, and should be a low-cost technology. Single molecule electronics are on the basic science level and knowledge development is necessary. Self-assembled molecular electronics has some possible application foreseen. Thin-film molecular electronics is most developed domain i.e. such technologies as the plastique electronics (OLED, OFET …) and some technologies and products already commercialized. There are certain issues associated with the molecular electronics. Transistor behaviour has been demonstrated at reasonable drain voltages but the drain current levels are still small, due to the low conductance per molecule, leading to requirement of relatively large devices. Simple logic gates have also been demonstrated with reasonable gain and low switching energy but performance are very low when compared to silicon MOSFET. In a SAMFET, where the SAMs form the channel of the FET, true saturation appears difficult to reach; device electrodes define true dimension and finally the stability at room temperature remains very poor.

Listed above alternative technologies are opening the challenges in design: Design technologies should enable equivalent scaling (high performance, low power, high reliability, low cost, high design productivity). Designs for variability should be addressed too with focus on the low power design (sleep modes, hibernation, clock gating, multi-VDD...) Homogeneous and heterogeneous multicore SoC architectures are a new field to explore as well. For this design factors can be listed as following levels: System Level Integration: bridging the hardware and software codesign gap; system-level architecture and multi-scale technology integration

6. Session 4: Technology and Design for devices with non-charge state variables

Jouni Ahopelto, VTT Technical Research Centre of Finland,
Piotr Grabiec, ITE Warsaw, Poland

(see ref. 6)

Spintronics has already demonstrated the examples of devices and concepts. Current spintronic technologies are among others such as the spin valves, giant magnetoresistance (GMR), Tunnel magnetoresistance (TMR), Memories, HDD (thermally assisted, bit patterned media, 2.5 Tbit/inch2), MRAM concepts. The emerging spintronics topics are in the area of the RF components, Spin Logics, Qubits and Quantum Computing, Spin Hall effects, Topological Insulators, Multiferroics, Spin Thermoelectronics and others. Short term spintronics application places R&D developments in the direction of the RF components i.e. to increase power output. Further demonstration of phase-locking of tens of oscillators needed as well as understanding of nonlinearities. To explore spin logics: material and design develops to improvement of nonlocal devices based on semiconducting and metallic materials; and also magnetization switching with pure spins currents generation. Long term spintronics research would explore more fundamental science and topics related to Spin Hall effects and Topological Insulators: extreme fundamental as well application interest. Focus on materials and device design needed. Spin Thermoelectronics – Fundamental research needed to understand phenomenology. Spin Qubits: Coupling between more than 2 qubits. Limit coherence from nuclei, molecular spin clusters, quantum control improvement, error correction, Application of new materials. All these issues to be addressed in all above should be complemented by the research of the interconnects and connecting nanoscale objects, variability, reliability and temperature stability.
MEMS/NEMS devices are based on the CMOS technology development supplemented by MEMS specific processes. They differ from CMOS by putting the main focus on integrating diverse functions per chip. Nowadays, deep miniaturization and increasing diversity exist in this technology contributing not only to More than Moore but also to the Beyond CMOS domains. The main role of MEMS/NEMS in ICT is seen as integrating functionalities with strong emphasize on applications, however NEMS technology may be used also to fabricate ULP switches with extremely high Ion/Ioff ratio. The use of the third dimension is one of the most important characteristics allowing to: (i) integrate specific functions, (ii) enhance performances, (iii) miniaturize a complete system. Important feature of the MEMS/NEMS devices is also utilization of not only electronic but also other specific properties of the materials: mechanical, chemical, optical etc. NEMS switches with stable, high performance are necessary for relay-based ICs. The on-state contact resistance should be as low as possible with reliability exceeding 1014 on/off cycles. Reliability issues for NEMS switches include permanent stiction (nano-scale physics), contact wear and plastic deformation, and environmental effects. Understanding of contact physics, friction, and wear at the nano-scale is essential for development of active power management, and logic applications. Moving towards More-than-Moore requires additional analysis of deep miniaturization, advanced technology development followed by upgrading of the CAD design and simulation tools to include the nano-scale multi-physics. Complexity (monolithic vs. heterogeneous solutions) must be considered with regard to new, extended functionalities, performance, reliability, volume and cost. Further multidisciplinary fundamental research towards application is needed to explore new materials and new functionalities in MEMS/NEMS devices and systems.

7. Session 5: Technology and Design of new computing Paradigms,

Dag Winkler, Chalmes University, Sweden
Georgios Fagas, University College Cork

(see ref. 7)
A memristive device is a semiconductor device with its conductance to be continuously tuned through the past history of state variables. The neuromorphic computing can be delivered i.e. by memristor. Main

characteristics and examples of devices and concepts for the euromorphic computing are memristor based devices, devices exploring “plasticity”, memristor digital memories, logic and neuromorphic functions for transitions below 10ns with less than 1pJ power consumption. The memristor can operate as Red-OC, phase change memory, in organic as well as purely electronic mode. In the context of Beyond CMOS – memristors can possibly develop further in the robotics area, associative learning and /or efficient image processing. The main Quantum Computation characteristics are resting on principles of quantum nature of states and the quantum coherent state which need of long coherence time. In the context of Beyond CMOS the Quantum Computation offers speed improvements for some problems polynomial while exponential for classical systems. In the same time only special algorithms, e.g., factorization, data base searches can be deployed. In the near future the Quantum Computation focus areas will be among others teleportation, measurement-based feedback and feed-forward, quantum error correction (QEC), simulation of quantum systems. The next 4-5 years may be decisive for the timescales for quantum information processing and reveal a realistic timescale for competitive quantum information processing. A realistic guess is 5-10 years for highly significant applications for simulation of physical models and communication of information. These include a variety of quantum systems: ions, atoms, impurity spins and superconducting circuits. Neuromorphic Computing should also address series of resulting issues: Concerning memristors the material and physical changes required for operation needs to be studied with respect to defect tolerances, reproducibility and the reversibility of the thermodynamic processes involved. At present, for switching functionality, the I-V loops indicate large dissipation. Therefore, local heating, which impacts power consumption, needs to be addressed, as well as co-firing and fan-out and scalability bounds need to be defined. Highly non-linear processes are involved which require an adequate theoretical framework. New architecture concepts will be needed in order to take into account that each memristor-based device will vary and therefore can process information differently. New architecture will also be needed to optimise inter-connectivity at neural level thereby improving the understanding of processes related to learning and transfer of training. The plasticity aspect can probably be tackled also by working on the pulse shape rather than on the material, in order to obtain more states with a controlled potential. For this, active memristors will be needed to test algorithms and their transferability. Memristor types suitable as devices for neuromorphic computing applications need to be identified together with a killer application for memristors to be successful. A possible candidate is pattern recognition based upon a CMOS “neuron” in conjunction with memristor “synapses”. On the classical side, applications may include approaches to solve problems that classical may include efficient simulation of the physics of quantum systems, materials science and biomolecular systems, as well as implementation of extremely sensitive measurement devices and interfaces. As an recommendation future Neuromorphic Computing activities need a cross-disciplinary “super IP” (10-20 MEuro/year during 5 + 5years) is essential as a real R&D project1, not a loosely organised program. Within such a "super-IP", quantum computing and neuromorphic computing should be embedded in digital environments via digital-analogue hardware and software interfaces, in order to create useful hybrid systems. Such a "super IP" should expose the way for important commercial applications in 5-10 years.

8. Session 6: Neuromorphic computing as a new computing paradigm

Prof. Dr Simon Thorpe, CNRS

(see ref. 8)

Biological and Computer Vision can used to simulate the Visual System exploring the classical artificial neural networks as well as spike based computing. Detection, identification and localisation of the objects and events in complex dynamically changing natural environments is a common, elementary problem which for many tasks should solved as fast and as reliably as possible. In the same time the system should

be using the most energy efficient hardware possible within the smallest size and weight IC footprint. The human brain has about 86 billion neurons of which 16 billion in the neocortex and only 4 billion are available for the vision. With an attempt to build and be able to implement brain style computing with conventional computing following questions have to be addressed: How many teraflops does the brain need? How much memory bandwidth? An answer is not direct, and it is depending if we can understand how the brain computes. Classic Neural Computing to simulate the visual system with 4 billion neurons and 10000 connections each having update rate at 1 kHz needs about 40 Petaflops. Temporal coding is an option. The temporal patterning of spikes across neurons is critical for computation. In the classic view ordering of spikes is critical. Assuming that neurons sendfloating point numbers, then the floating point numbers are transformed into spikes trains using a Poisson process. The temporal patterning of spikes across neurons is critical for computation using synchrony, repeating patterns, etc. Spike-Time Dependent Plasticity (STDP) is a solution to explore learning mechanisms and build competitive learning networks. STDP concentrates high synaptic weights on early firing inputs . An inhibitory connection between neurons allows them to function as a competitive learning system in which different neurons will tend to learn different stimuli. Only a small number of presentations may be needed for changes to occur. Moving towards Neuromorphic hardware one should address event representation (AER) coding, spiking retinas, spiking cochlears, memristor based hardware. Recent scientific papers have demonstrated use of the memristor devices to implement STDP in electronics. Memristive technologies broadly developed and include also Nanoparticle-Organic Memory Transistor (NOMFET), Phase Change Memories (PCM, PRAM or PCRAM), Conductive Bridging RAM (CBRAM), Resistive RAM (RRAM or ReRAM).

9. Session 7: Topological insulators

Prof. Dr. Laurens Molenkamp, University of Wuerzburg

(see ref. 13)

Topological insulators (TI) can be divided two dimensional 2D TI i.e. Quantum Spin Hall Effect based in the transport in HgTe quantum wells; and three dimensional 3D TI i.e. topological insulator and surface states as photoemission on BixSb1-x and Bi2 Se3 or transport in strained bulk HgTe materials. Characterized by energy gap, absence of low energy electronic excitations, TI can be distinguished as covalent insulators (e.g. intrinsic semiconductor), atomic insulators (e.g. solid Ar) or the vacuum. Topological band theory gives difference between a conventional insulator and the Quantum Hall State is a topological property of the manifold of occupied states. It has been classified by Chern (or TKNN) integer topological invariant. The TKNN invariant can only change at a phase transition where the energy gap goes to zero. Edge or gapless states must exist at the interface between different topological phases. This approach can actually be generalized to a spin full QHE at zero magnetic fields as in the Quantum Spin Hall Effect. There are two classes of 2D time reversal invariant band structures: Conventional Insulator (Even number of bands crossing Fermi energy) and Topological Insulator (Odd number of bands crossing Fermi energy) The (Hg,Cd)Te compound semiconductors could be used as an example. The HgTe-Quantum Wells has QW band structure derived using the k.p Model. First Observation of QSHI state has been shown using a multi-terminal probes (H-bars). The H-bar experiments showed suppression of the non-local QSHE using long leads or narrow wires, intrinsic metallic SHE only shows up for holes: larger spin-orbit. Further QSHE and iSHE application are spin injectors and detectors.
The 3D topological insulators can be: weak topological insulators (Related to layered 2D QSHI where Miller indices Fermi surface encloses even number of Dirac points) or strong topological insulator (i.e. topological metal: 1/4 graphene Berry's phase Pi). Theory predict Bi1-xSbx as a topological insulator by exploiting inversion symmetry of pure Bi, Sb. The bulk HgTe which is a semimetal can be seen also as a 3-D topological insulator with topological surface state overlaps with its valence band. Superconductor

topological insulator structures which host Majorana Fermions are potential platform for topological quantum computation.
From this point we are facing some challenges in the near future: to understand transport measurements on topological insulators and Superconducting structures; eventually create and detect Majorana bound states and corresponding Magnetic structures to be able creating chiral edge states, chiral Majorana edge states.

10. Session 8: Ecosystem technology

Alain Cappy, CNRS,
Thomas Swahn, Chalmers University of Technology

(see ref. 14)

A critical issue in beyond CMOS research is the availability of advanced technology. At the present the European technology ecosystem has many players. A clear definition of the roles of the respective players is needed in order to avoid non-constructive competition and waste of resources
The ecosystem technology has three main players with different access status: Academia (with an R&D horizon > 6 years, TRL 1-4) – basic understanding, test and validation of innovative architectures, materials and processes for future ICT. Research Institutes (RTOs, Integration Centers with R&D horizon 3–6 years, TRL 3-7) – could lead the technology implementation and the assessment towards Production Equipment; development of high performance components. Industry (with R&D horizon < 3 years, TRL 6-9) – Technology research, innovation and exploitation; Process introduction and continuous improvement with innovative approaches (yield, reliability,…).
Beyond CMOS address medium/long term technologies with the academia and large research institutes as the main players but the active role of local European industry is mandatory. The partners should jointly to contribute to the identification of relevant long-term fundamental research topics needed in the value chain; define expectations for ultimate CMOS technology, applications, and services (> 2015) as well as provide critical feedback to research institutes and academia.
Using the three device categories chosen for NanoTec WS4, we can describe the details the technology state of the art and the needs to push recent technology developments forward to digital with charge as state variable (i.e. new semiconductor transistor (TFET, i-MOS, III-V, nanowire…but also nanomechanical switch). Generally, the demonstration is carried out for a single device or low complexity circuits. To demonstrate better performance than CMOS (at least for one or two parameters), manufacturability is a key question. So the main difficulty is the access to large scale infrastructures (LSI) at reasonable cost. Design is not a problem if the new device can simply replace CMOS. Digital with state variable other than charge (Spin, molecular state….). For this domain, the objective is mainly to demonstrate the possibility to use of a new two state device to make digital circuits. Manufacturability on a semiconductor process line is a key question. Non digital (quantum, neuromorphic). For this domain, the notion of device is not relevant. Completely new technology (self assembly, etc.) can be proposed for which the technology ecosystem is not clear.
Bottom-up and open access approach: several coordinated proposals submitted (Myfab, NorFab, RENATECH, TRAIN2-network etc.) to the EU-open consultation (22 October) to connect small ecosystems (typically small RI, regional networks) to large institutes and industry. Not the complete picture – but the NANO-TEC map of our extended infrastructure network (inclusive approach). European research is strong in beyond CMOS technologies, but the transition from ideas arising from basic research to competitive product is a weak link in European nanoelectronics value chains.
To improve the beyond CMOS technology ecosystem and make a better interconnection the academic facilities should be taking best advantage of European scientific excellence in transforming the ideas

arising from fundamental research into technologies competitive at world level delivering proofs of concept and patents. Other partners representing "Pilot lines" consists of putting in place pilot lines having technology prototyping facilities to enable the fabrication of innovative prototypes. And finally "Industrial facilities" starting from product prototypes duly validated during the demonstration phase to create and maintain in Europe attractive economic.
It would be beneficial for entire Europe organize all the advanced academic technological facilities having a significant activity in beyond CMOS research in a European network with one and only one entry point in each country, each entry point having mission to represent/structure its national facilities. In order to avoid a new structure, it should be useful that this network could be managed by an existing initiative. This network will be complementary to the facilities of the RTO and tightly link to them in order to allow a smooth crossing of the 'valley of death'. Additionally, that Europe should create a multidisciplinary 'Beyond CMOS ' Erasmus Mundus program to educate a new generation of student to future information processing concepts: theory of information, binary and non-binary information processing, quantum computing, neuromophic computing. In the same time, insufficient level of feedback from industry is also a weakness in Europe. It is recommended that industry will define more clearly the expectations for ultimate current technology, future needs and roadmaps of long-term research. This feedback would increase the manpower on research on subjects that are considered as strategic by industry for the long term and avoid dispersion on subjects of minor importance.

11. Session 9: Design-technology integration Panel Discussion: "Design Tools for Beyond CMOS technologies"

Chair: Livio Baldi, Micron Technology Inc., Milan;
Panelists:

Wolfgang Rosenstiel, edacentrum GmbH and University of Tübingen
Paolo Lugli, Technical University of Munich
Sandip Tiwari, Cornell University, Ithaca
Mustafa Badaroglu, IMEC, Leuven

Details are available in a separate document [15].

12. Wrapping up and concluding remarks

Details are available in a separate document.
https://www.fp7-nanotec.eu/content/wrapping-and-concluding-remarks

13. Working Groups Recommendations

Available as separate documents: Charge-based state variables [9]; Non-charge-based state variables [10]; New computing paradigms [11]; Technology Ecosystem [14]; Design Panel [15].

14. Conclusions

The recommendations emerging from this workshop from part of the projects recommendations in D6.7 “Presentation of Main Achievement of the NANO-TEC workshop series” going under the title “Recommendations on beyond CMOS Nanoelectronics Research” for dissemination purposes.

15. References

[1] Presentation of Carles Cane-Welcome Address https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_00_cane.pptx

[2] Presentation of Clivia Sotomayor Torres-Introduction to ws 1 to 3 https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_01_sotomayor-torres_introductions_v1.pptx

[3] Presentation of Dirk Beernaert-Nanoelectronics in EU Horizon 2020 https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_02_beernaert.ppt

[4] Presentation of Victor Zhirnov-SRC views on Nanoelectronics https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_03_zhirnov.pptx

[5] Presentation of Guilhelm Larrieu and Mart Graef-Technology and Design for Devices with Charge as State Variables https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_04_charge_based_state_variable_v3.pptx

[6] Presentation of Jouni Ahopelto and Piotr Grabiec-Technology and Design for Devices with Non Charge as State Variables https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_05_non_charge.pptx

[7] Presentation of Georgios Fargas and Göran Wendin- Technology and Design of New Computing Paradigms https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_06_novel_computing_paradigms_final.pdf

[8] Presentation of S.Thorpe on Neuromorphic Computing https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/barcelona2012nanotec_thorpe.pdf

[9] Slides derived from Feedback of the WG on technologies with charge-based state variable https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_08_charge_feedback_from_wg.pptx

[10] Slides derived from Feedback of the WG on technologies with non-charge-state variables https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_08_charge_feedback_from_wg.pptx

[11] Slides derived from Feedback of the WG on Novel computing paradigms https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_10_paradigms_feedback_from_wg.pptx

[12] Adding remarks by G. Wendin on the discussion/recommendation of novel computing paradigms https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_10a_paradigms_adding_remarks_of_wendin_121107.ppt

[13] Presentation of Molenkamp on Topological Insulators https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/molenkamp_topological_insulators.pdf

[14] Presentation of Tomas Swahn on Ecosystems Technology https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/nano-tec_ws4_12_tech-ecosystem_ac_ts_121107.pptx

[15] Panel Slides of L. Baldi, W. Rosenstiel, M. Badaroglu and S. Tiwari https://www.fp7-nanotec.eu/system/files/_NANO-TEC/ct_presentation/panel.zip