Contract N° 257964

NANOTEC
Ecosystems Technology and Design for Nanoelectronics

Coordination Action
Information and Communication Technologies

Deliverable D 6.2
Report and presentations of workshop 1 available online

Due date of deliverable: M 9
Completion date: M 18

Start date of project: 1 September 2010 Duration: 30 Months

Organisation name of lead contractor for this deliverable: Ecole Politechnique Federale de Lausanne

Approval

WP Leader	☒	**Coordinator**	☒

Project co-funded by the European Commission within the Seventh Framework Programme (2007-2012)		
Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission	
CO	Confidential, only for members of the consortium (including the Commission Services)	

Partner	Please, give a short description (1-3 sentences) of partners contribution to this deliverable
ECN	Set up the functionality to upload and download the workshop presentations on the project platform.
ICN	Gather presentations from speakers, discussant and rapporteurs, upload them online and circulate link for downloading to all workshop attendants. Summarize all inputs into one consolidated report.
All partners	Contribute to the workshop by acting as discussants and/or rapporteurs and providing related-to documentation, such as public presentations and summaries of the discussions undertaken after each talk

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1. Aim of this task

The objective of this task is two-fold: on one hand, all the documentation arising from the workshop, and especially the presentations of the talks delivered, needed to be available to all the attendants of the event to ensure its follow-up and facilitate a consequent exchange of knowledge and a continuum to lead towards workshop 2. Secondly, the identification of most promising device/design concepts made during the workshop needed to result into a consolidated document that would serve as reference material for the nanoelectronics community. The document is annexed to this deliverable.

2. Work done

Right after the workshop ECN set up the functionality that would allow the project manager to upload the presentations of the workshop on the web platform. After gathering all the public versions of the presentations and obtaining written permission to publish them online, the project manager completed this task by the end of January 2011 and circulated the relevant link for downloading to all the workshop attendants. *Figure 1* shows two snapshots of the web pages where the presentations form each session can be downloaded. Moreover, prior to approval from each attendant to publish their name and contact details in a public mailing list, this one was also created, uploaded and circulated among the workshop participants in order to start the community building process of NANO-TEC. Finally, the inputs provided by the rapporteurs of each session were gathered into one document which summarized the whole workshop and made an analysis of the latter. This showed to take longer than expected as it was difficult to engage all rapporteurs to produce written documentation, and also, as clearer guidelines were needed by them in order to produce such summaries. This has been taken into account in the second workshop and is being further improved in the preparation of the third one, where the consortium is planning to organize a set of preliminary guidelines and conversations between the workshop committee, the speakers and the rapporteurs, in order to provide very clear indications on what each summary should include.

Despite the delay in completing the report-based part of this deliverable, the resulting final document is quite a comprehensive one which lays the basis for a newly developed methodology of workshops and related results, such as the one created in NANO-TEC. Also, the high number of downloads from the web, mainly concerning the workshop presentations, shows that the idea of a unique repository for the workshop material is quite effective, as shown in **¡Error! No se encuentra el origen de la referencia.**, where the increasing number of visits and downloads throughout the project lifetime is illustrated.

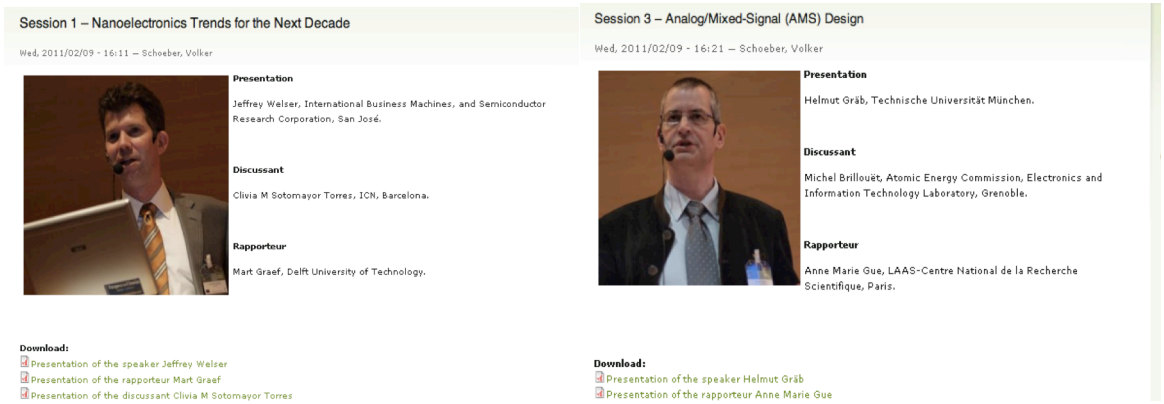

Figure 1: Snapshot of workshop 1 presentations available for downloading online

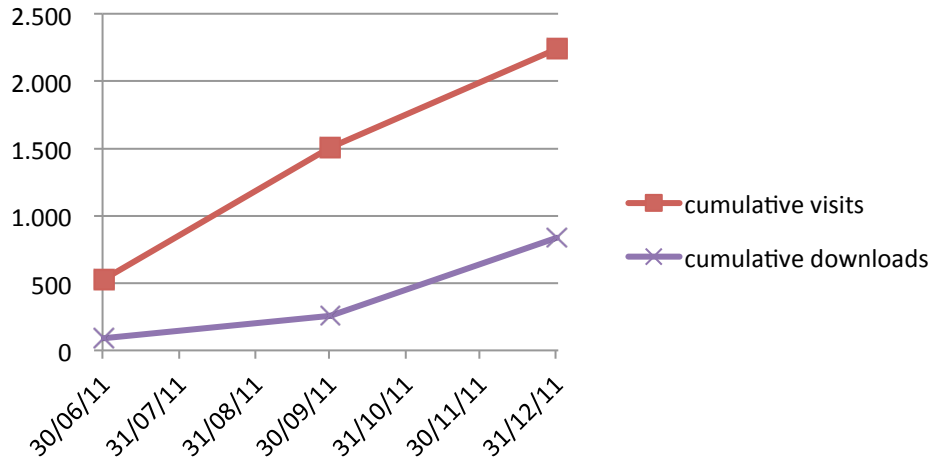

Figure 2. NANO-TEC web traffic

Annex I: Workshop 1 Report

Contract N° 257964

NANO-TEC
Ecosystems Technology and Design for Nanoelectronics

Coordination Action
Information and Communication Technologies

Report on Workshop 1: Identification of the main requirements for future ICT Devices

Submission date: 2.02.2012

Start date of project: 1 September 2010 Duration: 30 Months

Organisation name of lead contractor for this deliverable:
Catalan Institute of Nanotechnology

Revision [ ]

Approval

WP Leader	☒	**Coordinator**	☒

Partner	**Please, give a short description of partners contribution to this deliverable**
ICN	Compiled and edited report
All	Helped to suggest and invite speakers, acted as rapporteurs, discussants, chairs and contributed to a frank discussion.

Project co-funded by the European Commission within the Seventh Framework Programme (2007-2012)		
Dissemination Level		
PU	Public	
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Executive summary

This is the report of the 1st NANO-TEC workshop entitled "Identification of the main requirements for future ICT Devices" held in Granada, Spain from 20 to 21 January 2011 with over 70 participants from academia, research organisations and industry. It was the first of four planned workshops as part of the NANO-TEC project strategy to reach its aim of identifying the next generation of emerging device concepts and technologies.

The project NANO-TEC (Ecosystems Technology and Design for Nanoelectronics) addresses the crucial need to bring closer the technology and design communities to ensure uptake of the most promising emerging nanoelectronic devices and technologies. In the case of the next generation of devices and systems, design and technology go hand in hand in industrial R&D. However, for future generations in nanoelectronics, design and technology are not sufficiently integrated to ensure a fast exploitation in the form of products. The capability of Europe to transfer and exploit research results in nanoelectronics depends strongly on the availability of integrated solutions provided by a joint design and technology community.

This report is a working version of the final deliverable D3.1 which will be the White paper on "Identifying emerging nanoelectronic technology opportunities for application platforms" after discussion and approved by the NANOTEC consortium.

The workshop followed the strategy of first looking at the global nanoelectronics perspective based on a thorough exercise carried out by the NSF and the SRC in 2010 in which senior researchers from the USA, EU and Asia were involved. This was followed by critical presentations on technology addressing carbon- and silicon-based electronics, compound semiconductor based opto- and nano-electronics, spintronics and magneto electronics, molecular electronics and quantum computing. Concerning design, two presentations were given, one on analog mixed design and an overview of the issues needed attention in order to build the bridge between technology and design.

Open and frank discussions were facilitated by a discussant and records kept by a rapporteur for each session. The public versions of the presentations are available in the web site of the project.

Some of the main recommendations arising from the workshop ae:

- Address the cross-cutting issues like *power consumption* as a key factor affecting the uptake of future devices. Others were *manufacturability* and *cost vs. performance*.

- Research in device functionality at the nanoscale needs to be strengthened, simultaneously addressing the increasing need for new architectures and alternative concepts to do computation.

- Concerning *Beyond CMOS design issues*, the following aspects are seen as research needs:
  - Given that a variety of nanodevices can be reliably fabricated from various materials, novel circuits and architectures are going to be needed for a full exploitation of nano components.

- Attention has to be given to open questions concerning the mode of operation of such devices
- In the understanding that modelling and simulation can provide important answers, a multi-scale approach is needed in order to describe realistic systems.

With respect to specific technologies the recommendations are:

- Establish a *non-zero gap graphene-nanoelectronics program* with specific quantitative targets for graphene-based technologies to assess the possibility and test the suitability of fabrication and integration constraints for a combined Si-graphene new ICT technology, beyond sensors and single components.

- Concerning *spintronics*, although some basic concepts are already developed, support for device structure design and for developing disruptive new architectures is urgently needed.

- In the field of *molecular electronics*, the recommendations are to set up target-specific programs to identify the niche areas, the associated design and architecture needs, specifically addressing the interconnect question.

- The time scales of realising *quantum computation* were mentioned in terms of several decades. Here there is still a question concerning the “killer application” as well as specifying the best qubit and the number of qubits needed for a given application, while keeping the cost and power factors in mind.

3. Introduction

In Europe the interaction between the design and the technology research communities working in nanoelectronics, and especially in the Beyond CMOS area, is characterised by a diversity of terminology, modus operandi and the absence of a consensus on main priorities.

In the project NANO-TEC, the relationship between technology and design in nanoelectronics is seen as a mutually dependent two-block partnership. Consider a function of relevance to Beyond CMOS, which comes out of the myriad of possibilities arising from the fast progress in material sciences, coupled to developments in the control of morphology and or the nanostructuring of these materials. A crucial next step is to find a way to link this function to an established, or a new, logic. For this logic to work, ideas on design and architecture are needed. In this basic frame of analysis, design plays a key enabling role in the latter two steps, as well as in the consideration of the way the information-related function, based on the properties of these new materials and (nano) structures, is linked to a logic system.

The 1st NANO-TEC workshop entitled "Identification of the main requirements for future ICT Devices" was held in Granada, Spain from 20 to 21 January 2011 with over 70 participants from academia, research organisations and industry. It was the first of four planned workshops as part of the NANO-TEC project strategy to reach its aim of identifying the next generation of emerging device concepts and technologies.

This report is a working version of the final deliverable D3.1 which will be the White paper on "Identifying emerging nanoelectronic technology opportunities for application platforms" after discussion and approved by the NANOTEC consortium.

Hera a summary of main points, trends, specific discussion points and recommendations are given in each section. The text has been compiled by the rapporteurs, aided by the speaker presentation and the discussant brief presentation. The compilation and editing is the responsibility of the partner ICN.

The workshop followed the strategy of first looking at the global nanoelectronics perspective based on a thorough exercise carried out by the USA National Science Foundation and the Semiconductor Research Council (SRC) in 2010 in which senior researchers from the USA, EU and Asia were involved. This was followed by critical presentations on technology addressing carbon- and silicon-based electronics, compound semiconductor based opto- and nano-electronics, spintronics and magneto electronics, molecular electronics and quantum computing. Concerning design, two presentations were given, one on analog mixed design and an overview of the issues needed attention in order to build the bridge between technology and design.

The discussion on these topics is to be followed up in the 2nd NANO-TEC workshop where a benchmarking exercise is planned.

4. Nanoelectronics Trends for the Next Decade

Speaker: *Jeffrey Welser, IBM, and SRC, Research Triangle Park, NC, USA*
Discussant: *Clivia M Sotomayor Torres, ICN, Barcelona, Spain.*
Rapporteur: *Mart Graef, Delft University of Technology, The Netherlands.*

Jeffrey Welser presented an overview of the anticipated trends in nanoelectronics, partly based on a series workshops held in the USA, Europe and Asia in the course of 2010[1].

4.1. Trends

New device technologies, replacing CMOS will be needed around 2015, when the conventional CMOS architecture will reach its physical limits as critical dimensions become smaller than 20 nm. However, the most important issue in nanoelectronics will be dictated by power consumption constraints, rather than dimensional scaling (miniaturization). Another trend is the emergence of new functional devices, analog, micromechanical, sensing, actuating, etc., which will extend the functional range of digital semiconductor devices. These new functional devices should be capable of heterogeneous integration with CMOS. In particular, the USA Semiconductor Research Council and the Nanoelectronics Research Initiative have identified five research vectors:

- New devices: Devices with alternative state vector.
- New ways to connect devices: Non-charge data transfer.
- New methods for computation: non-equilibrium systems.
- New methods to manage heat: Nanoscale phonon engineering
- New methods of fabrication: Directed self-assembly.

4.2. Goals for 2020

In terms of device research, the quest will be for the development of new memory and logic devices, operating with greatly reduced energy dissipation. Device architectures will focus on emerging non-IT applications, e.g. in the healthcare, mobility, and energy management domains. All these will require the design of sophisticated sensor networks.
Manufacturing technologies for microsystems will achieve 3D near-atomic level control, combining lithography and self-assembly with resolution and control down to 1 nm. It is expected that advances will be essential in tools, chemistries for self-assembly, metrology (in situ, dynamic, non-invasive and in-line) and predictive modelling of materials and interfaces from atomic level up.

4.3. International perspective

Within the European Union, there will be an emphasis on More-than-Moore, i.e., multifunctional, heterogeneously integrated, related microsystems development, supported by basic technology and process research.
South-east Asia and the USA will also enter the More-than-Moore domain, but in these areas priority will be given to device concepts based upon novel state variables, quantum computing and molecular electronics.

4.4. Impact on society

Nanoelectronics will play a major role in addressing most of society's major needs. This is due to the fact that it will be able to provide extremely sophisticated, complex functionalities, implemented in smart compact microsystems at affordable costs. Nanoelectronics will provide components and systems for virtually every application field. Nanoelectronics will take over the role of microelectronics as *the* global economic driver.

[11] The sources of the presentation By Dr Welser were "Nanotechnology Research Direction for Societal Needs in 2020: Retrospective and Outlook", Chapter 8. Applications: Nanoelectronics and Nanomagnetism (J Welser, S Wolf, P Avouris and T Theis, Springer, Boston and Berlin 2010. See also http://www.wtec.org/nano2/; http://nri.src.org and http://www.itrs.net/links/2010ITRS/Home2010.htm

4.5. Discussion

What will be the next paradigm in nanoelectronics?

There is no lack of ideas, e.g. spin torque-based structures, carbon-based devices, quantum effects, out-of-equilibrium principles, but the success of new device concepts will be determined by their capability for heterogeneous integration. The major directions are the following:

- Device nanoscale functionality, which can be viewed as a continuation of 'Moore's Law'.
- New architectures and alternative concepts to do computation, as discussed in other sessions in this workshop.
- Due to the increasing complexity and multifunctionality of microsystems, design, software and architecture will become increasingly important and rate-determining for the development cycle of new technology options.
- Memory and logic device technologies will merge. In general, technology platforms will be developed to serve as generic solutions for a range of different products.

How will semiconductor equipment companies be involved?

At present, the involvement of the semiconductor equipment providers in pursuing the objectives in nanoelectronics seems to be insufficient. It is clear that the solution to many materials-related questions (graphene, nano-wires, etc.) will require collaborative efforts of process equipment suppliers and semiconductor manufacturers.

Is there a perspective for enhanced US/European cooperation on R&D?

Although there are several exchange modalities between US, European (and Asian) players on technology requirements, e.g. in ITRS working groups and INC conferences, programmatic cooperation is still rather limited. Both the American and European cooperative research programs do not exclude participation 'from the other side'. This should be pursued more actively.

Why are quantum information systems high on the agenda of India and the Western Pacific Rim?

These countries do have only limited capabilities to further develop more conventional technology domains, as these are very capital-intensive and require a well-developed industrial infrastructure. Therefore, they rather want to do something new.

5. Carbon-based Electronics

Speaker: *Jeong-Sun Moon, HRL Laboratories LLC, Malibu, CA, USA*
Discussant: *Jouni Ahopelto, VTT, Espoo, Finland*
Rapporteur: *Piotr Grabiec, ITE, Warsaw, Poland*

In his talk Dr Moon gave a comprehensive description of graphene as a new material for future electronics. He presented the unique physical properties of graphene with emphasis on those of fundamental importance for nanoelectronics, such as extremely high mobility, extremely high current density, unique mechanical properties (Young Modulus) comparable to diamond, flexibility, excellent thermal conductivity, among others.

5.1. Zero-gap grapheme and manufacturability

It was suggested that the issue of reproducible and effective techniques to produce good quality graphene layers has been already overcome with chemical vapour deposition (CVD) yielding epitaxial layers when deposited on SiC or SiC/Si substrates, thus promising easier integration of graphene with silicon devices.
Concerning device applications of graphene examples of the already manufactured devices presented. These included MOSFETs, with a record peak FET mobility of 9100 cm2/Vs and record transconductance as well as THz range devices. Furthermore, large area flexible electronics applications of graphene were mentioned as well as RF-NEMS.

5.2. Discussion

Fabrication of graphene.

It has been pointed out, that in spite of the considerable progress in technology, relatively high defect density makes the mono-layer graphene still not adequate for nanoelectronic circuits. Moreover, repeatable fabrication of uniform bi-layers required for band-gap engineered devices will even more difficult.

Comparison between carbon nano-tubes and graphene.

In both cases from the very beginning the new material has been considered as very promising for nanoelectronics, however, in the case of CNT the industrial nanoelectronic applications seem to be rather receding. For graphene perspectives are much more promising due to its much easier handling and better suitability for integration with CMOS.

The zero-band gap of graphene.

A single layer graphene is a zero-band gap material unsuitable for fabrication of nanoelectronic devices (MOS transistors).Band-gap engineering is feasible if a bi-layer graphene is used. Using this approach a narrow band electronic devices may be manufactured allowing for low voltage swing and thus very low power devices. Furthermore, the band gap may be modified using nano-geometry constrictions, interactions with substrate or other layers, e.g. SiC, or through chemical modification (functionalisation). This important issue is still under investigation and a reliable technical approach to allow stable and uniform band-gap engineering is still not clear. However, the combination of more than one approach, e.g. geometry and interaction with

other material, seems to have chances of success. Directly related to the band gap engineering is the problem of moderate or even low I_{on}/I_{off} ratio which may be a limiting factor for future graphene nanoelectronic circuits.

Integration of graphene based devices with silicon CMOS.

Currently, the use of graphene for the fabrication of integrated circuits is considered in the context of interconnect materials and material in which transistors are fabricated. However, in the latter case graphene/silicon integration will be needed because full-graphene devices would most probably not cover all functions required in the circuit. Furthermore, combining silicon and graphene poses a difficult challenge related to integration of the extremely thin graphene layer with components of the silicon IC device structure. The problem then are related to process compatibility, complex 3D topography and, last but not least, to the fabrication of a reliable, stable, low resistance electrical contacts. All these complex issues have to be thoroughly studied and solutions developed.

Graphene as a dominant material in Information Technology

Graphene as a fundamental material upon which an integral technology for Information and Communication Technology can be built is still questionable. Nevertheless, it is generally agreed that ICs based on graphene may find their way into broader nanoelectronic applications, in the More than Moore area, as a material for nanosensors, NEMS, photonic devices (e.g. tuning a transport of an EM waves) and many other. The wide-spread interest of the research community in this new material has led to acive research on similar 2D materials, such as MoS_2, which, may exhibit even more promising device-relevant properties. Thus, a stronger emphasis has to be place on studying fundamental properties of novel 2D materials in relation to interdisciplinary applications.

6. Analog Mixed Design

Speaker: *Helmut Graeb, Technische Universität München, Germany.*
Discussant: *Michel Brillouët, CEA-LETI, Grenoble, France.*
Rapporteur: *Anne Marie Gue, CNRS-LAAS, Toulouse, France.*

During the past ten years, the tremendous progress in nanoelectronics has been closely related to remarkable advances in manufacturing technologies. On the other hand, while design tools have also gained in maturity and performance, the increasing design capabilities still remains a major challenge in order to accompany these rapid evolutions.

5.1 Main issues

The main issues are related to:

- The diversification of devices and the increasing multi-functionality of systems which imposes an increasing variety of designs concerning functions and specifications.
- The process variation, for instance distribution of transistor parameters, which has to be taken into account in order to improve yield.
- The specificity of foundry-dependent processes leading to foundry-dependent design rules.
- The demand of an increasing reliability which requires understanding and modelling of aging effects or stress history of devices

In that context, it turns out that new models and new modelling methodologies are needed in order to predict complex behaviour and design complex devices in an increasingly complex production scheme. It is imperative that models do not become a bottleneck: they should be available and fast.
Identified bottlenecks are the availability and speed of models, the understanding of aging mechanisms and the analysis of yield, the availability of synthesis and optimization tools. General trends are going towards structural modelling with lumped elements, behavioural modelling and hierarchical modelling.

5.2 Priorities

According to this analysis, a prioritized strategy should be adopted to encompass:

- Interactive and semi-automatic Analog/Mixed-Signal design (circuit structure, place and route, yield and reliability).
- Standardized modelling and analysis of physical effects, including aging, and complex performance features.
- Parametric models and simulation of complex AMS blocks.
- Simulators with sensitivity analysis capabilities.
- Enhanced simulation speed.

7. Silicon-Based Electronics

Speaker: *Michel Brillouët, CEA-LETI, Grenoble, France.*
Discussant: *Wieslaw Kuzmicz, Warsaw University of Technology, Poland.*
Rapporteur: *Androula Nassiopoulou, NCSR Demokritos-IMEL, Athens, Greece.*

Si-based Nanoelectronics evolved the last decades through miniaturization that resulted in higher performance devices and circuits, higher integration density, increasing complexity of electronic functions in limited space, minimum weight and cost reduction. Scaling down changed radically digital systems.

7.1. Traditional scaling of a MOSFET

In a MOSFET device a scaling factor of α corresponds to t_{ox}, L and W reduction by 1/α, doping by α, voltage and delay by 1/α, integration density by α^2 and power dissipation per transistor by 1/ α^2. Last years, technology nodes evolved from 90 nm down to 45 nm and then to 22 nm with a reduction in each case of the surface area by a factor of 3. A key enabler towards miniaturization is lithography that evolved from 248 nm laser exposure line down to 193 nm, which is also used for the 32 nm technology node, with a need for a disruptive technology for future generations of lithography technologies (EUV, ML, others?). Resolution enhancement techniques are also investigated with the cost of mask a main bottleneck. Traditional scaling reaches actually its limits: further scaling down does not necessarily involve a performance increase.

7.2. Equivalent scaling of a MOSFET.

A new concept is thus introduced for MOSFET scaling down: the equivalent scaling. The saturation current of a MOSFET is given by: $I_{dsat} \sim \mu \cdot C_{ox} / L_g$, where μ is the semiconductor mobility, C_{ox} the gate oxide capacitance and L_g the gate channel length. New concepts involve: increase of μ (by strain or by introducing new substrate materials), increase of C_{ox} (by introducing high k materials) or decrease of L_g. The decrease of L_g faces actually the problems of a) lithography limits and b) short channel effects. This last bottleneck needs new transistor architectures for better electrostatic control of the current.

7.3. What drives memory technologies?

In a memory cell the need is for multiple stable and noise-immune states which can be modified and read from outside. The factors that drive the progress of a memory cell are:

- *Integration density*: As in digital devices, the need for high integration density holds also for memory devices. The way towards aggressive dimension scaling is the use of the 3rd dimension.
- *Consumption:* In the “read” and “write” states the need is mainly for high speed. In the “stand-by” state the main need is non-volatility.
- *Correction of defective information storage:* A “universal” memory has to be dense, fast, non-volatile, scalable, low power and reliable.

Unlike in the case of a MOSFET, there is no simple device that covers all requirements, but different devices are used for different requirements (dense: DRAM, fast: SRAM, non-volatile:

NAND, NOR). Emerging memory devices are of two types: charge-trapping devices (flash, FeRAM) and resistive devices (PCRAM, MRAM, RRAM, etc).

7.4. Interconnection technology

A major challenge in today's integrated circuit technology is the interconnection technology, the optimisation of which is very complex. The main needs are: high performance, high density, connectivity, reliability and high yield and low cost. In the short term there is no dream for technological breakthrough in the interconnection technology. The dream of optical interconnects does not seem to be a solution in the near future. The effort is thus towards new design and manufacturing solutions.

7.5. Discussion

Physical limits in CMOS scaling down

An important point of discussion is the existence or not of physical limits in electronics technology scaling down. The presenter M. Brillouët cited what R.W. Keyes said in IEEE spectrum in 1969: "I am not convinced that there is such thing as an "ultimate limit". Finding ways to surmount obstacles that, at present, seem to be the limits is what technology is all about".
Different alternative devices to the MOSFET were studied during the last decades. Examples are the resonant tunnelling device ('80s) that was said to allow multi-valued logic and the single electron transistor ('90s) that was said to be the "ultimate" charge-based device. Up to now, there was no convincing demonstration competing with the MOSFET.

The economical challenge

Apart from technology challenges, an important factor towards technology evolution is the economical challenge. With more R&D we have new technologies, new markets and increased revenues. However, the monthly sales/year passed after 1995 from 15-17% the previous years to ≈ 6% in the period 1995-2010. In addition, the technology landscape evolves, involving more product diversity. To microprocessors, memories and images we have to add ASICs, MEMs, power devices etc that concern more dedicated markets. We also pass more and more from the in-house technology to technology outsourcing.
Within the existing diversification of products, each European company has its own product priorities. Their development model is also different: "fablite", "fables", "asset-smart", specialty markets, diversification etc.

Design-Technology interaction

One of the major challenges in the 45 nm technology node and below is **variability**. What's new?

- Circuits are more sensitive to technology characteristics
- CMOS integration development is left to a few companies.
- The foundry – fabless model is dominating the minds of decision makers.
- Major fabless companies.
- Need to know in advance the details of future technologies.
- Intend to drive the technology.

As a consequence of the above, **design-technology interaction is now a must**. However, the way it can happen is not clearly settled.

More Moore versus More than Moore markets

The market share of the More than Moore field to the global electronics market was 21.5% in 2008, including mainly analog ICs, discrete devices, optoelectronic devices and sensors. The forecast for 2010 was 18.8%, with an increasing share of analog devices.
In the More than Moore field there is a wide diversity of new products. There is no established "CMOS like" legacy process or device. This means that there are no guidelines for device evolution and this opens opportunities both in R&D and in companies' involvement, based on economics of differentiated products. The model "1 product – 1 process" is replaced by "1 product = 1 process variation".
In addition, there are some drawbacks:

- In general there is low volume/product or process.
- There is high non-recurrent engineering (NRE) per product, i.e., the development costs is included in the product price..
- There is high entry barrier.
- Process control and yield are difficult.

On the other hand, the positive things are that:

- There is high added value from process optimization.
- We have long-lived products.

There is a need for road maps and standards in the core process that leads to process variations and product engineering.

Roadmapping

Is there a need of road-mapping in the More than Moore field? The necessary preconditions are:

- Figure of merit (FoM)
- Law of expected progress (LEP)
- Wide applicability of technology (WAT)
- Existing community (ECO)
- Willingness to share information (SHR)

An effort already started in this direction in ITRS (with a white paper) and in the CATRENE Scientific Community. However, an exhaustive roadmap for the More than Moore domain is not expected soon.

There is an "application-function-technology" interplay. On one hand the applications, lead markets and societal needs create the need for more functions. In the More Moore field the figure of merit was defined by designs and devices, processes and design tools, while in the More than Moore field the interplay is mainly between applications/lead markets and functions needed.

From the above, the following conclusions can be drawn:

- Be modest in predicting potential futures
- Don't be too pessimistic about microelectronics. Remember Mark Twain (1897) "The rumours of my death have been greatly exaggerated". This holds for CMOS technology.

Beyond CMOS technologies

An alternative technology to CMOS is not yet seen in the horizon. What is needed is not just a new switch. One should not underestimate the real complexity of building an information processing system. Innovation will arise by combining:

- Materials (Physics, chemistry, biology).
- Devices.
- System (Mathematics, etc.).
- And "soft" sciences.

8. Compound Semiconductor Based Micro (Nano) Electronics

Speaker: *William Stanchina, University of Pittsburg, USA.*
Discussant: *Thomas Swahn, Chalmers University of Technology, Gothenburg, Sweden..*
Rapporteur: *Alain Cappy, IEMN-CNRS, Lille, France.*

8.1. Context

Forty years ago, GaAs was projected to replace Si ICs for high speed digital applications while analog (microwave) technology and applications were developed in parallel. The digital GaAs activity stops in late 1980's due to many reasons such as (i) to much power dissipation, (ii) scaling difficulties, (iii) bad yield efficiency, (iv) too expensive technology and (v) the Si world simply out-ran and/or engineered away every challenge. RF and analog technology continued however to develop for some markets as cell phones. Through the 90's, III-V semiconductors other than GaAs gained prominence: InP for optoelectronics such as 10/40 Gbps optical communication systems and GaN that offered potential for 10X improvement over GaAs for μ-wave power applications. In 2000's, GaN technology made significant improvements and yielded viable application while other compounds (e.g. InAs, InSb, etc.) gained in interest and research efforts for higher speed and lower power applications. In the last few years, "Beyond Si" now includes III-V again as a candidate for digital applications: III-V transistor materials and bandgap engineering are being explored within the Si Infrastructure. Lastly, growth of III-V nanonanowires and research into nanowire based device are also explored by many groups worldwide but the interconnection of these nanodevices into useable circuits remains an issue.

8.2. Why III-V compounds?

III-V Compound semiconductors exhibit the highest peak electron velocity which is important for high operating frequency devices. The use of ternary and quaternary compounds and reproducible ways to grow them has led to even better material transport properties and the ability to detect/emit photonic wavelengths from UV through IR. III-V compounds show many possible choices of differing semiconductor bandgaps and band edge alignments. This has led to a variety of useful new "bandgap engineered" devices and quantum well devices with the most prominent to date are the Heterojunction Bipolar Transistors (HBT) and Heterojunction Field Effect Transistors (HFETs, HEMTs, MODFETs …). However, for MOSFET application the low effective mass in the Γ-valley provides high electron velocities but also a low density-of-states and it was mentioned that for small effective oxide thickness, Si beats III-V!

8.3. Discussion

After four decades of Compound Semiconductor technology developments, without a clear technology roadmap, many devices were, and are still, proposed ranging from new concepts to mature, well-characterized ones. Existing and emerging market for e.g. cell phones and solid state Lighting, respectively, all provide an environment and infrastructure support that will be helpful as new III-V technologies and capabilities are explored.

Three main trends can be seen in III-V Compound semiconductor technologies:

- Scaling of dimensions to 10's of nm along with development of new materials for contacts, dielectrics, etc. along with new processes for III-V HBTs and HFETs. There are a variety of III-V heterostructure material choices and variations in device physics employed.
- Compound SC integration in silicon technologies. Two examples: Incorporation of III-V materials synergistically with Si for higher speed n-channel and p-channel MOSFETs, i.e. getting the III-V on the Si and, InGaAs MOSFET with 3.5 nm channel on semi-insulating substrate wafer bonded to Si
- Interest on III-V nanotechnologies (nanowires) such as vertical wrap-gated nanowire transistors. But the questions of single transistor fabrication from each nanowire and interconnection of nanodevices into ICs is still open.

Many workshop participants noticed that III-V compounds have to follows scaling laws, but do not challenge CMOS on the digital playground. III-V's are already integrated with CMOS in systems today and III-V's allow us to facilitate key building block in systems in "widening bottlenecks". Compound-CMOS technologies should be considered as long-term potential only.
Workshop participants agreed that bandgap engineering is a very versatile toolbox for advanced devices which has led to very high speed performance (f_{max} 1 THz) but also very low-power performance when operated at lower speed. It was also emphasized that III-Vs still offers unique possibilities to integrate photonic and electronic functions. This is not new, but it is becoming more doable today. Bandgap engineering also provides high-power efficiency and high-power densities for power amplifiers (e.g. GaN) and, in a much broader view than just 'nanoelectronics', III-V's are playing a more and more important role in lighting, solar cells and power electronics.

8.4. Conclusion

III-V compound semiconductors constitute a vital set of material, especially within More than Moore, which is expected to continue to evolve and play important roles in future systems, due to advantageous properties given by nature and inventive approaches like, e.g., band-gap engineering. Recent nano-scale III-V structures (nanowires) have a potential for new devices bridging the nano-micro technology integration gap.
III-V compounds do not challenge silicon CMOS for digital applications but the incorporation of III-V materials synergistically with Si for higher speed n-channel and p-channel MOSFETs should be considered.

9. Spintronics and Magneto Electronics

Speaker: *Sergio Valenzuela, Catalan Institute for Nanotechnology, Barcelona, Spain*
Discussant: *Paolo Lugli, Technische Universität München, Germany*
Rapporteur: *Christian Pithan, Peter Gründberg Institut, FZ Juelich GmbH, Germany*

9.1. Overview

The presentation gave a comprehensive overview on the field of spintronics related to existing current technologies and presented novel developments focusing especially on effects related to GMR (Giant Magnetoresistance), TMR (Tunnel Magnetoresistance) and devices for MRAM (Magneto-resistive Random Access Memory). The fundamental phenomena associated herewith are understood and are based on the dependence of transmission spin currents depending on the orientation relation of adjacent ferromagnetic layers. In contrast to systems that are based on charge transport, spin dynamics opens the possibility for non-volatile low dissipation memory devices, since charges do not need to be in motion for information transport. Magnetoresistive devices for magnetic sensing and for data storage have been commercialized since quite a long time (Grünberg-patent). Currently, rather large memory-cells based on the "Toogle-RAM"-concept with low leakage currents, reduced dissipation, fast writing- and reading-cycles but requiring large power for writing are discussed. New present developments in the field of MRAM include the spin transfer torque RAM (lithographically refined domains allowing reduced cell dimensions), heat assisted switching RAM (TAS-MRAM where writing is performed at elevated temperatures) or other torque / switching mechanisms, for example using electric fields or exploiting multiferroics. The lecture then communicated the new race track memory concept proposed by IBM, where the magnetic domain structure along a ferromagnetic line is used to store information within a three-dimensional arrangement.

New fundamental physical phenomena and potentially emerging applications in the area of spintronics were presented. Here the transfer between pure scientific aspects and their future technological exploitation still represents an important issue. In addition, new visions based on experimental observations and theoretical expectations of the very recent past were presented. Currently, pure spin currents without charge transfer in integrated circuits are controlled by magnetic fields or spin-polarized charge currents. In the future they might be controlled by electric fields. Intriguing new physical discoveries from which practical possibilities could emerge are for instance RF-applications, spin logics, the spin-Hall effect, the spin-Seebeck effect and quantum computing. The recent advent of topological insulators, which carry non-dissipative spin currents, could lead to a paradigm change. Many encouraging proposals, developments and reports are documented in the scientific literature regarding these new topics, however, new fundamental physics and substantial scientific work is still needed here. At present, real possible applications utilizing these new discoveries are sometime still unclear.

9.2. Discussion

Level of maturity and impact on society

The impact of spintronics in information technology has been tremendous, in particular on magnetic storage. Spintronics is continuously evolving and promises devices that could reduce energy dissipation and that embed both functions, memory and logics, with repercussions in speed and functionality. This promising future is supported by the new fundamental discoveries in the last five years.

Role of contacts and interconnects in spin based devices

Electrical contacts have been a major issue in the progress of spintronics. What happens at interfaces usually determines the performance of a device. There have been major advances on this subject but reaching full understanding still requires great effort. Spin torque effects and the bias dependence of the magnetoresistance in magnetic tunnel junctions are highly influenced by interface properties. Potentially practical phenomena in topological insulator and Rashba spin-

orbit effects in metals are controlled by the surface/interface with other materials. Interconnects would be an issue on spintronics as in current technology but it could be minimized by multifunctional devices. Here, although some basic concepts are already developed, support for device structure design and for developing disruptive new architectures is needed.

Reliability and stability issues

As with any other emerging technology this has to be tackled on a specific application basis. It usually takes up to 10 years for a product to reach consumers after the concept is demonstrated in a research lab. Reliability issues have been solved in Toggle MRAM. For example, there are currently a number of companies that are working on spin-torque MRAM with the aim to reduce the switching currents.

Role of the superparamagnetic limit in the evolution of MRAM and spintronics

Superparamagnetic limits have been pushed using perpendicular recording, artificial antiferromagnets or materials with large perpendicular anisotropy.

Role of molecular spintronics or molecular magnets

The example of the Ferritin molecule was given.

10. The Bridge to Design

Speaker: *Paolo Lugli, Technische Universität München, Germany.*
Discussant: *Danilo Demarchi, Polytechnic University of Turin, Italy*
Rapporteur: *Volker Schoeber, Edacentrum GmbH, Hannover, Germany.*

10.1. Introduction

The presentation of emerging devices with respect to design requirements was separated into two parts. It was explained as a bridge from physical effects to engineering practices. The first part presented multi-scale approaches for nanostructures including possible simulation techniques of nanostructures and organic advanced material together with the principles of cross bar architectures. The second part of the talk gave an introduction in field coupling mechanism in quantum cellular automata including an approach to use these effects for magnetic logic gates.

While emerging devices have very attractive properties the design needed, to enable their use in large scale and in mass production to compete with classic circuit design is a completely different story. He presented the state of the art to handle one of the backbones of circuit design in electronics, which is the ability to simulate the behaviour of switching, storing or transporting information like circuit-based modelling (SPICE), drift-diffusion device simulation (OTFT, MOSFET,HEMT, etc), Monte Carlo device simulation (HEMT, QCL, etc), ab-initio modelling of molecules, NEGF calculation of carrier transport in molecules, or tight binding calculation of electronic properties of nanostructures. Paolo Lugli explained the theory and practical adaptations to use molecules or carbon nanotube transistors (CNT) in conjunction with the approaches to model, simulate or to create transition functions. As a result, he stated that there is the ability to simulate molecular structures and charging effects for a small number of atoms

but it is far away to simulate realistic systems. He presented research results to improve the scalability by using cross bars for memory applications and to show simulation results.

Furthermore he postulated requirements to create crossbar circuit structures:

- The $I_{on}/I_{on(1/2)}$ ratio should be 10^4
- The junction should deliver high currents at low voltage, ideally below 6 V.
- Stability with time (10 years) and to electrical cycling (10^{6-8} for reading, 10^4 for writing)

He also explained physical effects like nonlinearity of the molecule IV characteristics enhances read-out margin and coupling the molecular layer with solid-state diodes enables large-scale circuits. Furthermore, he showed simulated the crossbar performance of ZnO diodes for up to 1 Mbit.
In the second part of the presentation Paolo Luigi presented field-coupled architectures, like single electron transistors, coupled nanoscale magnets and Coulomb-coupled molecules and approaches to use primitive elements to create larger functions like drivers, inverters or majority gates.
He concluded his talk with the following statements:

- A variety of nanodevices can be reliably fabricated from various materials
- Novel circuits and architectures are going to be needed for a full exploitation of nano components
- Several open questions still exist concerning the mode of operation of such devices
- Modelling and simulation can provide important answers
- A multi-scale approach is needed in order to describe realistic systems

10.2. Discussion

The discussion centred on:

- Who will be the future EDA/CAD vendors?
- Can this design software also used for MEMS? Tools will come as need arises.
- Nanomagnets seem to be very interesting, also non-conductive molecules? Molecules are an option for the future.
- Are Carbon nanotubes dead? It depends on the application.
- Accuracy of single electron devices.

11. Molecular Electronics and Quantum Computation

Speaker: *Göran Wendin, Chalmers University of Technology, Gothenburg, Sweden*
Discussant: *Douglas Paul, University of Glasgow, United Kingdom*
Rapporteur: *Dag Winkler, Chalmers University of Technology, Gothenburg, Sweden*

11.1. Introduction

The speaker introduced the topic with a perspective on technological development on time scale. Among the new high performance computing future technologies carbon-based electronics, memristors and oxide electronics quantum coherent electronics and neural/brian networks were rated as being probably feasible within 10 years, while molecular electronics and synaptic molecular electronics/oxide networks were listed as needing a longer time scale.

11.2. Molecular electronics

An overview of the main results of the project “Pico-inside” was presented in the form of a SWOT analysis. Among the strengths, the nanoscale, potentially high device density and the recent experimental proofs of concept of diode and transistors were mentioned. Concerning opportunities the development of self-assembly, and of nano/multi scale technologies from atoms to laboratory scale as well as molecules being most interesting for basic research were highlighted. However, among the weaknesses, the poor reproducibility, the difficulties in wiring and making contacts, the slowness of information processes, the fact that no experimental circuits have been implemented as well as the eventual device size not really being smaller than Si CMOS were listed. Finally the main threat was perceived in terms of this approach had a very small probability of becoming a practical competitive technology.
Other SWOT analysis was discussed in particular for single-logic gates, for molecular thin film memristors, for thin film oxide memristors and for molecular neuromorphic networks.

11.3. Quantum computing

The main quantum device concepts were introduced. The results obtained so far by the project SOLID were presented, which deals with hybrid quantum information processing using solid state qubits.
The main challenges for solid state qubits were identified to be:

- Teleportation
- Error correction
- Simulation of quantum systems

The project SOLID identified some core technologies. One of them revolves around microwave engineering and includes: parametric amplifiers, Josephson metamaterials, microwave photon detection with qubit clusters and propagating quantum microwave fields and qubit clusters. With respect to materials science the challenges listed included:

- Improving coherent times of qubits
- Realisation of epitaxial superconducting and tunnel barrier layers for high Q resonators and phase qubits
- Minimisation of dielectric losses
- Quantum manipulation of individual two-level fluctuators in Josephson qubits
- Theoretical investigations of 2-level fluctuators as quantum resource.

The SWOT analysis showed among the strengths: experimental proofs of concepts, working devices, architectures, logic gates, algorithms and schemes for up scaling. The opportunities

included basic research, quantum few-qubit applications, the development of working technologies, paradigm shift in computing and a quantum internet. The weaknesses were the embryonic status of the research after over 20 years of programmed efforts, the small number of qubits since 50-100 are needed for competitive applications and the huge challenge to up scale. Finally the threats identified included the absence of a killer application and the possibility of quantum computing not becoming a competitive technology.

11.4. Discussion

The following factors were mention as particularly important for both technologies:

- Processor entangled compared to incoherent and classically well behaved
- Processor speed versus the chip area for synchronous clock – when do we loose the phase?
- Cooling per unit area
- Cooling for dissipation or for functionality (energy cost per switching)
- Consumer market vs. supercomputers and servers

11.5. Discussion on Molecular Computing

What are the applications? If memory and logic, are they cheap, dense or work at high speed? What are the functions that conventional electronics cannot do?
Concerning architectures, how big is the departure from conventional CMOS", the level of fault tolerance and the non-volatility of memory functions? How far are we from neural networks or other bio-inspired architectures?
Interconnects and contacts remain a challenge. Can "metallic" conductivity be achieved?
What technology or chemistry will be winner, organic, inorganic, biological?

Suggested benchmarks for molecular computing.

- Do we need different benchmarks for different applications?
- Performance (speed and bandwidth)
- Power
- Manufacturability (scalabilty, yields, etc). DO molecules increase or decrease variability?
- Cost
- Functions that can be performed that conventional CMOS cannot do.

11.6. Discussion on Quantum Computing

Whereas in quantum communications the technology demonstrated and maturing, there are full demonstrator systems undergoing testing and there is a clear application and (niche) market. In quantum computing the situation is less mature.
Concerning quantum information processing:

- What is the "killer application and market driver? Quantum simulator, database searching, encryption factoring?
- How many qubits are needed for each application? 20, 30?
- How scalable are the competing technologies?
- What is the cost? What is the "best qubit"

Benchmarks suggested for quantum computing

- Di Vincenzo guidelines but need comparison with other technologies.
- Number of qubits

- Performance (scale of problems that can be solved?)
- Cost
- Total system power (i.e. cryogenics, control lasers, etc…)
- Market size for applications (business case to develop?).

12. Recommendations

- General recommendations came out of Workshop 1 cutting across all technologies, which not surprisingly included issues like *power consumption* as a key factor affecting the uptake of future devices. Others were *manufacturability* and *cost vs. performance*.

- In general it was felt that research in device functionality at the nanoscale needs to be strengthened, while simultaneously addressing the increasing need for new architectures and alternative concepts to do computation.

- In the area of heterogeneous integration involving nanoscale devices, it is recommended to implement a more structured cooperative *interdisciplinary research* in nanoelectronics with the Americas and Asia, with a focus on applications as the main driver.

- It is recommended to address *design challenges in the More than Moore* area including:
  - Standardized interactive and semi-automatic Analog/Mixed-Signal design based on modelling and analysis of physical effects, including aging, and complex performance features.
  - Inclusion of parametric models and simulation of complex Analog/Mixed-Signal blocks using fast simulators with sensitivity analysis capabilities.

- In particular, concerning *Beyond CMOS design issues*, the following aspects are seen as research needs:
  - Given that a variety of nanodevices can be reliably fabricated from various materials, novel circuits and architectures are going to be needed for a full exploitation of nano components.
  - Attention has to be given to several open questions concerning the mode of operation of such devices
  - In the understanding that modelling and simulation can provide important answers, a multi-scale approach is needed in order to describe realistic systems.

With respect to specific technologies the recommendations are:

- Establish a *non-zero gap graphene-nanoelectronic program* with specific quantitative targets for graphene-based technologies to assess the possibility and test the suitability of fabrication and integration constraints for a combined Si-graphene new ICT technology, beyond sensors and single components.

- III-V compounds do not challenge silicon CMOS for digital applications but the incorporation of III-V materials synergistically with Si for *higher speed n-channel and p-channel MOSFETs* should be considered.

- Concerning *spintronics*, although some basic concepts are already developed, support for device structure design and for developing disruptive new architectures is urgently needed.

- In the field of *molecular electronics*, the recommendations are to set up target-specific programs to identify the niche areas, the specific design and architecture needs, specifically addressing the interconnect question.

- The time scales of realising *quantum computation* were mentioned in terms of several decades. Here there is still a question concerning the “killer application” as well as specifying the best qubit and the number of qubits needed for a given application, while keeping the cost and power factors in mind.