Collaborative project*

Project acronym: SNM

Project full title: "**Single Nanometer Manufacturing for beyond CMOS devices**"

Grant agreement no: 318804

Deliverable: D10.9 ("Report: "More-than-Moore" / beyond CMOS device demonstrator fabricated by SNM integrated process flow")

Name of the coordinating person: Prof. Dr. Ivo W. Rangelow, Email: ivo.rangelow@tu-ilmenau.de

List of participants:

Participant no.	Participant organisation name	Part. short name	Activity Type	Country
1 (Co)	Technische Universität Ilmenau	**TUIL**	HER	Germany
2	EV Group E. Thallner GmbH	**EVG**	IND; End-user	Austria
3	IMEC	**IMEC**	RES	Belgium
4	Mikrosistemi Ltd	**µS**	SME; End-User	Bulgaria
5	Universität Bayreuth	**UBT**	HER	Germany
6	Technische Universiteit Delft	**TUD**	HER	Netherlands
7	Spanish National Research Council	**CSIC**	RES	Spain
8	IBM Research GmbH	**IBM**	IND; End-user	Switzerland
9	École polytechnique fédérale de Lausanne	**EPFL**	HER	Switzerland
10	SwissLitho AG	**SL**	SME; End-User	Switzerland
11	Oxford Instruments Nanotechnology Tools Ltd	**OINT**	IND; End-user	UK
12	Imperial College London	**IMPERIAL**	HER	UK
13	The Open University	**OU**	HER	UK
14	Oxford Scientific Consultants Ltd	**OSC**	SME	UK
15	VSL Dutch Metrology Institute	**VSL**	IND	Netherlands
16	University of Liverpool	**ULIV**	HER	UK

<table>
<tr><td colspan="6">SNM
Work Package 10
Deliverable: D10.9 (“Report: “More-than-Moore” / beyond CMOS device demonstrator fabricated by SNM integrated process flow”)</td></tr>
<tr><td>Lead beneficiary number</td><td>2 EVG</td><td>Nature</td><td>D</td><td>Dissemination level</td><td>CO</td></tr>
<tr><td>Estimated Person-months</td><td colspan="5">12</td></tr>
<tr><td>Person-months by partner for the Deliverable</td><td colspan="5"><table><tr><td>OINT</td><td>EVG</td><td>IMEC</td><td>TUIL</td></tr><tr><td>1</td><td>3</td><td>6</td><td>5.4</td></tr></table></td></tr>
<tr><td>Estimated Delivery Date</td><td colspan="2">M48: 12/2016</td><td>Delivery Date</td><td colspan="2">27/03/2017</td></tr>
<tr><td>Author</td><td colspan="5">• Thomas Glinsner / EVG</td></tr>
<tr><td>Reviewed by:</td><td colspan="5">• WP10 Leader: Thomas Glinsner
• WPG4 Leader: Thomas Glinsner
• Coordinator: Ivo W. Rangelow</td></tr>
<tr><td rowspan="2">Criteria and Achieved Results</td><td colspan="3">Criteria</td><td colspan="2">Achieved result</td></tr>
<tr><td colspan="3">Demonstrating that More-than-Moore or beyond CMOS devices can be patterned with the SNM defined integrated process flow.</td><td colspan="2">SET devices were fabricated by FE-SPL which were used as masters for UV-NIL based nanoimprint lithography. High quality imprinted samples could be obtained.</td></tr>
</table>

Description of the Deliverable	**Executive Summary** This deliverable focuses on the strength of field-emission scanning probe lithography (FE-SPL) as a high resolution patterning technique in combination with UV-based nanoimprint lithography (UV-NIL) for a replication of such structures in a high throughput mode. Beyond CMOS devices, in particular single electron transistors (SETs) were fabricated by TUIL and used as masters for UV-based nanoimprint lithography at EVG. The imprinted samples as well as the original masters were measured at TUIL by using atomic force microscopy (AFM) and sent to IMEC for pattern transfer into silicon. For the majority of the samples the mean difference between channel widths of the master template compared to the replicas is approx. 10 nm. This variation can be caused by the positioning deviations of the section line and the extraction errors of the channel width (determination of 90% height). The deviation of line width of replicas compared to the master template is in the same range of 10 nm. Pattern transfer of the imprinted resist was performed using a three-step process, including a N_2-H_2 descum for residual layer removal, a SiO_2 breakthrough base on CF_4, and finally a SF_6/CF_4/N_2-based plasma for Si etch, leading to a 1:1 high fidelity transfer into Si for the smallest channel width.
Explanation of Differences between Estimation and Realization	NIL replication worked well in general. Line width, pitch and line depth are well reproduced. Replication of sample 5 exhibits some defects. This could be caused by pattern collapse on the stamp due to large aspect ratios (2:1 up to 5:1). Due to the complexity of the SET patterning and NIL optimization, samples for pattern transfer were delivered to IMEC on March 6th, 2017, giving limited time for pattern transfer optimization. The sum of the needed PM exceeds the estimation due to the complexity of the process chain which revealed some difficulties which were not anticipated.
Metrology comments	AFM TUIL: AFM topographic measurements were done by our home-built FE-SPL technology platform (WP1) employing the AM-AFM imaging mode. Active cantilever with a Si tips with tip radii of curvature ranging between 7.5-10 nm were applied. The system was calibrated by a home-made calibration sample. The traceability is ensured by calibration of the sample via the Nanopositioning and Measurement Machine of TUIL (http://www.sios.de/produkte/nanopositionier-und-

	nanomessmaschine/). SEM TUIL: SEM imaging was done by a FEI DualBeam Helios Nanolab 600i system. Calibration was done by reference samples provided and calibrated by the supplier of the system (FEI).

1. Introduction

The aim of this study was to verify the applicability of master templates fabricated at TUIL by FE-SPL and cryogenic plasma etching for UV-NIL. The focus was placed on replication of beyond-CMOS devices, in particular of single electron transistor (SET) layouts. Here, the layouts patterned by using FE-SPL (ref. WP1) have been already verified (D8.4). Room-temperature operating single electron transistor devices (ref. WP8) have revealed effective dot sizes of less than 2 nm (D8.5). In this context, the replication of this kind of devices by using UV-NIL is significantly enhancing the throughput capability. The demonstrated process flow integrates the complete nano-manufacturing chain starting from NIL master template patterning (FE-SPL, TUIL), pattern transfer for NIL master template fabrication (cryogenic plasma etching, TUIL), UV-NIL (EVG) as well as the pattern transfer of the replicas (Imec).

2. Master template fabrication (FE-SPL and cryoetching)

Two types of master templates were prepared by TUIL. The first type of samples contains simple test structures, which were intended to evaluate the resolution and general applicability of NIL master templates fabricated by the novel process chain (FE-SPL + cryogenic plasma etching). As substrate standard Si samples, p-doped with a total chip size of 1x1 cm² were applied. A 15 nm thick calixarene molecular glass resist was spin-coated on top, followed by exposure using FE-SPL (ref. WP1). The test layout includes meander lines of various pitch as well as dot structures. Arrays of features with different exposure doses were patterned resulting in a variation of characteristic patterning dimensions (width / diameter). The features were transferred by cryogenic plasma etching using SF6/O2 chemistry at -120°C. After plasma strip the master templates were characterized by AFM and SEM.

The second type of samples contains only SET layouts comparable to that ones, which have shown room temperature operation capability (Ref. WP8, D8.5). FD-SOI (12 nm top layer, 25 nm Box) chips with a size of 1.5x1.5 cm² were applied. For definition of the layout a mix & match approach was applied. In this context, contact pads as well as an active area for FE-SPL patterning were defined by optical lithography & standard reactive ion etching (RIE). Afterwards, FE-SPL and cryogenic plasma etching were applied for definition of all small scale features. 15 nm calixarene molecular glass resist was used. After resist strip the final features were characterized by AFM and scanning electron microscopy (SEM).

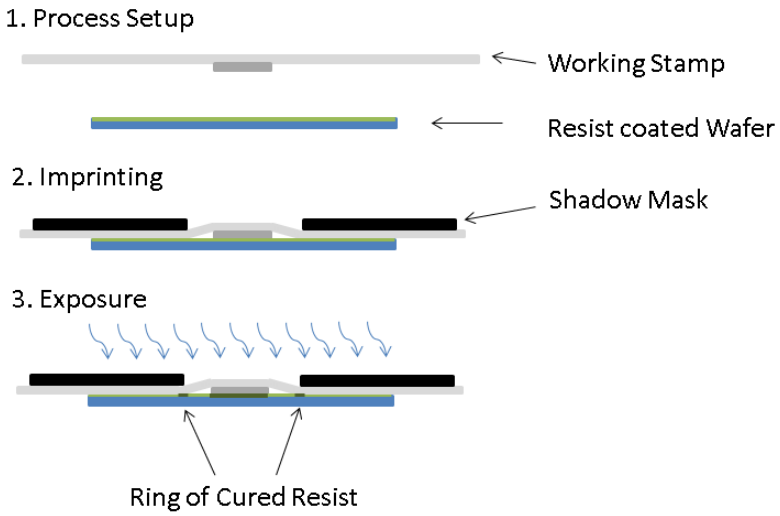
3. Imprinting process flow (single-step UV-NIL)

Both types of master templates were sent to EVG for replication by NIL. Replicas of three samples were sent back to TUIL for AFM measurements:

Sample Number	Features	Number of replica
2	SET	10
3, 5	Test structures	1 of each sample

After AFM analysis, replicas of sample 2 (10 imprinted wafer samples) were sent to IMEC for pattern transfer and final characterization.

An anti-sticking layer was applied on the master before working stamp (WS) fabrication started. The WS resist was spin coated on the master and transferred to a polymer backplane by applying the SmartNIL™ process and exposure. Replication was performed on 4 inch silicon wafer after adhesion promotor application by spin coating and subsequent baking. EVG NIL resist UV/A 1.2 µm (for samples 3+5) or EVG NIL UV/A 25 nm (for samples 1+2) was applied by spin coating. A SmartNIL™ process was carried out on the resist coated wafer. The overall process flow applied for the small masters is illustrated in the following figure:



In order to prevent resist at the surrounding area of the pattern of interest a shadow mask was used, which resulted in a small cured resist ring around the active imprinted area.

4. Measurements of the master template and comparison to their replicas (AFM, SEM)

1.1. Sample 3 (Test structure sample including meander lines with varying pitch)

Exposed features on sample 3 are raised; i.e. the defined pattern has an elevated height compared to the surrounding. 9 nm calixarene resist was used. For pattern transfer into the bottom Si layer the negative tone pattern was used (the exposed and thus crosslinked resist stays on the sample and protects the silicon).

In figure 1.1 the entire pattern contained on sample 3 is shown for the master and its replica, followed by zoom-in of chosen parts of the pattern.

Fig. 1.1 (a) SEM image of pattern on master sample 3

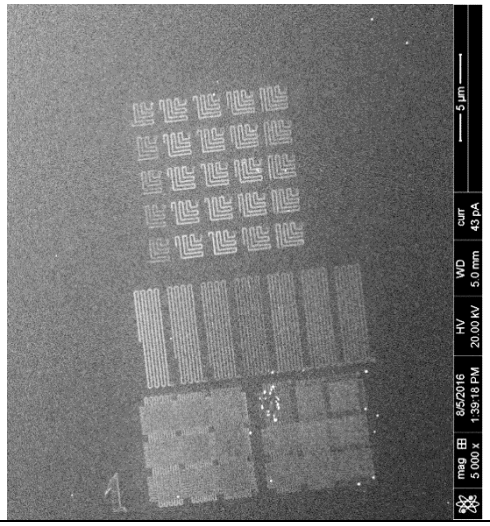


Fig. 1.1 (b) AFM image of replica, same pattern as in *(a)*

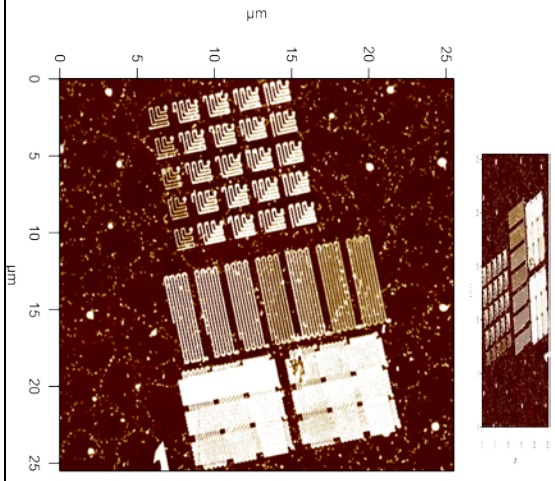


Fig. 1.1 (c) AFM image of master, close-up on part of pattern in *(a)*

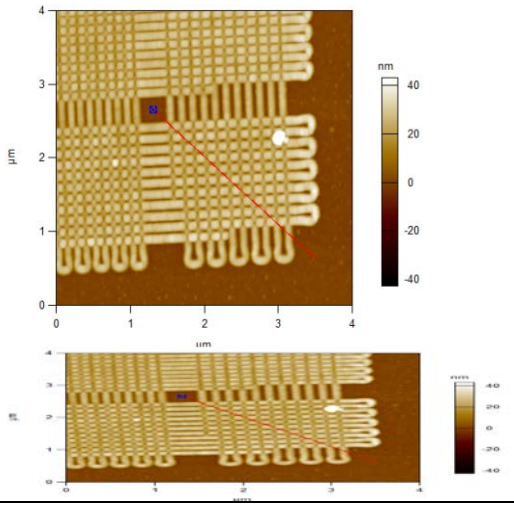


Fig. 1.1 (d) AFM image of replica, similar pattern as in *(c)*

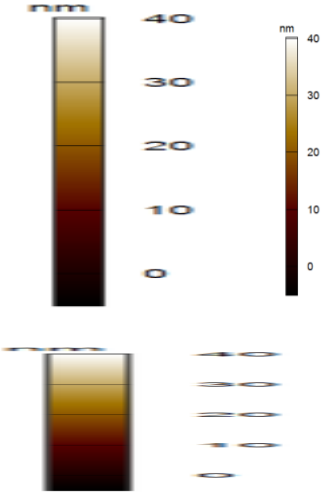


Fig. 1.1 (e) AFM image on master, close-up on part of pattern in *(a)*

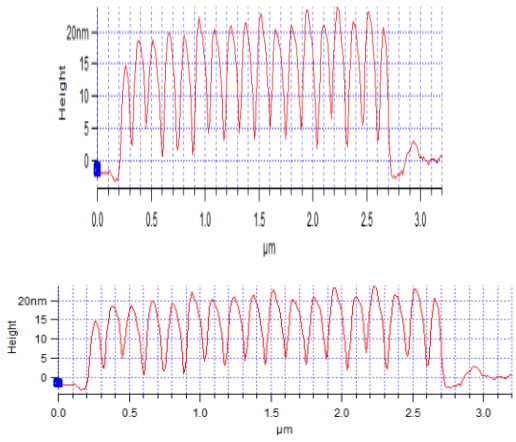
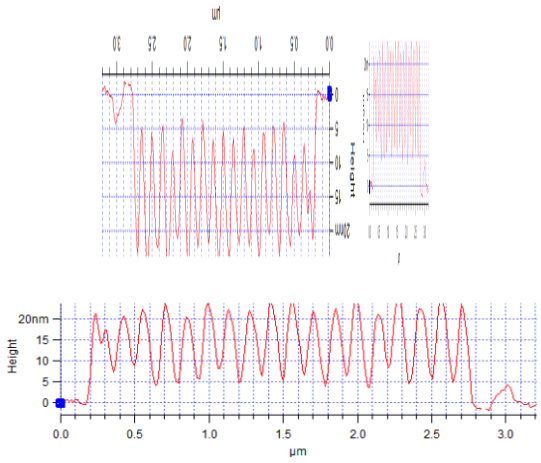


Fig. 1.1 (f) AFM image of replica, similar pattern as in *(e)*



As can be seen the replication of the pattern worked well, i.e. all structures are reproduced at the replica without obvious defects. In particular, profiles are comparable, as shown in the next figure, for meandering lines of different height. Here, the height of the original sample and the replica is similar as well as the pitch (distance between two peaks of one line and between lines), summarized in fig. 1.2.

Fig. 1.2 (a) AFM image on master

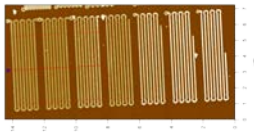


Fig. 1.2 (b) extracted profile, as shown in *(a)*
h1=17.8±0.6nm pitch=57nm h2=20.5±1.0nm

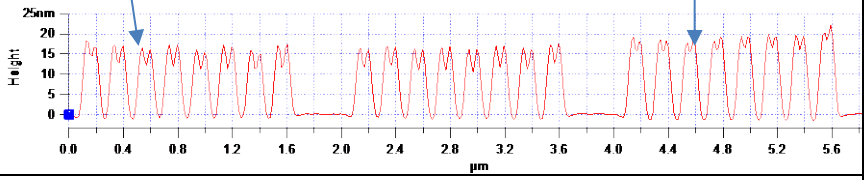


Fig. 1.2 (c) AFM image of replica, pattern as in (a)

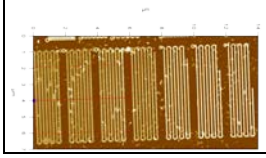
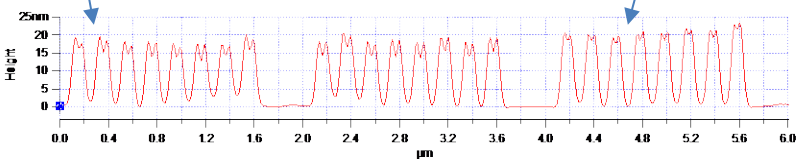


Fig. 1.2 (d) extracted profile, as indicated in *(c)* by red lines
h1=16.9±1.3nm pitch=55nm h2=20.48±1.2nm



Finally, a comparison of the master before and after imprint was done in order to evaluate changes of the master induced by the imprinting process. As can be seen in fig. 1.3, patterns are similar before and after imprint. However, some residual resist is left (visible in black). Overall, the master was not significantly changed in the imprint process.

Fig. 1.3 (a) SEM image of master before imprint

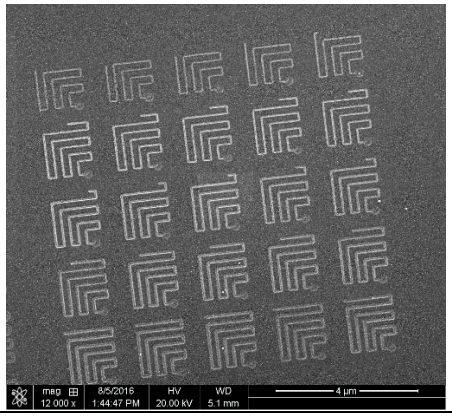


Fig. 1.3 (b) SEM image of master after imprint

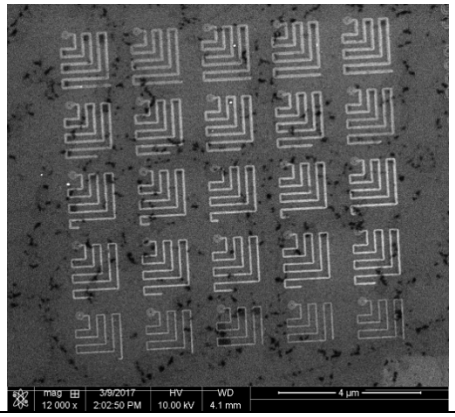


Fig. 1.3 (c) SEM image zoomed on meandering lines on master before imprint

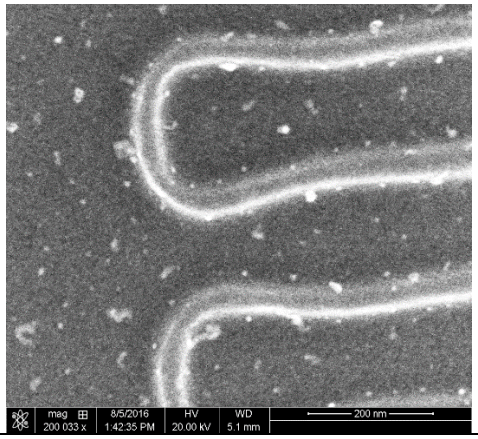


Fig. 1.3 (d) SEM image zoomed on meandering lines after imprint

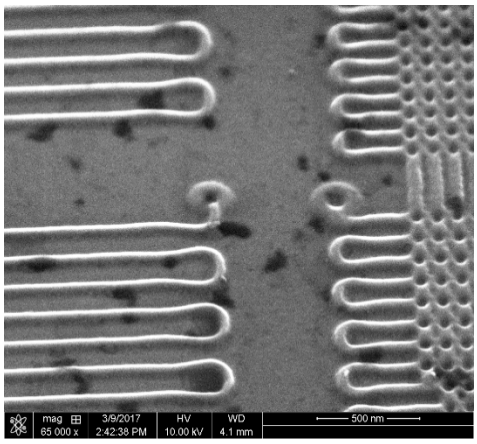


Fig. 1.3 (e) AFM image of master before imprint, zoom on square pattern

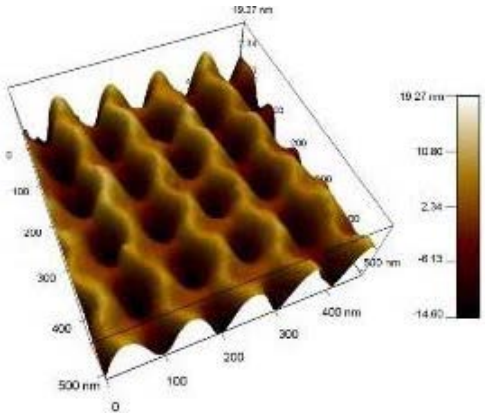
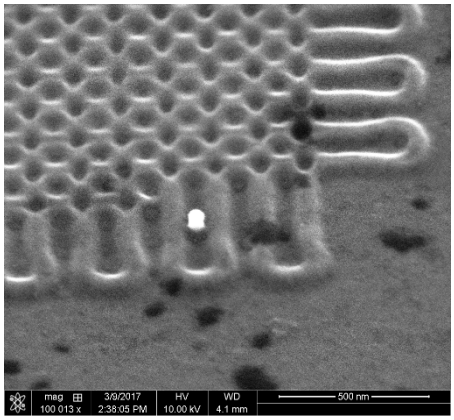


Fig. 1.3 (f) SEM image on master after imprint, same pattern as in *(e)*



1.2. Sample 5 (Test structure sample including dot features)

Samples 5 is patterned in positive tone, thus the transferred pattern has lower heights compared to the surrounding. UBT8-C60 molecular glass resist with a thickness of 10 nm, prepared by UBT (WP5), was applied. An overview as well as close-ups of different patterns of sample 5 comparing master and replica is summarized in Figure 2.1. The depth as well as width (line width) of the patterns of master and replica are similar, ref fig. 2.1 (b) - (f). However, parts of the pattern are not transferred completely, as revealed by fig. 2.1 (a) and (b) [within the center part of the pattern not all dots/squares are reproduced] and fig. 2.1 (h) [in replica lines are connected, which were separate in the master template fig. 2.1 (d)].

Fig. 2.1 (a) AFM image of master template

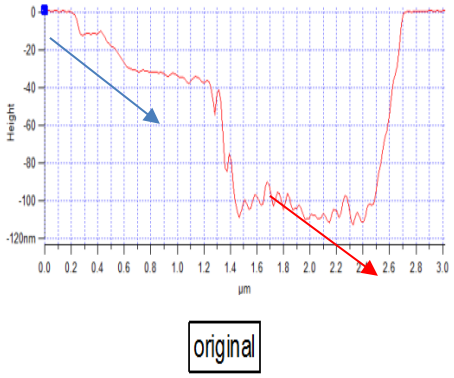


Fig. 2.1 (b) AFM image of replica

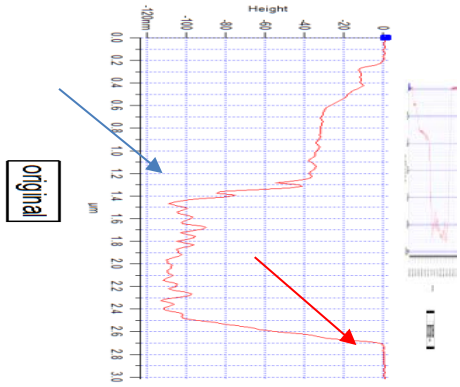


Fig. 2.1 (c) AFM profile, marked in *(a)* by a blue arrow

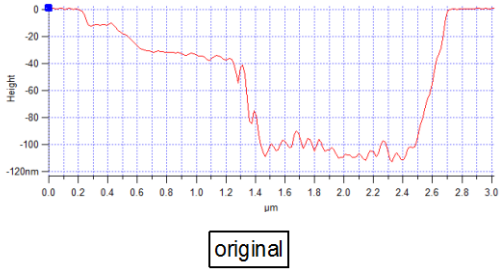


Fig. 2.1 (d) AFM profile, marked in *(b)* by a blue arrow

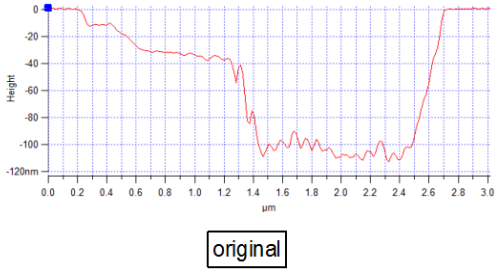


Fig. 2.1 (e) AFM profile, marked in *(a)* by a red arrow

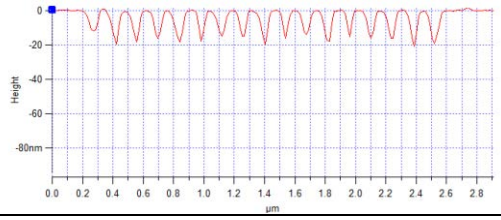


Fig. 2.1 (f) AFM profile, marked in *(b)* by a red arrow

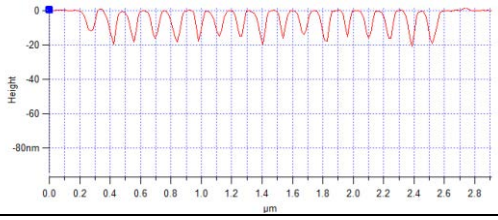


Fig. 2.1 (g) AFM image of meandering lines of master with extracted profile

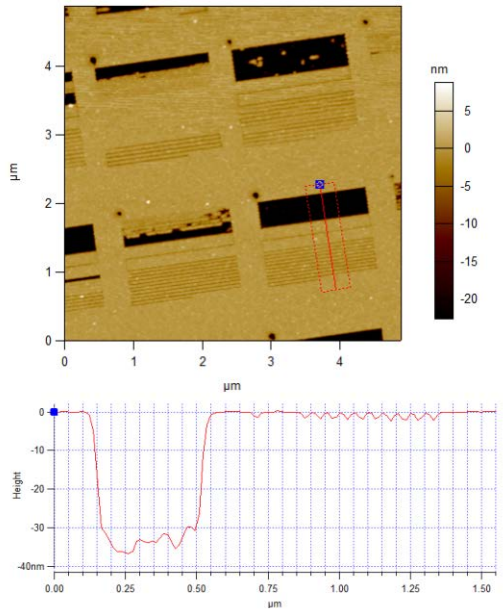
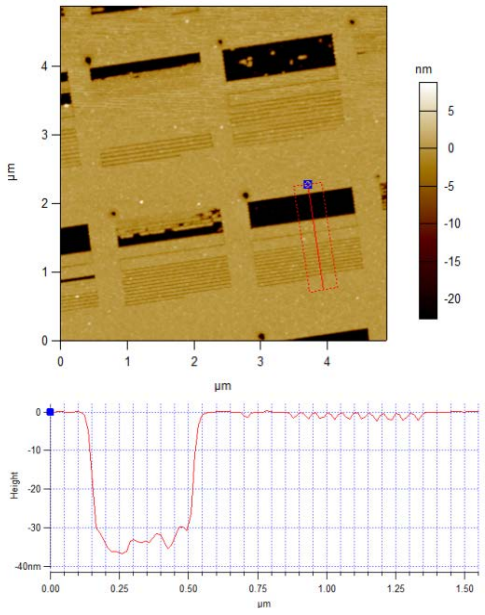
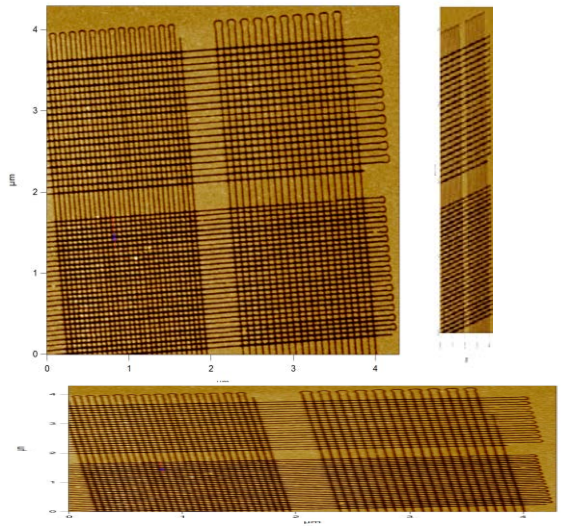


Fig. 2.1 (h) AFM image of replica, same pattern in *(g)* with extracted profile



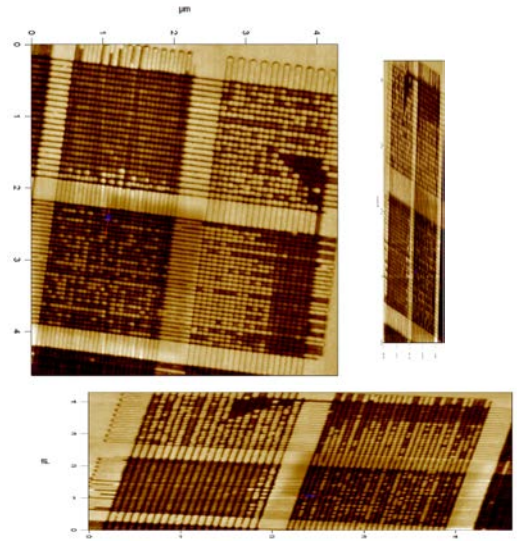
The parts of the patterns, which were replicated, exhibit a similar pitch and line width as the master, summarized in fig. 2.2.

Fig. 2.2 (a) AFM image of master template, showing dot/square-like pattern



Measurement result:
Pitch1: 60±3 nm, line width1: 40±3 nm
Pitch2: 81±2 nm, line width1: 38±2 nm

Fig. 2.2 (b) AFM image of replica, showing the same pattern as in *(a)*



Measurement result:
Pitch1: 60±4 nm, line width1: 39±4 nm
Pitch2: 80±5 nm, line width2: 51±3 nm

The partial problems of NIL replication could be caused by an erosion of the patterns on the master or a collapse of the patterns on the stamp used for fabrication of the replica. Thus, the patterns on the master were measured again after imprint. As can be seen in fig. 2.3, in comparison to the patterns before imprint the master template is not modified by the imprinting process. The SEM images of the tilted master reveal an etching profile exhibiting a slight sidewall bowing. This could be a possible cause why parts of the pattern could not be replicated by NIL. However, also the larger structures, which do not exhibit a (visible) side wall bowing [fig. 2.3 (d)], are not replicated completely [see fig. 2.2 (b)].

A pattern collapse on the stamp seems probable, in particular, since the pattern height is approx. 100 nm resulting in aspect ratios ranging from 2:1 (dots and squares) to 5:1 (meandering lines).

Fig. 2.3 (a) SEM image of master before NIL, same pattern as in *Fig. 2.2 (a)*

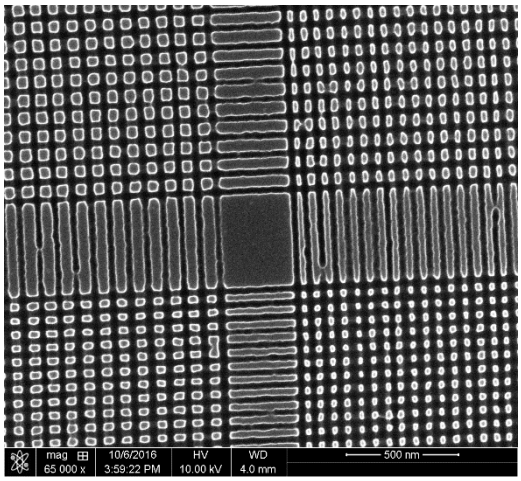


Fig. 2.3 (b) SEM image of master after NIL, same pattern as in *Fig. 2.2 (a)*

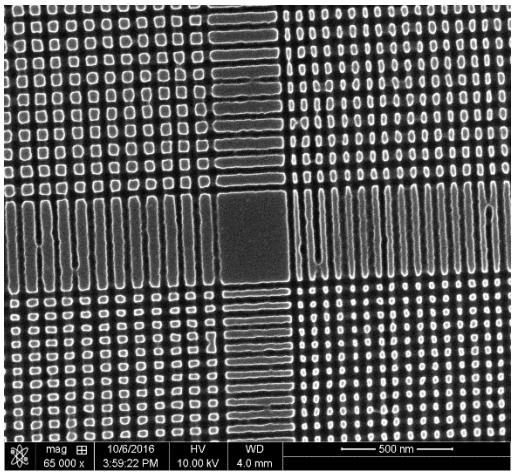
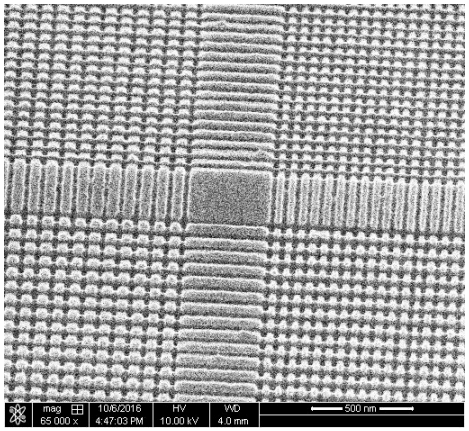
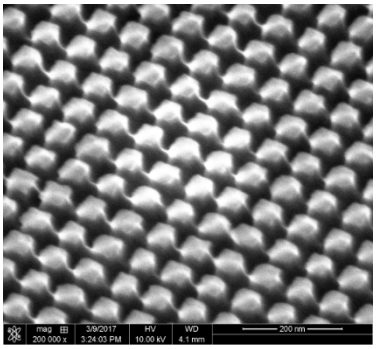
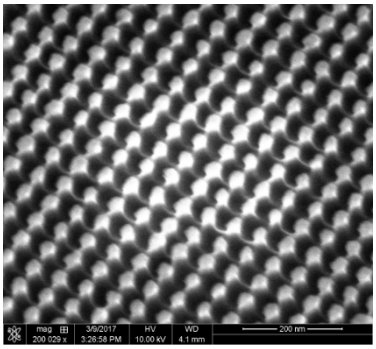
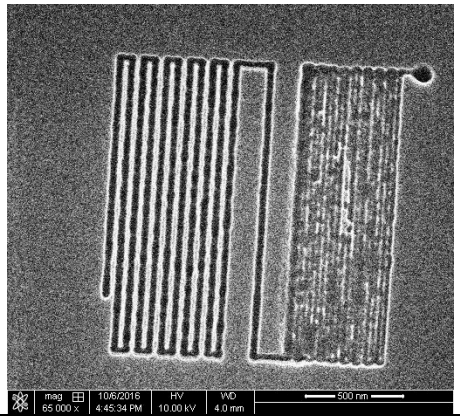
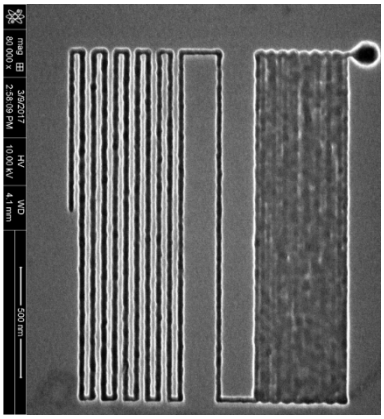


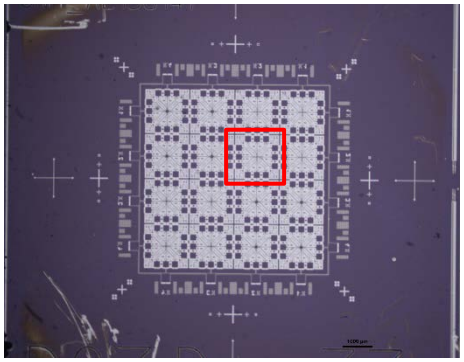
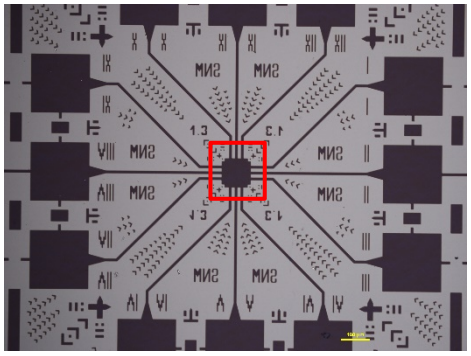
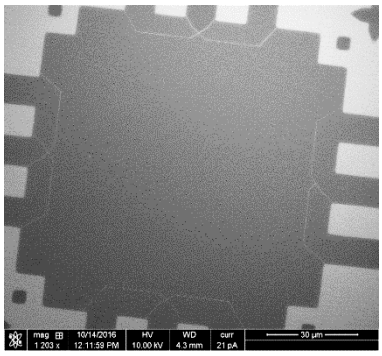
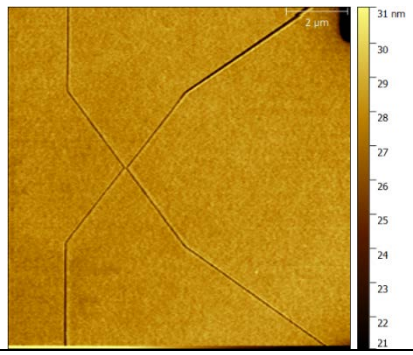
Fig. 2.3 (c) SEM image of tilted master before NIL , showing etch profile 	*Fig. 2.3 (d)* SEM image of tilted master after NIL, showing etch profile   [same part of pattern as in *(c)*]
Fig. 2.3 (e) SEM image of meandering line pattern before NIL 	*Fig. 2.3 (f)* SEM image of meandering line pattern after NIL 

1.3. Sample 2 (SET patterns)

Description of the master:

Sample 2 consists of large elevated patterns (contact pads), which have a height of approx. 25-28 nm, and small trenches, which have a depth of approx. 15 nm compared to the surrounding. Fig. 3.1 gives an overview of the pattern of sample 2. Thereby, blue regions in the optical image [(a) and (b)] are the elevated regions.

White lines on the SEM image (c) correspond to the trenches in the silicon. Four fields (f13, f14, f23, f24) were written with four SET patterns on each field. SET patterns are named by the middle contact (G2, G5, G8 or G11).

Fig. 3.1 (a) optical image of sample 2 	*Fig. 3.1 (b)* optical image of one field with contact pads [marked with red square in *(a)*] 
Fig. 3.1 (c) SEM image of middle field in (b) 	*Fig. 3.1 (d)* AFM image of SET pattern [marked in *(c)*] 

Description of measurement results for SET pattern:

10 replicas of sample 2 were produced by UV-NIL at EVG. The samples were measured by AFM at TUIL. For analysis of the SET patterns an overview of field f1.3 and f1.4 were measured as well as all SET patterns of field f1.3 and SET G2 at f1.4. On basis of this data the channel width (w1, w2) as well as the line width (lw) for all SET structures was obtained using AFM sections along the channel. An example thereof is shown in Figure 3.2.

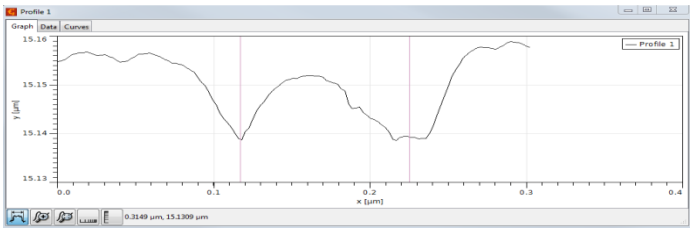


Fig 3.2 (a) channel width w1: distance between minima of lines

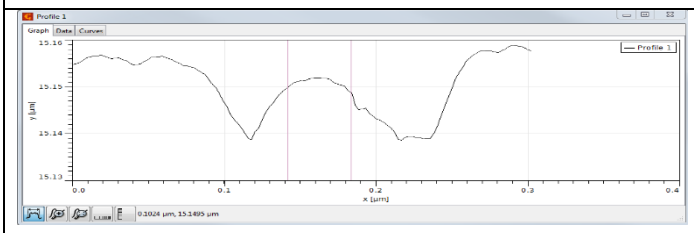


Fig 3.2 (b) channel width w2 = distance between approx. 90% height of middle bump (channel)

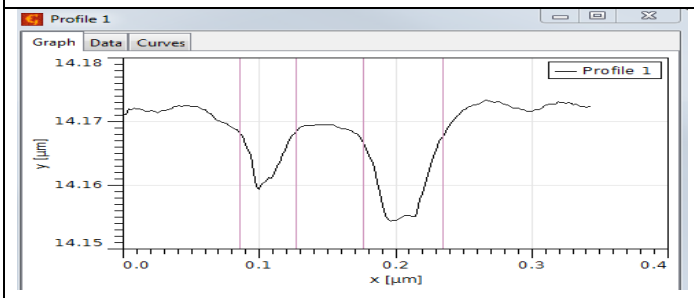


Fig 3.2 (c) line width lw = distance between approx. 90% height compared to the surrounding

The measurement reveals that the SET patterns and profiles are similar for master template and its replicas, as shown for SET G8 of f1.3 in fig. 3.3.

Fig 3.3 (a) AFM image of master template

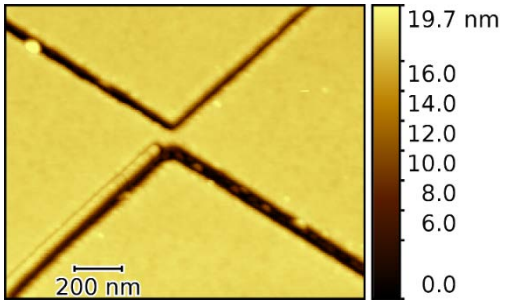


Fig 3.3 (b) AFM image of replica number 8

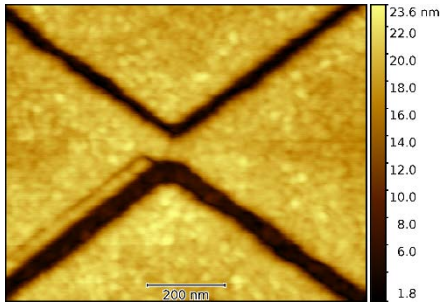


Fig 3.3 (c) extracted profile of *(a)*

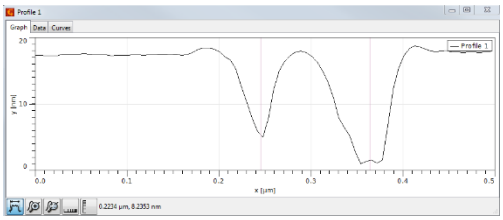
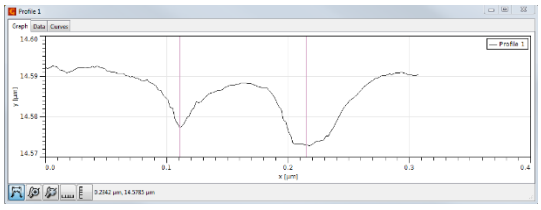


Fig 3.3 (d) extracted profile of *(b)*



In the following table the line width and channel width of master and replica are summarized. Values of replicas and master are comparable. Here, the influence of the AFM tip (tip convolution) has to be considered. All values are given in [nm]. The marked values were not used for the mean calculations since these are outliers.

f13m channel width		Master	replica wafer no.										
			1	2	3	4	5	6	7	8	9	10	mean
G2	w1	91	79	81	86	84	92	56	85	86	86	87	85,1
	w2	40	40	43	52	40	34	35	40	34	30	31	37,9
G5	w1	140	134	147	143	141	136	143	146	141	141	146	141,8
	w2	71	71	64	86	80	66	69	65	63	64	77	70,5
G8	w1	119	101	108	107	105	105	104	108	113	103	105	105,9
	w2	40	51	57	74	60	48	52	42	42	46	43	44,1
	Lw1	57	39	63	35	33	41	41	55	52	56	59	47,4
	Lw2	97	56	65	53	58	74	73	71	79	54	79	66,2
G11	w1	151	148	164	147	151	147	144	145	145	149	147	148,7
	w2	87	91	91	84	76	79	78	72	65	63	67	76,6

The mean difference between channel widths of the master template compared to the replicas is approx. 10 nm. This variation can be caused also by the positioning deviations of the section line and the extraction errors of the channel width (determination of 90% height). The deviation of line width of replicas compared to the master template is in the same range (10 nm). As can be seen from the table above, the line width analysis is more affected by extraction errors than the channel widths which are crucial for the SET characteristics.

The line depth was measured at SET G8 on f1.3. Therefore, 4 profiles were extracted and the line depth is given as the mean ± standard deviation of the difference between depth of the minimum of the line and the height of the surrounding. The values, given in [nm], are summarized in the following table. Despite replica no 2, all replicas exhibit a similar line depth as the original sample. For replica number 2, measurement result is not reliable due to imaging problems.

Line depth (f13m-G8)	Master	replica wafer no.									
		1	2	3	4	5	6	7	8	9	10
Mean [nm]	16	16	8	14	14	15	16	15	16	13	16
Std [nm]	1	1	1	1	1	1	1	2	1	1	1
Min [nm]	14	14	6	13	13	14	14	12	15	11	15

Max [nm]	17	18	9	15	16	17	18	18	17	15	18

The roughness of the replicas was measured on SET G2 at f1.4 of a 4x4µm² field. Therefore, the built-in functions of Gwyddion were used to obtain RMS as data variance and Ra as data variance with a different exponent in the data variance sum.

F14m	**Master**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Ra [nm]	0.58	0.78	0.86	1.17	0.92	0.92	1.71	1.48	1.50	0.77	0.87
RMS [nm]	1.1	1.13	1.27	1.52	1.37	1.16	2.57	1.96	4.20	1.08	1.11

The roughness measurement shows that the roughness of the replicas is slightly larger than the original sample. For some replicas (no. 6 and 8) the values are significantly larger (>2*RMS or Ra of original sample).

Summary for replication sample 2:

The SET patterns of sample 2 are quite well replicated by NIL, i.e. line depth, line width and channel width are similar within measurement errors. Furthermore, these values are similar for the 10 replicas, thus demonstrating reproducibility of NIL printing.

5. Etching of imprinted samples (IMEC)

10 samples with the SET pattern of sample 2 were replicated by NIL, in EVG, as described in the above paragraphs.

The locations for AFM inspections are described in the figure 5.1.

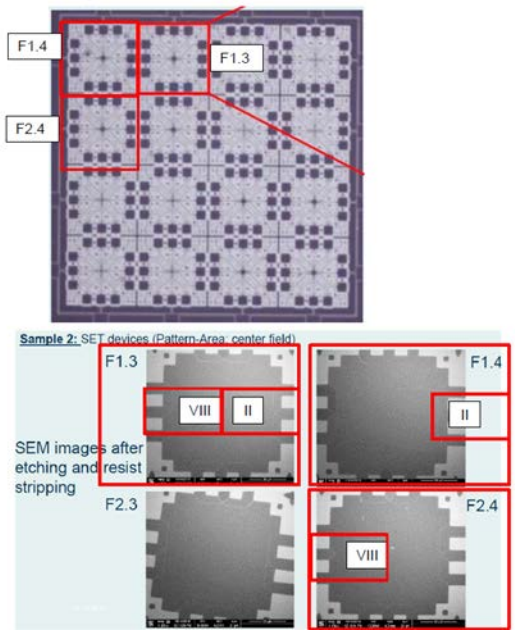


Figure 5.1: AFM measurement locations for the sample 2. Three sub-dies were inspected: F1.3, F1.4 and F2.4; in F1.3 two images were recorded.

The samples were etched in IMEC using a N_2-H_2 plasma in order to descum the residual layer, then a breakthrough step aiming at clearing the native SiO_2, followed by a final Si main etch step. The split matrix is shown in the following table 5.1. The N_2-H_2 plasma, in CCP geometry, is an anisotropic resist recess process aiming at thinning the resist in a direction normal to the wafer surface. The breakthrough (BT) step is a pure CF_4 process with high applied bias voltage (220V), in order to break the aiming at breaking the Si-O-Si strong bond. The Si main etch step is a high rate chemical Si etch, due to the presence of SF_6, with some selectivity to the resist (presence of CF_4 and N_2).

Recipe step	Process details		
N_2-H_2	20 mT / 100 + 30 W / 10-0 °C / 25 H2 / 200 N2 (CCP)		
Breakthrough (BT)	3 mT / 160W / 220V / 40 CF4 / 35 He / 50 °C (ICP)		
Si main etch	3 mT / 500W / 75V / 80 CF4 / 15 N2 / 20 SF6 / 50 °C (ICP)		
Wafer	**N_2-H_2 (s)**	**BT (s)**	**Si etch (s)**
D01	0	5	15
D02	0	5	30
D03	10	5	15
D04	10	5	30
D05	15	5	15
D06	15	5	30
D07	20	5	15
D08	20	5	30
D09	25	5	15
D10	25	5	30

Table 5.1: Description of process steps used for pattern transfer of SET-NIL replicates at IMEC

After etch, five of the above ten wafers were inspected by AFM, with a focus on positions F1.3 II and F1.4 II which have different pitch and spacing. The overall description of the results is described in tables 5.2 and 5.3. First, it can be seen for both F1.3 II and F1.4 II that, irrespective of the Si etch duration (15 or 30s), the etch depth is the same, i.e. we can conclude that resist was etched at same rate as the Silicon, and was stripped off during the process. This was confirmed by the AFM operator (typically resist causes sticking issue during measurement). It must be noted that, for F1.3 II, the best profile fidelity occurs for the shortest Si etch time (15 s, wafer D03), with a central channel height ~ 15 nm while for longer Si etch (30 s), the channel height is significantly recessed to ~ 7.5-10 nm. It can also be observed that the total width of the structure (originally ~ 165 nm) is preserved for 15 s Si etch, but widens to ~ 230 nm for 30 s Si etch. Both these observations are typical of enhanced etch rate at corners during un-masked patterning; i.e. indicate that likely after ~ 15 s Si etch the resist mask is gone and profile get lost. A similar analysis can be made for AFM inspections of the structure F1.4 II, despite the bad AFM scan likely due to particle contamination as observed by the analyst. Only for D03, the ‘valley-to-valley channel width’ and ‘channel width’ are both measured close to the reference values. It can therefore be concluded that the optimal Si etch time is ~ 15 s for these structures. The impact of varying the N_2-H_2 descum and breakthrough steps is not so clear and as a consequence, at this stage, no conclusion can be made on the optimal time for these steps.

The detailed images of wafer D03, and corresponding profiles are shown in the figure 5.2.

We can conclude from these tests that a SET pattern into a NIL resist, as described in previous paragraphs, can be transferred with high fidelity into ~ 15 nm Si by means of a combination of plasma descum, SiO_2 breakthrough and Si etch.

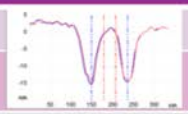
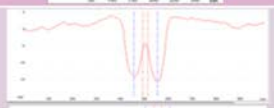
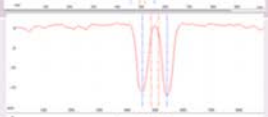
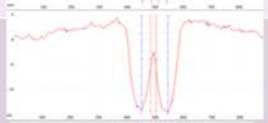
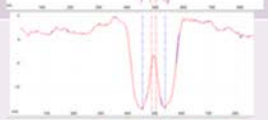
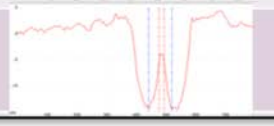
Location	Etch cond	Image	Channel width v-to-v (nm)	Channel width (top)(nm)
F1.3 II	Reference (not etched)		88	32
	Etch N2-H2 / BT / Si		↓	↓
D02	0 / 5 / 30		98	25
D03	10 / 5 / 15		89	30
D04	10 / 5 /30		93	15
D08	20 / 5 / 30		83	15
D10	25 / 5 / 30		78	20

Table 5.2: Summary of process conditions, images, valley-to-valley channel spacing and channel width for 5 wafers with different N_2-H_2, BT and Si etch times, for structure F1.3 II. First row describes the post-NIL profile (before etch).

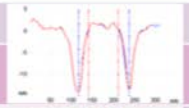
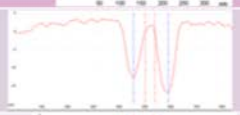
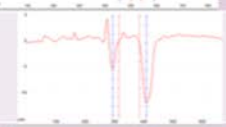
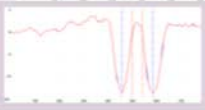
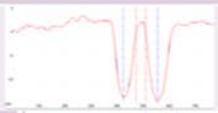
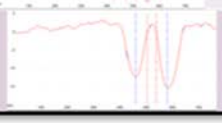
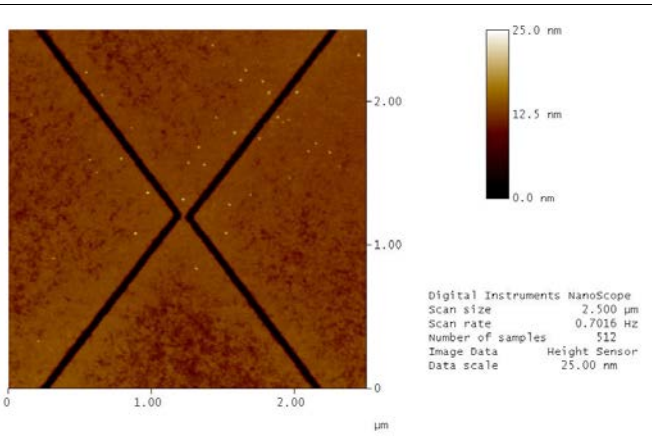
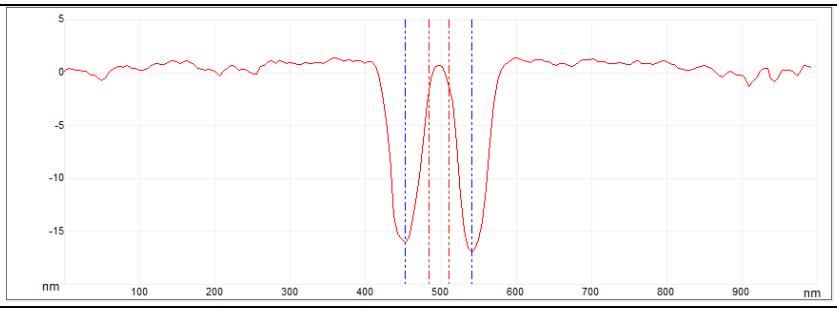
Location	Etch cond	Image	Channel width v-to-v (nm)	Channel width (top)(nm)
F1.4 II	Reference (not etched)		122	75
	Etch N2-H2 / BT / Si		↓	↓
D02	0 / 5 / 30		133	34
D03	10 / 5 / 15		113	69
D04	10 / 5 /30		128	39
D08	20 / 5 / 30		133	39
D10	25 / 5 / 30		118	34

Table 5.3: Summary of process conditions, images, valley-to-valley channel spacing and channel width for 5 wafers with different N_2-H_2, BT and Si etch times, for structure F1.4 II. First row describes the post-NIL profile (before etch)

F1.3 II AFM	
F1.3 II profile	

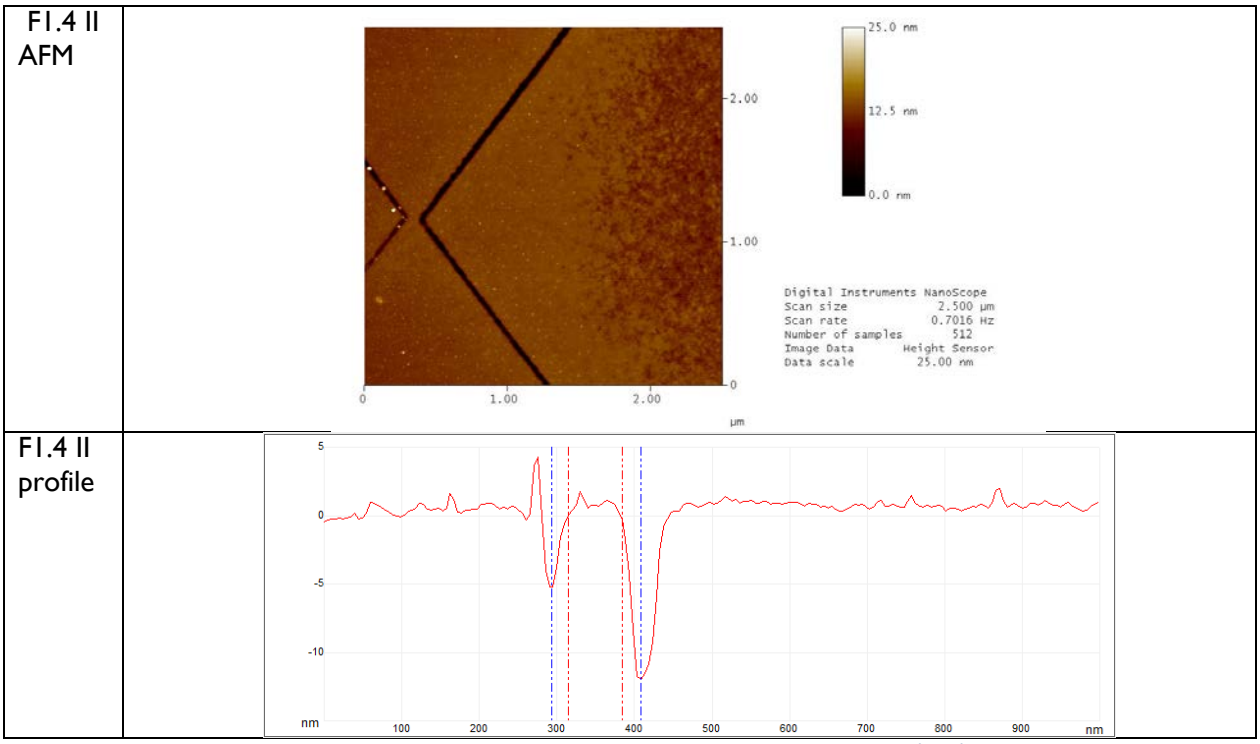


Figure 5.2: AFM image profile (through the channel) of the sample D03 after etch using a 10s / 5s / 15s sequence. The F1.4 II images and profiles are corrupted by the presence of a very large cluster of particles (Z > 200nm) close to the left side of the trenches.

6. Summary and Conclusions

NIL replication of sample 3 and sample 2 worked well. Line width, pitch and line depth are well reproduced. Replication of sample 5 exhibits some defects. This could be caused by pattern collapse on the stamp due to large aspect ratios (2:1 up to 5:1). Aspect ratios for sample 3 and 2 are in the range of 1:1 or 1:2. Pattern transfer into underlaying Si can be made with high fidelity at 1:1 amplification, giving ~ 30 nm channel width.