Collaborative project

Project acronym: SNM

Project full title: "**Single Nanometer Manufacturing for beyond CMOS devices**"

Grant agreement no: 318804

Deliverable: D6.1

“Scalability study over range 15-200 nm for hole patterning into SiO_2.
Demonstration of SiO_2 hole patterning down to 15nm & Si line patterning down to 12 nm.”

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3	IMEC	**IMEC**	RES	Belgium
4	Mikrosistemi Ltd	**µS**	SME; End-User	Bulgaria
5	Universität Bayreuth	**UBT**	HER	Germany
6	Technische Universiteit Delft	**TUD**	HER	Netherlands
7	Spanish National Research Council	**CSIC**	RES	Spain
8	IBM Research GmbH	**IBM**	IND; End-user	Switzerland
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15	VSL Dutch Metrology Institute	**VSL**	IND	Netherlands
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<table>
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Work Package 6
Deliverable: D6.1
(“scalability study over range 15-200 nm for hole patterning into SiO_2. Demonstration of SiO_2 hole patterning down to 15nm & Si line patterning down to 12 nm.”)</td></tr>
<tr><td>Lead beneficiary number</td><td>3</td><td>Nature</td><td>R</td><td>Dissemination level</td><td>PU</td></tr>
<tr><td>Estimated Person-months</td><td colspan="5">16</td></tr>
<tr><td>PMs by partner for the Deliverable</td><td colspan="5">IMEC: 9
OINT: 7</td></tr>
<tr><td>Estimated Delivery Date</td><td>15/12/2013</td><td colspan="2">Delivery Date</td><td colspan="2">15/12/2013</td></tr>
<tr><td>Description of the Deliverable</td><td colspan="5">DOW description: Deliver scalability study over range 15-200 nm for hole patterning into SiO_2: Deliver scalability study over range 15-200 nm for hole patterning into SiO_2. Demonstration of SiO_2 hole patterning down to 15nm & Si line patterning down to 12 nm. [month 12]

PART 1: Current 193i and EUV lithography techniques allow hole printing in the range [30 – 200]nm at relaxed pitch. EUVL will be extended in the coming years to ~ 20nm CD (half-pitch). By using plasma polymer shrink techniques, dimensions will tentatively be scaled down to 10-15nm. Target patterned material will be SiO_2. Masking strategy will be according to best time practice, as examples Photoresist/SiOC/amorphous Carbon tri-layer system or ALD (PVD) TiN metal hardmask.

PART 2: Lines: current 193i and EUV lithography techniques allow line printing of around 30nm and above; subsequent mask trim allows to decrease line size down to ~ 14nm at present, in 2014 objective is to reach dimension of 10nm at relaxed pitch. Spacer-defined (spacer material deposited by ALD or PECVD) patterning allows to reach similar dimensions but half-pitch. Based on these techniques, line patterning in the range [10-100] nm (relaxed pitch) will be executed and scaling challenges will be studied. Target patterned material will be polycrystalline Si or epitaxial Ge. Masking strategy will rely else on 193i/EUV lithography</td></tr>
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followed by plasma trim (relaxed pitch), else on spacer-defined double patterning (PECVD- or ALD-based)(dense pitch).

PART 1: contact holes

Two routes were pursued: using SiOC/α-C and TiN hardmasks. The patterning scheme is as described in the figure (1). Plasma polymer shrink technique (TiN mask) or tapered SiOC approach (SiOC/α-C mask) were used to reduce hole CD after lithography.

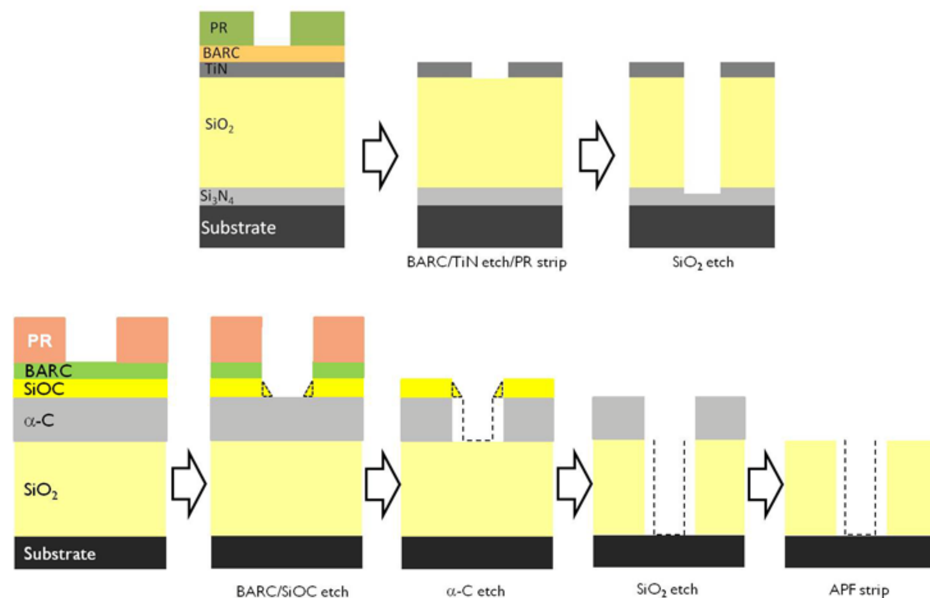


Figure 1: process flow for hole patterning. Top: using a TiN hardmask – a plasma polymer shrink may be used to reduce CD before BARC opening. Bottom: using a SiOC/α-C dual hardmask. Dotted lines indicate how hole dimension can be reduced by the 'tapered SiOC approach'.

In order to print such a wide range of dimensions, the lithography was using different masks, resists, and technologies (EUV, 193i, 193). In the case of EUV lithography, starting CD was 32.2nm (3σ=4.6nm). Holes shrinkage was performed by using plasma deposition techniques on resist or hard-mask sidewalls, and proven to be very challenging to get below 20nm in a reproducible and uniform manner.

For the TiN approach, the BARC was opened using a CF_4 CCP plasma, then the TiN was etched by means of an HBr/Cl_2 plasma (low bias voltage) in an ICP chamber. For the cases where CD was shrinked, polymers were preferentially deposited on resist sidewalls prior to BARC opening, using cycles of short N_2-CH_3F and CF_4 discharges, leading to a deposition rate of 1.6nm/cycle. After TiN opening, the photoresist was ashed by an O_2 plasma, afterwards, SiO_2 was etched by means of an Ar-CO-C_4F_8 discharges in a CCP chamber. O_2 was avoided, due to the fact that the presence of oxygen lead to faster erosion of the TiN mask, Ti-

containing byproduct re-deposition and slope formation.

For the SiOC/α-C approach, the complete process was done is a single CCP chamber. The SiOC was first opened with a CF_4/CHF_3 plasma, with for sub-35nm contact holes an increasing proportion of CHF_3. After that, the α-C was etched away (anisotropically) in a N_2-H_2 plasma which was at the same time stripping off the photoresist. After that, an Ar-C_4F_8-C_4F_6-O_2 plasma was used to pattern SiO_2. Etch rates were measured as a function of etch depth and found to be constant for the range considered.

The figure (2) shows the measured etch rate as a function CD, for both HM approaches. CD is measured at the top of the hole, which is the most sensitive place due to hard-mask erosion. One can see that with the C-based hardmask, there is a slight increase of etch rate for dimensions between 50 and 100nm, then a drop initiates for dimensions below 50nm, leading to ± 20% etch rate decrease at 20nm CD. Although this may indicate some start of change into the etch mechanism, it is likely that extending the process to the [10-20]nm range will not cause major difficulties. With TiN, on the contrary we can see that below 100nm a significant drop in etch rate occurs. This drop reaches 'etch-stop' for dimensions around 20nm. Few process modifications (N_2 addition, O_2 addition, CF_4 addition, power change) were tentatively tried without success.

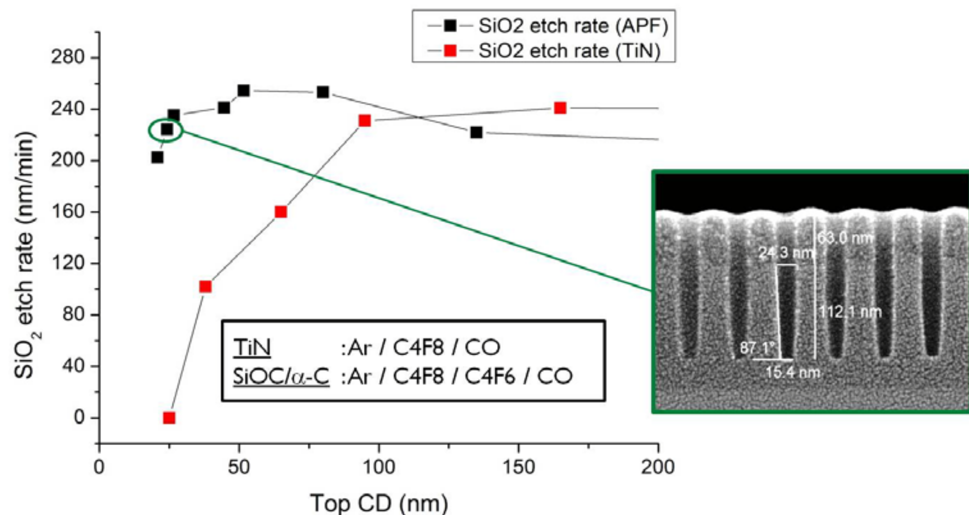


Figure 2: SiO_2 etch rate as a function of post-etch CD measured on top of the hole. The right image is a X-SEM (without resist strip) showing the type of structure studied. Top CD is ~24nm, bottom CD is ~15nm.

The figure (3) compares cross-section views of both TiN and SiOC/α-C HM approaches, looking at similar dimensions. For the SiOC/α-C case, holes are nicely shaped with almost vertical profiles. The α-C mask remains quite thick, allowing a nice pattern transfer without SiO2 top-corner tapering. In the opposite, with TiN, holes have irregular shapes and the mask is severely eroded. Complementary experiments (not shown) indicate that the presence of O in the discharge causes loss of TiN protection, which is then sputtered away,

oxidize, and re-deposits on hole sidewalls. It appears that this phenomenon occurs even with O released from the wafer itself (SiO_2), which can represent a flow of the order of 1-2 sccm. On the image 3(b), areas highlighted by white circles indicate Ti-O deposits (non-volatile).

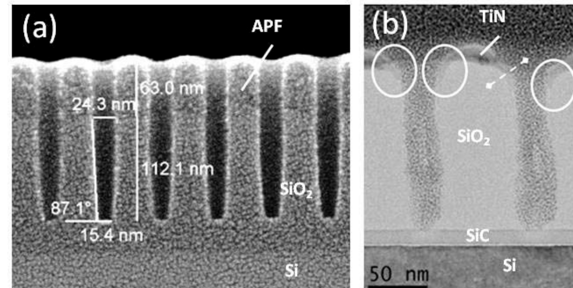


Figure 3: (a) XSEM image of contact hole etched into SiO_2 using a SiOC/α-C (APF) mask: good profile and vertical sidewalls; (b) (TEM image) using a TiN HM, Ti-O residues form on the neck and sidewalls, causing hole CD shrink & irregular shapes, ultimately leading to etch-stop.

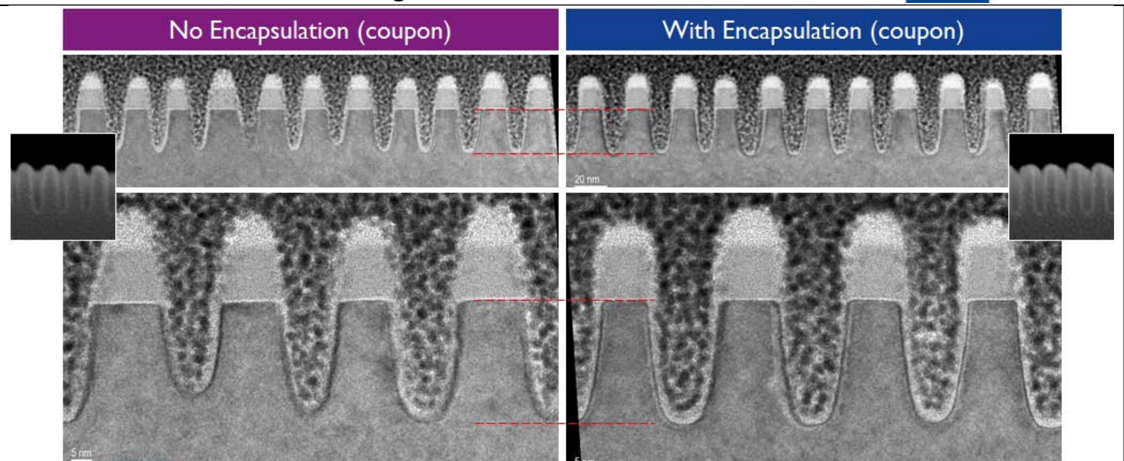
It can be concluded from these tests that

- Patterning tests with a C-based mask allows to safely extrapolate that SiO_2 hole etching can occur down to 10nm.
- Patterning tests with a TiN mask indicate that this mask is not suited for etching O-containing materials. Likely, any metallic mask which can easily form non-volatile oxides will lead to patterning issues when the target material contains a significant amount of O, which will be even more pronounced if the open area is larger (lightfield mask). Use of metallic HMs must be therefore considered with care, or be removed before pattern transfer into SiO_2 (in case of use of TiN/α-C dual HM).

PART 2: lines in Si

In between the SNM project submission (January 2012) and beginning of the project (January 2013), some thing have changed. Currently, at IMEC the line patterning effort for advanced dimensions is focusing on DSA using PS-PMMA block copolymers templates. As a consequence, the DSA patterning approach replaces the spacer-defined patterning as originally planned.

DSA patterning uses PS/PMMA block co-polymers that segregate into regular patterns under proper conditions of film composition, thickness, bake temperature. From a pattern transfer perspective, the dry development of PMMA selective to PS was optimized by introducing an SiO_2 encapsulation process (see figure below). This techniques allows to coat in-situ, during the etch process, SiO_2 preferentially on top and sidewalls of the PS rather than at the bottom of the feature.

	 **Figure 4: (left) no encapsulation, Si_3N_4 HM corner rounding; (right) with encapsulation, rectangular shape of Si_3N_4 HM is preserved.** Then the Si etch step was optimized, allowing us to obtain trenches in Si with a width of 11.5nm, depth of 20nm and LWR of 1.95nm (3σ=0.3nm on full 300mm wafer).
Explanation of Differences between Estimation and Realisation	Reference CD for SiO_2 holes was measured at the top of the holes, which is typically slightly larger than at the bottom. Lowest achieved CD corresponds to ~ 20nm (top CD) and ~ 10-13nm (bottom CD)(aspect/ratio 5). Achieving smaller CDs was found to be difficult, due to non-uniform plasma shrinkage when pushed to its limits, making the process non-reliable. Projected dimensions for Si pattern transfer (12nm) have been achieved using DSA PS-PMMA block copolymers approach i.o. spacer-defined double patterning (SDDP).