Funded by
the European Union

Collaborative project

Project acronym: SNM

Project full title: "**Single Nanometer Manufacturing for beyond CMOS devices**"

Grant agreement no: 318804

Deliverable: D6.7 ("Pattern transfer capabilities of ALD for SNL-patterned molecular resist")

Name of the coordinating person: Prof. Dr. Ivo W. Rangelow, Email: ivo.rangelow@tu-ilmenau.de

List of participants:

Participant no.	Participant organisation name	Part. short name	Activity Type	Country
1 (Co)	Technische Universität Ilmenau	**TUIL**	HER	Germany
2	EV Group E. Thallner GmbH	**EVG**	IND; End-user	Austria
3	IMEC	**IMEC**	RES	Belgium
4	Mikrosistemi Ltd	**µS**	SME; End-User	Bulgaria
5	Universität Bayreuth	**UBT**	HER	Germany
6	Technische Universiteit Delft	**TUD**	HER	Netherlands
7	Spanish National Research Council	**CSIC**	RES	Spain
8	IBM Research GmbH	**IBM**	IND; End-user	Switzerland
9	École polytechnique fédérale de Lausanne	**EPFL**	HER	Switzerland
10	SwissLitho AG	**SL**	SME; End-User	Switzerland
11	Oxford Instruments Nanotechnology Tools Ltd	**OINT**	IND; End-user	UK
12	Imperial College London	**IMPERIAL**	HER	UK
13	The Open University	**OU**	HER	UK
14	Oxford Scientific Consultants Ltd	**OSC**	SME	UK
15	VSL Dutch Metrology Institute	**VSL**	IND	Netherlands
16	University of Liverpool	**ULIV**	HER	UK

Funded by
the European Union

SNM **Work Package 6** **Deliverable: D6.7 ("Pattern transfer capabilities of ALD for SNL-patterned molecular resist")**									
Lead beneficiary number	14	**Nature**		R		**Dissemination level**		PU	
Estimated Person-months	19.5								
Person-months by partner for the Deliverable	OSC	TUIL							
	13	2							
Estimated Delivery Date	31/12/2016		**Delivery Date**			10/03/2017			
Author	• Ejaz Huq, Marcus Kaestner, Phil Prewett								
Reviewed by:	• WP6 Leader: Jean-Francois de Marneffe • WPG2 Leader: Mike Cooke • Coordinator: Ivo W. Rangelow								
Criteria and Achieved Results	**Criteria**				**Achieved result**				
	Provide hard masks for pattern transfer with molecular glass resists from WP5 and conformal coatings on non-planar features.				Achieved with some variations from the original plan: see report below.				

Funded by
the European Union

Description of the Deliverable	The deliverable is a report of work carried out on Atomic Layer Deposition (ALD) for the following intended applications 1. As a hard mask for pattern transfer by plasma dry etch, patterned by FE-SPL. 2. As a high-k dielectric coating intended for use in SNM devices. 3. In conjunction with a patterned block co-polymer template for Nano Imprint Lithography (NIL).
Explanation of Differences between Estimation and Realisation	Work on application 1 was curtailed since the novel molecular glass resists and fullerene polymer resist from WP5 achieved greater plasma etch resistance than anticipated. Work on application 3 was carried out instead as a deviation from the DoW in response to partner demand, in collaboration with CSIC, Barcelona. TUIL collaborated with Imec on an alternative "stack" hard mask. Details of these and other aspects of the work are contained in the report below. The total staff effort used by OSC in achieving deliverable D6.7 was 13 PM against an original estimate of 14 PM. The balance of allocated effort of 1 PM was expended instead in WP5 to do additional work on the novel fullerene resists, justified by their lithographic and etch performance in screening trials at IMEC. ALD equipment at Southampton University was used instead of equipment in Boston, USA and Cork, Eire as stated in the DoW. This provided greater experimental utility for OSC because of the close proximity of Southampton to Oxford.
Metrology comments	Helium Ion Microscopy (HIM) was used to inspect the results of ALD co-block polymer experiments.

Contents

Foreword……………………………………………………………………………………5

1. INTRODUCTION…………………………………………………………………...5

1.1 ALD Hard Masks………………………………………………………………………5

1.2 ALD High-k dielectrics……………………………………………………………..6

1.3 Mechanisms of ALD………………………………………………………………..7

2. EXPERIMENTS……………………………………………………………… .10

2.1 Hard Mask Deposition (Al2O3)……………………………………………………10

2.1.1 Wet etch of hard mask films deposited by ALD…………………………… 12

2.1.2 Dry etch of hard mask films deposited by ALD………………………………15

2.2 ALD Hafnium Oxide – high-k Gate Dielectric…………………………………… 16

2.3 Investigation of ALD hard masks for pattern transfer amplification in FE-SPL)…………………………………………………………………………………..17

2.4 Variation from the Plan …………………………………………………………..21

2.5 ALD for Nanoimprint Lithography Stamp Fabrication……………………………..21

CONCLUSIONS………………………………………………………………………25

References ……………………………………………………………………………..26

Foreword

This report includes contributions in collaboration with OSC from the University of Southampton (Sally Shi and Stuart Boden). OSC and Imec collaborated to produce the comparison of etch results for ALD hard masks. TUIL contributed by patterning using FE-SPL and initial pattern transfer experiments. Work towards a silicon stamp for NIL was done in collaboration between OSC and CSIC Barcelona. TUIL and Imec collaborated on FE-SPL of a hard mask stack.

Funded by
the European Union

1. INTRODUCTION

For nanoscale 'device fabrication' Atomic Layer Deposition (ALD) [1] was selected as one of the enabling technology options for thin film deposition and pattern transfer in the SNM project.

The primary advantages of ALD are derived from the sequential, self-saturating, gas-surface reaction control of the deposition process. Above all, conformity of ALD-deposited films is most often the critical factor in choosing this technique over CVD or sputtering. Uniformity and conformal coverage of high aspect ratio and 3D materials is made possible by the self-limiting characteristic of ALD, which restricts the reaction at the surface to no more than one mono-layer of the precursor used. Also, the pulsed precursor can easily diffuse into deep trenches, allowing complete reaction with the entire surface. Subsequent cycles then produce uniform growth on high aspect ratio structures, as compared to CVD and PVD, which suffer from non-uniformity due to faster surface reactions and shadowing effects, respectively.

In particular it was felt at the outset of the project that the ALD technique would be useful in providing hard masks for pattern transfer by plasma etch and FE-SPL, and as high-k dielectric material for nanoscale devices such as Single Electron Transistors (SETs).

1.1 ALD Hard Masks

In nanoscale fabrication resist thickness has to be scaled down for maximal lithographic resolution. But these thin resists (in the order of 5 nm) are not always suitable as etch masks. In order to find optimum materials as etch masks, the concept of hard mask has been devised [2]. The hard mask material is etched with a photoresist or, for high resolution, an electron beam sensitive resist. The resist is then stripped off and the etch process of the underlying layer is performed using the hard mask only. The hard mask material can be optimized to suit the application, irrespective of the resist.

In reactive ion etch processes for pattern transfer, many materials have been tried as hard masks, including silicon dioxide, aluminium nitride (AlN) and aluminium oxide (Al_2O_3). These materials are very resistant in many process plasmas, but can be wet etched readily using KOH and even dilute NaOH photoresist developer. This allows processing to be easier, reliable and faster.

One of the attributes of ALD is that ultrathin pin-hole free continuous films (a few nm thick) can be conveniently produced on a wide variety of substrates. Therefore for nanoscale device fabrication, whether it is for a hard-mask layer or a gate oxide layer, this pin-hole free

deposition is vitally important. The film thickness can be controlled with sub-nm precision by simply controlling the number of deposition cycles.

1.2 ALD High-k dielectrics

Conventionally, silicon dioxide (SiO_2) has been used as a gate oxide material, for decades. As transistors have decreased in dimensions, the thickness of the silicon dioxide gate dielectric has also been decreasing to increase the gate capacitance and thereby drive current, raising device performance. As the thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high-k material allows increased gate capacitance without the associated leakage effects. The current state of the art high-k dielectric is hafnia (HfO_2) which has a dielectric constant between 4 and 6 times that of SiO_2 depending on the deposition method [3].

The capacitance of the gate dielectric layer is

$$C = k\varepsilon_0 A / t \tag{1}$$

where k is the relative dielectric constant, ε_0 is the permittivity of free space and t is the thickness of the capacitor oxide. Since leakage limitation constrains further reduction of t, an alternative method to increase gate capacitance is by replacing silicon dioxide with a high-*k* material. In such a case, a thicker gate oxide layer might be used which can reduce the leakage current flowing through the structure as well as improving the reliability of the gate.

1.3 Mechanisms of ALD

The substrate to be coated is exposed in a vacuum chamber to two reactants or precursors A and B in a sequential manner. Each reactant reacts with the surface in a self-limited way where the reactant molecules can interact with a limited number of reactive sites present on the surface. When all the available sites have been consumed in the reaction, the growth process stops. The remaining reactant molecules are pumped away and reactant B is introduced. Alternating exposures of A and B produces the desired thin film. When describing an ALD process one refers to dose time, which is the time a surface is being exposed to a precursor and purge time, which is the time between doses for the precursor to evacuate the chamber for each precursor. The dose-purge-dose-purge sequence produces an ALD cycle. Also, instead of growth rate, ALD processes are commonly described in terms of their growth per cycle.

Funded by
the European Union

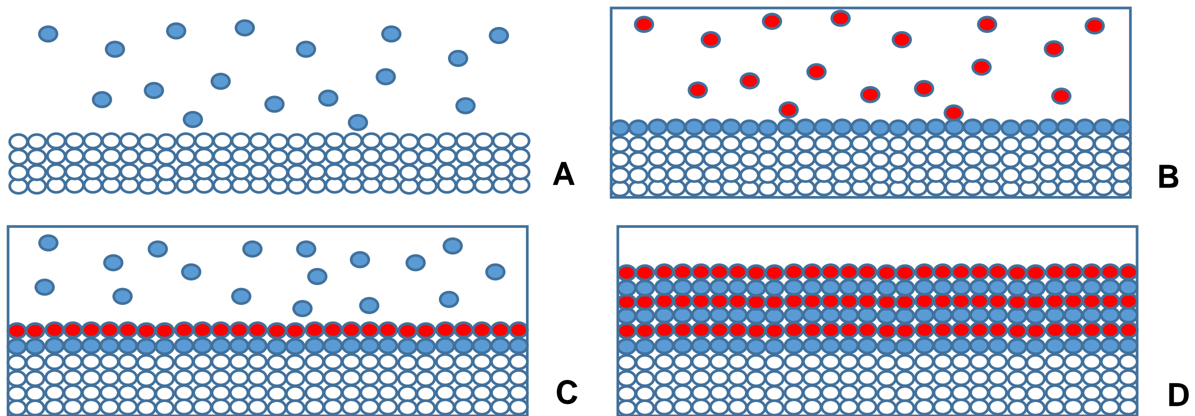


Fig. 1 Four stages of ALD film formation

A schematic of the ALD process is shown in Fig 1. Precursor 1 (in blue) is added to the reaction chamber containing the material to be coated by ALD (A).

After precursor 1 has adsorbed on the surface, any excess is removed from the reaction chamber. Precursor 2 (red) is added (B) which then reacts with precursor 1 to create the next layer on the surface (C). Precursor 2 is then removed from the reaction chamber and this process is repeated until a desired thickness is achieved and the resulting product resembles (D). The process requires ultra-high vacuum and rapid switching of gas valves controlling the precursors in a system as shown schematically in Figure 2. The temperature of the process can be controlled in a way which balances the speed of the gas chemistry against the need to avoid thermal damage to the substrate.

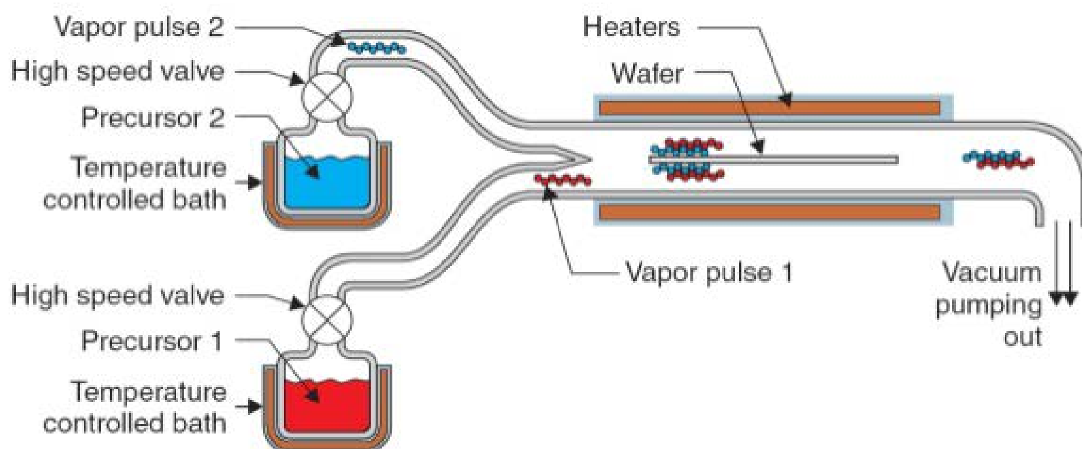


Fig.2 Schematic of a typical atomic layer deposition system

Despite the many unique advantages of using ALD, its biggest drawback is the slow deposition rate. Long cycle times involved in pulsing and purging precursors and the layer-by-layer nature of the deposition, does not allow ALD rates to exceed 100–300 nm/h.

This rate is strongly dependent on the reactor design and the aspect ratio of the substrate. As the surface area and volume of an ALD reactor increase, so does the time needed for pulsing and purging. High aspect ratio substrates also require longer pulse and purge times to allow for the precursor gas to diffuse into trenches and other three dimensional features. The rate of adsorption measured in molecules per second per unit area of the sample is governed by the rate of arrival of molecules at the surface and the fraction of incident molecules which undergo adsorption. This can be expressed as the product of the incident molecular flux *F* and the sticking probability, *S*.

$$R_{ad} = SF \tag{2}$$

The flux of incident molecules [molecules $m^{-2}s^{-1}$] is given by the Hertz-Knudsen equation

$$F = \frac{P}{(2\pi MkT)^{\frac{1}{2}}} \tag{3}$$

Where P is the local gas pressure [Nm^{-2}], M is the mass of one molecule [kg], T is the temperature [K]. The sticking probability is a property of the adsorbate/substrate system under consideration but must lie in the range $0 < S < 1$. It may depend upon various factors - foremost amongst these being the existing coverage of adsorbed species (θ) and the presence of any activation barrier to adsorption. In general, therefore

$$S = f(\theta)e^{-\frac{E_a}{kT}} \tag{4}$$

E_a is the activation energy for adsorption and $f(\theta)$ is function of the existing surface coverage of adsorbed species. Combining the equations for *S* and *F* yields the following expression for the rate of adsorption:

$$R_{ad} = \frac{P}{\sqrt{2\pi MkT}} f(\theta)e^{-\frac{E_a}{kT}} \tag{5}$$

If a surface is initially clean and it is then exposed to a gas pressure under conditions where the

rate of desorption is very slow, then the coverage of adsorbed molecules may initially be estimated simply by consideration of the kinetics of adsorption.

$$R_{ad} = \frac{dN_{ad}}{dt} = SF \tag{6}$$

Where N_{ad} is the number of adsorbed species per unit area of surface.

In general, this equation must be integrated to obtain an expression for N_{ads}, since the sticking probability is coverage (and hence also time) dependent. However, if it is assumed that the sticking probability is essentially constant, which is a reasonable approximation for low coverages, the number of molecules adsorbed on the surface increases linearly with time, thus

$$N_{ad} = SFt \tag{7}$$

2. EXPERIMENTS

2.1 Hard Mask Deposition (Al_2O_3)

Oxford Scientific Consultants Ltd. (OSC), in collaboration with Southampton University, investigated ALD Al_2O_3 for hard mask applications in the SNM project. Silicon wafers were coated with Al_2O_3 by thermal ALD at Southampton University. The ALD process sequence is shown in Fig. 3. To begin with, two wafers were coated; the average thickness of the wafers was 28.75nm and 31.25 nm. Wafers were sent to Imec for etch characterization and benchmarking against IMEC's own ALD deposition facility.

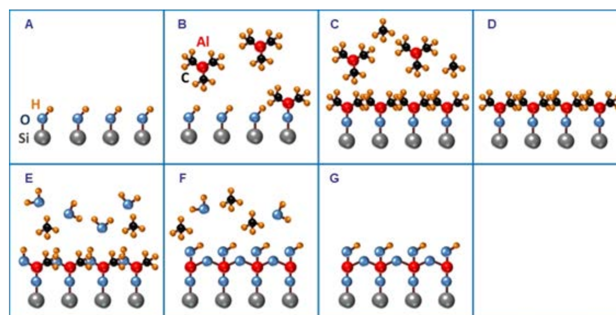


Fig.3 ALD Sequence for Al_2O_3 film formation.

Deposition of Al_2O_3 from water and trimethyl aluminium (TMA) precursor follows the key principles of ALD. A complete cycle of Al_2O_3 growth on a silicon substrate is outlined in Figure 3. There are five steps in the deposition cycle as follows:

1. Substrate surface is hydroxylated by exposure to air, oxygen or ozone (A).
2. The TMA precursor is pulsed. TMA reacts with the OH groups on the surface but not with itself and the monolayer of TMA passivates the surface (B, C).
3. Unreacted TMA molecules and by-products are removed by evacuation and/or purging with nitrogen (D).
4. Water vapour is pulsed into the ALD chamber where it reacts with TMA to create a layer of Al-O-Al bridges and passivates the surface with Al-OH termination. Methane (CH_4) is formed as a gaseous by-product (E, F).
5. Unreacted H_2O and CH_4 are purged with nitrogen carrier gas during pumping after the water pulse (G).

Steps (A)-(G) form a cycle. Each cycle produces a maximum of 1.2 Å of Al_2O_3 layer depending on temperature. Thus, 100 cycles produces ~12 nm of Al_2O_3.

Because the film thicknesses of thermal ALD deposited films are typically only a few nanometers it is convenient and more accurate to measure the thickness using optical techniques such as ellipsometry, based on polarisation of light. Fig. 4 shows the thickness variation of Al_2O_3 film ~5 nm thick deposited by ALD on a 2 x 2 cm test sample. The maximum thickness variation is only 0.15 nm confirming the degree of uniformity possible using ALD for ultra-thin film deposition.

The statistics of the ALD deposited Al_2O_3 film, taken from Fig 4 are presented in Table 1, showing an average of 4.82 nm thickness with a standard deviation (1 sigma) of 0.05 nm.

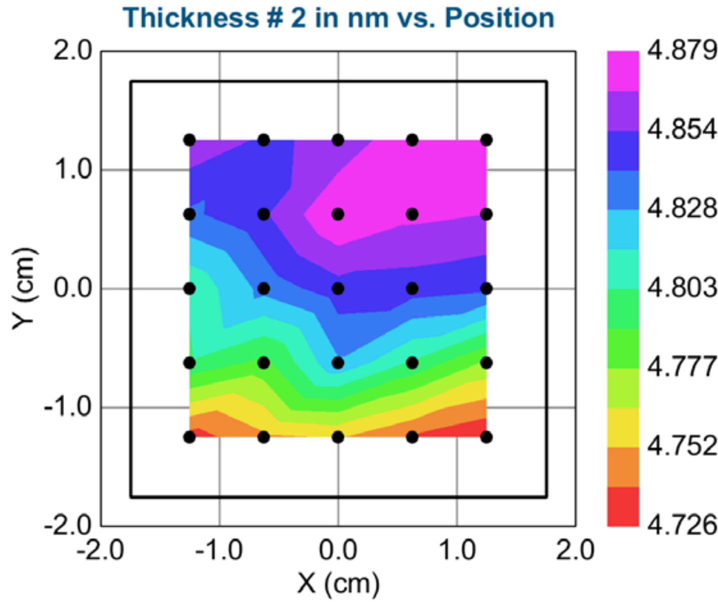


Fig.4 Nominal 5nm Al_2O_3 ALD film: thickness variation over 2cm square sample (ellipsometer measurements)

Parameter	Average	Std. Dev.	Minimum	Maximum	Range	# of Points
Thickness vs. Position	**4.81956**	**0.0498**	**4.72601**	**4.87907**	**0.15305**	**25**

Table 1. Thickness variation of Al_2O_3 film deposited by ALD. Thickness measured using an ellipsometer.

2.1.1 Wet etch of hard mask films deposited by ALD

For fine scale pattern transfer, plasma etch is the most suitable technology available, widely used in semiconductor fabrication processes. In this technique a combination of chemical reaction and energetic particle beam is used to selectively remove material from the substrate surface. However, one of the limitations of plasma etch is the erosion rate of the etch-mask, which protects the underlying layer. Polymer films have poor etch resistance and are therefore often not suitable, particularly in defining nanometer structures. Metal films are more useful due to their significantly higher etch selectivity compared to polymer films. Inorganic ALD films are of particular importance in nanoscale pattern transfer owing to the film uniformity and pinhole free deposition. Metal films to be used a hard-masks must be characterized for etch selectivity before proceeding with pattern transfer. Aluminum oxide acts as a good hard mask material and often used for pattering low dimensional structures.

The reason for carrying out the wet etch trials was that the Al_2O_3 hard mask must be removed completely after use in plasma etching. Because of its high plasma etch resistance, this is best done by wet etch which must be included in the process flow. It is therefore necessary to determine the etch rate for hard mask removal in order a) to control the process and b) to study the effect of Helium ion exposure to the hard mask material during scanning helium ion beam lithography (SHIBL) and its possible effect on the etch rate.

The etch rates of Al_2O_3 films deposited by ALD were determined. Samples were cleaved into small chips and etched in a standard aluminium etchant (H_3PO_4:HNO_3:H_2O) at 50^oC for different times. Layer thicknesses before and after etch were measured by ellipsometer. Typical etch characteristics are shown in Fig. 5 below for different initial layer thicknesses. The wet etch rate of the Al_2O_3 varies from 11.07 nm/min for the film of 5 nm thickness, through 7.49 nm/min for the 10 nm film to 6.95 nm/min for the 20 nm thick film. It is proposed that exposure to He^+ ions during SHIBL will cause this etch rate to increase, say to double to 22 nm per min. It should then be possible to specify an etch time (~14 s) which will fully remove the exposed regions but leave ~2.5 nm thickness of Al_2O_3 in the unexposed regions. The pattern will then have been defined in a 2.5 nm thick layer of alumina, e.g. for use as an ultra-thin gate insulator. Through the above experiment, preliminary work has been carried out to characterize the baseline etch rate of ALD deposited alumina of different thickness, in readiness to characterize the etch rate of alumina exposed to a helium beam. The etch rate of as-deposited alumina is slow enough to be controlled by dipping and rinsing. If it etches too quickly then it would be difficult to stop the etching when the He exposed material has been removed but some of the unexposed material remains. It is not entirely clear why the etch rate changes with film thickness but it is possibly an annealing effect since the material in the thicker films is held at the growth temperature for longer due to the longer deposition time needed. This could cause changes in density that lead to a variations in etch rate in the acids.

Funded by
the European Union

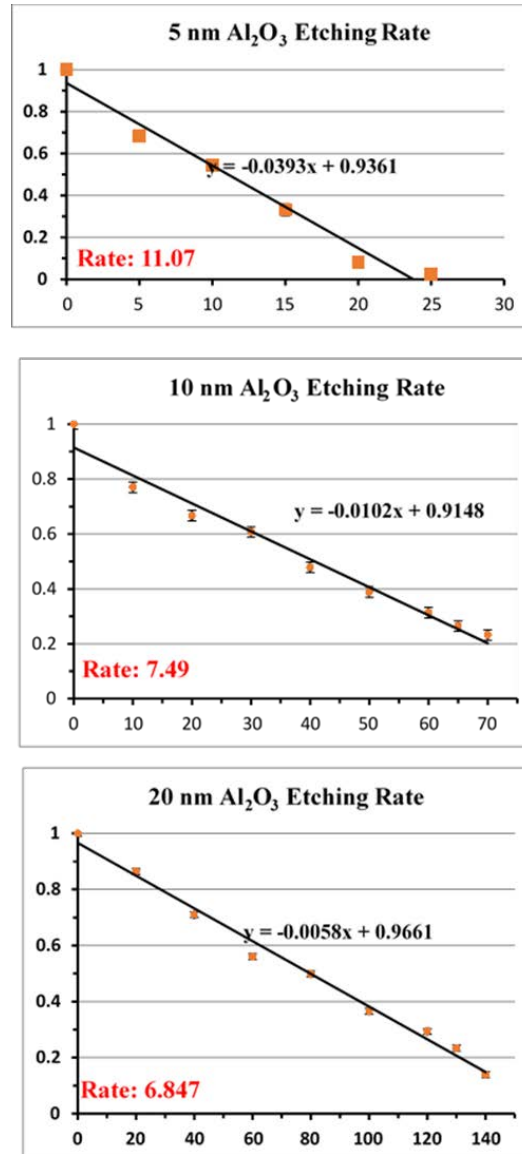


Fig.5 Wet etch rate of ALD-deposited Al_2O_3 hard mask films of initial thickness 5 nm, 10 nm and 20 nm.

2.1.2 Dry etch of hard mask films deposited by ALD

As described earlier, whilst wet etch is desirable for final removal of hard masks following pattern transfer, dry etch is necessary for the high resolution pattern transfer step and this stage of the process relies on the dry etch durability of the hard mask. The ALD - produced hard masks were therefore evaluated for dry etch durability using an inductively coupled plasma (ICP) etcher. The etch plan was as follows:

- 4” wafers were diced into quarters
- Etched in an ICP system using a 300 mm dummy carrier wafer
- ICP power: 450 W, Bias voltage: 100 V

- Etch gases: BCl_3, Cl_2, CF_4, SF_6, HBr and NF_3

Process Flow:

- Pre-etch thickness measurement on each samples using ellipsometer
- Carry out 60 sec etch process on each sample (six different chemistries)
- Perform post-etch thickness measurement to access the etch rates

Wafers were also sent to IMEC for etch characterization and benchmarking against IMEC's own ALD deposition process. The results of this comparison are shown in Table 2 below.

Plasma	IMEC ALD Al_2O_3					OSC ALD Al_2O_3				
	Pre Etch		Post Etch		ER	Pre Etch		Post Etch		ER
	t_m nm	3σ nm	t_m nm	3σ nm	nm/min	t_m nm	3σ nm	t_m nm	3σ nm	nm/min
BCl_3	36.2	0.4	24	2	**12.2**	28	0.7	14.2	0.7	**13.8**
Cl_2	41.3	0.2	39.2	0.3	**2.1**	28.8	0.4	26.7	0.3	**2.1**
CF_4	43.7	0.5	43.3	1	**0.4**	28.8	0.4	27.9	0.4	**0.9**
SF_6	44.5	0.5	45	1.2	**-0.5**	28	0.8	27.4	0.4	**0.6**
HBr	44	1.2	43.6	3.1	**0.4**	29	0.1	29.6	0.9	**-0.6**
NF_3	43	0.4	41.8	0.7	**1.2**	29.1	0.6	27.9	0.2	**1.2**

Table 2. Comparison of dry etch resistance of Al_2O_3 hard masks from IMEC and OSC for various plasma chemistries

The mean thickness t_m of each film is measured before and after a 1 min etch in 6 different etch gases as shown in Table 2. The two negative etch rates are due to contamination leading to a film overgrowth, almost certainly due to carbon.

2.2 ALD Hafnium Oxide – high-k Gate Dielectric

The deposition process for HfO_2 using the FlexAl™ plasma ALD tool from Oxford Instruments is shown below in Table 3. Deposition was carried out at 250 ^{o}C using TEMAH as the source and growth rate ~0.12 nm/cycle. Prior to deposition the silicon wafer substrates were cleaned in HF to remove the native oxide. Samples of ALD-deposited HfO_2 and Al_2O_3 were provided to TUIL from OSC for patterning trials using Field Emission Scanning Probe Lithography (FE-SPL), as described in section 2.3 below.

Funded by
the European Union

Precursors	TEMAH - $Hf(N(C_2H_5)(CH_3))_4$ - liquid bubbled @ 70°C
Non-metal precursors	H_2O thermal, O_3 thermal, O_2 plasma
Temperature range	140°C - 290°C
Growth rate per cycle	1.1 Å/cycle @ 290°C (plasma), 0.8 Å/cycle @ 290°C (thermal)
Deposition rate	0.8nm/min @ 290°C
Refractive Index	2.01 – 2.05 @ 290°C
Uniformity	± 1.5% over 100, ± 2.5% over 150mm, ± 3.5% over 200mm (FlexAL™)

Table 3. ALD process for HfO_2 in a FlexAl™ ALD system.

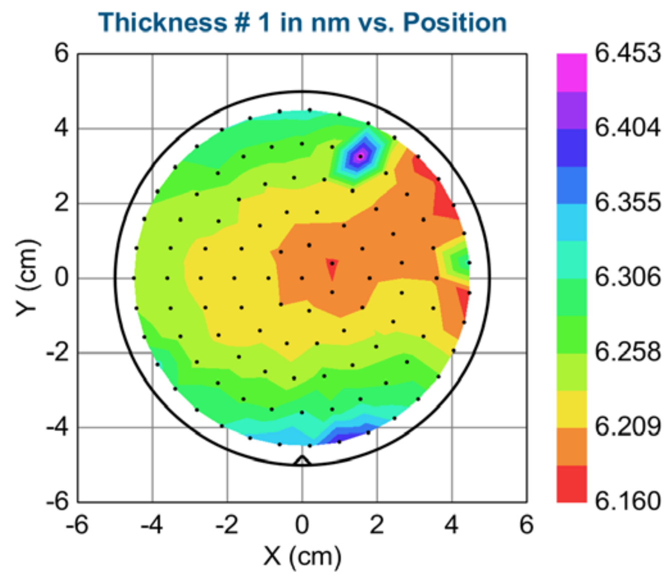


Fig.6 Thickness variation of HfO_2 deposited by ALD in a FlexAl™ tool. Thickness measured using an ellipsometer.

Parameter	Average	Std. Dev.	Minimum	Maximum	Range	# of Points
Thickness vs. Position	6.24884nm	0.05046nm	6.15979nm	6.453nm	0.29321nm	108

Table 4. Thickness variation of HfO_2 film deposited by ALD.

Funded by
the European Union

2.3 Investigation of ALD hard masks for pattern transfer amplification in Field Emission Scanning Probe Lithography (FE-SPL)

In FE-SPL, patterns are defined in ultra-thin molecular glass resist materials using low energy electron exposure. Typical resist layer thicknesses applied are in the range 5 - 40 nm. Since increasing resist layer thicknesses lead to a deterioration of the lithographic resolution capability, resist layer thicknesses ≤10 nm are required. Linked with that, the pattern transfer by plasma etching becomes challenging. Thus, during the initial stage of the project TUIL has investigated hard mask materials applicable to amplified pattern transfer of FE-SPL patterns. Since the current regulation in FE-SPL requires a conductive bottom layer, in case of application of dielectric hard masks (e.g. Al_2O_3, HfO_2) layer thicknesses of ≤7 nm are required in order to measure the current flow. In this context, the preparation of hard mask layers by ALD was favored. OSC provided HfO_2 and Al_2O_3 ALD layers, which were investigated by TUIL for FE-SPL application. However, experiments revealed that the HfO_2 hard mask acts as a catalyst by which the underlying silicon is oxidised by the FE-SPL exposure process. An example is shown in Figure 7, wherein a 6.6 nm thick HfO_2 hard mask is exposed (a) without resist layer on top and (b) with a 20 nm layer of calixarene molecular resist on top. The image reveals that: (a), on pure HfO_2 hard mask layer (without resist layer on top), features with height up to 2-7nm (depending on exposure dose) are measurable directly after lithography. Thus, the hard mask layer itself is altered during FE-SPL exposure by the growth of sub-10 nm features. As discovered, this is linked with an oxidation reaction of the bottom Si layer.

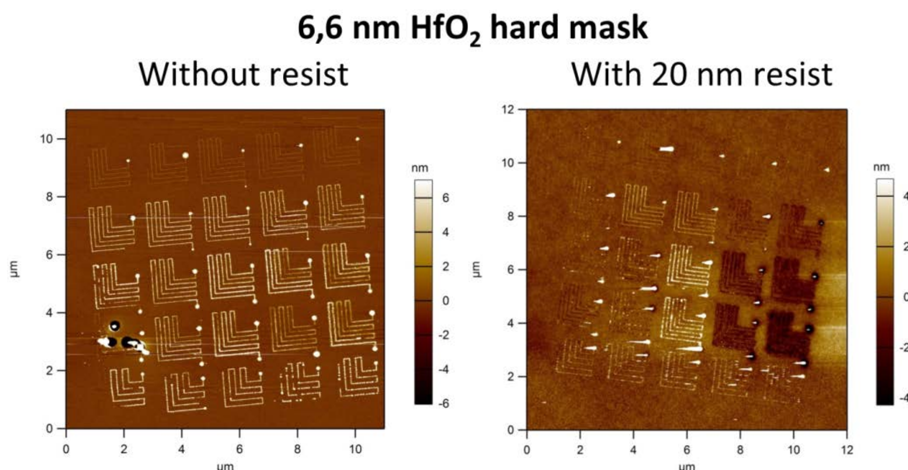


Figure 7. FE-SPL exposure of HfO_2 hard mask layer (a) without resist layer (→ modification of

the HfO_2 hard mask layer itself is visible) and (b) with a 20 nm calixarene resist layer spin-coated on top of the HfO_2 hard mask

According to [4, 5], HfO_2 acts as a catalyzer for Si oxidation. The same oxidation, but with less oxide growth (3-4 times lower compared to HfO_2 hard mask) was observed in the case of Al_2O_3 hard mask layers. In conclusion, a single hard mask layer prepared by ALD is not suited to FE-SPL exposure, since, during exposure, the hard mask is modified. This effect was not investigated further. Instead, TUIL switched from a single layer hard mask strategy to a two layer hard mask stack proposed by Imec. The structure of the hard mask stack is summarized in Figure 8.

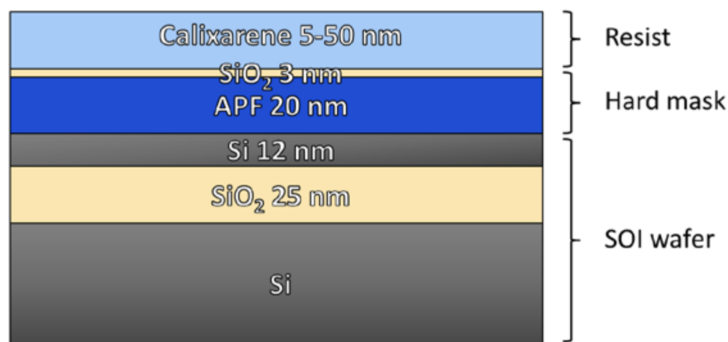


Figure 8. Two-layer hard mask stack consisting of 20 nm APF and 3 nm SiO2 layer suitable for pattern amplification.

A hard mask stack consisting of an APFxHD layer (20 nm) plus top SiO_2 layer (3 nm) were prepared by Imec on top of an ultra-thin top layer SOI wafer. On top of the hard mask stack a calixarene resist layer of thickness ~ 10 nm was PVD-coated by UBT (WP5). FE-SPL exposure tests on the resist-coated hard mask stack has revealed good applicability, as clearly shown in Figure 9. The zoom-in AFM images show 25 nm hp dense line/space features. More details are provided in the frame of the 3rd year project report of WP1. However, as observed, surface roughness and aging / de-wetting effects of the resist on top of the hard mask stack seems to limit the resolution capability.

Advantageously for beyond CMOS (SET) device features, which were targeted by the project, two developments evolved during the intensive WP collaboration, which led to the circumvention of hard masks for pattern transfer amplification: (a) 14 nm etching depths are sufficient since FD-SOI wafer with a top Si layer thickness of 14 nm were applied; (b) The molecular glass resists show sufficient selectivities using a cryogenic plasma etching process that hard mask layers are not required (Selectivities are 4-5 for single component molecular

glass resists; 8-15 for two component hybrid molecular glass resists, ref. WP1/WP5/WP6 reports).

	Complete dose and pitch test field patterned by TUIL using WP1 FE-SPL

Figure 9. Pitch-dose exposure test array example patterned into calixarene molecular glass resist prepared on top of the APF/SiO_2 hard mask stack.

2.4 Variation from the Plan

The ALD enabling processes for dry etch hard mask and high-k dielectric described above were developed in anticipation of a predicted requirement from WP6 and WP8. In the event, this “market pull” did not materialize for the following reasons:

a) The dry etch durability of the new resists developed in WP5 were sufficiently high that hard mask processes were not required.
b) The device partners in WP8 did not require access to the high-k dielectric process developed in anticipation of their needs.
c) Single hard mask layers were abandoned in favour of a stacked layer approach from Imec.

The above changes provided an opportunity to explore a new application for ALD - fabrication of Nano Imprint Lithography (NIL) stamps in a collaboration between OSC and CSIC Barcelona, which is described below.

2.5 ALD for Nanoimprint Lithography Stamp Fabrication

Nanoimprint lithography (NIL) is a rapidly growing technique for fabricating nanometer scale patterns. Advantages of the process include its simplicity, low cost, high throughput and high resolution. Patterns are created by mechanical deformation of imprint resist and subsequent processes. The imprint resist is typically a monomer or polymer formulation that is cured by heat or UV light during the imprinting process. Adhesion between the resist and the template is controlled to allow ease of structure release. In the SNM project a novel approach has been devised to create NIL stamps using a combination of PMMA/Polystyrene bock copolymer and ALD. The schematic in Figure 10 below shows the fabrication process carried out in a collaboration between OSC and CSIC Barcelona.

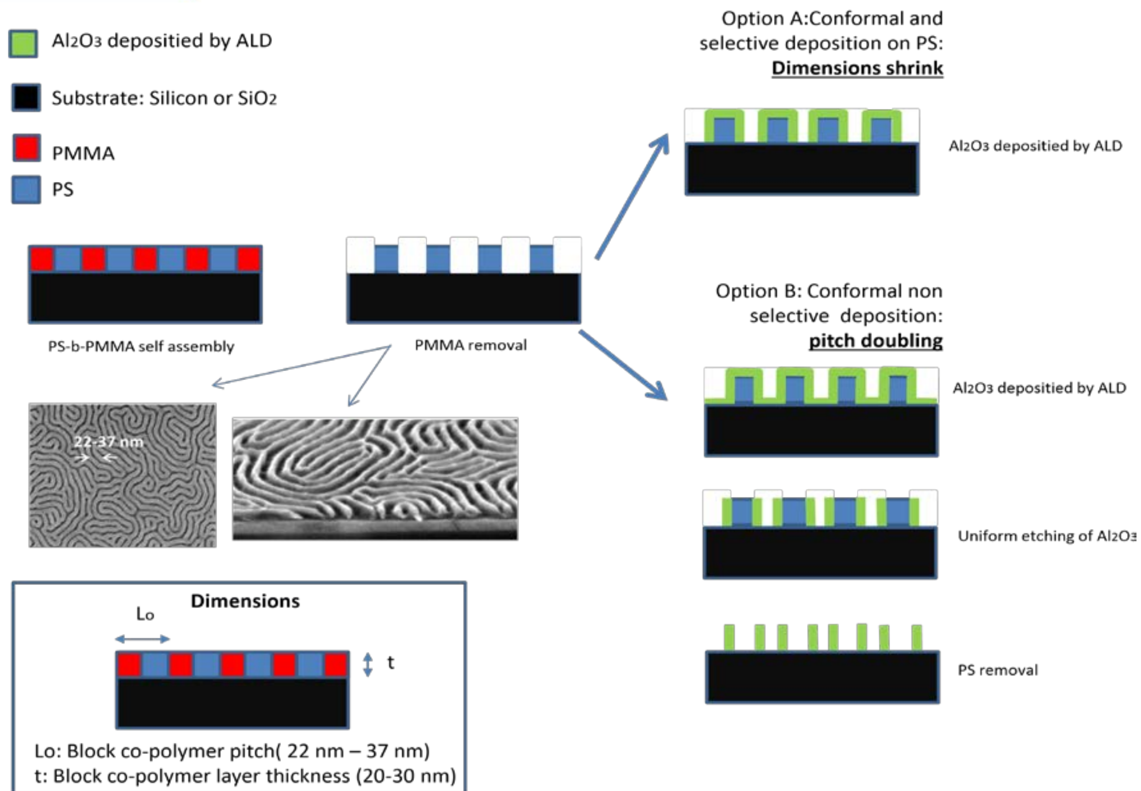


Fig.10. Process sequence for high resolution nanoimprint lithography stamps using a combination of block copolymer films and ALD deposited hard mask for pattern transfer (courtesy of CSIC Barcelona).

The objective is to use atomic layer deposited Al_2O_3 as an etch mask to create high resolution structures in silicon. To begin with, PMMA/polystyrene is coated on a silicon substrate using a self-assembly process creating nanometer scale desired features. The PMMA is then removed leaving the patterned polystyrene in place. The structures in the organic film do not have suitable etch resistance, so that to enable pattern transfer into the underlying silicon using dry etching, a thin conformal layer of Al_2O_3 is deposited by ALD to act as a hard mask. For depositing Al_2O_3 layer as a hard mask on organic resists such as polystyrene and PMMA, the film growth temperature is limited by the melting point of the resist material. The goals of this work therefore included development of an ALD process with a low growth temperature of 80°C and to demonstrate conformal deposition onto the nanostructured organic film.

Both precursors were pulsed for much longer than usual (1 sec compared to 0.015 sec and 0.075 sec) during each step, to allow adequate time for the required chemical reactions at 80°C. The wait time between each step was also much longer (20 sec compared to 12 sec) to ensure a complete purge of the precursors. Several trial deposition runs were carried out on planar silicon substrates followed by thickness measurements using ellipsometer to determine

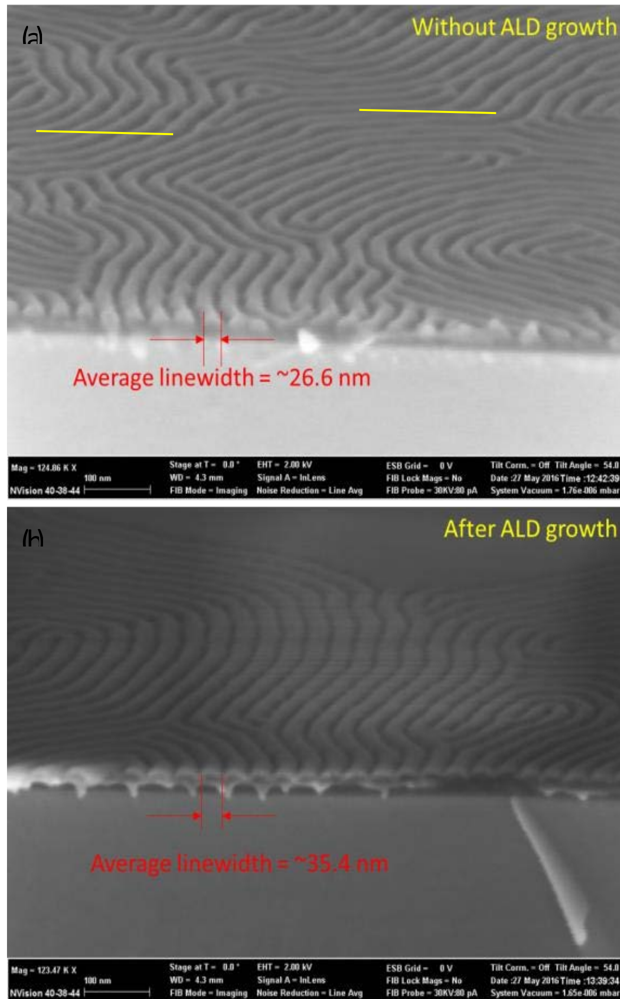
the growth rate.

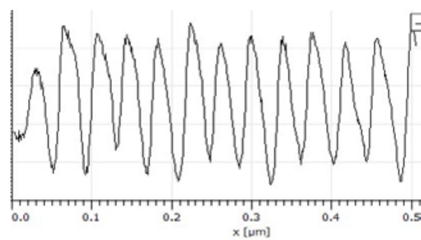
Optimized deposition conditions were used on silicon substrates patterned at CSIC with the organic block co-polymer films. The samples were cleaved and viewed in cross-section using scanning electron microscopy (SEM). The average linewidth of the features in the patterned organic film was measured with and without the ALD growth using SEM. Cross-sectional SEM images (Figure 11) were taken on the patterned polystyrene samples with and without the Al_2O_3 overgrowth. As expected, lines appear thicker with narrower spacing between features after Al_2O_3 ALD growth, shown in Figure 11 (b) compared to Figure 11(a). The average linewidth without the ALD growth is 26.6 nm and 35.4 nm with the ALD overgrowth. The difference between the two confirms that a layer of thickness ~4.5 nm of Al_2O_3 has been grown.

Using plasma etch and the Al_2O_3 hard mask, the nanometer scale pattern can be transferred to the underlying silicon followed by the removal of the hard mask and the polystyrene using the wet etch process described earlier. It will be possible to double the pitch of the structures as shown in the schematic in Fig. 10 above. In partnership with CSIC, OSC will seek to bring these experiments to a conclusion even after the SNM project and they are ongoing at the present time.

The line profiles in Figure 11 show the SE contrast curves along the yellow scan lines in the images, further confirming that Al_2O_3 has been grown using the low temperature thermal ALD process. The average linewidths before and after deposition are 35nm and 44.4nm respectively. Further work is required to achieve pattern transfer into the underlying silicon.

Funded by
the European Union





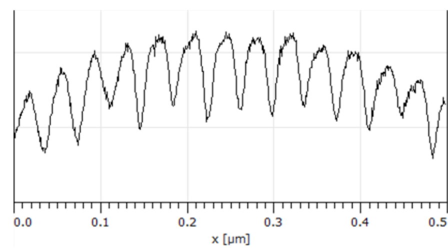


Figure 11. SE contrast curves from the SEM images of patterned polystyrene NIL template (a) without ALD growth and (b) after ALD growth of Al_2O_3 hard mask.Average linewidths before and after deposition are 35nm and 44.4nm respectively.

CONCLUSIONS

Experiments on Atomic Layer Deposition (ALD) were carried out by OSC to develop processes for Al_2O_3 hard mask coatings for use in silicon etch. Both wet etch and plasma dry

Funded by
the European Union

etch experiments were completed. The wet etch rate fell non-linearly with increase in film thickness between 5 nm and 20 nm, which is thought to be due to an increase of annealing effects with deposition time in the thermal ALD process. ALD-grown hard masks of Al_2O_3 and the high-k dielectric HfO_2 were subjected to FE-SPL patterning at TUIL.

It was concluded that, due to FE-SPL induced morphology changes, single layer ALD hard masks are not suited for pattern transfer amplification of FE-SPL patterned features, whereas multi-layer hard mask stacks consisting of a bottom polymer and a top layer oxide are favored. It was found that in order to achieve the main goals of the project, namely fabrication of single-digit nanometer beyond-CMOS electronic devices, no hard mask layers were required for a successful pattern transfer. In contrast, TUIL's attention was focused onto cryogenic plasma etching, which is reported in more detail in WP1 reports (e.g. D1.3 and periodic reports) as well as in D6.9. The strategy of cryogenic plasma etching and application of FD-SOI wafer has been confirmed successfully, which circumvents the requirement of additional hard mask layers. In this context, the PMs spent by TUIL for D6.7 were reduced from the initially planned 5.5 PM to 2 PM. The remaining 3.5 PMs were transferred to D6.9, wherein TUIL report progress in cryogenic plasma etching for pattern transfer of FE-SPL defined features.

Though this work was originally part of the DOW, for use in conjunction with molecular glass resists from WP5, it was less important to the SNM project than originally thought because of the high plasma etch resistance of these resists and the fullerene polymer resists. (For example, the HM01-A resist from OSC/IM, developed in WP5 for particle beam lithography, was found to have an erosion rate of less than 50 nm/min in silicon etch applications). In addition, selected ALD coatings were found to be incompatible with FE-SPL.

As a consequence of these developments, OSC's efforts in the latter part of the project were focused on two alternative applications: an Al_2O_3 hard mask for use with a block co-polymer template of PMMA and PS, intended for fabrication of a stamp for NIL and a conformal coating of HfO_2 for use as a high-k gate dielectric having ~5x the dielectric constant of conventional silicon dioxide gate insulators. OSC's staff effort on D6.7 was reduced from 14 PM to 13 PM by transfer of 1 PM to WP5 for additional work on the HM-01 fullerene resists.

Funded by
the European Union

References

[1] S M George (2010) Chem Rev **110**, 111-131

[2] Y Widjaja and C B Musgrave (2002) J Chem Phys **117**, 10.1063

[3] L Kang, B H Lee, W-J Qie, Y Jeon, R Nieh, S Gopalan, K Onishi, J C Lee (2000) IEEE Electron Device Letters **21**, 181-183

[4] N. Miyata, M. Ichikawa, T. Nabatame, T. Horikawa, and A. Toriumi, "Thermal stability of a thin HfO2/ultrathin SiO2/Si structure: Interfacial Si oxidation and silicidation," *Japanese journal of applied physics*, vol. 42, no. 2B, p. L138, 2003.

[5] M. Park, J. Koo, J. Kim, H. Jeon, C. Bae, and C. Krug, "Suppression of parasitic Si substrate oxidation in HfO[sub 2]–ultrathin-Al[sub 2]O[sub 3]–Si structures prepared by atomic layer deposition," *Applied Physics Letters*, vol. 86, no. 25, p. 252110, 2005.