Collaborative project*

Project acronym: SNM

Project full title: "**Single Nanometer Manufacturing for beyond CMOS devices**"

Grant agreement no: 318804

Deliverable: D8.1 (Initial single-electron and quantum dot devices)

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List of participants:

Participant no.	Participant organisation name	Part. short name	Activity Type	Country
1 (Co)	Technische Universität Ilmenau	**TUIL**	HER	Germany
2	EV Group E. Thallner GmbH	**EVG**	IND; End-user	Austria
3	IMEC	**IMEC**	RES	Belgium
4	Mikrosistemi Ltd	**µS**	SME; End-User	Bulgaria
5	Universität Bayreuth	**UBT**	HER	Germany
6	Technische Universiteit Delft	**TUD**	HER	Netherlands
7	Spanish National Research Council	**CSIC**	RES	Spain
8	IBM Research GmbH	**IBM**	IND; End-user	Switzerland
9	École polytechnique fédérale de Lausanne	**EPFL**	HER	Switzerland
10	SwissLitho AG	**SL**	SME; End-User	Switzerland
11	Oxford Instruments Nanotechnology Tools Ltd	**OINT**	IND; End-user	UK
12	Imperial College London	**IMPERIAL**	HER	UK
13	The Open University	**OU**	HER	UK
14	Oxford Scientific Consultants Ltd	**OSC**	SME	UK
15	VSL Dutch Metrology Institute	**VSL**	IND	Netherlands
15	University of Liverpool	**ULIV**	HER	UK

SNM Work Package 8 Deliverable: D8.1 (Initial single-electron and quantum dot devices)										
Lead beneficiary number	ICL	**Nature**		Report	**Dissemination level**			Public		
Estimated Person-months	12									
Person-months by partner for the Deliverable	ICL									
	3.61									
Estimated Delivery Date	31.12.2013		**Delivery Date**			10.12.2013				
Description of the Deliverable	Please see attached report (pages 3-9).									
Explanation of Differences between Estimation and Realisation	Scientific and technical objectives of the deliverable have been successfully completed. For details, see attached report. The manpower that has been used to date is much lower than had been planned and is indeed much lower than that required to enable the technical results achieved with the completion of Deliverable D8.1. ICL manpower for the first year included allowance for the funding of Research Assistant. A position was approved within Imperial and advertised. Applications were received from 28 individuals, a shortlist of three was identified and interviews were held. A candidate was selected, offered the position, accepted and the processes for appointment initiated. As a non-EU national, a work permit was obtained, but then the process hit a problem. There was initially no response from the candidate. It later emerged that he had been seriously injured in an accident overseas and we had not been notified, and it was only later after the offer was withdrawn that we learnt about this situation. The replacement recruitment process is now in hand. Fortunately, it has been possible to undertake work on the project outside of the EC support. This has enabled good progress to be made, demonstrated by the completion of Deliverable D8.1.									

Silicon Nanowire Single Electron Transistors

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Abstract— Single-electron transistors (SETs), defined in silicon-on-insulator (SOI) material, have been fabricated and characterised at Imperial College London (ICL). The devices are based on heavily doped, *n*-type Si nanowires (NWs) with dual in-plane side gates. SETs were measured from 8 – 300 K, and single-electron operation established from 8 K to ~220 K. 'Coulomb staircase' drain-source current I_{ds} vs. drain-source voltage V_{ds} characteristics were observed at 8 K, and the Coulomb gap could be modulated periodically by gate voltage V_{gs}. The Coulomb staircase persisted up to ~220 K. Single-electron Monte Carlo simulations have been used to explain the details of these characteristics. SET operation may be explained by formation of a multiple-tunnel junction along the Si NW.

1. Introduction

Successful 'beyond CMOS' technology is likely to require new approaches to semiconductor electronic devices, in combination with lithographic and fabrication technology at the sub-5 nm scale [1]. The SNM project is investigating technology platforms based on a combination of high resolution Scanning Probe Lithography (SPL) and Nano Imprint Technology (NIL) with highly nanoscale single-electron and quantum dot devices. In large-scale integrated (LSI) circuit applications, as planar MOSFET scaling limits are reached, in the near-term a transition may occur from non-planar fin-FET devices to Si nanowire FETs. Here, the channel cross-section can be scaled in both dimensions to ~10 nm, gates fully surrounding the channel, and the devices remain mainly 'classical' in nature. However, a far greater technological challenge is a subsequent transition to quantum-effect devices with scaling in all three dimensions to < 5 nm, e.g. single-electron and quantum-dot (QD) based devices [2, 3]. These devices, unlike 'classical' devices, inherently tend to improve in performance with reduction in size.

We now report on the fabrication and measurement of individual single-electron transistors (SETs) defined in silicon-on-insulator (SOI) material, for future integration with SNM lithography and fabrication processes [1, 4]. The devices are based on heavily doped, oxidised Si nanowires (NWs), with dual in-plane side gates and have been fabricated by electron beam lithography (EBL) at ICL [4]. Single-electron operation has been established from 8 K to ~220 K. 'Coulomb staircase' drain-source current (I_{ds}) vs. drain-source voltage (V_{ds}) characteristics have been observed at 8 K, and the Coulomb gap modulated periodically by gate voltage V_{gs}. The Coulomb staircase persisted up to ~220 K. Single-electron Monte Carlo simulations have been

used to explain the details of these characteristics. SET operation may be explained by formation of a multiple-tunnel junction along the Si NW.

2. FABRICATION

EBL and trench isolation have been used to fabricate Si NW SETs in SOI material. Devices with NWs width down to 30 nm and length 1 μm have been defined. Figure 1(a) shows a schematic diagram of the device. The Si NW and dual, in-plane gates parallel to the NW were defined in the top Si layer of the SOI material, using EBL and reactive-ion etching for trench isolation from the gates. The NW current was controlled using one or both gates. SEM images of a NW SET are shown in Figures 1(a) and 1(b). Here, the NW is 40 nm in width and 1 μm in length. Trenches ~200 nm deep were used to define the device pattern. Oxidation of the structure was used to thin the Si core of the NW to ~20 nm.

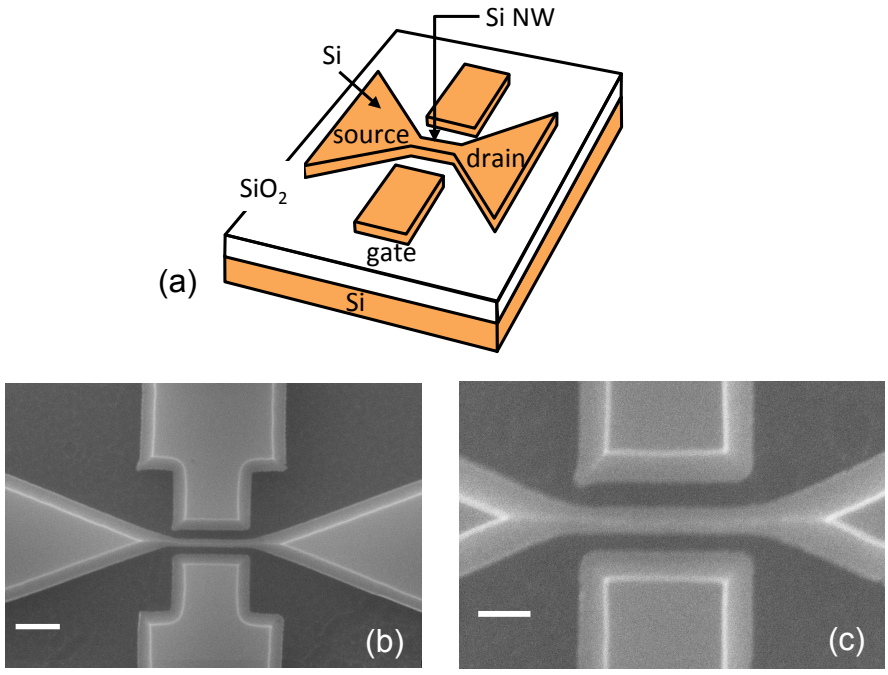

Figure 1. (a) Schematic diagram of a Si NW SET in SOI material. (b) SEM image of a Si NW SET with dual, in-plane gates. Scale bar is 1 μm (c) Magnified image, scale bar 400 nm.

In our Si NW SETs, roughness in the SiO_2/Si interface, in combination with disorder in the interface state density, can pinch-off sections of the NW and create a chain of tunnel barriers and conducting islands or quantum dots (QDs) along the NW. Such a multiple-tunnel junction (MTJ) device can show strong single-electron effects, with the maximum operating temperature determined by the charging island size and/or the heights of the tunnel barrier. Furthermore, for a Si island ~20 nm or less in size, the quantum confinement energy E_k ~0.01 eV or larger [1]. This

implies that at low temperatures below ~100 K, E_k will contribute to the Coulomb blockade of the island. The addition energy needed to add an electron to the island is then $E_a = E_k + E_c$, where $E_c = e^2/2C$ is the single-electron charging energy and C is the total island capacitance. For a Si island ~20 nm or less in size, E_c ~0.02 eV or larger [1]. The Si NW SET then shows a combination of MTJ and QD behaviour, with the addition energy for each island/QD ~ 0.03 eV.

Details of the fabrication process are as follows:

(i) Top Si layer thinning:

A SOI wafer with a 120 nm thick top Si layer, was oxidised at 1100°C for 2 hours, with a ramp time of 1 hour. This forms a ~200 nm thick SiO_2 layer, capping the top-Si. The process consumed close to ~100 nm of the top-Si, resulting in a top Si layer as thin as ~20 nm. A 5 min HF dip was then used to remove the unwanted SiO_2 cap.

(ii) Spin-on-doping (SOD):

The nanowire SETs were fabricated in an *n*-type, phosphorous doped SOI (100) wafer (resistivity $\rho \sim 10^{-3}$ Ωcm). A SOD layer using phosphorus dopant was spun-on at 2000 rpm for 45 sec, forming a layer ~ 3 μm thick. The layer was then baked at 200°C for 10 minutes, until solid. A rapid thermal annealing (RTA) process in nitrogen ambient, 2 minutes long and at 950 – 1000°C, was used for dopant diffusion. Our aim was a doping concentration of ~10^{19} or greater. This was confirmed using 4-point probe measurement of resistivity.

(iii) SET pattern definition:

SET patterns were exposed using EBL, with PMMA resist. A single-pass line, at a line exposure dose of 2 nC/cm, was used to define the NWs. After development in MIBK/IPA, this left a sub-50 nm wide developed NW. The source, drain and gate lead-in areas, aligned with the NWs, were exposed using an areal dose of 300 μC/cm^2. A lift-off process was then used to transfer the pattern of the NW and lead-in areas into metal (usually Al). Optical lithography was then used to define the bond-pad regions in metal, aligned to the EBL patterns. This was followed by reactive ion etching in SF_6, to transfer the NW/lead-in area/bond-pad patterns into the Si. Trenches ~200 nm deep were etched with an etch time of 1 minute, to trench isolate the NW from the gates. The samples were then passivated by thermal oxidation at 1000°C for 15 minutes. This process creates tunnel barriers / islands along the NWs, and reduces the Si core in the NW, estimated to be in the range ~10- 20 nm.

(iv) Ohmic contact and wire bonding:

The devices used Ohmic contacts, formed by evaporation of 20 nm Cr / 200 nm Al layers. The contacts also formed the device bond pads. SETs were arranged as groups of four within a 100 μm square field, and connected to 12 bond pad regions surrounding the field. Finally, all the bond pads were bonded using Au wire, for electrical measurement.

3. ELECTRICAL CHARACTERISTICS

Figure 2(a) shows Coulomb staircase I_{ds}-V_{ds} characteristics of a Si NW SET, measured with an Agilent 4155B parameter analyser, from 8 K to 160 K. The curves here are offset 0.1 nA per temperature step for clarity. In this device, the NW Si core diameter was estimated to be < 20 nm, and the NW length was ~1 µm. The long NW length implies that a MTJ can exist along the NW. At 8 K, the first step occurs at ~7 V. In the MTJ system formed along the NW, the Coulomb gap and step widths are large as they are a function of the charging energies of many islands along the NW. The step width reduces with increasing temperature, as thermally activated current increases and single-electron effects are overcome in the larger islands, which have smaller charging energies. Figure 2(b) shows the Coulomb staircase at 8 K, as a function of gate voltage V_{gs}. As V_{gs} increases from 0 V to 30 V, a series of Coulomb diamonds can be observed. Here, the diamonds cannot be fully modulated by the gate voltages, as some of the MTJ islands do not couple to the gate.

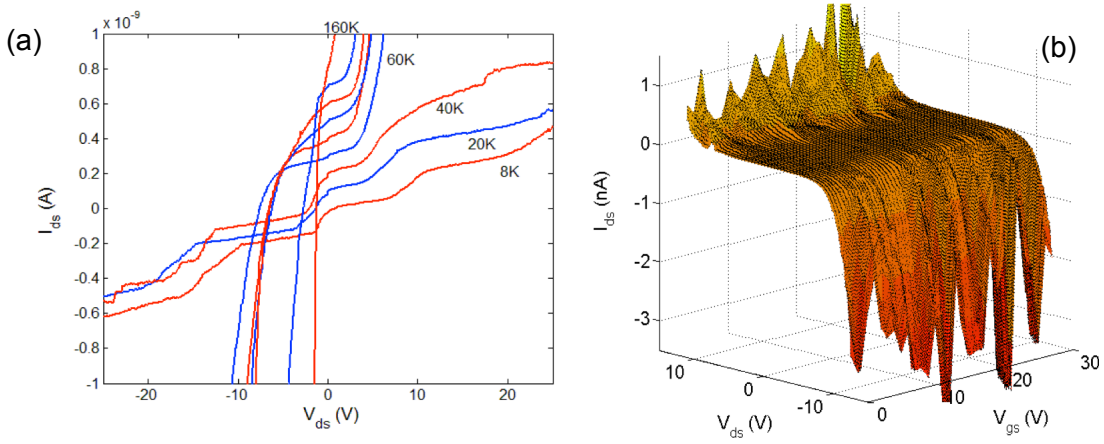

Figure 2. (a) Coulomb staircase I_{ds}-V_{ds} characteristics in a Si NW SET, from 8K – 160K. Curves offset 0.1 nA per temperature step for clarity. (b) Coulomb staircase at 8 K, modulated by gate voltage V_{gs}.

The temperature dependence of the I_{ds}-V_{ds} characteristics, from 8 K to 300 K, is shown in Figure 4, on log (a) and linear (b) scales. The Coulomb staircase persists up to ~220 K, beyond which it is thermally overcome. A low-current Coulomb blockade region is observed up to

~140 K. A maximum temperature for single-electron effects of ~200 K suggests an effective MTJ single-electron charging energy ~17 meV and capacitance ~5 aF. Room temperature operation requires a reduction of this to ~1 aF or less.

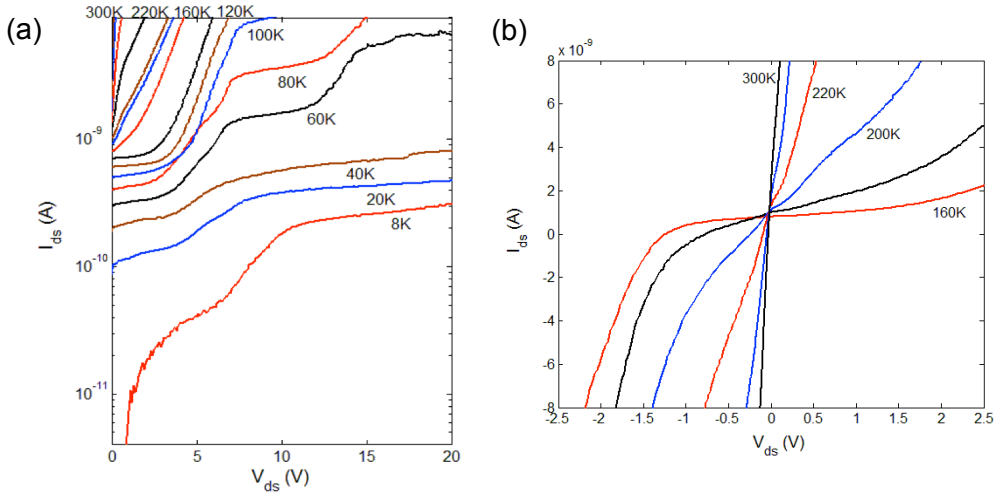

Figure 3. Temperature dependence of the I_{ds}-V_{ds} characteristics of a NW SET. (a) Log scale, from 8 – 300 K. (b) Linear scale, 160 – 300K.

The electrical characteristics may be explained using single-electron Monte Carlo simulation to model the device. We assume a MTJ formed by an array of tunnel capacitors C_n, with the intermediate 'island' regions coupled by gate capacitance C_g to the gate voltage (Fig. 4(a)). For an MTJ NW SET formed by 10 islands, at temperature T = 4.2K and with $C_n = C_g$ = 0.12aF, the simulated Coulomb staircase characteritics are shown in Fig. 4(b) with all islands coupled to the gate, and (c) with one island coupled to the gate. Our experimental characteristics lie between these two characteristics, suggesting that only some of the islands in the MTJ are coupled to the gate.The capacitance values are chosen from our previous work on ~10 nm diameter islands [5]. The tunnel resistances are varied to allow a Coulomb staircase rather than a linear increase in current outside the Coulomb gap. The Coulomb blockade regions near V_{ds} = 0 V are modulated periodically by V_{gs}, forming 'diamond' shaped regions where the total electron number varies by one.

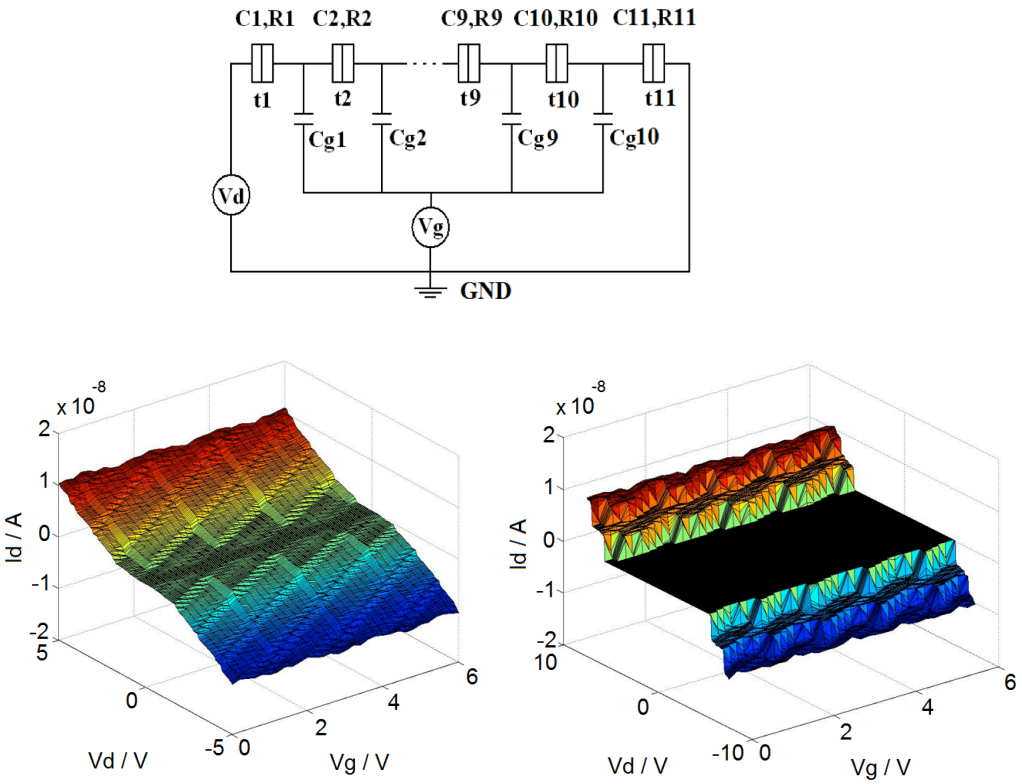

Figure 4. Monte Carlo simulation of Coulomb staircase. (a) MTJ circuit diagram. (b) *I-V* characteristics for a 10 island MTJ with all islands coupled to the gate, and (c) only the central island coupled to the gate.

4. Conclusions

We have fabricated and electrically characterised Si NW SETs, defined in SOI material, for future integration with SNM lithography and fabrication processes. The devices are based on heavily doped, oxidised Si nanowires (NWs), with dual in-plane side gates and are fabricated by EBL at ICL. The width of the Si NW as written by EBL is ~30 nm. Following oxidation, the width of the Si core is estimated to be ~20 nm. Single-electron operation has been observed in the temperature range 8 K to ~220 K. 'Coulomb staircase' I_{ds}-V_{ds} characteristics have been observed at 8 K, and the Coulomb gap can be modulated periodically by gate voltage V_{gs}. The Coulomb staircase persisted up to ~220 K. Single-electron Monte Carlo simulations have been used to explain the details of these characteristics. SET operation may be explained by formation of a multiple-tunnel junction along the Si NW.

5. REFERENCES

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