SNM
Work Package 8
Deliverable: D8.4 ("Room temperature operation of a single electron transistor")

Addendum

Author	• Mervyn Jones and Zahid Durrani	
Reviewed by:	• WP 8 Leader: Zahid Durrani • WPG 3 Leader: Zahid Durrani • Coordinator: Ivo W. Rangelow	
Criteria and Achieved Results	**Criteria of Achievement**	**Summary of Achieved Results**
	5. The fabrication by Field Emission Scanning Probe Lithography (FE-SPL) of RT operating SETs	Initial results have been achieved in fabricating and electrical characterising a RT operating SET, defined using FE-SPL and geometric oxidation.
Description of the addendum	Preliminary work is reported on the use of the field emission scanning probe lithography (FE-SPL) in conjunction with geometric oxidation to fabricate devices showing RT SET characteristics. Various developments and additions that have been made to the original deliverable D8.4 are listed below.	

Room temperature operation of a single electron transistor

Abstract

Additional to the already reported EBL devices, initial results are presented on the development of RT SET devices using FE-SPL and geometric oxidation on IMEC patterned thin Si SOI wafers. A more comprehensive study of SPL- defined room-temperature operating SETs will be reported in D8.5.

RT QD development with SETs defined using FE-SPL at TUIL

In a collaboration between TUIL and ICL work has started on the design, fabrication and testing of point-contact room-temperature operating SET devices. Details of the fabrication process for these devices have been described in depth in milestone MS17 and are therefore not repeated here. However, summarising, ultra-thin SOI chips with a top Si layer ~12 nm thick and highly *n*-doped at $>10^{20}$ /cm^3 were used. The top SOI layer was pre-patterned to give a central Si square where active devices could be made with leads to contact pads. The line features were defined by a direct ablation process of a molecular glass resist material, triggered by the field electron exposure emitted from cantilever tip of the field-emission scanning probe lithography (FE-SPL) tool. The line pattern was transferred into the silicon layer by cryogenic plasma etching. The basic concept of the SET device structure using this method is shown schematically in Fig. 13. Geometric oxidation is used to form the actual device, by isolating QDs within the nanoscale SiO_2 region formed at the point-contact neck.

Devices were measured electrically to determine the existence of RT SET operation. As the basic point-contact SET layout is similar to EBL defined devices, similar characteristics are expected. Measurements at RT from an initial device are shown in the Fig. 14.

The results of Fig. 14 show an RT Coulomb blockade characteristics very similar to the EBL fabricated devices. Two large low-current Coulomb diamond-like regions (dark blue central regions, lower plot), with an additional, finer oscillation, can be seen. However, this central region is very broad, implying the existence of a significant series or underlying potential barrier in addition to the QD (Sec. 2 of original deliverable D8.4).

A more extensive discussion and further results of SPL- defined room-temperature operating SETs will be reported in D8.5.

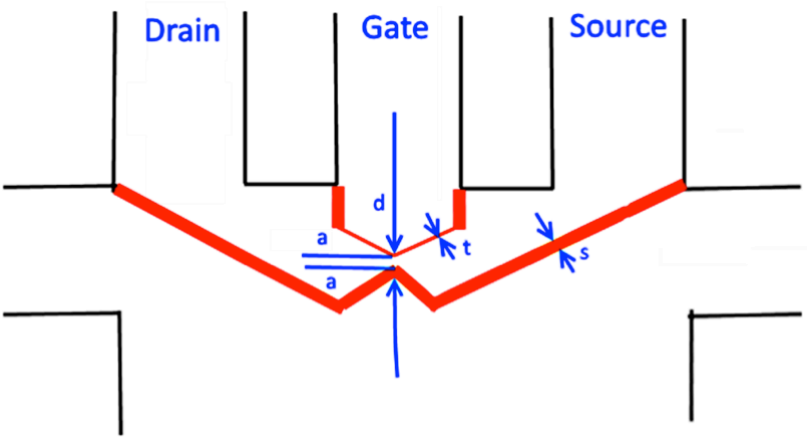

Figure 13 Schematic diagram showing the principles of SET fabrication using a pre-patterned wafer, FE-SPL exposed resist and cryo-etching of the silicon, followed by oxidation and contact formation. The red lines show regions for FE-SPL and cryogenic etching.

Device: Box10_S9_D11_G5

ed for 5 min. at 850°C

- *Probed measurements at 290 K*

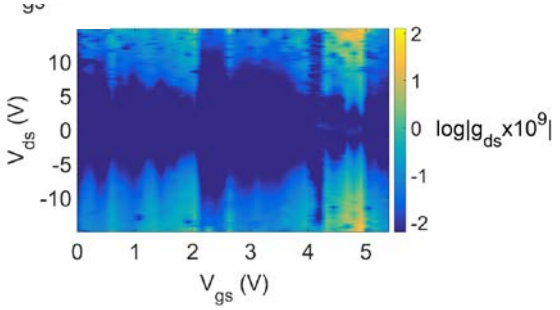

Fig. 14 The RT characteristics of Device 10_S9_D11_G5 are shown as a 3D plot of I_{ds} vs. V_{ds} and V_{gs} and as a linear colour plot of log $|g_{ds} \times 10^9|$ vs. V_{ds}, V_{gs}. These results show clearly the existence of a Coulomb gap and several coulomb diamonds, indicating RT SET behavior.