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Collaborative project*

Project acronym: SNM

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Deliverable: D8.5 ("Room temperature quantum dot devices")

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3	IMEC	**IMEC**	RES	Belgium
4	Mikrosistemi Ltd	**µS**	SME; End-User	Bulgaria
5	Universität Bayreuth	**UBT**	HER	Germany
6	Technische Universiteit Delft	**TUD**	HER	Netherlands
7	Spanish National Research Council	**CSIC**	RES	Spain
8	IBM Research GmbH	**IBM**	IND; End-user	Switzerland
9	École polytechnique fédérale de Lausanne	**EPFL**	HER	Switzerland
10	SwissLitho AG	**SL**	SME; End-User	Switzerland
11	Oxford Instruments Nanotechnology Tools Ltd	**OINT**	IND; End-user	UK
12	Imperial College London	**IMPERIAL**	HER	UK
13	The Open University	**OU**	HER	UK
14	Oxford Scientific Consultants Ltd	**OSC**	SME	UK
15	VSL Dutch Metrology Institute	**VSL**	IND	Netherlands
16	University of Liverpool	**ULIV**	HER	UK

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SNM
Work Package 8
Deliverable: D8.5 ("Room temperature quantum dot devices")

Lead beneficiary number	12 ICL	**Nature**	R	**Dissemination level**	PU					
Estimated Person-months	15									
Person-months by partner for the Deliverable	ICL	TUIL								
	29.1	5.85								
Estimated Delivery Date	31.12.2016	**Delivery Date**	09. 02. 2017							
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Reviewed by:	• WP 8 Leader: Zahid Durrani • WPG 3 Leader: Zahid Durrani • Coordinator: Ivo W. Rangelow									

Criteria and Achieved Results	**Criteria**	**Achieved result**
	1. Design of quantum dot (QD) device structures to enable single-electron transistors (SETs) and multi quantum dot device to be measured.	Circuits have been designed enabling multiple device structures using several different lithography tools (Electron beam lithography (EBL), Electric field SPL (EF-SPL), and thermal SPL (t-SPL).
	2. Fabrication of individual point-contact QD device structures in SOI layers.	Devices with a variety of designs fabricated, on two different types of SOI wafers, enabling successful 290 – 10 K electrical characterisation.
	3. Electrical measurements of QDs at room temperature (RT) – i.e. 290 K.	QD characteristics at RT observed, with both charging and quantum confinement, in EBL and SPL devices.
	4. Measurement of RT QD temperature dependence, and extraction of electrical device parameters.	Observation of QD electron addition energy ~0.8 eV, resonant tunnelling through excited states, and modeling of thermal behaviour of QD states.

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	5. Measurement for coupled double QD (DQD) devices.	DQD operation at RT observed, confirmed by Monte Carlo simulation. First observation of these effects at RT.
Description of the Deliverable	• Quantum dot devices fabricated using both EBL and SPL, using two types of silicon-on-insulator (SOI) wafers, and characterised electrically at RT. • The devices use thin (~10 nm) heavily-doped (> 10^{20}/cm^3) *n*-type Si layers, and geometric oxidation of a point-contact forms a key step in their fabrication. • Strong 'Coulomb diamond' characteristics have been observed at RT in the drain-source current I_{ds} vs. drain-source voltage V_{ds} and gate voltage V_{gs} characteristics. These allow extraction of QD size. Here, QD diameter ~1.6 nm. QD addition energy E_a = 0.8 eV, the highest yet reported. Resonant tunnelling through excited states in the QD is also observed at RT. • Statistics have been collected from 19 SETs working at RT. The maximum probability of obtaining an RT SET is ~11%, for 20 nm pre-oxidation point-contact width. The QD radius r lies in a relatively narrow band, 0.8 nm < r < 2.35 nm, given the single nanometre scales involved, with mean 1.47 nm. The most likely origin of the QD is the potential well formed by a donor atom embedded in the thin SiO_2 region formed by geometric oxidation of the point-contact neck. • Operation of RT SETs fabricated by both EF-SPL at TUIL and t-SPL at IBM has been confirmed. Fabrication of more advanced SET inverter and a SET memory devices using SPL has been demonstrated. • The electrical characteristics of double, electrostatically coupled QD devices operating at RT have been observed experimentally, and simulated theoretically. Here, the two QDs may be formed by two donor atoms. • Nanogap transistors in SOI, fabricated using a modified point-contact fabrication process at ICL, have been used for electron beam induced deposition (EBID) QDs at TUD. Measurements of these devices have been conducted at ICL.	
Differences between Estimation and Realisation	1. Scientific and technical objectives of the deliverable regarding the fabrication and operation of multiple RT quantum effect devices have been successfully completed. Here measurements are provided demonstrating RT quantum effects in single and double QD devices, fabricated both by EBL and by two different SPL techniques (in collaboration with IBM/SL and TUIL). An additional SNM device configuration, using EBID QDs at TUD, has also been fabricated and measured. While the EBID devices did not explicitly form part of the original objectives, very promising results regarding nanostructure deposition at TUD allowed the direct incorporation of these methods into Si quantum device structures. The work demonstrates a third SNM nanodevice technology, in addition to SPL and EBL methods. For details, see attached report.	

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	2. Our emphasis on fully establishing the fabrication and operation of SPL and EBID RT quantum devices, following up from the Year 3 review recommendations, resulted in effort being diverted away from magnetic field measurements of our QDs (spin blockade and the possibility of qubit formation). Here, the decision was taken to concentrate on SNM fabrication techniques for new devices, rather than additional measurements on existing EBL devices. 3. The total PM for the deliverable are 34.95 PM, much greater than the originally envisaged 15 PM. This is mainly due to greater effort than planned, to both fabricate and measure multiple working RT devices, with the cores defined using different SNM methods. Furthermore, measurements (particularly temperature dependences) have proved to be more time consuming than originally envisaged. The additional PM were transferred from D8.1, D8.2, D8.4 and T-10-10. The deliverables of WP8 were underspent due to issues by hiring the personnel (explained in the deliverable reports) and in WP10 no electrical characterization took place.
Metrology comments	With the negligible electron contrast difference between Si and SiO_2, assessment of dimensions of a <5 nm Si island, encapsulated within a SiO_2 layer by SEM is currently extremely challenging. Creation of a TEM lamella or trench through the actual device structure (as opposed to a test structure, e.g. a long nanowire of the same cross-section) is also highly difficult. Hence, QD size is extracted from the physics of the electrical measurements.

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Room temperature quantum dot devices

Abstract

Single-electron quantum dot (QD) devices, defined in silicon-on-insulator (SOI) material, have been fabricated and electrical characterisation undertaken. The devices are based on SOI wafers heavily doped at IMEC, with an ultra-thin (~10 nm) *n*-type top Si layer. Electron beam lithography and a geometry dependent controlled oxidation process is used to isolate single or double QD single-electron transistors (SETs). Here, oxidation of silicon point-contacts, with either single or dual in-plane side gates, enables <10 nm point-contact channels to be defined and controlled. This work extends the work reported in D8.4, where early work on single QD SET devices operating at room temperature (RT) using this process was reported.

In this deliverable, full QD operation at RT, with observation of both charging and excited quantum confinement states, is reported. Furthermore, both single and double-coupled QD operation is demonstrated, and the presence of ultra-small, few nanometre scale QDs in multiple devices verified. Electrical characterisation results from RT down to temperatures of ~100 K are discussed. A remarkably large QD electron addition energy E_a ~ 0.8 eV = 30 k_BT at 290 K, the largest yet reported, has been obtained. Here, the quantum confinement energy ~0.3 eV, implying the formation of a QD only ~1.6 nm in size. In measurements of 19 RT devices, the extracted QD radius lay within a narrow band, from 0.8 nm to 2.35 nm, emphasising the single-nanometre scale of the QDs and the reliability of the fabrication processes. Here, the likely origin of the QD is a potential well formed by a donor atom embedded in the thin SiO_2 region formed by geometric oxidation of the point-contact neck. In dual-gate measurements, hexagonal charge stability regions, a signature of double, electrostatically coupled QDs, are observed at RT. These results are reproduced using single-electron Monte Carlo simulation, verifying the double QD origin of the data.

Work undertaken with partners (TUIL, IBM/SL, TUD) is also reported, where additional lithographic and fabrication techniques developed within SNM are used to fabricate RT SET devices. The RT operation of SET devices, defined using scanning probe lithography (SPL), has been demonstrated in collaboration with TUIL and IBM. The fabrication of a single-electron inverter structure with TUIL, and a memory device in collaboration with IBM and SL is demonstrated. Finally, results are reported of investigations performed in collaboration with TUD, to fabricate and characterise QD transistors formed using an electron beam deposited metallic QD, inserted into a nanogap transistor structure.

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1. INTRODUCTION

During the last 40 years, by reducing device dimensions and developing new device structures, CMOS technology has delivered dramatic and continuous improvements in the speed, complexity and packing density of integrated circuits. At the scaling limit for planar MOSFET devices, a transition to non-planar Fin-FET devices for the 14 nm device node and beyond is already occurring. However, increasingly challenging barriers are being encountered in both device physics and technology. In addition to the major technological challenges posed by any successor 'beyond CMOS' technology at these scales (< 10 nm), quantum effects are increasingly likely to influence the behaviour of all these devices adversely, even those which are not specifically quantum-dot (QD) devices. Developing quantum electronics into a practical technology requires devices at the single-nanometre scale, which both operate at room temperature (RT) and are manufacturable. Single nanometre quantum dots (QDs) have great potential in this regard, for applications in 'beyond CMOS' nanoelectronic circuits, quantum computation, single molecule sensing, and energy scavenging. QD transistors are particularly attractive because, unlike 'classical' transistors, a reduction in size inherently improves their performance. Quantum dots may now be defined towards the single nanometre scale, or even by a single donor atom, of great interest for quantum computation devices.

A far greater technological challenge is a subsequent transition to quantum-effect devices, with scaling in all three dimensions to < 5 nm, e.g. single-electron transistor (SET) and quantum-dot (QD) based devices. These devices, unlike 'classical' devices, inherently tend to improve in performance with reduction in size. Here single-electron (SE) devices look increasingly attractive where, unlike 'classical' FETs, these devices inherently show performance improvements with reduction in size. Single-electron transistors (SETs) operating at room temperature (RT), where the presence of a sub-10 nm scale 'island' or QD for single-electron charging is essential, have been reported by several groups using various approaches. These include QDs formed 'naturally' within Si nanowires in the presence of surface roughness or doping disorder, high-resolution lithographic and pattern dependent oxidation of nanowires and point contacts to define QDs in a more controlled manner, Si nanocrystals and nanochains using QDs formed by material synthesis, and ultrathin Si channels where surface roughness forms QDs. High-resolution lithography is essential for many of these approaches, either to pattern the QDs directly, or in combination with material synthesis methods.

In this report we show how conventional technology can be developed for the fabrication of QD devices. In the first section we describe how this has been achieved using electron beam lithography to fabricate devices, which have shown RT QD operation and have been extensively characterised. This work extends the device work reported in D8.4, where earlier work on SET devices operating at room temperature (RT) using this process had been reported. We also show the results of investigations into how double QDs behaviour occurs at RT within dual-gated point-contacts. In subsequent sections we show (a) the RT operation of SET devices made using electric field (EF) SPL at TUIL, and building on this work, the fabrication of a SPL defined SET inverter; (b) work in progress in collaboration with IBM and SL, again using thermal SPL, to fabricate a SET memory structure; and (c) work with TUD to fabricate SET devices using focused electron beam deposition (FEBD), to deposit a metal dot in a predefined nanogap between the silicon source and drain electrodes of a device.

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In this deliverable we present results which:

(i) Describe the fabrication and measurement of individual QD single-electron transistors defined in silicon-on-insulator (SOI) material using a geometry dependent EBL and oxidation process.
(ii) Explain the device characteristics including the first identification of RT quantum confinement excited states.
(iii) Present statistical information that relates the QD size to RT SET operation, and raises the likelihood of a donor atom origin for the QDs.
(iv) Describe results on the fabrication and operation of double, electrostatically coupled QD devices operating at RT.
(v) Report on results from a collaboration with TUIL on devices fabricated by EF-SPL, which shown RT SET operation. In addition there is initial work towards the SPL fabrication of a SET QD inverter circuit.
(vi) Describe some developmental work undertaken in collaboration with IBM and SL using SPL to form a SET-based memory circuit.
(vii) Report experiments undertaken in collaboration with TUD in which the QD was a deposited metal dot or nanowire, defined using a novel technique of electron beam deposition. Here, the electrical characterisation results from RT – 50 K are reported.

2. RT QD SET DEVICES MADE BY EBL

In D8.3 and D8.4 a description had been given of how SET devices were defined in heavily doped *n*-type Si nanowires (NWs) formed on silicon-on-insulator (SOI) material, with dual in-plane side gates fabricated by electron beam lithography (EBL). Originally, these devices had been formed in Si NWs where the lengths had been varied from 1 μm to ~100 nm, with widths down to ~50 nm, but the results suggested the strong potential of a point-contact SET design for RT SET fabrication. Hence, the development of the devices has continued on this basis[1].

[1] The work presented in this section has been accepted for publication:

"Excited states and quantum confinement in room temperature few nanometre scale silicon single electron transistors", Durrani, Z, Jones, M, Wang, C, Liu, D, Griffiths, J, *Nanotechnology* 28, 125208 (2017), https://doi.org/10.1088/1361-6528/aa5ddd

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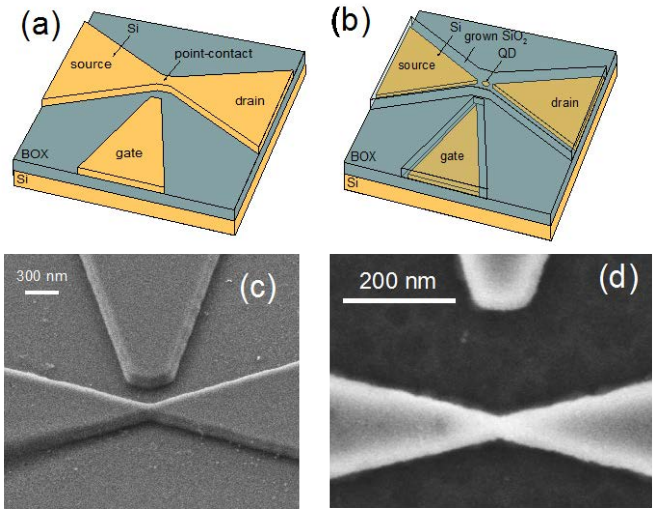

Figure 2.1 Device fabrication using geometric patterning. (a) Schematic diagram of a silicon-on-insulator wafer with *n*-type, degenerately doped (>10^{20} /cm^3) top silicon thinned to 20 nm or less, defined by electron beam lithography, and plasma etched to leave a narrow point contact. There is an overlap between two triangular EBL patterns defines and controls the central point-contact width. (b) Following oxidation at 850ºC, the silicon is both thinned and a quantum dot (QD) formed between the source (S) and drain (D). A side gate (G) controls the QD characteristics. (c) Scanning electron micrograph (SEM) of the final device, taken at high angle to show the etched and oxidised device structure on the buried oxide (BOX). The QD is encapsulated within the oxide at the centre of the S/D contacts. (d) A second device seen at higher magnification, from a plan view orientation.

A key step in the QD fabrication process is the geometric oxidation step, which is outlined in to Figure 1. **This process concept forms the basis for the device definition using EBL, and has also been adapted in various different ways for the work done in collaboration with TUIL, IBM-SL and TUD**. Here, a source, drain and gate structure is defined in a thin silicon layer (thickness ~ 10 – 30 nm) on top of the buried oxide (BOX) layer of an SOI wafer, seen in (A). When this is heated in a dry oxygen rich environment, the surfaces oxidise and at the point-contact 'neck' between the source and drain an island, or QD, forms. Oxidation is self-limiting at the centre of the neck, due to increasing stress in the Si core. At the edges of the neck, reduced stress allows greater oxidation and pinches off the Si core from the source and drain regions, forming tunnel barriers and isolating a Si island. Thus the ability to form the island is determined by the lithography and shape of the defined silicon neck, and the degree of oxidation. The exact nature of this QD is discussed later. The full details of the fabrication process have been reported in D8.4 and are not repeated here

Chips have been used which have dimension of either (a) 10 mm × 10 mm, in which 16 'chiplets', each having an overall dimension of 1.6 mm square are arranged in a 4 × 4 array, or

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(b) 15 mm × 15 mm in which 20 of the same ‘chiplets’ are arranged as a ‘picture frame’ around the edges of the chip. These chiplets contained 8 devices within a central area of 200 µm × 200 µm, each of which could be individually characterised, with access from 20 contact pads around the periphery of the chiplet. An optical micrograph of this central area with the 8 devices is shown in Figure 2.2.

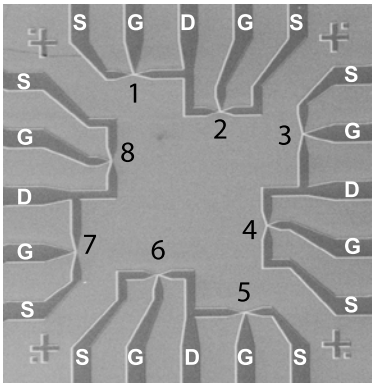

Figure 2.2 Layout of one of the 16 mini-chips showing the central area containing 8 numbered transistors, and a single side gate

2.1. ELECTRICAL CHARACTERISATION OF RT SET DEVICES MADE BY EBL

The room temperature (RT = 290 K) measurements of drain-source current (I_{ds}) vs. drain (V_{ds}) and gate (V_{gs}) voltage were made using a probe station under the control of an Agilent 4155B parameter analyser, and subsequent analysis was undertaken using Matlab. The measurement process is identical to that reported in Deliverable D8.4. The RT ‘Coulomb diamond’ characteristics for a single nanometre scale QD (QD1) are shown in Fig. 2.3. Here, the QD diameter is estimated to be only ~1.6 nm (value extracted from electrical characteristics, see below). The characteristics are plotted (a) using a 3-D plot, and (b), as log|I_{ds}| vs. V_{ds}, V_{gs}. The drain-source differential conductance g_{ds} vs. V_{ds}, V_{gs} characteristics are shown using 3-D (c) and colour scale (d) plots. Multiple Coulomb diamonds, seen clearest in (d), and Coulomb staircases, seen clearest in (a), are observed in the characteristics. Within the Coulomb gap, I_{ds} is strongly suppressed by Coulomb blockade to within the measurement noise floor (~1 pA). However, noise peaks inherent to the device at the ~10 pA scale are seen at some gate voltages, e.g. these are more prominent for V_{gs} values from 6.5 – 8.5 V. In comparison with QD measurements at cryogenic temperatures, as our measurements were at much higher (room) temperature, thermally activated stochastic charging of defect states nearby the QD can occur, leading to noise in the device. A large peak-valley ratio ~10 is observed in I_{ds} vs. V_{gs}. The I_{ds} magnitudes and oscillation peak heights are greater for negative V_{ds} bias, due to a small diode-like asymmetry in the characteristics.

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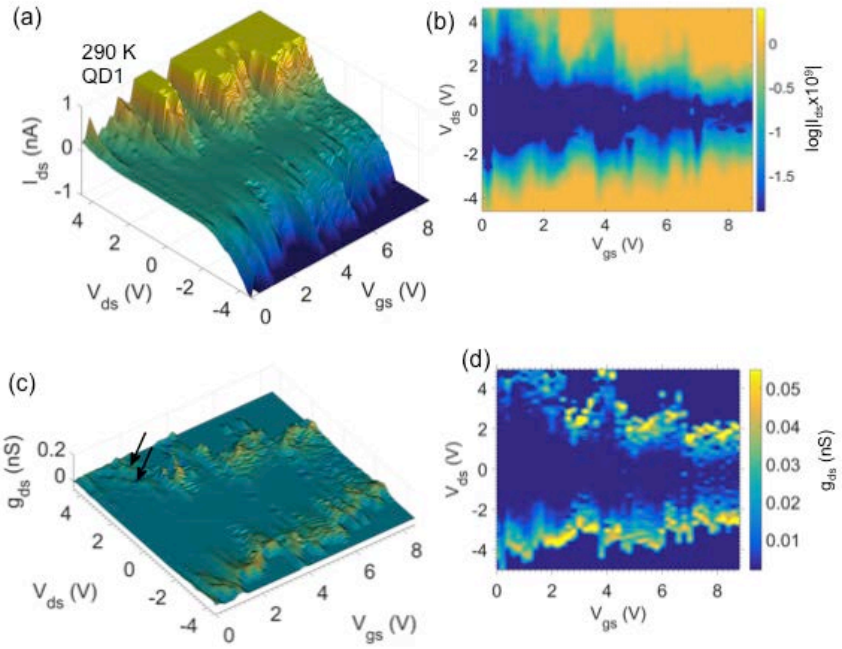

Figure 2.3 Room-temperature (RT = 290 K) drain-source current (I_{ds}) vs. drain (V_{ds}) and gate (V_{gs}) voltage 'Coulomb diamond' characteristics for a point-contact QD device (QD1), with point-contact pre-oxidation width of ~25 nm. I_{ds} in the measurement is limited to ±1 nA to avoid device damage. The characteristics are plotted (a) using a three-dimensional (3-D) plot, and (b), log|I_{ds}| vs. V_{ds}, V_{gs}, using a linear colour scale. (c) The drain-source differential conductance g_{ds} vs. V_{ds}, V_{gs} characteristics, shown using a 3-D plot, and (d) in a colour scale plot, with a linear colour scale for g_{ds}.

Resonant tunnelling occurs through QD excited states, even at room temperature, in the device. In Fig. 2.3 (c-d), differential conductance peaks running parallel to the Coulomb diamond edges are seen (e.g. indicated by arrows in (c), and forming bright lines in (d), a signature of resonant tunnelling through excited states. Given that these features run parallel to the diamond edges, both the diamonds and the features are associated with states in the same, dominant QD. For V_{gs} < 4 V, it is seen that the diamonds do not reduce to zero, implying either a potential barrier in addition to the QD, or a band offset between the energy at the base of the QD and the source conduction band edge. In the former case, the potential barrier may be associated with additional series QDs, i.e. a multiple tunnel junction (MTJ) system, or with a SiO_2 or depleted Si region in series with the dominant QD. The threshold voltage V_t for I_{ds} is then given by a combination of the voltage drop across this barrier and QD Coulomb blockade. The former is pulled down in energy as V_{gs} increases, reducing V_t. In the case of additional series QDs forming an MTJ, a dominant QD is still necessary to explain the observation of resonant tunnelling lines running parallel to the diamond edges. Within the MTJ model, if multiple QDs of various sizes are capacitively coupled to the gate, this leads to the formation of subsidiary, smaller Coulomb diamonds lying between larger diamonds in the electrical characteristics. In Fig. 2.3(d), the Coulomb diamond at V_{gs} = 2.4 V may be formed by this effect. Finally, vertical features, parallel to the V_{ds} axis are also observed in (b) and (c). These appear to have only weak, very limited dependence on V_{ds}, implying that the underlying level is decoupled from V_{ds}. These lines may be associated with charging of a defect state in the oxide in the proximity

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of the QD as V_{gs} is varied, or with an additional QD within an MTJ, where this is only weakly coupled to the drain, similar to doped nanowire SETs.

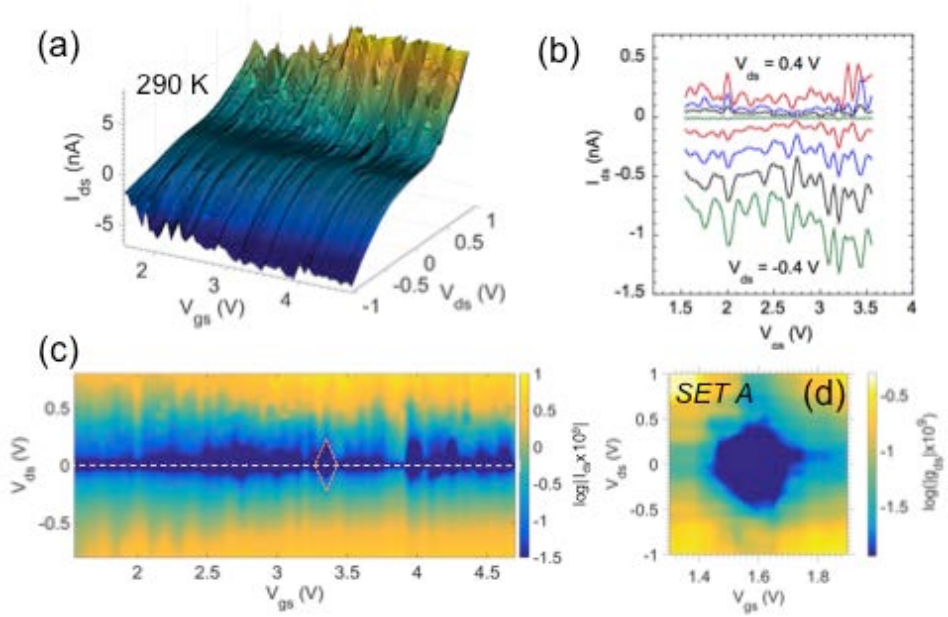

Figure 2.4. Electrical characteristics at RT for an additional device, QD2 (a) Measurements of I_{ds} as a function of V_{ds} and V_{gs} at V_{ds} values between ± 1 V, shown using a three-dimensional (3-D) plot. (b) Oscillations in the dependency of I_{ds} on V_{gs} at values of V_{ds}, between +0.4 and -0.4 V. (c) The log|I_{ds}| vs. V_{ds}, V_{gs}, characteristic of QD2 shown with a linear scale for log|I_{ds}|. A large number of Coulomb diamonds are shown, with one highlighted as an example. (d) Coulomb diamond in an additional device (SET A) at 290 K. The diamond 'pinches-off' to zero width along V_{ds} at V_{gs} = 1.4 V and 1.9 V.

RT QD single-electron effects have been observed in multiple devices (19 devices), fabricated using 4 processing runs, on different samples. The characteristics from a second device (QD2) are shown in Figure 2.4 (a – c). Current oscillations with changing V_{gs} at V_{ds} values between +0.4 V and -0.4 V are shown in (b) and multiple Coulomb diamond like features (c) can be identified (one of these is marked in (c)), corresponding to a large, one-by-one change in electron number N. As in QD1, a small diode-like asymmetry is seen in the characteristics, increasing the current magnitudes for negative V_{ds} values and creating a small asymmetry in the diamond shapes in (c). In comparison with QD1, any additional potential barriers or band offsets are less significant, with a minimum threshold voltage ~ ±25 mV. However, a variation in Coulomb diamond size occurs, suggesting an MTJ is formed where the constituent QDs are gate-coupled. Figure 2.4(d) shows a Coulomb diamond in detail, from an additional device (SET A) at 290 K. Here, any additional potential barrier is negligible as the diamond 'pinches-off' to zero width along V_{ds}, at V_{gs} = 1.4 V and 1.8 V. This behaviour is less typical in our devices, where the fabrication process in likely to form an additional potential barrier creating a constant threshold voltage offset. The differential conductance at V_{ds} = 0 V changes from g_{ds} ~60 pS at V_{gs} = 1.4 V to g_{ds} ~ 12 pS at V_{gs} = 1.6 V.

A third quantum dot (QD3) has been fabricated in SOI material with a higher doping level (5×10^{20} /cm^3). This allowed electrical characteristics to be measurement down to 150 K, below

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which an increasing device resistance prevented further measurements. The effect of temperature on the electrical characteristics are shown in Figure 2.5, with I_{ds} vs. V_{ds}, V_{gs} characteristics at (a), (b) 290 K and (c) 150 K. Figure 2.5(b) shows in detail the I_{ds} vs. V_{ds}, V_{gs} characteristics at 290 K (measured in a different cycle to (a)), around a region of Coulomb oscillations in I_{ds}, at a higher $|V_{ds}| \leq 4$ V. A rich structure is seen, with multiple step Coulomb staircase I_{ds} - V_{ds} characteristics (e.g. steps labelled 'A'), where the shoulders form diagonal lines (e.g. labelled 'B'). Resonant tunnelling current peaks may also be seen, with negative differential resistance regions, e.g. labelled 'C'. The device resistance is ~20 MΩ outside the central potential barrier region, much lower than in QD1. Intermediate temperature dependencies are shown in Fig. 2.6, discussed in detail later. Arrhenius plots of $\ln(I_{ds})$ vs $1/T$ extracted from these are shown in Fig. 2.5 (d) and the variation with V_{ds} of the activation energy E_A obtained from these is shown in (e). These characteristics, and those shown in Figure 2.6 illustrate the combined effect of a QD and an additional potential barrier in our devices. As argued earlier, the potential barrier may be created by an MTJ, or by a SiO_2 region in series with or underlying the dominant QD. At RT (290 K) the potential barrier has only a limited effect, creating a small threshold voltage $V_t \sim \pm 0.15$ V approximately constant with varying V_{gs} (Fig. 2.6(a)). For $|V_{ds}| > |V_t|$, Coulomb oscillations occur in I_{ds}. At low temperature (150 K), the effect of the potential barrier is much stronger as any thermally activated current is supressed, increasing $|V_t| \sim 1$ V. I_{ds} then rises sharply beyond this, as the contact resistance of the degenerate source, drain and lead-in regions reduces. Detailed changes also occur, e.g. in this device, some oscillations are supressed at $V_{gs} > 2$ V, possibly due to a change in the QD environment. The Arrhenius plot in Fig. 5(d) shows thermal activation of I_{ds} from 290 K – 200 K. Linear fits to the data facilitate extraction of the activation energy E_A vs. V_{ds}. It is seen that as V_{ds} decreases towards zero, E_A reduces. Extrapolation of a polynomial fit to the data (Fig. 5(e)) shows a minimum activation energy $E_{A1} = 0.125$ eV at $V_{ds} = 0$ V. Furthermore, E_A saturates at a maximum activation energy $E_{A2} \sim 0.235$ eV at $V_{ds} = 0.5$ V. As the potential barrier dominates at low bias, $E_{A1} = 0.125$ eV may be associated with the height of this barrier.

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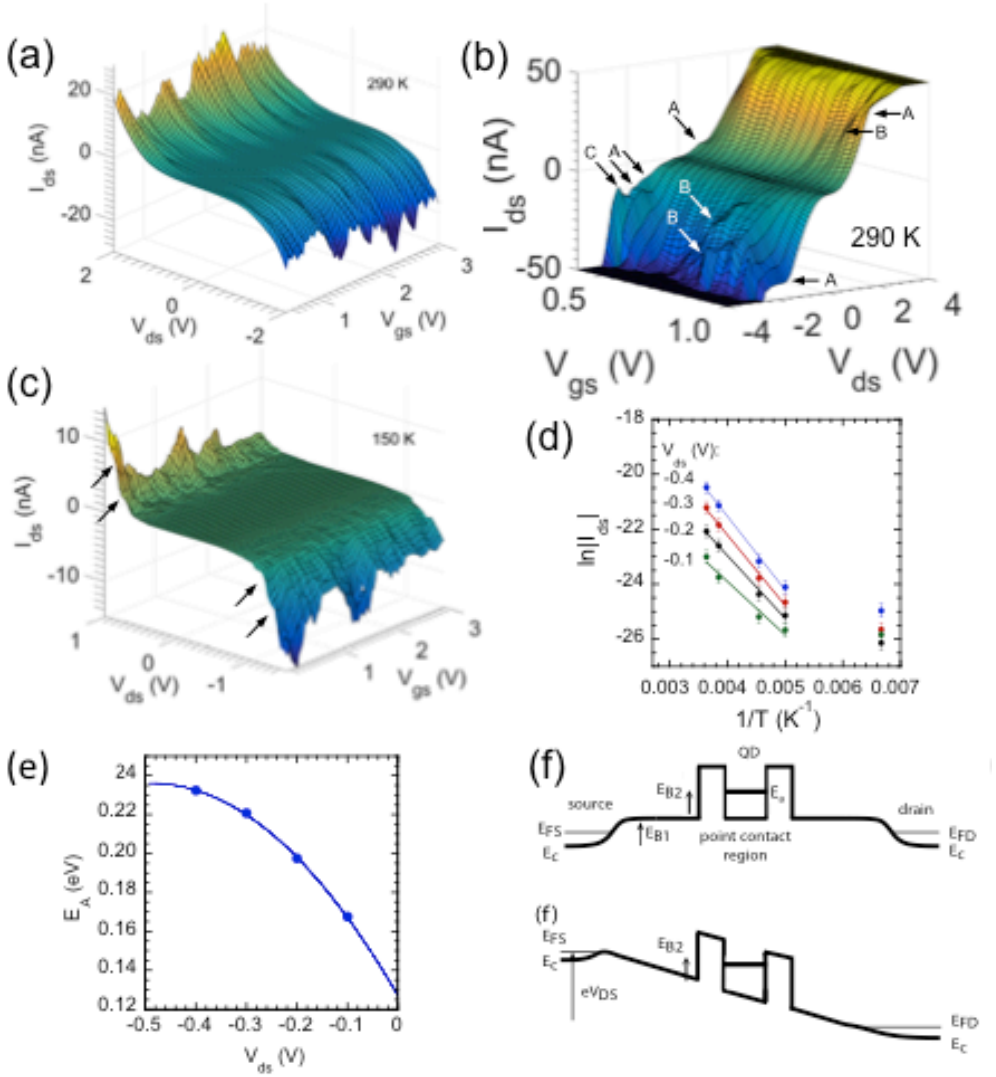

Figure 2.5 Temperature dependence of the electrical characteristics of QD3. (a), (b) show the I_{ds} vs. V_{ds}, V_{gs}, at 290 K and (c) at 150K. (Further temperature dependence characteristics are shown in Fig. 2.5 where the variation of log|I_{ds}| with V_{ds}, V_{gs} is shown). (b) shows detail in the I_{ds} - V_{ds}, V_{gs} characteristics at 290 K (measured in a different cycle to (a)), around a region of Coulomb oscillations in I_{ds}. Coulomb staircase characteristics are observed, with arrows indicating (A) current steps, (B) lines formed along shoulders of steps and (c) current peaks. The Arrhenius plot in (d) shows thermal activation of I_{ds} from 290 K – 200 K. Linear fits to the data allow extraction of the activation energy E_A as a function of V_{ds}, shown in (e). As V_{ds} decreases towards zero, E_A reduces and extrapolation of a polynomial fit to the data shows a minimum value of 0.125 eV at V_{ds} = 0 V. (f) A schematic band diagram showing the area of the point contact regions with an additional potential barrier, at zero bias (top), and under an applied bias (bottom).

This is shown schematically in Fig. 2.5(f), where a potential barrier with height $E_{B1} \sim E_{A1}$ exists in series with and on either side of a dominant QD. At higher bias, V_{ds} = 0.5 V, the potential barrier is pulled down (Fig. 2.5(bottom)) and Coulomb oscillations are observed. E_{A2} ~ 0.235 eV may then be associated with the charging energy in the QD. We observe that for this

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device, $E_{A1} < E_{A2}$, i.e. the potential barrier is less significant than the charging energy to the electrical characteristics.

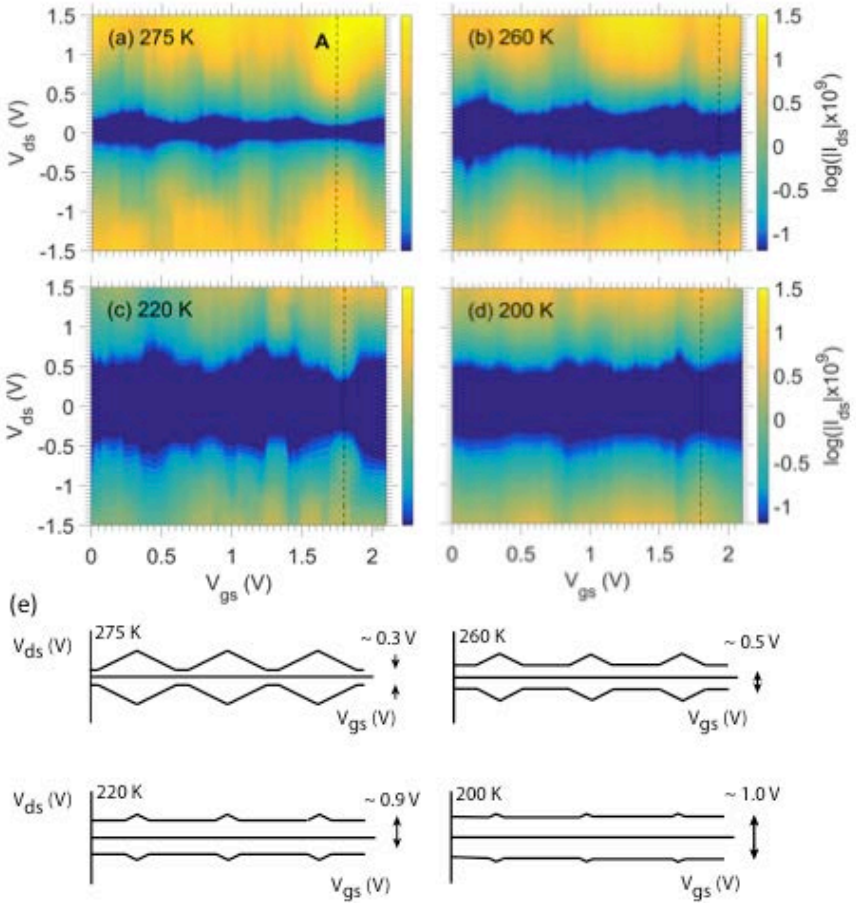

Figure 2.6 Temperature dependence of the electrical characteristics of QD3. The evolution with temperature of the Coulomb diamonds is shown in the colour plots of $\log|I_{ds}|$, as a function of V_{ds} and V_{gs}, at temperatures of (a) 275 K, (b) 260 K, (c) 220 K, and (d) 200 K. In addition the increasing influence of the potential barrier with decreasing temperature is shown. As a guide, (e) shows a diagrammatic representation of this effect, with the central low current region increasing in width along V_{ds} from ~ 0.3 V at 275 K to ~1.0 V at 200 K.

The evolution of the Coulomb diamonds in QD3 with decreasing temperature is shown in Figure 2.6, with characteristics taken at 275 K – 200 K (a – d). A schematic representation of the variation in the central low current region (dark blue region in (a) – (d)) is shown in Fig. 2.6(e). For $|V_{ds}| > |V_t|$, Coulomb oscillations in I_{ds}, create triangular half-diamond features on either side (e.g. Fig. 2.5(a)). Four Coulomb diamond features (associated with the QD), offset by a central threshold region (associated with the potential barrier), are observed at (a) 275 K (b), 260 K (c), 220 K and (d) 200 K. It is seen that the centre threshold regions increases in

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significance with reducing temperature. Additional fine structure appears along the diamond edges at 220 K. The increasingly significant potential barrier begins to supress the diamond features by 200 K, though current oscillations still persist. The higher doping level of this sample reduces the height of any potential barriers along the current path. Furthermore, the source/drain contact resistance is improved, as the degenerately doped nature of the source and drain contact regions is maintained to a point closer to where doping concentration fluctuations become significant at the point-contact neck.

The variation of a current peak with temperature (along line 'A' in Fig. 2.6(a)), for a bias (0.4 V) at the edge of the central threshold region at 200 K is shown in Fig. 2.7(a) and at high V_{ds} bias (1 V, Fig. 2.7(b)). The thermal broadening for a current oscillation may be expressed as $I/I_0 = A(\cosh^{-2}(|V_{peak} - V_{gs}|/Bk_BT))$, where V_{peak} is the peak position, $V_{peak} - V_{gs}$ indicates the offset to V_{peak}, k_B is Boltzmann's constant, and A and B are constants. This function, plus a linear background, is used to fit the data in Fig. 2.7 (a) and (b). The data predicts a linear dependence of the peak width (the denominator Bk_BT within the $\cosh^{-2}$ term above) with T, and this is seen to be the case (inset to (a)). Extrapolation of the fit suggests that in this device, the current peak would disappear by ~120 K. This implies that some of the available thermal energy at a given temperature is essential to overcome potential barriers in addition to the QD charging energy, supporting the model for these devices, shown in Fig. 2.5(f – g). In Fig. 2.7(b), for V_{ds} = 1 V, a current oscillation peak is still observed even for 150 K. However, this peak is broader than expected, implying a change in the parameter B associated with the bias drop across the device capacitances, providing further support to our observation of a change in the electrical parameters of the QD and its environment by 150 K, also seen in Fig. 2.5(c).

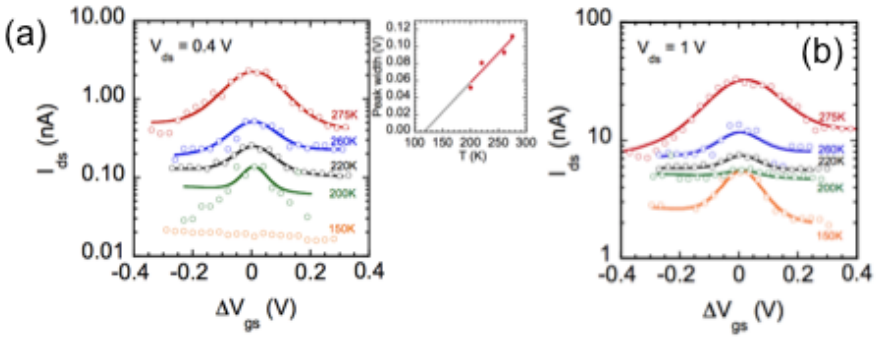

Figure 2.7 Temperature dependence of a current peak from 275 K – 150 K. Data extracted for the peak lying along the dotted lines in Fig. 2.6. The current peak is plotted for $\Delta V_{gs} = V_{peak} - V_{gs}$, where V_{peak} is the peak centre, (a) for V_{ds} = 0.4 V, near the edge of the central threshold region, and (b) for V_{ds} = 1 V, well outside the threshold region. Data shows thermal broadening in V_{gs}, which is fitted with a $\cosh^{-2}(|\Delta V_{gs}|/Bk_BT)$ dependency[18], plus a linear function. Here, B is a constant. For (a), the peak width of this (Bk_BT) is plotted as a function of temperature in the insert, demonstrating the anticipated linear temperature dependence of the function.

Data from QD1 is analysed in Figure 2.8. Figure 2.8(a) shows the g_{ds} vs. V_{ds}, V_{gs} plot of Fig. 2.2(d), but now overlaid with two Coulomb diamonds marked by white lines. Here, a linear plot of g_{ds} is used as the edges of the Coulomb diamonds are clearer in this, with the white lines approximately following the 2.5 pS contour. A large number of resonant peaks create lines

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across the plot (e.g. indicated by dotted red lines), forming two groups lying parallel to both the left and right diamond edges. A schematic Coulomb diamond with N electrons on the QD, including resonant tunnelling through excited states, is shown in Fig. 2.8(b). The insets to the figure show the energy diagram for the QD at various points with respect to the Coulomb diamond. $E_c = e^2/C$ is the Coulomb gap in the QD, where C is the total QD capacitance. $E_a = E_{c1} + E_k$ is the QD single electron addition energy, where $E_{c1} = E_c/2 = e^2/2C$ is the energy needed to add an electron from the source to the QD, ignoring quantum confinement, and E_k the quantum confinement energy. E_a defines the ground state for the QD. E_N and E_{N+1} correspond to N and $N + 1$ electrons on the QD respectively. Excited states above and below this are shown by blue dotted and red solid lines respectively. Electron tunnelling occurs when QD states E_N, E_{N+1}, or these in combination with the excited states, lie within an energy window $E_{FS} - E_{FD} = eV_{ds}$, where E_{FS}, E_{FD} are the source, drain Fermi energies.

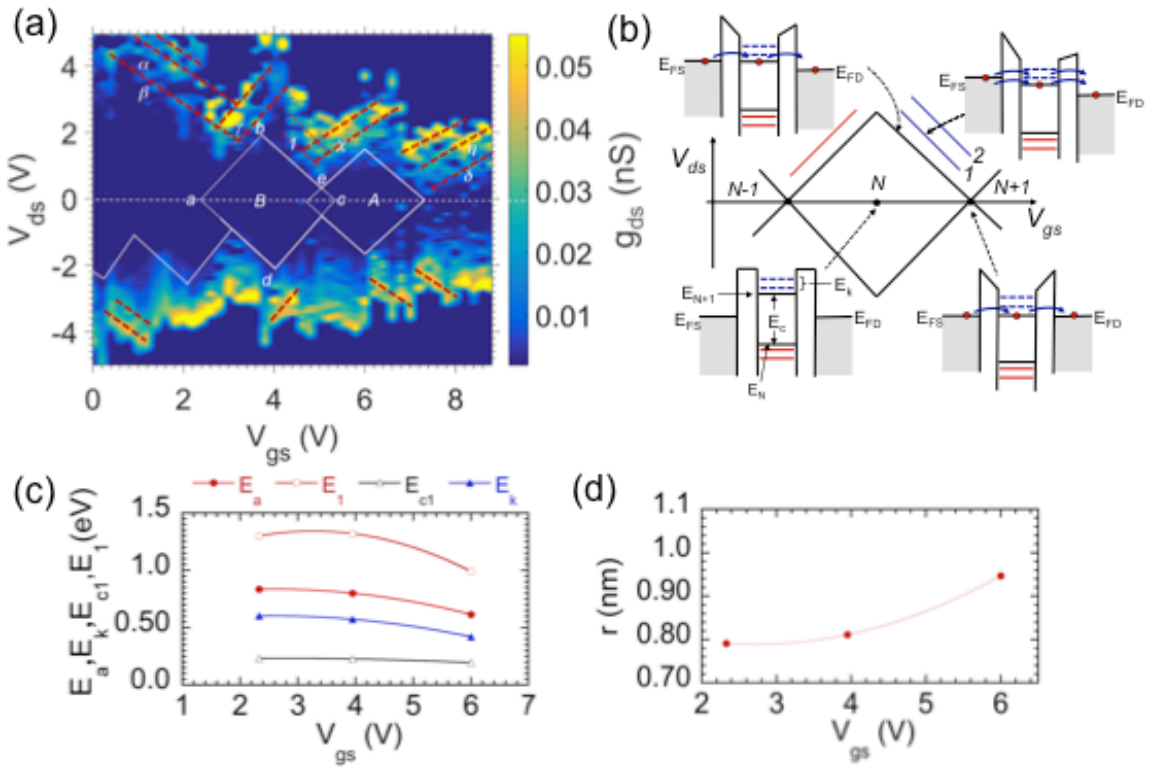

Figure 2.8 Analysis of the characteristics of QD 1. (a) Fig. 2.2(d) is repeated, but now the edges of the Coulomb diamonds marked by solid white lines, parallel to the g_{ds} contours. Extension of these lines (dotted orange lines) defines the Coulomb diamonds A and B, with the overlap between the diamonds at V_{gs} = 5 V caused by the additional potential barrier. A large number of lines in g_{ds} are observed (e.g. indicated by the dotted red lines). (b) A schematic Coulomb diamond with N electrons on the QD, including resonant tunnelling through excited states in the QD. Insets associated with the diamond show the energy diagram for the QD at various points with respect to the Coulomb diamond. (c) The values of E_a, E_k, $E_{c1} = E_c/2$ and E_1 extracted from the diamond and their dependence on V_{gs}. (d) The values of the QD radius, r, derived from these values.

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Comparison of the data (Fig. 2.8(a)) with Fig. 2.8(b) allows attribution of the g_{ds} lines to room temperature resonant tunnelling through excited states, and extraction of E_a = 0.83 eV ~ $30k_BT$ at 290 K, a very large value (details of the model and calculation may be found in Sec. 7, Appendix). Here, lines with negative slope, e.g. α, β, *1*, correspond to excited states above the Coulomb gap (blue lines, (Fig. 2.8(b)) and lines with positive slope, e.g. δ, γ, η, χ, to lines below the Coulomb gap (red lines, Fig. 2.8(b)). The Coulomb diamond allows measurement of E_a and the energy of the first excited state above the Coulomb gap, E_1. Furthermore, assuming a spherical QD of radius *r*, appropriate for our oxidised point-contact structures, it is possible to calculate E_{c1} and E_k. For Coulomb diamond *B*, we find E_a = 0.83 eV ~ $30k_BT$ at 290 K, E_1 = 1.3 eV and *r* = 0.8 nm. Here, the separation of the first excited state from the ground state $\Delta E = E_1 - E_a$ = 0.5 eV. E_a appears to be the largest, and *r* the smallest value yet reported for a QD transistor. E_a, E_c, E_k and E_1 (Fig. 2.8(c)) can be extracted for the Coulomb diamonds centred at V_{gs} = 2.3 V, 4 V (diamond *B*), and 6 V (diamond *A*) in Fig. 2.8(a), with the corresponding QD radius in Fig. 2.8(d)). As V_{gs} is reduced, *r* decreases from a maximum of 0.95 nm to 0.79 nm, implying that the QD can be electrically 'squeezed' to reduce its radius, which resembles the different size of the Coulomb diamond shape in Figure 2.8(a).

The nature of the few nanometre scale QDs in these devices is now considered. The central point-contact region in this device is oxidised to close to, or just at pinch-off. Here, if a crystallite Si core still remains due to incomplete pinch off by SiO_2, then given the small size of the core, it is probable that this will behave as an ultra-small QD embedded within the SiO_2. Alternatively, as the device starting material was heavily doped Si, a single or just a few donor atoms may remain embedded within the SiO_2 region. Current transport then occurs either by direct tunnelling into a single donor atom QD, or along a path made by a few donor atoms forming an MTJ. In the later case, one of the donor atoms along the MTJ may dominate the characteristics, if this is isolated by a greater separation from its neighbours associated with donor concentration variability.

The data from 19 working RT SETs, fabricated in SOI material with 20 nm and 12 nm thick top Si layers is shown in Figure 2.9. These devices were obtained from a total of 326 fabricated devices, in 4 processing runs (2 runs for each of the two SOI thicknesses). The 19 devices correspond to an overall percentage of 5.8% of the fabricated total. Here, criteria for a 'working' device were the RT observation of gate oscillations in I_{ds}, and/or the observation of a Coulomb staircase. The device I_{ds}-V_{ds}, V_{gs} characteristics were qualitatively similar to those in Fig. 2.3 – 2.5. The percentage of working devices vs. the pre-oxidation point-contact cross-sectional area, from 120 nm^2 (10 nm × 12 nm) to 2000 nm^2 (20 nm × 100 nm) is shown in Figure 2.9(a). Devices were oxidised to give a nominal SiO_2 thickness of ~5 nm (12 nm SOI) and ~10 nm (20 nm SOI). The number of fabricated devices for a given cross-section is shown in brackets at each data point. For devices larger than 400 nm^2, the point-contact width was larger than the height even in the 20 nm SOI material, implying that here, the critical minimum dimension was the SOI top Si thickness. It is seen in Fig. 2.9(a) that as the point-contact cross-sectional area increases, the percentage of working devices falls (a polynomial line is added to the plot as a guide to the eye). The highest percentage of 10.7% was observed for 200 nm^2 pre-oxidation area. There were no working devices by the 2000 nm^2 data point, and it was necessary to have an area ~700 nm^2 or less to find more than one working device. The trend

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seen in Fig. 2.9(a) emphasises the need to reduce the point-contact pre-oxidation cross-section to obtain an increased likelihood of working devices.

The QD radius r and addition energy $E_a = E_{c1} + E_k$ vs. pre-oxidation cross-section, extracted using the model of Fig. 2.8 are shown in Figure 2.9(b) and (c) respectively. Here, data from 12 devices are shown, where the gate oscillations in I_{ds} were sufficiently clear to apply the model. It is seen that r lies in a relatively narrow band, 0.8 nm < r < 2.35 nm, particularly given the single nanometre scales involved. Here, the mean value and standard deviation are 1.47 nm and 0.53 nm respectively. The maximum variation in r corresponds to a length of only 7 – 11 atoms in crystalline Si, depending on the crystallographic direction. The narrow range of r tends to support the origin of the QD due to potential wells created by isolated donor atoms embedded within SiO_2, which would tend to be similar for different devices. Both the 12 nm and 20 nm SOI devices have similar average r, 1.49 nm and 1.42 nm respectively, though there is greater variation in the 20 nm SOI devices (the standard deviation in the 12 nm and 20 nm SOI is 0.46 nm and 0.67 nm respectively). The average radius across all devices is 1.47 nm. Furthermore, for both SOI thicknesses, r tends to reduce slightly with pre-oxidation cross-section (a linear fit is added as a guide to the eye). E_a (Fig. 2.9(c)) correspondingly increases as r reduces (a linear fit is added as a guide to the eye), as expected in the model.

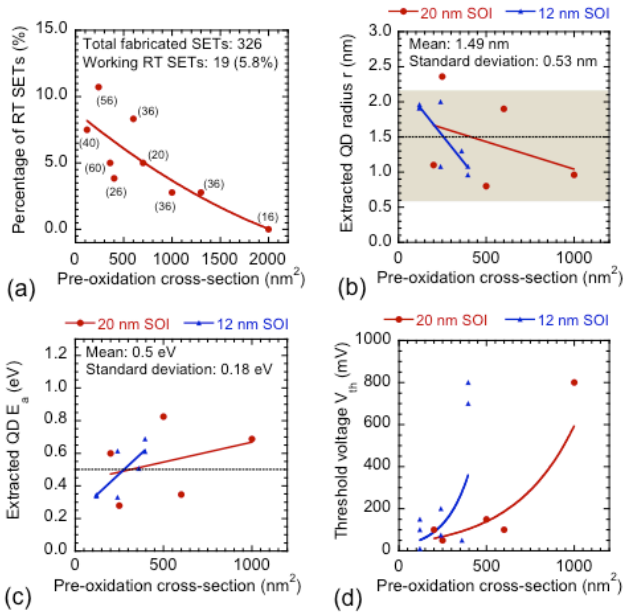

Figure 2.9 Analysis of working RT SET devices. (a) Percentage of working RT SETs vs. pre-oxidation point-contact cross-sectional area. 19 working devices were measured from 326 fabricated devices, in SOI material with 20 nm and 12 nm thick top Si layers. Number of fabricated devices at given cross-section is shown in brackets at each data point. (b) QD radius r vs. pre-oxidation cross-sectional area, extracted using the model of Fig. 7. (c) Addition energy E_a vs. pre-oxidation cross-sectional area for the RT SETs of (b), extracted using the model of Fig. 2.8, (d) Threshold voltage V_{th} in the RT SETs of (b), vs. pre-oxidation cross-sectional area.

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The trends shown in Fig. 2.9(a-c) imply that while a reduction in point-contact size leads to increasing likelihood of working RT SETs (Fig. 2.9(a)), this does not lead to a smaller QD size (Fig. 2.9(b)). Instead, there is an unexpected trend towards slightly larger QD radius for smaller point-contacts. Furthermore, for both 12 nm and 20 nm SOI, the average extracted QD radius is similar. These trends may be understood by plotting, the threshold voltage V_{th} for drain-source current in the RT SETs, as a function of the cross-section area, where V_{th} corresponds to the minimum V_{ds} value at the edge of the central low current band (schematic diagram in Fig. 2.6(e)). It is seen that V_{th} increases rapidly with cross-sectional area (an exponential fit is added as a guide to the eye). As V_{th} is related to the height of additional underlying (Fig. 2.5(f – g)) or series potential barriers in the devices, this implies that in RT SETs obtained with a larger pre-oxidation cross-sectional area, any additional barriers are more significant. As these barriers are likely to be created by the oxidation process, RT SET characteristics observed with a larger pre-oxidation cross-section occur only if there is a greater oxidation occuring in a particular device due to process variations. Furthermore, higher V_{ds} values are necessary to pull a higher and/or longer potential barrier down (see schematic in Fig. 2.5(g)). If a large QD with a smaller Coulomb gap exists, then the effect of this may be overcome as the voltage approaches V_{th}, due to the gap being pulled down well below the source Fermi energy (Fig. 2.5(g)). This behaviour would then lead to the ‘self-selection’ of smaller QD sizes when a working RT SET is observed at larger pre-oxidation cross-sectional area (Fig. 2.9(b)). However, the likelihood of finding such a device would be small (Fig. 2.9(a)).

In summary, we report RT operation of Si point-contact SETs, where an ultra-small, single nanometre scale QD (diameter ~1.6 nm) forms the device core. A remarkably large QD electron addition energy ~0.8 eV, and quantum confinement energy ~ 0.3 eV, are observed. These very large values (the highest values reported to date) enable room temperature observation not only of Coulomb blockade, but also of resonant tunnelling through excited states. In measurements of 19 RT SETs, the likelihood of finding one of these devices is seen to increase with reduction in point-contact size to the ~10 nm scale, and the extracted QD radius is found to lie within a narrow band, from 0.8 nm to 2.35 nm. At these sizes, in addition to the single-electron charging energy, the effect of quantum confinement and resonant tunnelling effects on the electrical characteristics cannot be ignored. Finally, the QD radius tends not to reduce as the point-contact dimensions are reduced, supporting a picture where the QD is associated with the material properties such as donor atoms, rather than directly with the point-contact size. The results demonstrate that with careful control ‘beyond CMOS’ QD point-contact transistors, showing Coulomb blockade and resonant tunnelling through excited states, all at room temperature, can be produced using current ‘conventional’ semiconductor device fabrication techniques.

This work shows that in the limit of the point-contact approach, it is possible to form ultra-small, few nanometre scale QDs, where the full QD characteristics, including excited states, are measurable at room temperature. By combining thin silicon on insulator (SOI) wafers, specific device geometry, and controlled oxidation, it is possible to define <10 nm nanoscale point-contact channels using ‘conventional’ techniques. These are small enough to allow a dominant QD associated with a Si nanocrystal, or a dopant atom[6], to be addressed. A remarkably large QD electron addition energy ~0.8 eV, and a quantum confinement energy ~0.3 eV, are observed, implying a QD only ~1.6 nm in size. These large values enable room temperature

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observation not only of Coulomb blockade, but also of resonant tunnelling through excited states. In measurements of 19 RT SETs, the likelihood of finding one of these devices is seen to increase with reduction in point-contact size to the ~10 nm scale, and the extracted QD radius is found to lie within a narrow band, from 0.8 nm to 2.35 nm. At these scales, in addition to the single-electron charging energy, the effect of quantum confinement and resonant tunnelling effects on the electrical characteristics cannot be ignored. Finally, it is seen that the QD radius tends not to reduce as the point-contact dimensions are reduced, supporting a picture where the QD is associated with the material properties such as donor atoms, rather than directly with the point-contact size. Here, a dopant atom origin has the advantage of ultra-small QD size, but the disadvantage remains of statistical variation between devices. However, a minimum size ~5 nm for the point-contact channel (height and/or width) remains essential to observe RT Coulomb diamonds, as this allows addressing of single or a few dopants along the current path. Finally, the ability to address single dopant is of great interest for control of semiconductor qubit for quantum computation, as very long coherence times in the millisecond to second range are possible for phosphorus atom spins in Si. This creates a further application for the RT point-contact devices presented in this deliverable.

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3. DOUBLE QUANTUM DOTS IN SILICON POINT-CONTACT SETS

The nanoscale Si point contact SETs discussed in Sec. 2 were operated using a single side gate. Analysis of the electrical characteristics of these devices, from 290 – 150 K, showed that a dominant QD, combined with an additional potential barrier, existed within the point-contact. In these devices, given the heavily-doped (>10^{20} / cm^3, *n*-type) nature of the point-contact, and the few nanometre scale (< 5 nm) QD size extracted from the electrical measurements, the likely origin of the QD was a potential well created by a donor atom. Furthermore, the origin of the additional potential barrier along the current path was likely to be a potential created by the oxidation of the point-contact region, and/or additional series QDs with weaker coupling to the gate electrode in comparison with the dominant QD. If additional QDs existed these would also arise from isolated donor atoms within the point contact.

In this section, measurements investigating control of two, electrostatically coupled QDs at RT are reported. As the point-contact is heavily doped, a strong likelihood exists of additional donor atoms within the point-contact region. It is possible to investigate the presence of multiple QDs by using two gate electrodes, one on each side of the point-contact. As the donor atoms would be spatially distributed within the point-contact, they have different capacitive coupling to the two gate electrodes. Furthermore, quantum confinement states within a pair of QDs can couple electrostatically to each other, creating a double QD (DQD) system analogous to an artificial molecule. If the QD electron addition energies $E_a > k_BT$ = 25 meV at 290 K, then it becomes possible to observe double QD effects at RT. We note that at present, DQD effects have been observed only at cryogenic temperatures.

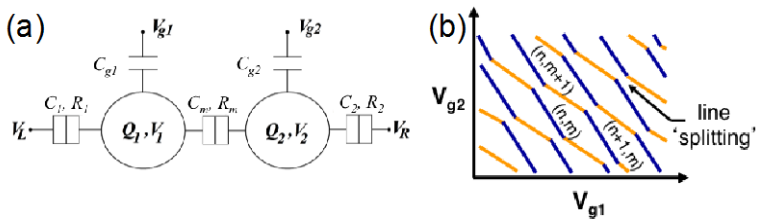

Figure 3.1. (a) Series, coupled double QDs. The two QDs are capacitively coupled to separate gate voltages V_{g1} and V_{g2} and tunnel coupled to the left (V_L) and right (V_R) electron reservoir voltages, and to each other. (b) Hexagonal charge stability regions are created in a plot of I_{LR} vs. V_{g1} and V_{g2}, due to single-electron charging of the QDs. The electron number (n, m) is stable within a hexagonal region.

Figure 3.1(a) shows the circuit diagram for a double QD device, with two QDs in series[2]. Here, the two QDs are capacitively coupled to separate gate voltages V_{g1} and V_{g2} by C_{g1} and C_{g2}, and tunnel coupled to the left (V_L) and right (V_R) electron reservoir voltages by C_1, R_1 (capacitance,

[2] van der Wiel, W. G., De Franceschi, S., Elzerman, J. M., Fujisawa, T., Tarucha, S., and Kowenhoven, L. P. (2003). Electron transport through double quantum dots, *Rev. Mod. Phys.* , 75, pp. 1–22.

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resistance of tunnel barrier) and C_2, R_2. Furthermore, the QDs are mutually tunnel coupled by C_m, R_m. As both QDs couple to both gates, either directly via C_1, C_2 or through C_m and C_1, C_2, each QD leads to the single-electron current oscillation peaks in I_{LR} vs. V_{g1} and V_{g2}, at constant voltage bias V_{LR}, and the position of these peaks moves diagonally across the plot. Figure 3.1(b) shows this schematically, where the blue and yellow sets of lines give the nominal positions of the single-electron current oscillation peaks caused by the two QDs respectively. At the intersection points between the two sets of lines, addition of a single electron to one of the QD shifts the nominal position of the current line corresponding to the other QD, and vice versa, splitting the lines and leading to signature hexagonal charge stability regions, with electron number (n, m) on the two QDs. Here, the slopes of the lines defining the regions can be used to extract circuit parameters for (a). Crossing one of the edges of a hexagonal region changes either n or m by one. Note that for the series configuration shown in (a), current can flow *only* when the states in the two QDs are resonant, implying that a current peak is observed at the corners of the hexagonal regions only. The plot of I_{LR} vs. V_{g1} and V_{g2} then shows a pattern of current peaks, arranged hexagonally. In contrast, for two QDs in parallel (circuit diagram not shown), the edges of the stability region lying along the yellow and blue lines in (b) are seen.

Figure 3.2 shows the dual gate electrical characteristics at 290 K from two point-contact devices in ultra-thin SOI, where the top Si layer was ~12 nm thick. In the first device (Dev. A, Fig. 3.2(a)), a pattern of current peaks, with some of the peaks interconnected by weaker lines, is observed. For some of the peaks (marked a – f), a hexagonal pattern can be identified (dashed lines). Here, peaks a and b blend together, due to measurement at RT (see simulations in Fig. 3.3). A similar hexagonal region exists to the left of the marked region (for $2 < V_{gs1} <$ 3.7 V, and $0 < V_{gs2} <$ 0.4 V). Other hexagonal regions of varying size may also exist, implying a change in device capacitances at different gate voltages. The hexagonal region a – f may be attributed to two serial coupled QDs, to our knowledge the first observation of this behaviour at RT.

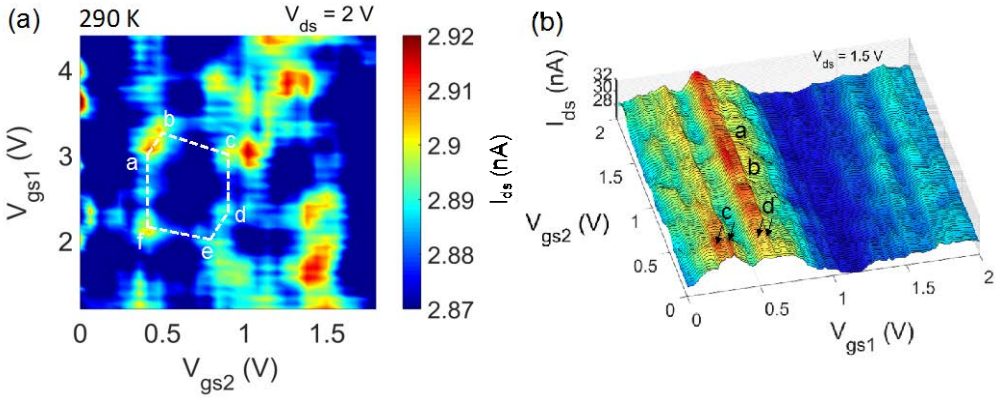

Figure 3.2. Dual-gate electrical characteristics for two point-contacts, at 290 K (a) Serial coupled double QD hexagonal charge stability regions in the I_{ds} vs. V_{g1} and V_{g2} from the first device (Dev. A). A hexagonal region is marked by dashed lines. (b) I_{ds} vs. V_{g1} and V_{g2} from the second device (Dev. B) shows a pattern of lines (dashed lines and arrowed 'split' lines). The line splitting (arrows at c and d) implies coupling of the underlying QD to an additional state or QD.

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Figure 3.2(b) shows the dual gate characteristics from a second device (Dev. B), where the current peaks are arranged in patterns of lines. In this case, isolated peaks are not observed, suggesting that the underlying QDs are in parallel. Both diagonal lines (two of these are marked *a* and *b*) and vertical (parallel to the V_{gs2} axis) 'split' lines (arrowed at *c* and *d*) may be seen. The diagonal lines follow the trend for one set (yellow or blue) of lines in Fig. 3.1(a), implying a single QD coupled to both gates. However, the vertical lines parallel to the V_{gs2} axis are seen to split into two parallel lines, implying charging by one electron of an electrostatically coupled state nearby the QD creating the line. In our heavily doped devices, this state is likely to be formed by a nearby donor atom QD.

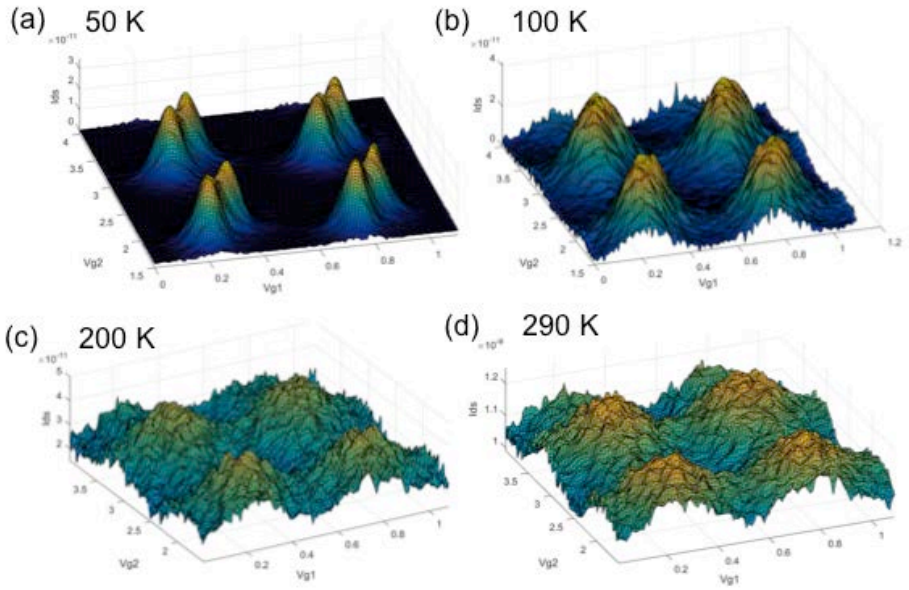

Figure 3.3. Single-electron Monte Carlo simulations of the double coupled QD circuit of Fig. 3.1(a). Capacitance values are chosen to match the experimental data in Fig. 3.2(a). Data is shown as a 3D plot, for 50, 100, 200 and 290 K.

It is possible to establish a coupled QD origin for the hexagonal patterns in Fig. 3.2(a) by using single-electron Monte Carlo simulation of the circuit of Fig. 3.1(a) to reproduce the pattern in Fig. 3.2(a). Figure 3.3 and 3.4 show 3D (Fig. 3.3) and corresponding colour scale (Fig. 3.4) plots of the simulated characteristics for a double QD circuit with C_{g1} = 0.3 aF, C_{g2} = 0.127 aF, C_1 = 1 aF, C_2 = 1.17 aF, and C_m = 0.325 aF. Simulations are conducted from 290 K – 50 K, to determine the possibility of RT observation of the hexagonal charge stability regions. It is seen that at 50 K, peaks at the corners of the hexagon are well resolved. While the peaks tend to merge as the temperature increases, even at RT = 290 K, the stability region can still be identified. Here, each pair of peaks (e.g. peaks *a*, *b*, Fig. 3.4) tend to form an oblong peak stretched along the two shorter sides of the hexagonal region (sides *a*-*b* and *d*-*e*). This behaviour is very similar to the experimental characteristics in Fig. 3.2(a). The QD addition energies are remarkably similar, $E_{a1} = E_{a1} \sim 0.05$ eV, again suggesting a similar origin and size for the QDs. The ability to observe double QD behaviour is a consequence of the very small QD capacitances, ~1 aF or less, such that the QD addition energy > k_BT = 25 meV. However,

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E_{a1} is only $2k_BT$, leading to the relatively weak peaks observed in both experiment and simulations.

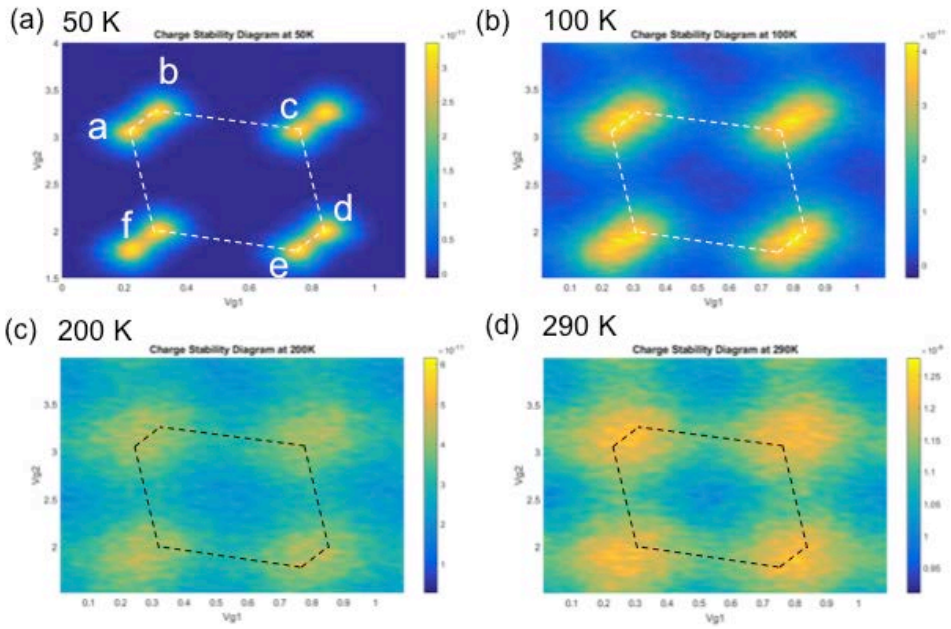

Figure 3.4. Single-electron Monte Carlo simulations of the double coupled QD circuit of Fig. 3.1(a). Capacitance values are chosen to match the experimental data in Fig. 3.2(a). Data corresponds to Fig. 3.3 and is shown here as a colour scale plot.

In summary, we have established the formation of double, electrostatically coupled QDs in dual gate point-contact SETs at RT = 290 K. Current peaks are observed in the I_{ds} vs. V_{g1} and V_{g2} characteristics at constant V_{ds}, defining hexagonal regions of charge stability on the QDs. The experimental results are matched using single-electron Monte Carlo simulations from 50 – 290 K. Addition energies ~ 0.05 eV ~ $2k_BT$ at 290 K are extracted, sufficient to allow observation of hexagonal regions even at RT. These results appear to be the first observation of double, electrostatically coupled QD behavior at RT.

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4. RT QD DEVELOPMENT WITH SETS DEFINED USING FE-SPL AT TUIL

Room-temperature point-contact SET devices have been developed in a collaboration between TUIL and ICL. Details of the fabrication process for these devices have been described in depth in milestone MS17 and are therefore not repeated here. In summary, ultra-thin SOI chips with a top Si layer of ~12 nm were used, where the top Si-layer was highly *n*-doped at IMEC, at $>10^{20}$ /cm^3. In addition, the top SOI layer was pre-patterned to give a central Si square where active devices could be made with leads to contact pads. The line features were defined by a direct ablation process of molecular glass resist material, triggered by the field electron exposure emitted from cantilever tip of the field-emission scanning probe lithography (FE-SPL) tool. The line pattern was transferred into the silicon layer by cryogenic plasma etching. The basic concept of the SET device structure using this method is shown schematically in Fig. 4.1. It will be seen that once again, geometric oxidation can be used to form the actual device, by isolating QDs within the nanoscale SiO_2 region formed at the point-contact neck.

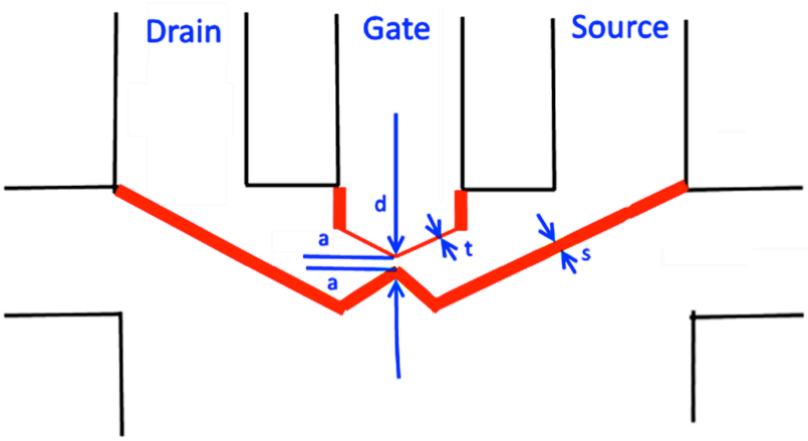

Figure 4.1 Schematic diagram showing the principles of SET fabrication using a pre-patterned wafer, FE-SPL exposed resist and cryo-etching of the silicon, followed by oxidation and contact formation. The red lines show regions for FE-SPL and cryogenic etching.

The principles of SET device fabrication can be understood with reference to Figs. 4.1 and 4.2. Within a central 50 μm × 50 μm silicon square, the pattern of the line features shown in red (Fig. 4.1) is exposed in the molecular glass resist by FE-SPL, resulting in the features being ablated. This pattern is then transferred into the silicon by cryo-etching. Figure 4.2 shows the pattern of the silicon device square and leads (a), together with how four separate discrete devices can be arranged (b), and finally a SEM micrograph showing transferred device patterns in the silicon. The wafer is then oxidised, decreasing the silicon neck width and forming a SET island in an identical way to the EBL defined SETs at ICL (Sec. 2). Electrical contacts are made away from the device area, connected to the device by wide silicon lead in regions.

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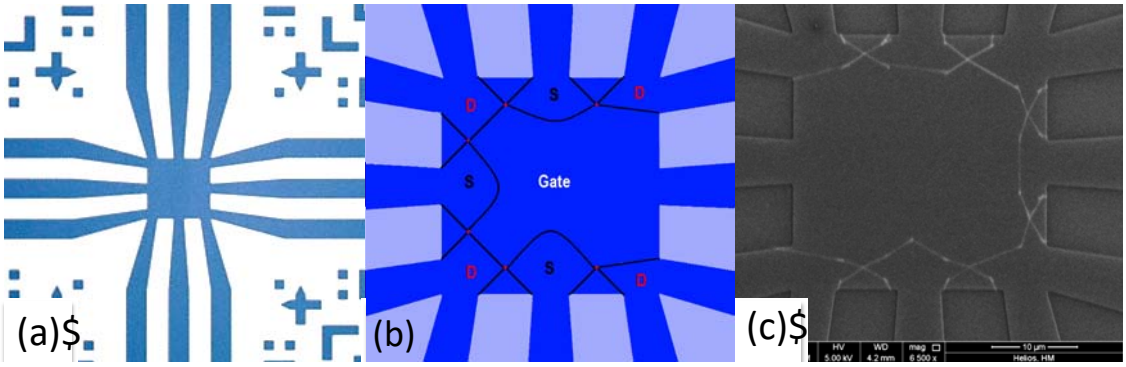

Fig 4.2 Stages of SET definition. (a) A silicon square 50 μm × 50 μm in size, with leads to contact areas (not shown) and surrounding registration marks, (b) the principle of how SET structures can be formed, and (c) low magnification SEM micrograph showing transferred SET patterns.

Devices were measured electrically to determine the existence of RT SET operation. As the basic point-contact SET layout is similar to EBL defined devices, similar characteristics to those discussed in detail in Sec. 2 were expected. Measurements at RT from two separate devices are shown in the Figs. 4.3 and 4.4.

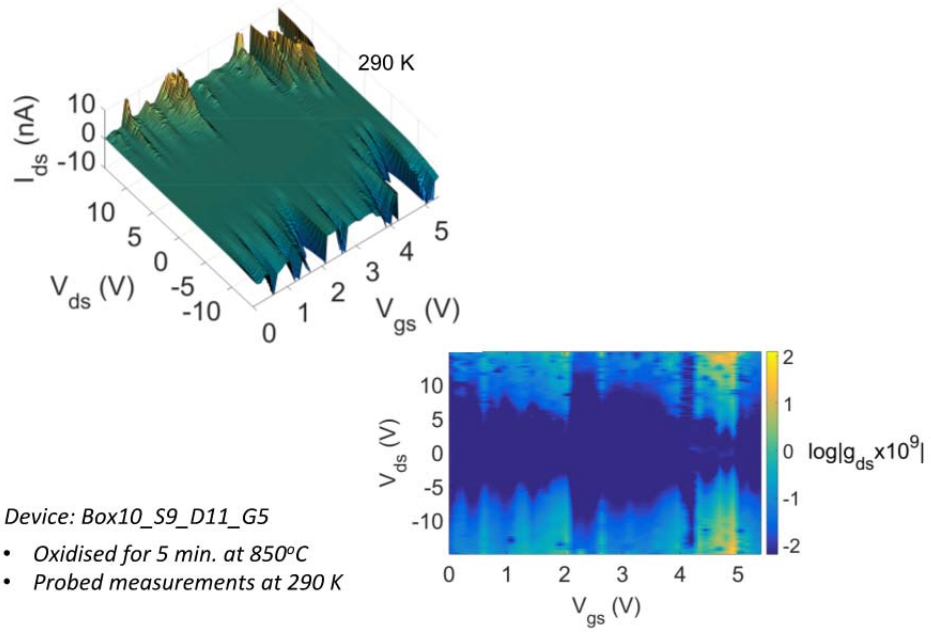

Fig. 4.3 The RT characteristics of Device 10_S9_D11_G5 are shown as a 3D plot of I_{ds} vs. V_{ds} and V_{gs} and as a linear colour plot of log $|g_{ds} \times 10^9|$ vs. V_{ds}, V_{gs}. These results show clearly the existence of a Coulomb gap and several coulomb diamonds, indicating RT SET behavior.

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The results of Fig. 4.3 show an RT Coulomb blockade characteristics very similar to the EBL fabricated devices. Two large low-current Coulomb diamond-like regions (dark blue central regions, lower plot), with an additional, finer oscillation, can be seen. However, this central region is very broad, implying the existence of a significant series or underlying potential barrier in addition to the QD (Sec. 2). In contrast, the results of Fig. 4.4 show a device where the Coulomb diamond widths are ~ ±1.5 V, comparable to the results shown in Sec. 2. It is also possible to fully modulate the diamond width to zero, e.g. for the diamond centered at V_{gs} = 0.3 V.

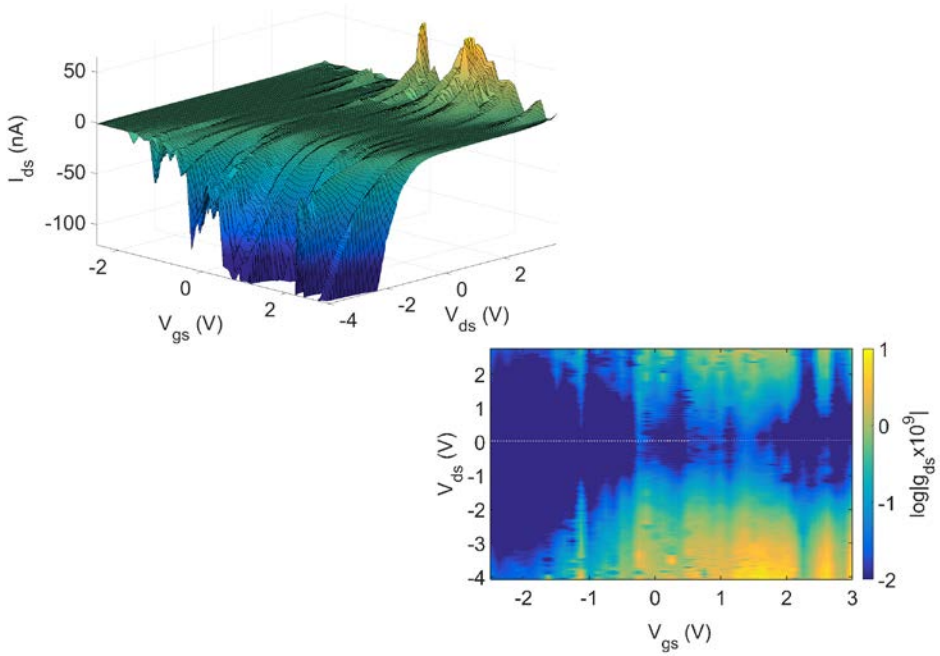

Fig. 4.4 The RT characteristics of Device 10_S10_F22_G8 are shown as a 3D plot of I_{ds} vs. V_{ds} and V_{gs} and as a linear colour plot of log $|g_{ds} \times 10^9|$ vs. V_{ds}, V_{gs}. These results again show clearly the existence of a Coulomb gap and several coulomb diamonds, indicating RT SET behavior.

Figure 4.5 shows the log $|g_{ds} \times 10^9|$ vs. V_{ds}, V_{gs} results of Fig. 4.4 with three Coulomb diamonds, *A*, *B* and *C*, marked by dashed lines. Using the model presented in Sec. 2, it is possible to extract electrical parameters for the underlying QD. It is found that the QD diameter is ~1.7 nm, very similar to the results for EBL fabricated devices. The QD total capacitance and gate capacitance are C = 0.364 aF and C_g = 0.16 aF, respectively. This corresponds to a QD addition energy E_a = 0.753 eV, again similar to the best devices fabricated by EBL. We note the close match in extracted QD size, even though the device was fabricated by a different method, with a slightly different layout. This supports our model of isolated donor atoms forming the QDs.

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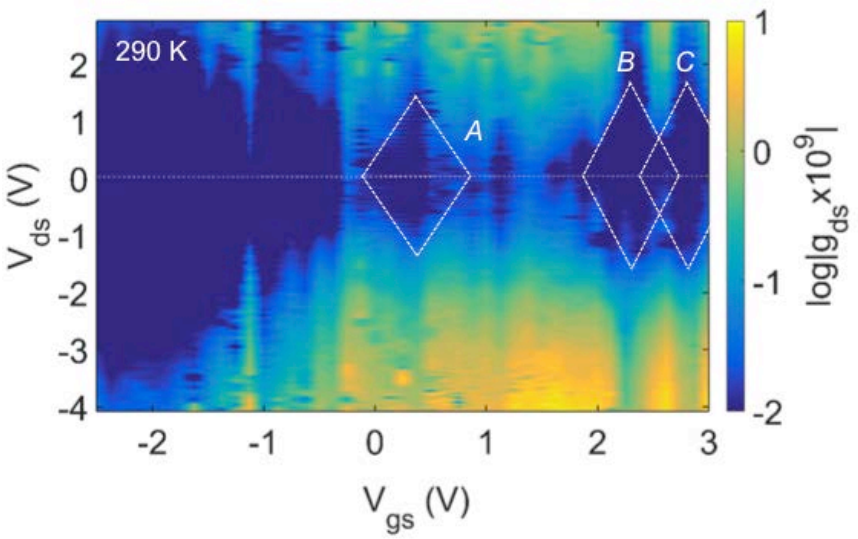

Fig. 4.5 Three Coulomb diamonds marked for the results of Fig. 4.4. Diamond 'A' is fully modulated by V_{gs}.

In addition to the work on single SET structures, the fabrication of a SPL defined inverter circuit has also been demonstrated. The principal of this can be seen by reference to the circuit diagram in Fig. 4.6, where 2 SETs are connected in series. The gate terminals for the two devices are used to bias these on upward (i.e. increasing current) part of a current oscillation (lower SET) and a downward (i.e. decreasing current) part of a current oscillation. The lower and upper SETs are then analogous to *n*- and *p*-FETs respectively, creating an inverter circuit.

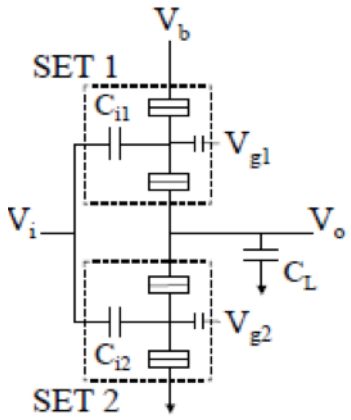

Fig. 4.6 Circuit diagram for the design of an inverter circuit, based on the use of two SETs

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This has being realised using a similar approach to the individual devices (Fig. 4.7). Work is currently in hand to complete the fabrication (oxidation and bond pad definition) and hence subsequent testing of these circuits.

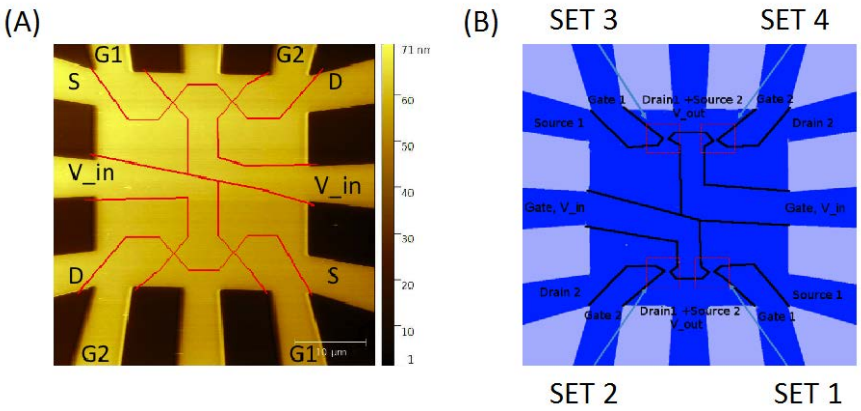

Fig. 4.7 A diagrammatic representation of the SPL lithography of a 2-SET inverter circuit showing the exposed lines.

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5. RT QD MEMORY DEVELOPMENT WITH SETS DEFINED AT IBM-SL

Room temperature, thermal SPL (t-SPL) fabricated point-contact SET devices have been used as the basis of a single-electron memory circuit, in a collaboration between IBM/SL and ICL. Details of the fabrication process for t-SPL point-contact SETs have been described in depth in milestone MS17 and are therefore not repeated here. In summary, ultra-thin SOI chips with a top Si layer of ~12 nm were used, where the top Si layer was highly *n*-doped at IMEC, at $>10^{20}$ /cm^3. In addition, the top SOI layer was pre-patterned to give a central Si square where active devices could be made with leads to contact pads. The device features were defined by thermal SPL and dry etching at IBM/SL. Devices were then sent to ICL for thermal oxidation and contact/bond pad definition. It will be seen that once again, geometric oxidation was used to form the actual device, by isolating QDs within the nanoscale SiO_2 region formed at the point-contact neck.

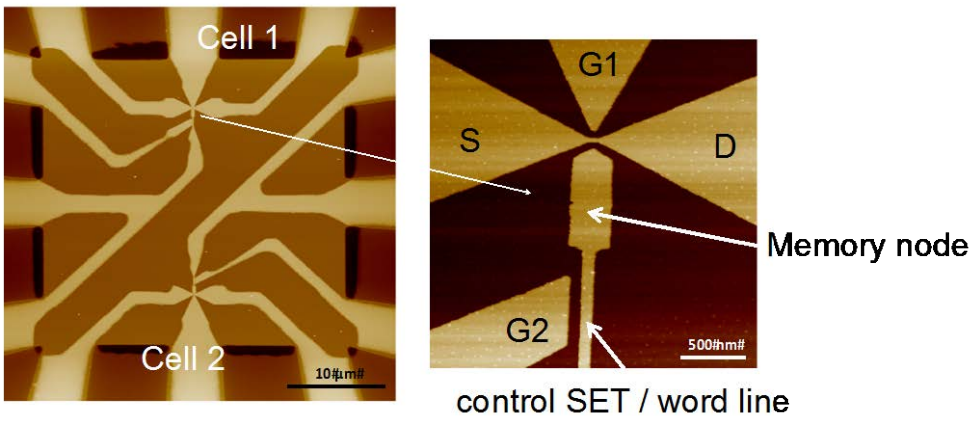

Figure 5.1 AFM Micrograph showing the design of a SET-based memory device, using t-SPL to define the structure in PPA (polyphthalaldehyde) resist, for etching into the top silicon layer.

Figure 5.1 shows AFM images of a field of two memory cells (left image). Details of one of the cells are shown in the right image. Here, charge is trapped on a memory node by the Coulomb blockade of a nanowire SET, which forms the word line for the device. This charge is then sensed by a point-contact sense SET (source, drain and gate regions are labeled *S*, *D* and *G1*). The cell may operate as a single-electron memory at RT if the control SET is able to operate at RT. The sense SET allows sensing with single charge precision.

Figure 5.2 shows the $I_{ds} - V_{ds}$, V_{gs} characteristics at RT= 290 K, for a sense SET controlled through the word line (V_{gs} was applied to this line). A very strong current oscillation is observed in I_{ds} with V_{gs}. The $I_{ds} - V_{ds}$ characteristics are asymmetric, with a stronger current peak observed for $V_{ds} > 0$ V. The curves are qualitatively similar to the EBL point-contact SETs discussed in Sec. 2. However, in the device of Fig. 5.2, the conductance appears to be somewhat higher than is typically observed for the EBL fabricated devices, with $I_{ds} \sim 100$ nA

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for an oscillation peak, at V_{ds} = 0.3 V, implying a resistance ~ 3 MΩ. This is due to a somewhat wider pre-oxidation point-contact width ~60 nm, implying lower lead in contact resistances. Furthermore, the strength of the current oscillation suggests a resonant tunnelling effect through the underlying QD electron state. The measurement of full memory cell operation in these devices is however ongoing.

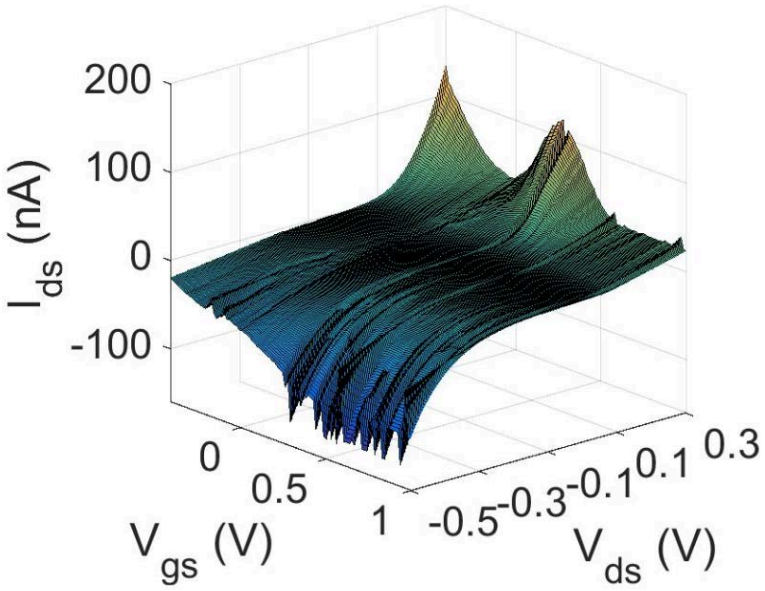

Figure 5.2 I_{ds} – V_{ds}, V_{gs} characteristics at RT= 290 K, for a sense FET controlled through the word line. A strong single-electron current oscillation is observed.

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6. ELECTRICAL CHARACTERISATION OF NANOGAP TRANSISTORS INCORPORATING ELECTRON BEAM DEPOSITED ISLANDS

This section reports on work conducted in collaboration with TUD, on the fabrication and measurement of nanogap transistors incorporating electron beam deposited islands. Device structures were fabricated initially at Imperial College London (ICL), using the standard SET process, based on EBL definition of side-gated point-contact structures in silicon-on-insulator (SOI) material. A (100) oriented, *n*-type heavily-doped SOI chip (1 cm^2 area) was used, with a ~20 nm thick top Si layer doped at ~10^{20} /cm^3. Normally, a geometric oxidation process is used to reduce the width of the silicon channel from ~5 nm to zero in the narrowest part of the point-contact. This leads to a small silicon island or dopant atom creating a quantum dot in the point-contact 'neck'. However, for devices used in this work, the neck was 'cut back' in the EBL patterns to leave a nano-gap in the silicon between the source and drain, as shown in Figure 6.1.

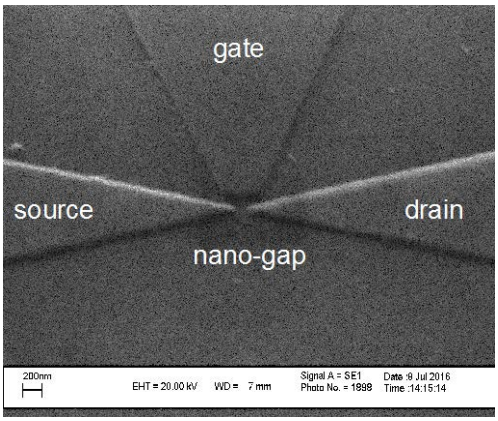

Figure 6.1 An SEM micrograph of the nano-gap point-contact, showing the source, drain and side gate regions in the doped silicon of the top layer of the SOI wafer. A ~100 nm wide nano-gap is etched between the source and drain regions.

Devices were fabricated within 16 mini-chip areas, arranged in a 4 × 4 matrix, as shown in Figure 6.2.

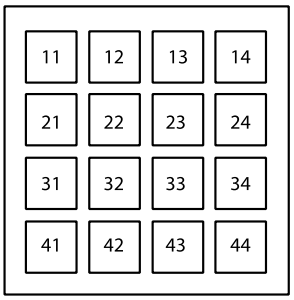

Figure 6.2 Mini-chip arrangement within the 10 mm × 10 mm chip

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Each of the mini-chips incorporated 8 devices, in which the source, drain and gate electrodes could all be independently addressed. Figure 6.3 shows a SEM image of the device layout on a mini-chip. Each device shares the drain contact with its neighbour, while the source and gate contacts are unique for each device. Following fabrication of the nano-gap structures, the devices were sent to Delft for electron beam induced metal deposition in the nano-gap region. Nanowires, and nanodots were deposited across the nano-gaps in 23 devices, to allow electrical measurements to be preformed in these structures and investigate the nature of the deposited nano-structures. $I_{ds} - V_{ds}$, V_{gs} measurements were performed initially using a room-temperature (RT) prober. 10 of the devices could be measured at RT, as in these devices both non-zero I_{ds}, and gate leakage current I_{gs} ~ 10 pA or less was observed. Following these measurements, promising devices were wire-bonded for low-temperature measurement, and of these, two devices, i.e. device 31-4 and 33-5, could be measured down to 50 K and 8 K respectively.

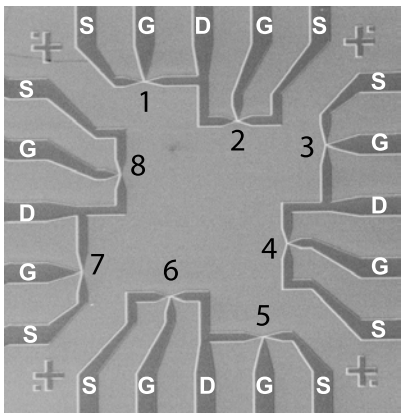

Figure 6.3 Layout of one of the 16 mini-chips, showing the central area containing 8 transistors (numbered), each with a ‘nano-gap’ and a single side gate.

The RT $I_{ds} - V_{ds}$, V_{gs} characteristics of 10 devices having electron beam deposited nanostructures, placed across Si nano-gap point-contacts, were measured. These nanostructures consisted of 6 nano-dot devices (11 nm – 16 nm across), and 4 nanowire devices (~12 nm – ~60 nm width). A range of *I-V* characteristics were observed, with symmetrical non-linear (3 devices), asymmetric diode-like (2 devices), and linear behaviour (1 device). Weak oscillations in I_{ds} with V_{gs} were observed in 4 nano-dot devices, and current steps in 3 nano-dot devices. Three of these devices, 31-4, 33-5, and 34-1 were of specific interest and are summarised below. The SEM image of the specific structure, RT $I_{ds} - V_{ds}$, V_{gs} characteristics, and comments regarding the deposited nanostructure size, and the electrical characteristics, for each device, are provided. The average device conductance *G*, outside any central low current threshold region in V_{ds}, is also reported for each device.

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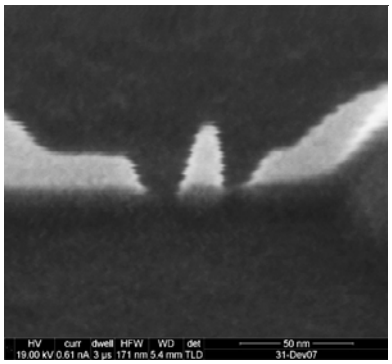
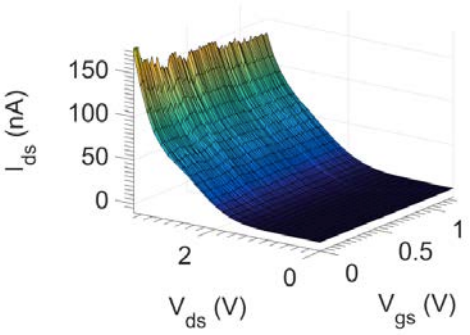
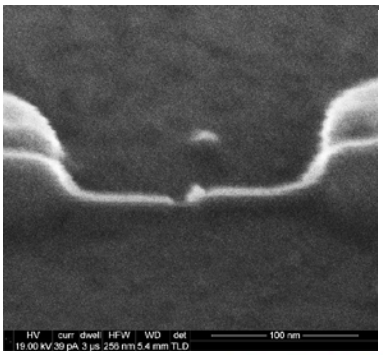
Device 31-4

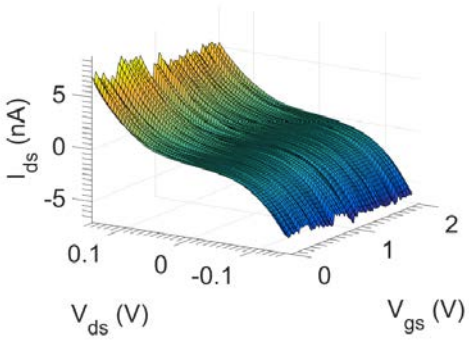


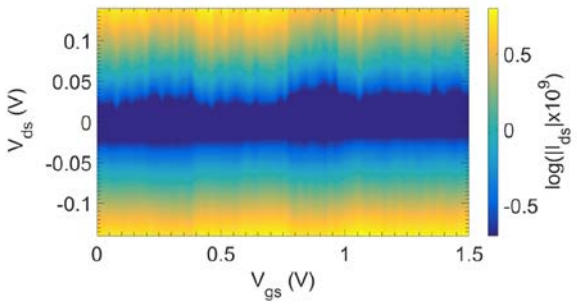


Device No.	*Type/Dimension (nm)*	*Avg. G (nS)*	*Comment*
31-4	Dot/16	72	*I-V* characteristics asymmetric, forward bias shown. Current step observed at V_{ds} ~ 3V. This is modulated by V_{gs}, and a weak I_{ds} oscillation with V_{gs} is seen. Curve origin may be a Coulomb staircase, or traces of a thermally overcome resonant tunnelling peak.

Device 33-5







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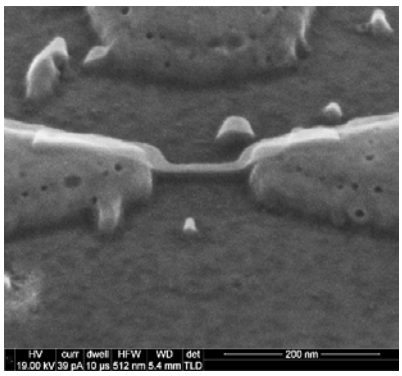
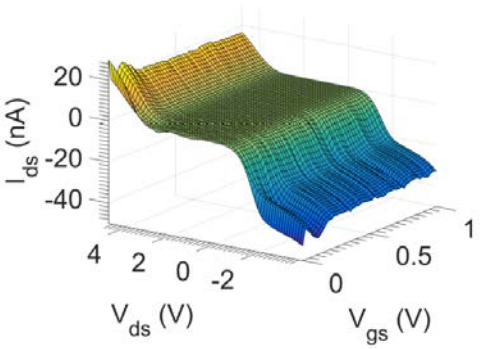
Device No.	*Type/Dimension (nm)*	*Avg. G (nS)*	*Comment*
33-5	Dot/11.1	33.3	*I-V* characteristics symmetric, with small threshold drain-source voltage V_{th} ~ 0.02 V. An I_{ds} oscillation with V_{gs} is seen, creating weak diamond like regions. An image plot of log $\|I_{ds}\|$ vs. V_{ds}, V_{gs} also shows diamond like regions. Device resembles RT SETs fabricated by ICL in Si, though the current oscillation is weaker. Dot size is small, only ~ 10 nm. Dot may be connected to lead-in region on the right hand side better than on the left hand side.

Device 34-1





Device No.	*Type/Dimension (nm)*	*Avg. G (nS)*	*Comment*
34-1	Nanowire/12.5	12.5	*I-V* characteristics symmetric, with threshold drain-source voltage V_{th} ~ 2 V, this is larger than in the previous device, No. 33-5. An I_{ds} oscillation with V_{gs} is seen, similar to the previous device, No. 33-5. Device resembles RT SETs fabricated by ICL in Si, though the current oscillation is weaker. Rather than a dot, this device has a nanowire of small dimensions ~10 nm. Given that the characteristics are similar to the dot based device No. 33-5, the characteristics may be due to disorder along the lead-in regions, creating a dot like structure. Alternatively, thinning of the nanowire as it crosses onto the Si may create a long ‘nanowire’ like dot in the nano-gap.

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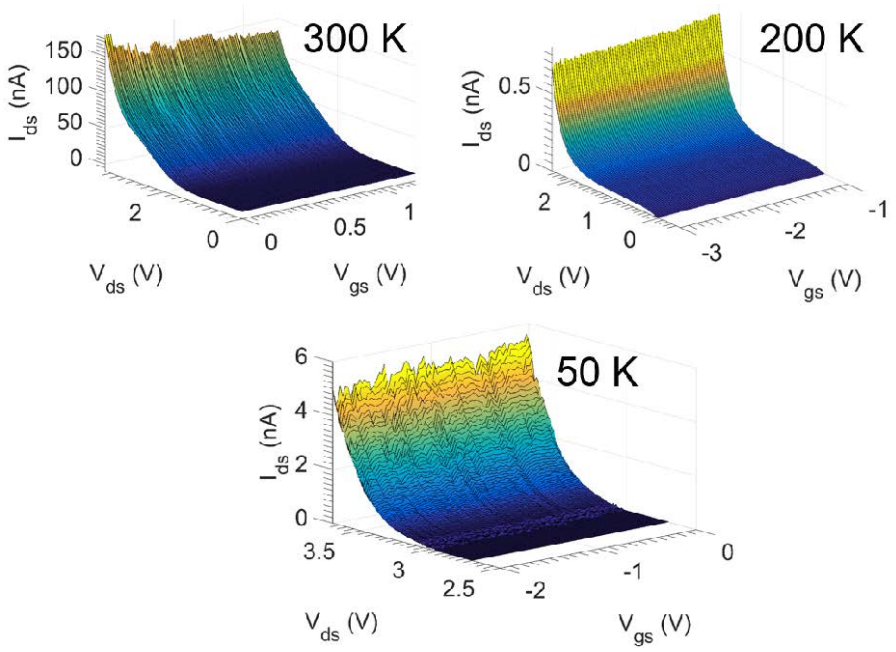
In device No. 33-5, with the smallest dot size (11 nm) the current oscillations are clearest for the nano-dot devices, and though weaker, resemble RT results for Si point-contact SETs. It may be possible to attribute these characteristics to RT SET operation, though further analysis is needed. In the nanowire devices, the electrical characteristics in 2 devices are symmetrical and non-linear, in 1 device are broadly linear, and in 1 device are asymmetric and diode-like. In device No. 34-1, the current oscillations are clearest for the nanowire devices, and resemble the nano-dot device No. 33-5. Given this, the nanowire device characteristics may be due to disorder along the lead-in regions, creating a dot like structure. Alternatively, thinning of the nanowire as it crosses onto the Si may create a long 'nanowire' like dot in the nano-gap. It may be possible to attribute these characteristics to RT SET operation, though further analysis is needed.

In 9/10 devices the overall the average conductance was found to lie between ~10 nS and 70 nS, and appears not to depend on the nanostructure width. This suggests that the Si/metal contact is dominant. In this case, a Schottky barrier at one of the Si/metal interfaces would lead to the diode-like curves, and at both of the Si/metal interfaces (back-to-back Schottky like), would lead to the symmetrical, non-linear curves. The Schottky barrier behaviour is additional to any single-electron charging effects in the devices.

The temperature dependences of two of the devices (nano-dots, Nos. 31-4 and 33-5) were measured following wire-bonding. (During this process can induce gate current leakage, preventing further characterisation of a device.) The two temperature dependencies are presented below.

Temperature Dependence of Device 31-4:



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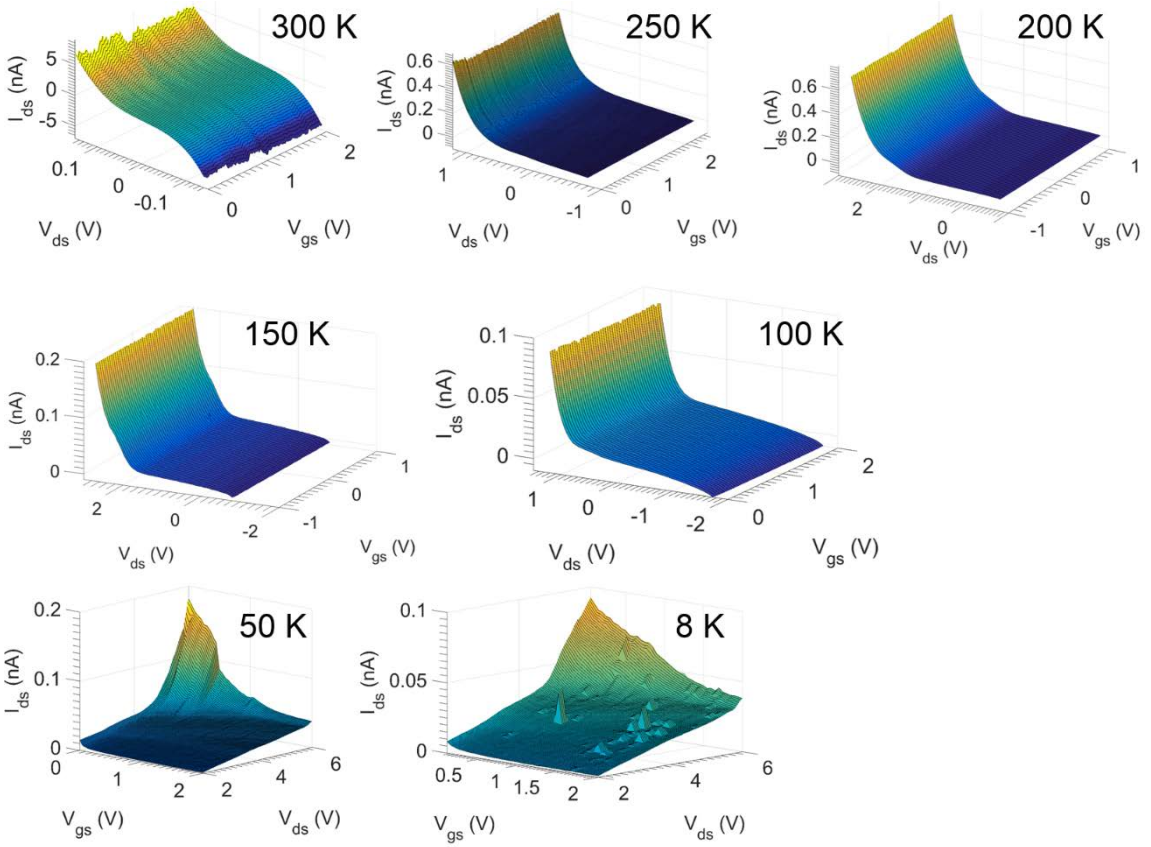
This device consisted of a 13 nm size nano-dot, with *I-V* characteristics which were asymmetric and diode like (forward bias shown above). At RT, a weak current step observed at V_{ds} ~ 3V. A drain-source threshold voltage V_{th} ~2 V exists at RT, tending to increase to ~ 3 V at 50 K. The weak current oscillations in I_{ds} with V_{gs} are not consistent as the temperature reduces, however qualitatively, these become more pronounced at 50 K. The step-like characteristics do not become more pronounced at lower temperature, making it difficult to attribute these to a Coulomb staircase in this device.

Temperature Dependence of Device 33-5:



This device consisted of a 11 nm nano-dot, with symmetric *I-V* characteristics, and a small threshold drain-source voltage V_{th} ~ 0.02 V at RT. An I_{ds} oscillation with V_{gs} is seen at RT, creating weak diamond like regions. The device resembled RT SETs fabricated by ICL in Si, although the current oscillation is weaker. As the temperature was reduced, the oscillation in current disappears, implying that a thermally activated current was essential to observe these. Furthermore, the *I-V* characteristics become asymmetric and diode like below 250 K. This suggests that a Schottky barrier at the Si/metal interface becomes significant at lower temperatures, and supresses the thermally activated RT current oscillation. The device conductance reduces as the temperature is reduced. At lower temperatures, 50 K and 8 K, where any thermally activated current is low, tunnelling across the Schottky barrier can dominate. In this regime, a strong gate effect occurs, with suppression of the current as V_{gs}

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increases. This is *p*-type device like behaviour is accompanied by the recovery of non-linear variation in the current as gate voltage is varied, and the appearance of steps in the current with V_{ds}. A Coulomb charging origin is possible for the results at 50 and 8 K, possibly associated with the full length of the deposit forming the charging island, and the Si/metal Schottky barriers forming the tunnel barrier. Further analysis of the data, including extraction of barrier heights from the Arrhenius plots of the current vs. inverse temperature, may help to support this model.

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7. APPENDIX

7.1 Energy band diagrams for a QD:

A discussion of the Coulomb diamond region, shown schematically in Fig. 2.8(b) and reproduced here as Fig. A1, is now provided.

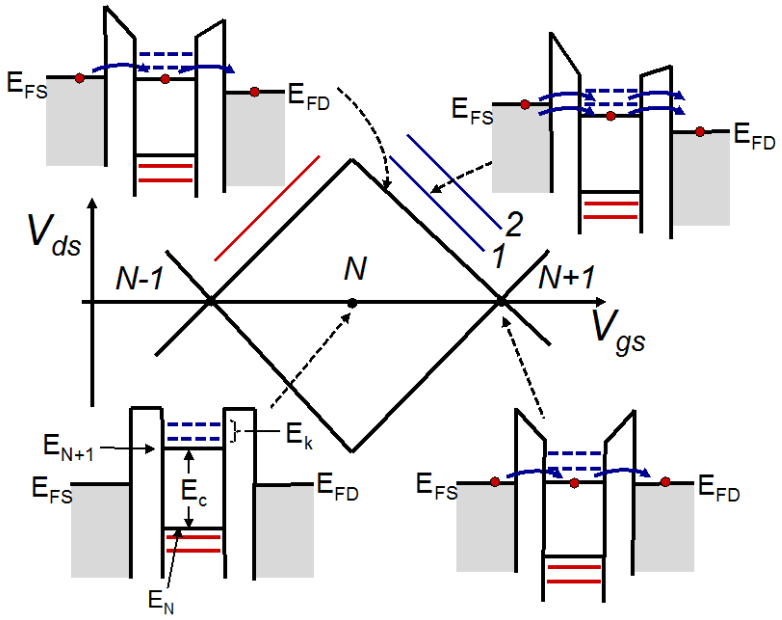

Figure A1. Schematic interpretation of the energy band diagrams associated with the Coulomb diamond region in the V_{ds} *vs.* V_{gs} plot for transistor QD1.

At the centre of the Coulomb diamond (bottom left inset), Coulomb blockade is imposed. At the corners of the Coulomb diamond along the V_{ds} = 0 V axis, a transition occurs to $N + 1$ (right corner) and $N - 1$ (left corner) electrons. The bottom right inset shows the energy diagram with E_{N+1} aligned to the source/drain Fermi energies E_{FS}/E_{FD}, allowing electron tunnelling across the QD. Along the edges of the diamond, either E_{N+1} (top, bottom right edges) or E_N (top, bottom left edges) remain aligned with either E_{FS} (top half of diamond) or E_{FD} (bottom half of diamond) respectively. The top-left inset shows the situation for the top right diamond edge.

Resonant tunnelling can occur through excited states outside the Coulomb diamond. The top right inset shows the energy diagram when E_{N+1} and the first excited state above this lie within the energy window $E_{FS} - E_{FD}$. Resonant tunnelling can then occur through both E_{N+1} and the first excited state, leading to a peak in g_{ds}. This leads to a conductance line parallel to the right diamond edge. For larger $E_{FS} - E_{FD}$ windows, additional excited states (blue lines) can lie within this, creating additional resonant tunnelling lines along the Coulomb diamond. Finally, for lines parallel to the left diamond edge, resonant tunnelling states below E_N (red lines) lie in the $E_{FS} - E_{FD}$ window.

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7.2 Extraction of E_a, E_c, E_k and E_1:

E_a may be extracted from the width ΔV_{ds} of part of the Coulomb diamond lying outside the overlapping sections (solid white lines, Fig. 2.8(a)), e.g. for diamond *B*, $\Delta V_{ds} = V_{ds,b} - V_{ds,e}$. Here, $V_{ds,b}$ and $V_{ds,e}$ are the V_{ds} values for point *b* and *e*, in Fig. 2.8(a). The addition energy is then $E_a = e\Delta V_{ds}/2$, where we assume equal voltage drops across both tunnel barriers. Here, the Coulomb gap (Fig. 2.8(b) and A1) is $E_c = e^2/C$. We then assume a spherical QD of radius *r*, appropriate for a QD formed within an oxidised, symmetrical point-contact structure. The QD self-capacitance may be used for the total capacitance, $C = 4\pi\varepsilon_r\varepsilon_0 r$, where $\varepsilon_{\square}$ is the relative permittivity of SiO_2 and ε_0 is the dielectric constant. The energy needed to charge the QD by an additional electron as V_{ds} is increased (ignoring the contribution of quantum confinement) is then $E_{c1} = E_c/2 = e^2/2C = e^2/(8\pi\varepsilon_r\varepsilon_0 r)$. For a spherical quantum QD, $E_k = \pi^2\hbar^2/2mr^2$ where *m* is the electron effective mass in Si. The equation $E_a = E_{c1} + E_k = e^2/(8\pi\varepsilon_r\varepsilon_0 r) + \pi^2\hbar^2/2mr^2 = e\Delta V_{ds}/2$ may then be solved to find *r* and hence E_c and E_k. For Coulomb diamond *B*, we find E_a = 0.83 eV ~ $30k_BT$ at 290 K, and *r* = 0.8 nm. Finally, the separation in V_{ds} between the resonant tunnelling lines and the Coulomb diamond edge (e.g., for diamond *B*, these are line '1' and edge *bc*) gives the first excited state energy E_1. For diamond *B*, E_1 = 1.3 eV, with a separation from the ground state $\Delta E = E_1 - E_a$ = 0.5 eV.