Funded by
the European Union

Collaborative project*

Project acronym: SNM

Project full title: "**Single Nanometer Manufacturing for beyond CMOS devices**"

Grant agreement no: 318804

Deliverable: D9.5 ("Report on the fabrication of a scaled MoS_2 transistor with a sub-10 nm channel length")

Name of the coordinating person: Prof. Dr. Ivo W. Rangelow, Email: ivo.rangelow@tu-ilmenau.de

List of participants:

Participant no.	Participant organisation name	Part. short name	Activity Type	Country
1 (Co)	Technische Universität Ilmenau	**TUIL**	HER	Germany
2	IBM Research GmbH	**IBM**	IND; End-user	Switzerland
3	École polytechnique fédérale de Lausanne	**EPFL**	HER	Switzerland

SNM
Work Package 9
Deliverable: D9.5 ("Report on the fabrication of a scaled MoS_2 transistor with a sub-10 nm channel length")

Lead beneficiary number	9	**Nature**	R	**Dissemination level**	PU
Estimated Person-months	14				

Person-months by partner for the Deliverable

EPFL	IBM	TUIL					
5	5	4					

Estimated Delivery Date	M48: 31/12/2016	**Delivery Date**	10/03/2017 05/09/2017 revised
Author	• Sajedeh Manzeli, Andras Kis (EPFL, Lausanne); Armin Knoll (IBM Zurich)		
Reviewed by:	• WP9 Leader Andras Kis • WPG2 Leader: Zahid Durrani • Coordinator: Ivo W. Rangelow		

Criteria and Achieved Results	**Criteria**	**Achieved result**
	Use of SNM methods for patterning MoS_2	t-SPL and FE-SPL have been applied to patterning MoS_2
	Pattern dimensions, Half pitch	Half pitch as low as 18 nm

Description of the Deliverable

This deliverable is related to the successful fabrication of ultra-narrow nanoribbons of two-dimensional material MoS_2 using lithographic techniques developed by the SNM consortium.

Two approaches are currently being pursued, reported previously in MS20: a) Thermal scanning probe lithography (t-SPL) in collaboration with A. Knoll. and b) Field-Emission scanning probe lithography (FE-SPL) in collaboration with I.W. Rangelow.

a) **Thermal scanning probe lithography.** In collaboration with Armin Knoll, thermal scanning probe lithography used to fabricate field effect transistors (FETs) with MoS_2 channels.

Initial attempts on patterning MoS_2 using t-SPL have been facing difficulties due to problems with the adhesion of the resist layer on the substrates. The poor adhesion seriously limited the throughput of t-SPL patterned MoS_2. We identified the source of this problem to be the humidity and water adsorption on the substrate surface. Therefore, we tried to minimize the exposure of substrate to the humidity by storing the samples in Ar ambient and minimizing the time between the transfer of CVD MoS_2 on the substrate and coating the resist stack. This strategy has proven to be effective in resolving the adhesion issue.

The other factor that limited the throughput of t-SPL patterned MoS_2 was the damage introduced to the material during the resist-stripping step after the pattern transfer. This issue also restricted the use of more robust patterning stacks that would allow higher patterning resolution. To address this issue, at this point, we have decided to skip stripping of the patterning stack and it would remain on top of the transferred patterns. Figure 1. schematically illustrates the process flow for t-SPL patterning of MoS_2-based devices.

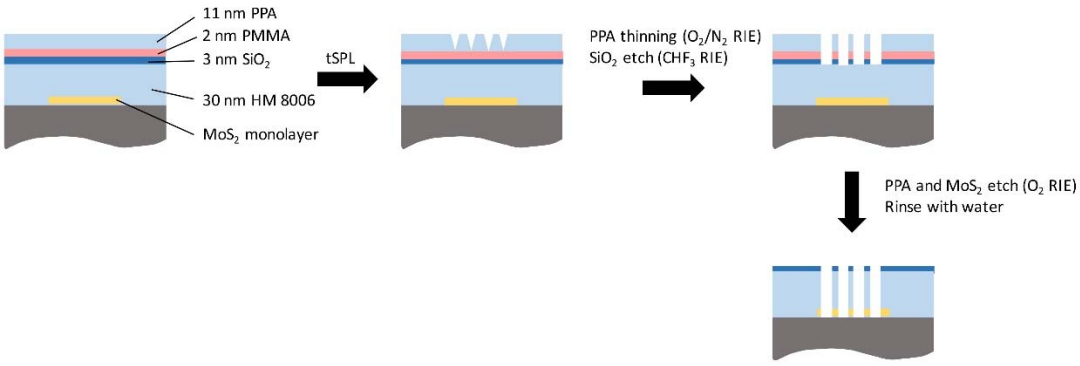


Figure 1. Schematic of the process flow used for patterning the MoS_2. The initial resist stack allowing the enhanced the patterning resolution. Following t-SPL, the pattern transfer has been achieved in two steps of dry etching.

The proposed process flow is briefly outlined here:

1. Transfer of CVD-grown monolayer MoS_2 onto a chip, consisting of degenerately

doped Si covered with a 270 nm SiO_2 layer, used as a standard substrate for device fabrication at EPFL. (done at EPFL)

2. Deposition of metal electrodes on MoS_2 using standard electron beam lithography (EBL) (using double layers resist) and thermal evaporation of Ti/Au (3 nm/17 nm) followed by lift-off. The use of double layer resist is crucial to prevent the deposition of metal on the resist sidewalls leading to the formation of "ears" from the lift off process. Such features strongly disrupt the spin coating of the pattern transfer stack required for the t-SPL. (done at EPFL)
3. Removing the residual MoS_2 between the metal electrodes using O_2 plasma etching. (done at EPFL)
4. A 30 nm thick layer of HM 806 or other similar resist layer was deposited first. (done at IBM)
5. SiO_2 deposition (3 nm thickness). (done at IBM)
6. 2 nm thick layer of PMMA is deposited to enhance the patterning resolution. (done at IBM)
7. Finally, the pattern stack would be completed with deposition of 11nm of PPA. (done at IBM)
8. Scanning probe lithography step resulting in local removal of PPA. (done at IBM)
9. Pattern transfer from PPA to SiO_2 using O_2/N_2 RIE and CHF_3 RIE respectively. (done at IBM)
10. Pattern transfer from SiO_2 to HM 8006 and MoS_2 using O_2 RIE followed by DI water rinse. (done at IBM)

Unlike in the case of FE-SPL or o-SPL (oxidation scanning probe lithography), the t-SPL method does not require the material to be electrically contacted. Therefore, the second step of the process flow is not necessary in case of investigations of optical properties.

Figure 2 shows the AFM topography image of a monolayer MoS_2 single-crystal domain, patterned using above-mentioned process flow. The high-magnification AFM image of the flake (Figure 2.a) shows the t-SPL patterned lines with the height profile along the solid line (Figure 2.b) indicating a half-pitch equal to 32 nm.

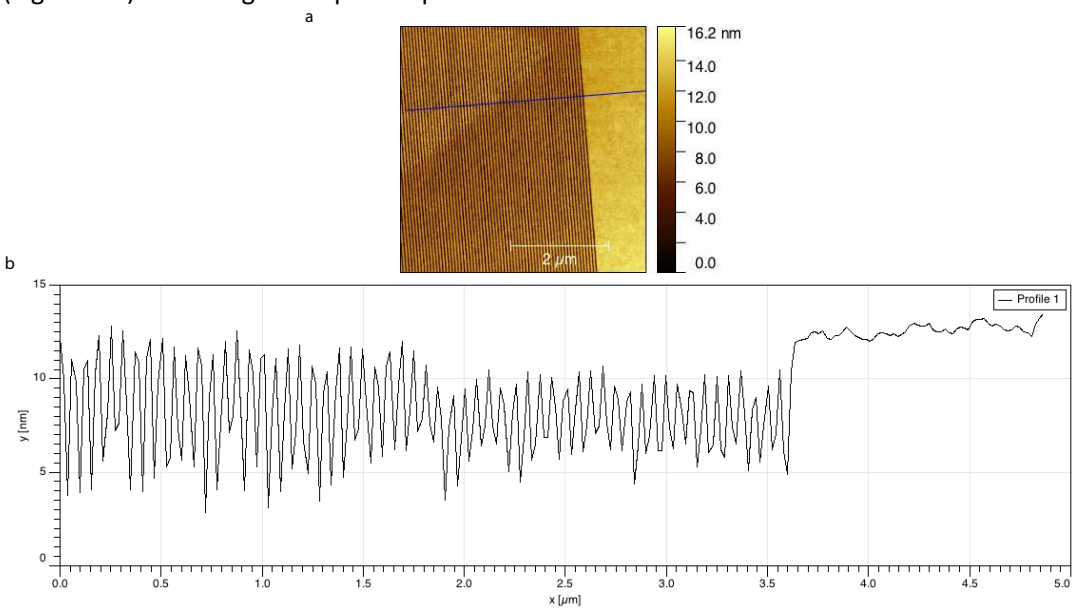


Figure 2. (a) High magnification AFM image of a t-SPL patterned monolayer MoS_2 single-

crystal flake. (b) The height profile along the solid line in (a). The half-pitch is 32 nm.

Similarly, t-SPL is used to pattern the channel areal of MoS_2-based FETs. Figure 3.a and 3.b show respectively, the low-magnification AFM image of the height profile and phase of such a FET where an array of narrow ribbons have been patterned along the width of the channel (marked by the red box). Figure 3.c shows a high-magnification height profile of the patterned area demonstrating ribbons of width ~18 nm and length ~350 nm.

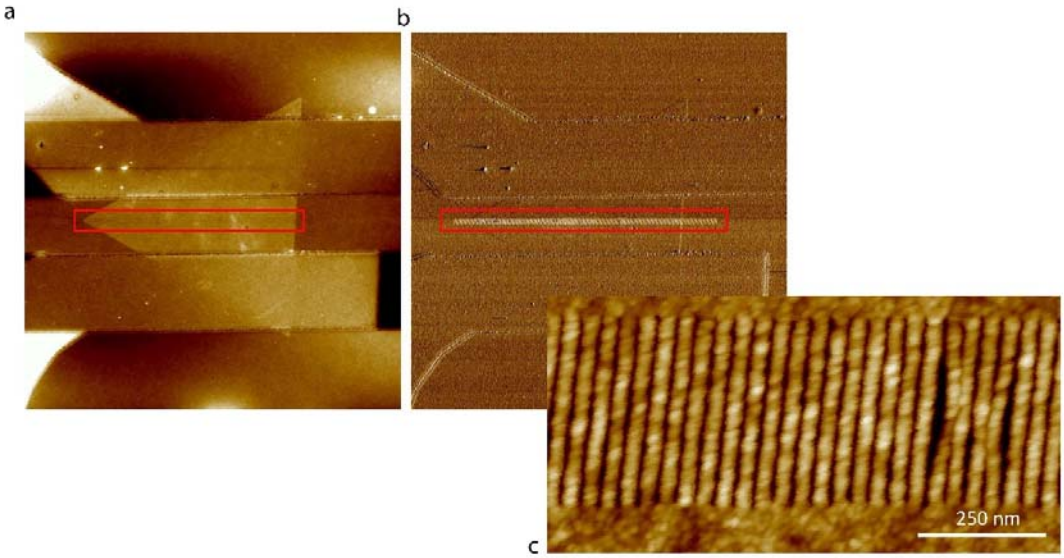


Figure 3. (a) AFM topography image of the monolayer MoS_2 channel and the metal electrodes. T-SPL has been used to pattern an array of ribbons (width ~18 nm and length ~350 nm), along the width of the channel. (b) AFM phase image of the same device as in (a). (c). The high-magnification AFM topography image of the patterned ribbons.

Skipping the steps required for stripping the patterning stack off the material, not only allowed the higher resolution of patterning but also resulted in an increased yield of the devices. The remained patterning stack is expected to be optically and electrically in-active. This assumption would be verified during the subsequent electrical and optical characterization of the patterned materials.

b) **Field-Emission scanning probe lithography**. Field-emission scanning probe lithography (FE-SPL) in collaboration with I. Rangelow at TU Ilmenau, has been used to pattern the channel area of FETs based on MoS_2. Using FE-SPL, it is possible to induce local chemical transformations which would convert MoS_2 to Mo oxide. Mo oxide is water-soluble and could be removed via rinsing the sample with water.

First proof of the concept used exfoliated MoS_2 flake on top of degenerately doped Si substrate, showing written lines as small as 19 nm after patterning and the narrowest ribbons after water wash were as narrow as 15 nm, shown in Figure. 4.

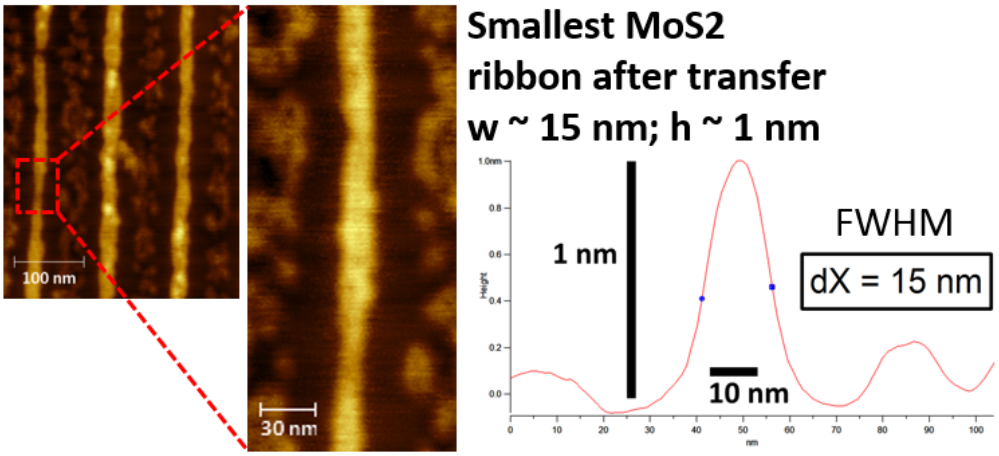


Figure 4. Smallest MoS_2 ribbon defined by FE-SPL. The AFM topographic image and corresponding section shows the MoS_2 nanoribbon after water rinse. A FWHM of 15 nm was achieved.

However, from an application point of view, MoS_2 deposited on a conductive substrate, such as degenerately doped Si, is not relevant. This is due to the fact that the conductive substrate would result in the quenched photoluminescence and also any electrical device designed on such substrate would, inevitably, have shunted electrodes.

Using FE-SPL to pattern MoS_2 on top of non-conductive substrates, requires electrically contacted materials since, in contrast to t-SPL, FE-SPL requires a ground path for the charges induced on MoS_2 during the patterning. While this would limit the ability of FE-SPL for patterning the non-processed atomically thin MoS_2 layers for the optical studies, FE-SPL could potentially be used for patterning the FETs based on MoS_2 channels.

To this end, CVD MoS_2 samples with metal electrodes have been sent to TU Ilmenau to be patterned using FE-SPL. However, despite the presence of conductive path for the charges, the FE-SPL resulted in a low yield of devices due to the occurrence of “spikes” due to the considerable charging of the MoS_2 channel. To address this issue, we applied an initially conductive resist layer which is coated prior to patterning and allows an efficient discharging of the channel.

The proposed process flow is briefly outlined here:

1. Transfer of CVD-grown monolayer MoS_2 onto a chip, consisting of degenerately doped Si covered with a 270 nm SiO_2 layer, used as a standard substrate for device fabrication at EPFL. (done at EPFL)
2. Deposition of metal electrodes on MoS_2 using standard EBL (using double layers resist) and thermal evaporation of Ti/Au (3 nm/17 nm) followed by lift-off. The use of double layer resist prevents the deposition of metal on the resist sidewalls leading to the formation of “ears" from the lift off process. Such features strongly disrupt the spin coating of the conductive resist required for the FE-SPL. (done at EPFL)
3. Removing the residual MoS_2 between the metal electrodes using O_2 plasma etching.

(done at EPFL)

4. Spin-coating and prebake of 25 nm conductive film (P3HT). (done at TUIL)
5. FE-SPL. (done at TUIL)
6. First wet development step (WD1) to remove polymer film: dipping in monochloro-benzene (10 s). Note that the crosslinked resist cannot be fully removed via wet development and stays over the pattern. (done at TUIL)
7. Second wet development step (WD2) to remove Mo oxide: water wash (10-15 seconds) cross-linked resist is partially removed during WD2. (done at TUIL)

FE-SPL patterning of the channel in MoS_2 based FETs is shown in Figure 5. Figures 5.a and 5.b schematically show an array of ribbons patterned along the width of the MoS_2 channel, where respectively, the ribbons length could cover part of or the entire channel length. Figure 5.c shows the AFM topography image of the patterned MoS_2 channel corresponding to Figure 5.a. The MoS_2 nanoribbons are patterned along the armchair direction of the lattice with the FE-SPL pitch of 220 nm, which resulted in a line width of ~ 80 - 120 nm of the nanoribbon after WD2 (= minimum expected ribbon width – see measurement limitations). Figure 5.d shows the AFM topography image of the patterned MoS_2 channel corresponding to Figure 5.b. The MoS_2 nanoribbons are patterned along the zigzag direction of the lattice with a SPL pitch of 140 nm, which has resulted in a nanoribbon line width of ~ 80 nm after WD2).

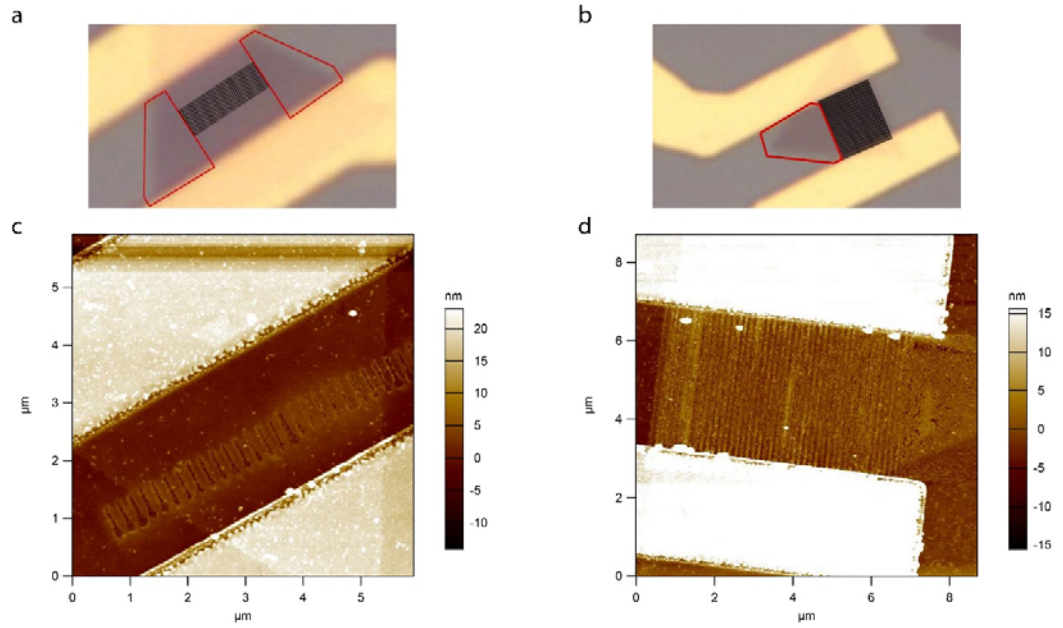


Figure 5.(a) Schematics of the design of an array of ribbons patterned along the width of the MoS_2-FET channel with the ribbons length covering part of the channel length. (b) Schematics of the design of an array of ribbons patterned along the width of the MoS_2-FET channel with the ribbons length covering the entire channel length. (c) The AFM topography image of the patterned MoS_2 channel corresponding to Figure 5.a. The MoS_2 nanoribbons are patterned along the armchair direction of the lattice with the FE-SPL pitch of 220 nm and a nanoribbon line width of ~ 80 - 120 nm after WD2. (d) The AFM topography image of the patterned MoS_2 channel corresponding to Figure 5.b. The MoS_2 nanoribbons are patterned along the zigzag direction of the lattice with a pitch of 140 nm resulting in ~ 80 nm nanoribbons after WD2.

Figure 6.a shows a high-magnification AFM topography image of patterned ribbons from Figure 5.c. The height profile along the red line is plotted in Figure 6.b.

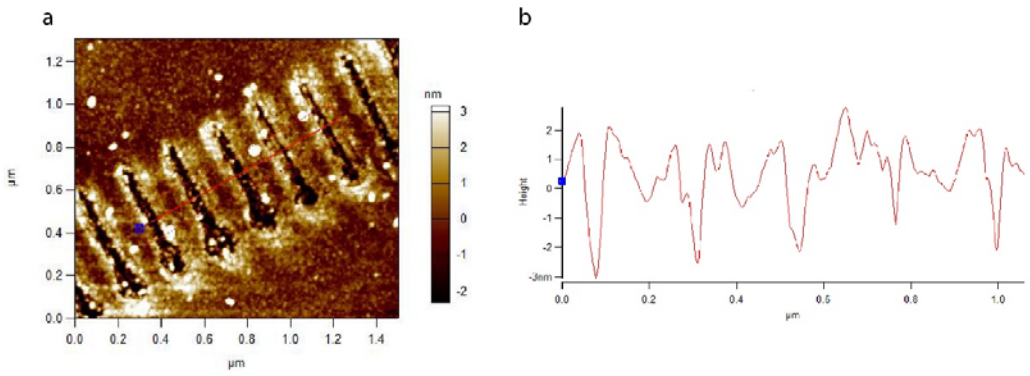
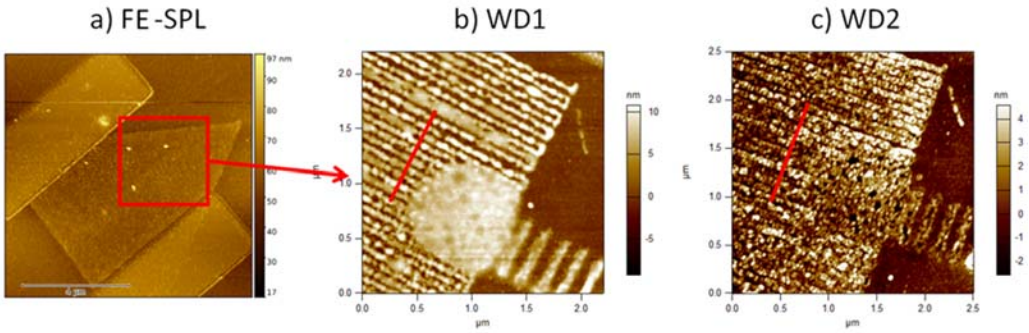
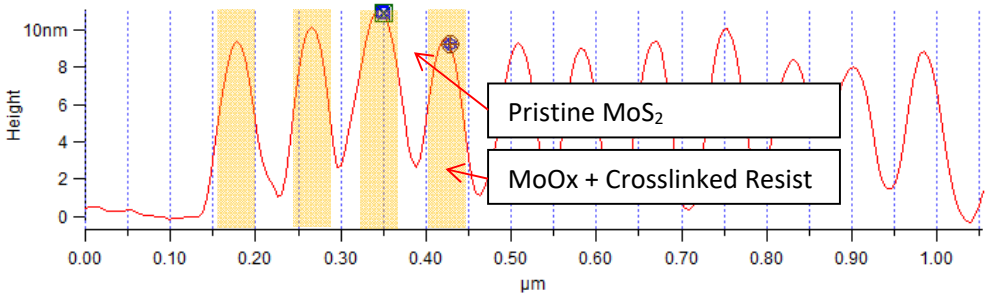


Figure 6.(a) High-magnification AFM topography image of patterned ribbons from Figure 5.c. (b) Height profile along the red line in (a).

Measurement constraints in FE-SPL patterning method:



AFM topography section corresponding to (b) – WD1



AFM topography section corresponding to (c) – WD2

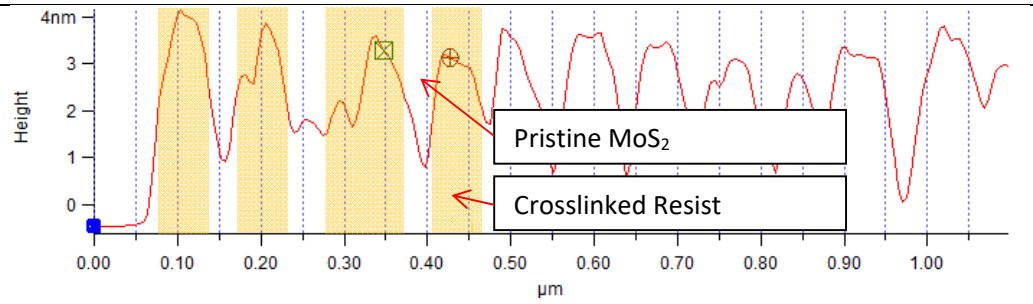


Figure 7. Measurement limitation and estimation of the nanoribbon line width. (a) AFM topographic image directly after FE-SPL exposure; (b) AFM topography after WD1; (c) AFM topography after WD2.

TUIL's pre-tests show that the MoOx lines (formed underneath the resist pattern within the MoS_2) are wider than the negative tone lines formed in resist (which are measured after the first wet development step). To assure the formation of MoS_2 ribbon TUIL increased the line in subsequent experiments. However, the exact size of the MoS_2 ribbon cannot be determined due to resist residuals left behind aside of the removed MoOx lines.

A corresponding example is shown in Figure 7. Clear distinguishable lines with a pitch of 80 nm are visible directly after the lithography. After the first wet development step, WD1, in order to remove unexposed resist, the lines become uneven (significant LER increase), but still remain recognizable. The measurable line width is approx. or less than 50 nm (due to the tip-sample convolution effect the real nanoribbon width cannot be determined). This is illustrated in section graph of Fig. 6-b by shaded areas. After the second wet development step (WD2), a water wash in order to remove the formed MoOx, the lines are only hardly recognizable (see section graph Fig. 6-c). During this process the height of the features are also removed from initially 10 nm after WD1 to approx. 4 nm after WD2. Due to the residuals of the resist, the final pattern in MoS_2 flake cannot be directly seen. The resist residuals can only be removed by a O_2 plasma process but this process would remove also the leftover MoS_2 flake. As for t-SPL, it was decided to skip the resist removing step and keep the leftover resist on top of the flake (resist residuals are non-conductive according to ref. *Brian A. Mattis, Yunan Pei, and Vivek Subramanian:* ***Nanoscale device isolation of organic transistors via electron-beam lithography,*** *APPLIED PHYSICS LETTERS* ***86****, 033113, 2005)*. The real ribbon size can only be measured by a surface sensitive analysis method with nanometer resolution, e.g. Nano-Auger spectroscopy (not available at TUIL). Thus, the real ribbon sizes can only be estimated and it is expected that the nanoribbon width is smaller than the measured gap between the crosslinked resist lines (FE-SPL patterning defines the place where the MoS_2 is converted into MoOx; the MoS_2 nanoribbon is then formed by the gap between the FE-SPL patterned lines).

Conclusion:

In the framework of SNM project, three different scanning probe lithography technique have been used to pattern MoS_2 as a representative of the 2D materials. These techniques

include Thermal scanning probe lithography (t-SPL), oxidation scanning probe lithography (o-SPL) and Field-emission scanning probe lithography (FE-SPL).

The results would rank these techniques according to their suitability for patterning of 2D materials as t-SPL and FE-SPL being the most promising approach followed by o-SPL due to the following arguments. First the highest patterning resolution achieved has been using t-SPL and FE-SPL which is below 20 nm for t-SPL and 15nm for FE-SPL. An advantage of t-SPL is the degree of freedom to pattern the 2D materials whether they are electrically contacted or not offers lots of flexibility for preparing the material according to the type of studies. This allows fabrication of patterned 2D layers without exposing them to additional micro fabrication steps, which is especially interesting for a variety of optical studies on the reach physics of this family of materials. However, by using conductive resists for FE-SPL processing the same capability as with t-SPL can be reached. FE-SPL as well as t-SPL has the drawbacks that for processing a stack of layers had to be placed on top of the MoS_2. In both cases, the resist remains on top of the MoS_2 layer.

In this context, o-SPL and FE-SPL offer the possibility to pattern directly the MoS_2 material without the necessity of etching steps.

In the case of o-SPL, the smallest channel width achieved is around 200 nm (D 9.3), limited by the line-edge roughness of the pattern. However, o-SPL offers the advantage over FE-SPL that the electrical contact required for discharging the 2D channel could be the same metal contacts as the FET source and drain terminals.

Feasibility report on the possibility to realize sub-10 nm MoS_2 transistor

t-SPL technique for realization of sub-10 nm MoS_2 devices:

The t-SPL technique is demonstrated to have the capability for reliably transferring sub-10 nm feature sizes into Si. Using optimal conditions, 14 nm half pitch lines were transferred into an ultrathin (12nm) silicon on insulator (SOI). After the pattern transfer, 7nm feature size and the line-edge roughness (LER) of 2.6 nm (3σ) is measured. Due to the presence of elevated topography between neighboring written lines, the feature size is not limited by the minimum half-pitch. Instead, the writing process and the applied transfer characteristics favor wider trenches and narrower walls. Therefore, the 14 nm half-pitch patterns, generally, lead to sub-10 nm feature size. The patterning and the etch transfer process is the same for MoS_2 as the SOI. Therefore, from the t-SPL technology point of view, the MoS_2 lines could also be done at the same dimensions.

As explained in the current report, the restriction on the use of more mechanically robust patterning stacks – that would allow sub-10 nm resolution patterning- comes from the difficulties of removing the stack after the pattern transfer. To address this issue, we decided to allow the patterning stack to remain on top of the material. This, however, limits the access to the material after the pattern transfer and, therefore, the electrical contacts are deposited prior to the deposition of the patterning stack. While MoS_2 ribbons as narrow

as 18 nm are demonstrated in the current report, to improve the resolution, the thickness of the patterning stack must become thinner. However, in the current state, the thickness of the film is limited due to the significant topography from the pre-deposited electrodes, with the minimum thickness required to ensure that the thin film would not have openings at the interface between the contacts and the MoS_2.

In the absence of such lower limit on the film thickness, one could use the same pattern transfer stack as the SOI substrates, and; since the stack decouples the writing process from the underlying substrate, the sub-10 nm feature sizes could be reliably patterned in MoS_2.

Therefore, the limitation on the realization of sub-10 nm MoS_2 transistors is not due to the lack of feasibility of printing sub-10 nm features using t-SPL technique. Further miniaturization of the achieved feature sizes on MoS_2, requires developing a process that allows reduction of the thickness of the patterning stack while ensuring its effective removal for further nanofabrication processing (e.g depositing electrical contacts).

In conclusion, t-SPL technique offers the combination of a reliable sub 5 nm overlay accuracy and the potential to fabricate sub 10 nm features without proximity correction in a controlled and reproducible manner which opens possibilities for sub-10 nm MoS_2 device fabrication.

<u>FE-SPL technique for realization of sub-10 nm MoS_2 devices:</u>

In the following, the feasibility of realizing sub-10 nm MoS_2 transistors using FE-SPL technique is discussed from two aspects. The first aspect would be regarding the intrinsic limitations of the technique in patterning sub-10 nm features on MoS_2 layers. In this case, the MoS_2 layers are prepared in a way that would be most suitable for the requirements of the FE-SPL technique which means that the MoS_2 layer is deposited on top of a conductive substrate. However, the presence of a conductive substrate makes it impossible to use the MoS_2 for electronic or optoelectronic applications. This brings about the second aspect of this discussion which covers the challenges of optimizing a process that would allow high-resolution patterning of MoS_2 on top of an insulating substrate which would allow integration with field-effect transistors.

Since the FE-SPL technique induces electrical charges in MoS_2, the presence of an efficient ground path is necessary for using this technique. Aiming to assess the intrinsic potential of FE-SPL technique in patterning MoS_2 atomic layers, we deposited the material on top of conductive (Si ++) substrate, therefore; the patterning resolution is not limited by charging and occurrence of “spikes”. The results show that, under ideal conditions, sub-20 nm wide lines with depths of 1.5 nm could be obtained with direct writing. 15 nm wide MoS_2 nanoribbons with heights of 1.0 nm was left standing after water rinse.

The LER value for FE-SPL is 2.1 nm (3 Sigma), which is in the same range as the t-SPL results. Thus, the LER issue is a limiting factor for both FE-SPL and t-SPL methods. The LER is an indicator of how close two sidewalls could be patterned without breaks or bridges.

	Considering that in the case of FE-SPL and t-SPL the locations where MoS_2 is removed and the nanoribbon is then formed by the distance between the sidewalls, the width of the ribbon is limited by the LER. A ~2-3×LER is a good approximation for the feature size that could be achieved. Furthermore, the LER could slightly increase with reducing the patterning half-pitch, which means that the feasibility of patterning sub-10 nm MoS_2 ribbons in the case of FE-SPL and t-SPL is limited by the LER rather than the capability of the technique in printing smaller features. From an application point of view, patterning of MoS_2 transistors has to be done on top of an insulating substrate which makes it challenging to achieve the sub-20 nm resolution mentioned above. We explained earlier that the issue of discharging the MoS_2 channel is addressed by using a conductive resist layer. However, the presence of this resist layer reduces the resolution because the patterned MoOx lines (where the MoS_2 is converted to MoOx due to the FE-SPL exposure) are wider than the lines formed in the resist. Therefore, to assure part of the underlying MoS_2 remains unexposed to form the ribbon, the half-pitch has to be higher. Due to the presence of cross-linked resist that could not be removed during wet development, the reliable determination of the ribbon size is not possible. FE-SPL studies on conductive resist, coated on top of pristine Si or SOI samples revealed similar resolution capabilities as for other FE-SPL resists, i.e. sub 10nm half pitch can be achieved. Furthermore, a comparable stack of layer, as used for t-SPL, can be applied for the FE-SPL patterning. Here, only the top layer resist has to be replaced with a conductive type. This would be comparable to the patterning of Si on SOI samples, where minimal line widths of approx. 5 nm and distance between lines of 20 nm after etching could be demonstrated. In conclusion, the feasibility of patterning sub-20 nm MoS_2 features using FE-SPL technique is demonstrated and further reduction of the feature size is possible. Optimization of the resist and development process is required to achieve this resolution in the MoS_2 transistors.
Explanation of Differences between Estimation and Realisation	D9.5 has been partially achieved. Two SNM techniques (t-SPL and FE-SPL) have been used to pattern MoS_2. The current critical dimension size is 18 nm using t-SPL technique. While various SPL techniques are generally more optimized for the commercial 3D semiconducting devices, further optimization of these patterning technique allows their full adoption for the case of 2D materials and is expected to result in reduction of the nanoribbon width. Due to the absence of dangling bonds in pristine 2D semiconductors, resist coating and stripping faces additional complications compared to the case of 3D semiconductors. The issue of resist coating and stripping is the main challenge for t-SPL technique and further optimizations would be in this direction. On the other hand, FE-SPL requires further design optimization to provide the electrical path

	for discharging of the field-emission induced charges. A new type of conductive resist has been developed that could allow sufficient discharge of the 2D semiconductor channel. For the case of FE-SPL technique, further optimizations should focus on improving the lithography resolution on the conductive resist layer, identifying the potential effects of the overlaying conductive resist on the electrical performance and alternative designs for discharge path.
Metrology comments	Within the deliverable 9.5 atomic force microscopy (AFM) was used which was calibrated using standard methods.