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List of participants:

Participant no.	Participant organisation name	Part. short name	Activity Type	Country
1 (Co)	Technische Universität Ilmenau	**TUIL**	HER	Germany
2	IBM Research GmbH	**IBM**	IND; End-user	Switzerland
3	École polytechnique fédérale de Lausanne	**EPFL**	HER	Switzerland

SNM Work Package 9 Deliverable: D9.6 (“Electrical characteristics of patterned MoS2 and other related 2D semiconductor”)					
Lead beneficiary number	9	**Nature**	R	**Dissemination level**	CO
Estimated Person-months	14				
Person-months by partner for the Deliverable	EPFL: 7; IBM: 4; TUIL: 3				
Estimated Delivery Date	M48: 31/12/2016	**Delivery Date**	13/03/2017		
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Criteria and Achieved Results	**Criteria**	**Achieved result**			
	Realization of various structures based on 2D materials to be incorporated into electronic devices	Structures such as quantum point contacts, ribbons and ribbon arrays along different crystallographic directions have been produced using various SPL techniques			
	Electrical characterization of MoS_2 FETS patterned using t-SPL technique	t-SPL have been applied to patterning MoS_2, the electrical characterization of the devices show typical n-type behaviour for MoS_2-FETs			

Person-months by partner:

EPFL	IBM	TUIL					
7	4	3					

	Electrical characterization of MoS_2 FETS patterned using FE-SPL technique	FE-SPL have been applied to patterning MoS_2. Electrical characterization of the device using polymer electrolyte gates show ambipolar charge transport mechanism in MoS_2-FETs
	Electrical characterization of other 2D materials	The knowledge on 2D materials, in particular studying the growth of high-quality MoS_2, $MoSe_2$ and WSe_2 by chemical vapor deposition (CVD) has been significantly expanded. Furthermore, transport properties of monolayers of WS_2 and ReS_2 has been studied. Efforts towards patterning of 2D materials has been mainly focused on MoS_2 patterning since it is the most suitable material to work with in terms of stability, contact resistances and large area integration. Patterning of MoS_2 was a priority and several technical challenges were resolved within SNM project making it possible to achieve low device dimensions. Knowledge achieved on patterning of MoS_2 is useful and will be applied in future to other 2D materials.
	Device characterization at low temperatures	The fabricated devices up to this point could not be used for temperature-dependent studies of quantum phenomena on nanoscale due to high impedance. We foresee that samples with higher quality transport would be suitable for temperature-dependent measurements in future.

Description of the Deliverable	This deliverable is related to the electrical characterization of the fabricated ultra-narrow nanoribbons of two-dimensional material MoS_2 using lithographic techniques developed by the SNM consortium. Two patterning techniques have been pursued, reported in D9.5: a) Thermal scanning probe lithography (t-SPL) in collaboration with A. Knoll. and b) Field-emission scanning probe lithography (FE-SPL) in collaboration with I.W. Rangelow. Following SPL patterning the devices were characterized at EPFL. For both t-SPL and FE-SPL samples, the devices were annealed in high-vacuum at temperatures up to 70^{o}C for 24 hours to remove the contaminations from fabrication process. Electrical characterization of the devices was carried out using an Agilent E5270B parameter analyzer while the samples were kept in high vacuum. a) **Thermal scanning probe lithography.** In collaboration with Armin Knoll, thermal scanning probe lithography is implemented on field effect transistors (FETs) with MoS_2 channels, reported in D9.5. Following t-SPL patterning, the samples are shipped to EPFL for electrical characterization, where the chips are bonded onto chip carriers and loaded in to a setup which allows vacuum-annealing and in-situ electrical measurements. In order to measure the transfer characteristics of the device the substrate has been used as a back-gate. In this configuration, the SiO_2 underneath the channel acts as the gate dielectric and the voltage is applied via the degenerately doped (Si++) substrate. Figure 1.a shows the AFM topography image of a representative device. The single-crystal triangle of monolayer MoS_2 is electrically contacted with Ti/Au electrodes. An array of ribbons was patterned along the width of the channel using t-SPL technique, with the width of patterned ribbons $\sim$ 18 nm. Figure 1.b shows the transfer characteristic of the device from Figure 1.a. The MoS_2 FET shows a typical n-type transport with the threshold voltage $\sim$ 12 V. The bias voltage was kept at 1V while the back gate voltage was swept from -70 V to 70 V. Interestingly, the hysteresis in the gate voltage sweeps is negligible which could be a sign of the absence of slow traps which would charge and discharge during the sweep. ON/OFF current ration of $\sim 10^{-3}$ is extracted from this measurements, indicating that MoS_2 patterned into ribbons as narrow as $\sim$ 18 nm preserves it's semiconducting nature. Figure 1.c shows the gate leakage current versus back-gate voltage for the same device. The gate leakage increases with increasing the gate voltage reaching the maximum value of $\sim$ 120 pA at the gate voltage of 70 V which is in the same order of magnitude as conventional MoS_2 FETs. The output characteristics of the same MoS_2 FET is shown in Figure 1.d, where the bias voltage is swept from -1 V to 1V at the back-gate voltage of 70V. This figure shows that the metal-semiconductor-metal junction behave Ohmic up to the drain-source voltage V_{ds} of $\sim$ 0.4 V. For V_{ds} above this value, the Schottky nature of the metallic contacts to MoS_2 is observed. The Schottky junctions occur as a result of Fermi level pinning and pose barriers towards the injection of charge carriers. As shown on Figure 1.d, the Schottky barriers behave symmetrically under reverse bias voltage polarities.

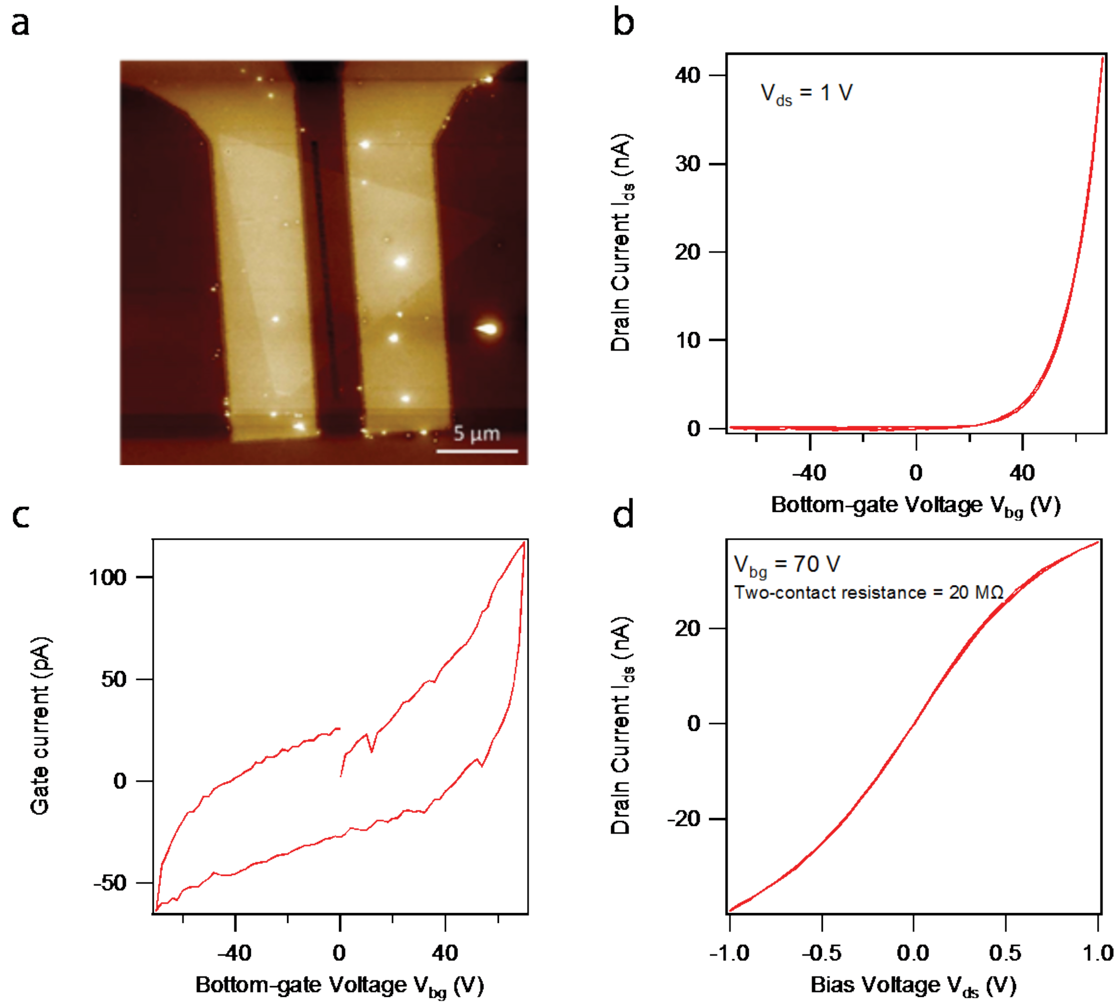

Figure 1. (a) AFM topography image of single-crystal monolayer MoS_2, electrically contacted with metallic electrodes. An array of ribbons with width of ~ 18 nm is patterned along the width of MoS_2 channel. (b) Transfer characteristics of MoS_2 FET, using the SiO_2 substrate as the back gate dielectric. The MoS_2 FET shows a typical n-type behavior with the threshold voltage ~ 12 V. (c) The gate leakage current as a function of back-gate voltage. (d) The output characteristics of the MoS_2 FET with the back gate voltage at 70 V.

b) **Field-Emission scanning probe lithography (FE-SPL)**. FE -SPL in collaboration with I. Rangelow at TU Ilmenau, has been used to pattern the channel area of FETs based on MoS_2, as reported in D9.5.

Following t-SPL patterning, the samples are shipped to EPFL for electrical characterization, where the chips are bonded onto chip carriers and loaded in to a setup which allows vacuum-annealing and in-situ electrical measurements.

In order to achieve higher gating efficiency, polymer electrolytes have been used as gate dielectric. The use of polymer electrolyte gates result in enhanced electrostatic control, therefore, the charge carrier densities could be modulated to very high values. Access to such high levels of doping allows control over the location of Fermi level in a wide range of energies covering energies higher than the conduction band edge and lower than the valence band edge. As a result, both electron- and the hole-doped regimes could be observed, known as ambipolar charge transport.

MoS_2 in the channel area is patterned using FE-SPL technique to form array of ribbons which go from one metal electrode to the other, along the entire length of the channel (Figure 2. a and c). AFM topography image of the ribbons patterned along the armchair direction of the MoS_2 lattice is shown on Figure 2.a, while the ribbons patterned along the zigzag direction are shown in Figure 2.c. We have characterized the transfer characteristics of both devices by sweeping the voltage applied to the gate electrodes with the polymer electrolyte acting as a liquid dielectric layer. The results are presented in Figures 2.b and 2.d for ribbons along the armchair direction and the zigzag direction, respectively. Ambipolar charge transport is observed in both cases with n-type behavior for the positive gate values and p-type behavior for negative gate values. The transfer characteristics of such ambipolar devices could be divided between different charge transport regimes. The hole transport regime (p-side) and the electron transport regime (n-side) appearing in both Figure 2.b and Figure 2.d. Furthermore, a regime at high charge carrier density where the current saturates is appearing in Figure 2.b which corresponds to the high n-doping and high p-doping on the corresponding side.

The difference between the threshold voltage (ΔV_{th}) on the n-side and the p-side corresponds to the electrostatic doping required to move the Fermi level from the conduction band to the valence band and should provide a rough estimation of the electronic bandgap of MoS_2. The ΔV_{th} is 1.72 V and 1.75 V for the armchair ribbons and the zigzag ribbons respectively, which is in agreement with the 1.8 eV of electronic bandgap in pristine monolayer MoS_2. One advantage of ambipolar charge transport is that the Fermi level could be located in the valence band of monolayer MoS_2 where the spin/valley coupling is strong and leads to new and interesting physics.

ON/OFF current ratio of $\sim 10^{-3}$ is extracted from transfer characteristics for both devices. Furthermore, the study of gate leakage current shows maximum gate leakage current of 40 pA and 75 pA for ribbons along the armchair direction and the zigzag direction, respectively.

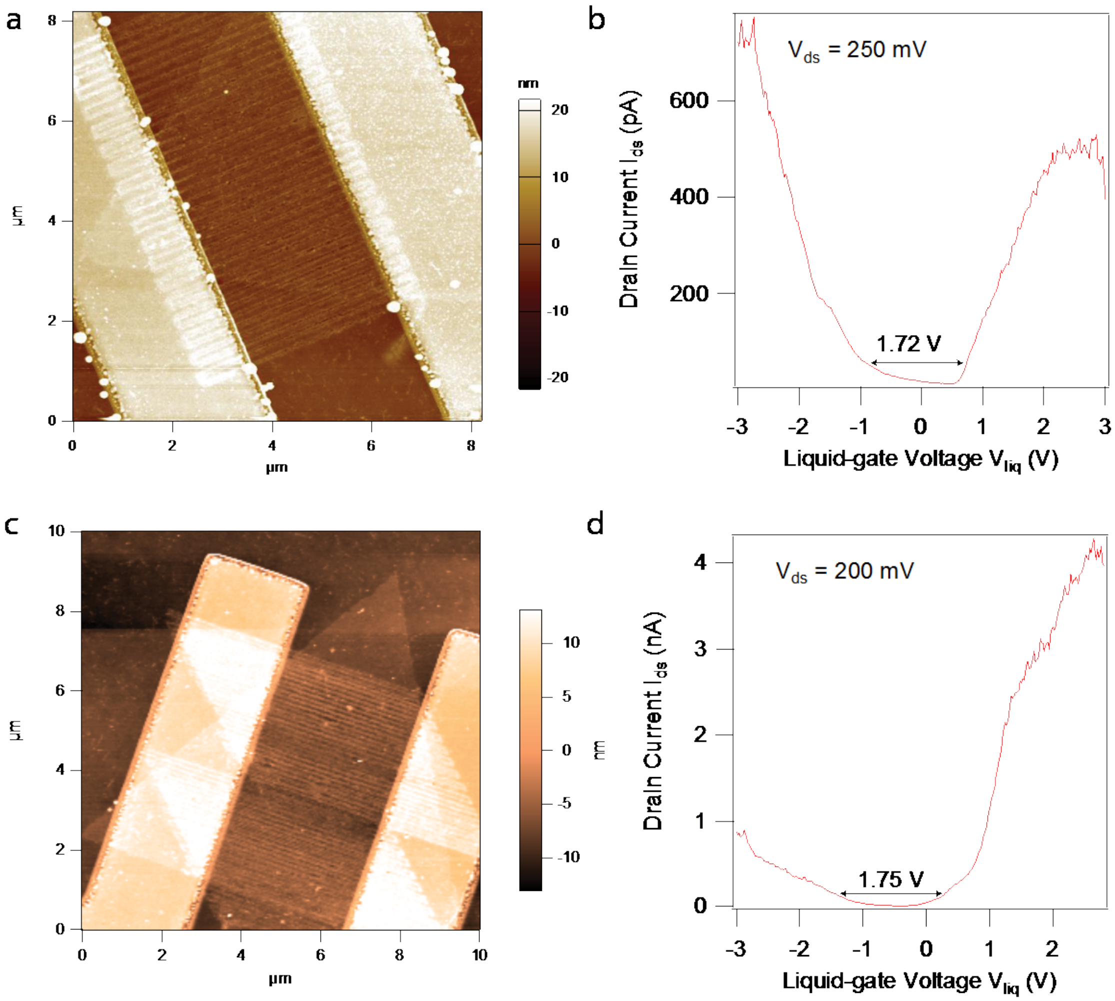

Figure 2. (a) AFM topography image of MoS_2 FET, where ribbons have been patterned along the armchair direction of lattice and expand over the entire length of the channel. The ribbon width is expected to be ~ 120 nm. (b) Transfer characteristics of the device from (a) using polymer electrolyte as the gate dielectric. Ambipolar charge transport is observed for the liquid-gate voltage sweeping from -3 V to 3V at the drain-source voltage V_{ds} of 250 mV. The difference between the threshold voltages on the n-doped side and p-doped side is 1.72 V. (c) AFM topography image of MoS_2 FET, where ribbons have been patterned along the zigzag direction of lattice and expand over the entire length of the channel. The ribbon width is expected to be ~ 40 nm. (d) Polymer electrolyte gating of the MoS_2 FET from (c) showing ambipolar charge transport with n-type behavior for the positive gate voltages and p-type behavior for negative gate voltages. The threshold voltages are 1.75 V apart between the n-doped side and p-doped side.

Conclusion:

Electrical characterization of devices based on patterned MoS_2 was carried out. Atomically thin layers of MoS_2, as a representative of the 2D materials, were patterned using two different scanning probe lithography techniques. These techniques include thermal scanning

	probe lithography (t-SPL) and field-emission scanning probe lithography (FE-SPL). The patterned devices show behavior that is expected from MoS_2 FETs. Typical n-type transport has been observed in back-gated MoS_2, patterned using t-SPL. In the case of FE-SPL patterned devices, ambipolar charge transport has been achieved using polymer electrolyte gates. This study demonstrated one of the first successful fabrication of FETs based on MoS_2 nanoribbons with width lower than 20 nm. Such devices are expected to provide a platform for study of quasi-one-dimensional quantum confinement in MoS_2 as well as giving insight into the influence of edges on the transport properties of this material. The devices studied in this work serve as a proof of concept for such devices, confirming that ultra-narrow MoS_2 devices preserve the semiconducting nature of 2D MoS_2 layers. This work opens the way for a systematic study of edge effects on MoS_2 transport properties, allowing the fabrication of highly scaled, high-performance MoS_2 field effect transistors using novel lithography techniques.
Explanation of Differences between Estimation and Realization	D9.6 was partially achieved. We significantly expanded the knowledge on 2D materials, in particular studying the growth of high-quality MoS_2, $MoSe_2$ and WSe_2 by chemical vapor deposition (CVD). Furthermore, we studied transport properties of monolayers of WS_2 and ReS_2. These materials are promising for future extended studies of lithography techniques and miniaturized devices. Within the framework of this project monolayer MoS_2 grown by CVD was used as prototypical material for exploring possibilities of patterning *via* different lithography techniques developed within SNM project. It is indeed possible to pattern ribbons as small as 18 nm and to modulate conductivity by external gate as it is typically done in field-effect transistors. However, further detailed optimization is required for operation of these devices at high frequencies. Typically low resistance devices and high current densities are required for high frequency operation, while in our case only resistances in the MΩ range were achieved. The possible sources of high resistance include contamination due to lithography process and edge roughness. Furthermore, these devices up to now could not be used for temperature-dependent studies of quantum phenomena on nanoscale due to high impedance. We foresee that samples with higher quality transport (one signature of high quality transport could be field-effect mobility measured at room temperature) would

	be suitable for temperature-dependent measurements in future. Knowledge, achieved on patterning of MoS_2 within the framework is useful and will be applied in future to other 2D materials. We focused mainly on MoS_2 patterning since it is the easiest material to work with in terms of stability, contact resistances and large area integration. We believe that patterning of MoS_2 was a priority and several technical challenges were resolved within SNM project making it possible to achieve low device dimensions. However, further work is required for optimization of fabricated devices. Regarding patterning itself, the dimensions below 10 nm were not achieved with 18 nm being demonstrated. 2D materials differ significantly from other materials also in terms of surface chemistry. Normally, 3D materials have surface dangling bonds, which make adhesion and chemical treatment easier, while 2D materials do not have them. This fact requires additional efforts to adapt lithography techniques, including resist spin coating, for applications in 2D materials field.
Metrology comments	Within the framework of D9.6 various techniques were used, in particular atomic force microscopy (AFM) for measurements of critical dimensions. AFMs used were calibrated using standard methods. For electrical measurements, Source-Measurement Units (SMU) were used, for example Agilent E5270B with low noise level (<1fA).