Collaborative project*

Project acronym: SNM

Project full title: "**Single Nanometer Manufacturing for beyond CMOS devices**"

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(First Quarter)

Deliverable: 12.2 ("SNM two-page fact sheet for publication & EC public presentation")

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List of participants:

Participant no.	Participant organisation name	Part. short name	Activity Type	Country
1 (Co)	Technische Universität Ilmenau	**TUIL**	HER	Germany
2	EV Group E. Thallner GmbH	**EVG**	IND; End-user	Austria
3	IMEC	**IMEC**	RES	Belgium
4	Mikrosistemi Ltd	**µS**	SME; End-User	Bulgaria
5	Universität Bayreuth	**UBT**	HER	Germany
6	Technische Universiteit Delft	**TUD**	HER	Netherlands
7	Spanish National Research Council	**CSIC**	RES	Spain
8	IBM Research GmbH	**IBM**	IND; End-user	Switzerland
9	École polytechnique fédérale de Lausanne	**EPFL**	HER	Switzerland
10	SwissLitho AG	**SL**	SME; End-User	Switzerland
11	Oxford Instruments Nanotechnology Tools Ltd	**OINT**	IND; End-user	UK
12	Imperial College London	**IMPERIAL**	HER	UK
13	The Open University	**OU**	HER	UK
14	Oxford Scientific Consultants Ltd	**OSC**	SME	UK
15	VSL Dutch Metrology Institute	**VSL**	IND	Netherlands

SNM
Work Package 12
12.2 ("SNM two-page fact sheet for publication & EC public presentation")

Man-months by partner for the first 3 month period	TUIL									
	1									

Major achievements in period of First Quarter

D12.2

Single Nanometer Manufacturing (SNM) for beyond CMOS devices

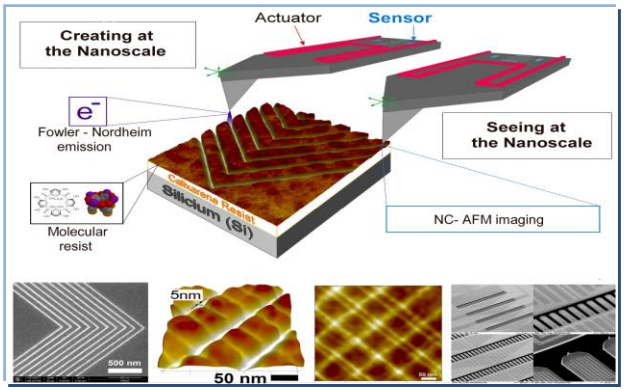
The aim* of the *Single Nanometer Manufacturing* (SNM) *project is to investigate and develop *novel Technologies for* Single Nanometer Manufacturing (SNM), reaching the theoretical limit of future nanoelectronic and nanomechnanical systems.

High performance Single Nanometer Manufacturing is an enabling technology for nanoelectronics, capable to open new horizons in the emerging world of nanotechnology. Sustainable competence and excellence in the project should secure a new path for manufacturing ultimate electronic, optical and mechanical devices never done before. A 15 member strong team from industry, academia and research institutes,

led by Prof. Ivo W. Rangelow, Head of Department of Micro- and Nanoelectronic Systems at the Ilmenau University of Technology is working together in an SNM integrated project (IP) to achieve ambitious goals:

- **Pushing the limits** of the nano-manufacturing down the single nanometer digit
- **Development** of nano-lithographic methods for nanometer-size features, overlay placement, inspection and integration in novel nanoelectronic devices
- **Enabling** of novel ultra-low power electronics, quantum devices and manipulation of individual electrons (s.c. Single Electron devices).
- **Open new horizons** for beyond CMOS technology by novel cost-effective, global, nano-lithographic technologies.

The Moore's Law has been the basis in long-term planning in the technological developments, resulting in an exponential increase in the number of transistors Si-MOSFET (Silicon Metal-Oxide-Semiconductor Field-Effect Transistor) per chip. European Project "SNM" will contribute to next generation nano-manufacturing technologies, for building future quantum electronics and *pushing this nanotechnology into many new areas*. Dimensions of electronic devices on silicon chips have been sinking steadily in size for over 40 years. From the very commencement in the 1960s, Gordon Moore prophesied that the number of transistors on a silicon chip would double every two years. This trend, the famous Moore's law, has become a forecast, driving industry requirements for each new generation of silicon chips and leading to intense increases in the speediness and performance. Existing large-scale integrated circuits use CMOS technology based on Silicon field-effect transistors (MOSFETs). Each following generation of

	CMOS circuits has seen a reduction in the dimensions of the MOSFET, and at present, the minimum dimensions of this device are only ~35nm. It is expected that the MOSFET can remain viable down to the 10nm scale. However, below this, difficulty in controlling the device current, and the strong influence of quantum mechanical effects such as electron tunneling, may require new devices. Furthermore, increasing difficulty in fabricating large numbers of highly nano-scale devices using conventional optical lithographic techniques greatly compounds the problem. This indicates that a different approach may be essential to create a 'beyond-CMOS' generation of electronic devices. Manufacturing next generation devices in nanoelectronics, nanophotonics, and nanoelectro-mechanical systems (NEMS) requires lithography at the single-nanometer level with high alignment accuracy between patterns, acceptable throughput, cost, and high reliability. To address this, SNM-team is working on technology using a combination of high-resolution scanning probe lithography (SPL) and nanoimprint lithography (NIL). SNM suppose that this arrangement is a promising candidate for high-throughput device fabrication even at the sub-5nm scale. Scanning probes are capable of confined nanoscale interactions for imaging, probing of material properties, and lithography at the single-nanometer scale or even smaller. SNM-team is investigating novel single-nanometer manufacturing technologies using advanced scanning probes to pattern molecular-glass-based resist materials (see Figure 1). Due to the small particle size (<1nm) and truly monodisperse nature (i.e., the particles are all of similar size) of molecular resists, a more uniform and smaller lithographic pixel size can be defined in comparison with conventional resists. Our lithographic process uses the same nanoprobe for atomic force microscope (AFM) imaging to allow pattern overlay alignment, direct writing of features into molecular resists using a highly confined, development-less resist removal process via emission of low-energy electrons, and AFM post-imaging for final in situ inspection. SNM-technology offers an encouraging direction toward single-nanometer lithography and can improve throughput significantly by employing parallel, self-actuated, and self-sensing probe systems. Probe-based closed-loop lithography can be used for sub-5nm fabrication of nanoimprint templates, as well as reproducible nano-scale prototyping of 'beyond CMOS' nano-electronic devices like quantum-dot and single electron devices.  **Figure 1**

Risks and issues arising	*none*
Deliverables in WP12 due for next 3 month period	*D.12.3; D.12.4*