NANOFUNCTION Project Periodic Report

Period covered: From September 2011 to August 2012

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Periodic report: **1st ☐ 2nd X 3rd ☐ 4th ☐**

Period covered: **from 2011-09-01 to 2012-08-31**

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Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate):

  ☒ has fully achieved its objectives and technical goals for the period;

  ☐ has achieved most of its objectives and technical goals for the period with relatively minor deviations;

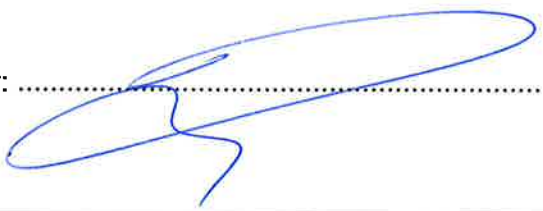
  ☐ has failed to achieve critical objectives and/or is not at all on schedule.

- The public website is up to date, if applicable.
- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 6) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 5 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: Francis Balestra

Date: 17/10/ 2012

Signature of scientific representative of the Coordinator: .....



1. Publishable summary

Introduction:

The NANOFUNCTION Network of Excellence aims to integrate at the European level the excellent European research laboratories in order to strengthen scientific and technological excellence in the field of novel nanoelectronic materials, devices and circuits for developing new integrated functions and disseminate the results in a wide scientific and industrial community. The NoE is particularly focusing on the convergence of Advanced More than Moore (MtM) for adding functionalities to ICs and Beyond-CMOS, which could be integrated on CMOS platforms. In particular, the interest of these nanodevices for the development of innovative applications with increased performance in the field of nanosensing, energy harvesting, nanocooling and RF is thoroughly investigated.
It is worth noting that novel MtM technologies will certainly have in the future strong link with Beyond CMOS technologies. The interaction between classical approaches and Beyond CMOS disruptive functions will offer significant opportunities for emerging markets. There are two main motives for using nanoscale devices in the MtM domain: i) miniaturisation remains a major enabler for price reduction, functionality multiplication, and integration with the electronics; ii) nanoscale structures can improve device's intrinsic performance or enable new functionality (such as ultra-high-sensitivity detection for chemical and biological applications). As a very good example, nanowires have received much attention from the R&D community as future components for electrical circuits based on CMOS compatible processes. These activities have been initiated to address the future need of IC technologies beyond the physical limits of CMOS, but nowadays other very interesting research activities are devoted to using NW to create innovative MtM products.
Other fields in which nanostructured materials and nanodevices could be very interesting are: i) energy autonomous systems using energy harvesting; these systems will become very important in the future for the development of "green/sustainable" applications; ii) high-performance, small size, low cost RF circuit based on new passives; optimisation of antenna architectures; iii) electronic cooling in CMOS compatible nanoscale systems by the management of the heat transfer. The integration of many different types of devices will be needed in the future, e.g. bio-sensors, NEMS devices, energy scavenging systems and RF interfaces, it is therefore very valuable to join our effort in this NoE to overcome the major challenges we are facing for the development of these future nanoelectronics systems.

This work is carried out through a network of joint processing, characterisation and modelling platforms. The consortium works closely with European industry and feeds back data and know-how on devices that deliver the required performance. This interaction will strengthen European integration in nanoelectronics, help in decision-making and ensure that Europe remains at the forefront of nanoelectronics for the next decades. A strong link has been established between modelling/simulation, processing and characterization activities within each WP/task. During the second year of Nanofunction, close links have been developed with other European Projects, in particular with the Guardian Angels FET Flagship. Indeed, 13 Nanofunction Partners have been involved in the Pilot phase of the FET Flagship Guardian Angels Project (May 2011-April 2012) and in the preparation of the next Phase (May 2012 – October 2012). The competences and most promising activities in the field of nanosensing, energy harvesting and RF have been used to give significant contributions to the future 10 years Roadmaps of the Guardian Angels (GA) Project. We have also established cooperation with the AENEAS organization and National projects in the same fields in order to enhance the overall efficiency of the European Research in Nanoelectronics.
We have studied some of the main scientific and technical challenges put forward by European nanoelectronics community in this field. The scientific results obtained in the joint Nanofunction projects, showing significant improvements over the state-of-the-art, and the integration and spreading of excellence activities organized by Nanofunction Partners, are summarized below for all the Work Packages.
All these activities will contribute to the durable integration of the partners. However, some very important specific actions have been developed for the strengthening of this durable integration: i) a

new Partner became Members of the Sinano Institute in 2012, which is a legal entity (Scientific Association) created in January 2008 for the coordination of the European Academic Community working in the field of Nanoelectronics ; ii) the Joint Processing, Joint Characterization and Modelling Platforms, which have been developed and used in the framework of the Sinano, Nanosil and Nanofunction NoEs for our joint research activities are fully integrated as open Research Infrastructures in the Sinano Institute ; iii) a lot of Nanofunction partners have been strongly involved in the ENI2 initiative (European Nanoelectronics Infrastructure for Innovation) launched by STMicroelectronics, which is now embedded in AENEAS. ENI2 proposes a long term strong European structuring with 3 levels representing all the European nanoelectronics activities in the full value chain: level 1, leaded by the Academic Community represented by the Sinano Institute – including all the Nanofunction Academic Partners- for long term research, level 2 managed by the pre-industrial European Institutes, and level 3 coordinated by the European industry including ST, Infineon, NXP, Micron, ASM, Thales, STE and IBS.

i) WP1 "Nanosensing with Si based nanowires"

Work package 1 "Nanosensing with Si based nanowires" focus on Si based nanowire FETs as sensors taking advantage of the mature and reliable CMOS process technology. A primary focus is placed on nanowires for detection of molecules in gases or liquids for gas monitoring, chemical analysis or biotechnology. Implementation of nanowires in arrays is an efficient and low cost approach to achieve fast acquisition of information. To permit silicon nanowires and arrays to reach their full potential as sensors, it will be necessary to integrate active elements, at each location of the array, to function as highly sensitive and selective sensors of molecules. Sensor arrays also provide the possibility of having different sensing elements in the array and thereby simultaneously detect various molecules. We explore the use of Si based nanowires / nanowire-FETs for improvement of sensitivity, resolution, selectivity and response time of the sensor. Special emphasis is put on the integration with CMOS technology in order to achieve low cost More Than Moore solution for a sensor with a high density (>1000/mm^2) of nanowires each working as an individual sensing elements. The work package deals with nanowire fabrication, nanowire functionalization, simulation and modeling and nanowire sensor integration with CMOS readout circuits. During the first year of Nanofunction CMOS compatible nanowire fabrication processes have been developed and pros and cons of different process schemes was evaluated with respect to a sensor array application. Silicon nanowires were fabricated to be distributed between partners for sensing experiments. During the second year nanowire functionalization techniques in liquid and vapour phase for DNA grafting was developed and evaluated. Localized functionalization of the nanowires was confirmed by fluorescence images. The fundamental detection limit of silicon nanowires as charge sensing element was evaluated using a non-equlibrium Green function quantum microscopic approach for transport. It was shown that single charge detection is possible in dry environment and that the sensitivity is reduced in liquid ionic solutions due to ionic screening effects. Furthermore a straight-forward implementation of an "electrolyte" material into the commercial TCAD simulator was demonstrated. This approach has the advantage of exploiting all the features of the TCAD tools but a disadvantage of the relatively simple treatment of the electrolyte. The approach were compared with the NEGF approach and shown to be in reasonable agreement both in dry and ionic solutions for 5x5 nm^2 Si nanowires. A silicon nanowire based sensor was designed with 1024 individual nanowire pixels together with associated read-out circuits. A process was developed to integrate the silicon nanowire pixels into a fully depleted SOI CMOS process. Furthermore a full impedance sensing circuit was designed and fabricated to measure both magnitude and phase of silicon nanowires.

ii) WP2 "Exploration of new materials, devices and technologies for Energy Harvesting"

T2.1 investigates **nano-materials and devices for harvesting energy from vibration present in the ambient**. During the second year, the activities were focused on the investigation of **silicon-integrated piezoelectric MEMS transducers based on aluminum nitride (AlN)**. Prototypes of

piezoelectric-based MEMS cantilever have been fabricated by adopting a novel fabrication protocol. Measurement results however have shown that voltage and power are in the mV and pW range, i.e. too low to be used by any dedicated AC-DC power converter circuits. For this reason, further activities in this field were dedicated to the design of vibrating MEMS structures with larger sizes and to the development of MEMS micro-generators on silicon exploiting both piezoelectric and electromagnetic effects. The piezoelectric part of the vibration energy harvester will allow achieving a larger output voltage, compensating the low output voltage achievable using the electromagnetic effect, which, on the other hand, provides the largest energy density. The FEM modelling has been used to optimize vibration energy harvesting devices on silicon (GEN-1) proposed by Tyndall, which exploits both piezoelectric and electromagnetic effects.

In Task 2.2 most efforts were devoted to **improve the thermoelectric properties of Si-based materials**, as an alternative to rare or toxic elements, and for the integration opportunities that they offer. To this end, **several materials systems are being developed and characterized**. A first approach, leading to a real demonstrator, was based on the **integration of metal/doped poly Si thermocouples on a thick porous Si layer**. This porous layer is an excellent platform for TEG integration as it combines low thermal conductivity due to nanostructuration induced phonon confinement and reduced electron transport. The second approach consists in engineering materials with better thermoelectric properties. In particular, it is expected that **materials nanostructuration allows electron conduction to be preserved while heat conduction is decreased by phonon confinement** (in ultra thin Silicon membranes, superlattices or nanowires**) or by phonon scattering** (with additional interfaces, heterojunctions, or rough surfaces). Control of growth parameters for the Si-Ge system was improved, making it possible to fabricate both heterostructured nanowires and superlattice thick stacks. The impact of phonon confinement effects on heat transport was simulated and experimentally characterized using ultra-thin Si membranes as test beds. In parallel, 3D atomistic approaches are being used to simulate phonon properties and heat flux in confined structures such as semiconductor nanowires, taking into account spatial fluctuations. Finally, a more exploratory study aims at better understanding an alternative mechanism, **the *spin* Seebeck effect**, which generates spin currents and associated voltages in the presence of a temperature gradient in a ferromagnet.

Nanowires solar cells (T2.3) are expected to outperform the planar counterpart in terms of optical absorbance. In addition, the high-aspect-ratio of nanowires permits to reduce significantly solar cell thickness while simultaneously providing effective carrier collection in the case of radial junction. The activity driven by IUNET and FMNT has been devoted to the **simulation, elaboration and characterization of nanowires based solar cells** in order to define an optimized photovoltaic structure from an optical and electrical point of view. Two types of materials have been analysed: **silicon nanowires** as the reference material with indirect band gap and **ZnO nanowires with CdTe radial heterojunction** as the direct band gap material for comparison. Simulations activities have been performed using a Fourier modal method (RCWA) tool for the **optical simulations** and a commercial TCAD tool for **electrical simulations**. Solar cells based on Si and ZnO/CdTe nanowires have been simulated and an optimized geometry from an optical point of view has been defined for each type of material. It has been shown that the nanowire structure permits to increase significantly photons absorption compared to planar structure with the same amount of material especially in the case of indirect band gap semiconductor. Electrical simulations have been shown that interfacial recombination plays an important role on the efficiency of the solar cell and special care should be given to interfacial passivation.

Finally, T2.4 aims to **integrate into demonstrators based on the 'applications orientated' specifications for energy harvesting, storage and power management circuits and devices**.

As a more general comment, the activity in task T2.4 has been instrumental to reduce the choice of materials, methodologies, approaches for the basic technologies by focusing on the best ones as demonstrated by tables 1 and 2 in this report. For **energy storage, MnO2 cathode nanowires** developed by Tyndall on electronically conducting arrays have an active surface area 113 times that of the planar footprint resulting in a significant increase in rate capability (power output). This abundant, low cost and green material also possesses more than 2 times the energy storage capacity of the standard costly and toxic cobalt oxide. IUNET continued work on a **new generation multiple independent piezoelectric source power harvester based on standard CMOS technology** and intrinsic nano-power consumption, in collaboration with a leading industrial partner. As in previous prototypes in discrete components, the architecture is scalable and can be easily increased. First

simulations demonstrate operation with a very low value of intrinsic current consumption of 300nA for handling one transducer and additional 75nA for every additional transducer. The circuit was designed in a 0.35um process and includes about 10k transistors. Circuit design and simulations are complete and the design will be sent to foundry for the next run of fabrication.
UCL work has been focused on setting up a **fully-automated and portable design methodology (model) for ULP multi-stage voltage rectifier and multiplier** to interface AC energy harvesters and provide a DC output voltage. Initial demonstration circuits were produced on UCL SOI CMOS 2μm process and tested with embedded SOI or external small size PV cells and 13.56MHz RF antenna with inductive power transfer, respectively. Optimized designs have been submitted for fabrication on a 0.25μm bulk CMOS technology, targeting low-100μW energy harvesting with μW-consuming power management circuits.

iii) WP3 "Nanocoolers"

WP3 is concerned with the development of a new technology called "Cooltronics", whereby huge performance enhancements or new regimes of operation are enabled when critical components in an electronic circuit are cooled to ultra-low temperatures (<100mK). A prime example is THz radiation sensors, particularly those involving a superconductor. A major aim of this technology is to eliminate "wet" cryogenic fluids from the cooling process, and this involves using electronic cooling (e-cooling) to cool the components from 300mK to the lowest temperatures.
A new type of electron cooler is being developed involving strained silicon (sSi) and a superconductor; we have shown that this combination enables the electrons in the sSi to be highly thermally isolated from the sSi lattice phonons, and hence much more responsive to incoming radiation. Very significant improvements in junction quality have been achieved in the second year, by passivating the silicon prior to deposition of the superconductor (Al), and this should lead to cooling to much lower temperatures. Work on our newly proposed cold electron bolometer (CEB) sensor involving Si and sSi has also progressed well, with the control Si CEB showing good sensitivity in the THz range for the first time. The sSi CEB has also been fabricated and promises to significantly outperform existing all-metal bolometers. Reduced temperatures dramatically reduce electronic noise and increase responsivity. Good thermal isolation of the sensor is therefore critical, not only through reduced electron-phonon coupling but also through minimisation of heat leakage by phonon transport. New approaches to thermal isolation are being explored, including using porous silicon (PS) platforms which are very robust compared to the thin SiN membranes currently used. Thermal conductivity (k) is a critical parameter in this regard and the first k measurements on PS down to 4K, indicate comparable values to SiN – a very encouraging result. Crystalline semiconductor membranes offer the potential for full sensor integration (eg sSi CEB) and, to this end, sSi and sGe platforms have been fabricated. The first studies of phonon dispersion relations and transport (including k measurements) in membranes down to < 50 nm thickness were carried out in the 2nd year. These suggest dramatic reductions in k are possible in the thin membranes.

iv) WP4"Exploration of new materials, devices and technologies for RF applications"

The main focus of WP4 is to explore the potential of nanowires (NWs) and other nanostructured materials in RF applications on the Si wafer. The targeted applications include the development of substrate materials for the on-chip RF shielding from the Si substrate, the on-chip integration of RF and mm-wave passive devices on the developed low-loss substrates, and the investigation of nanowires as building blocks in RF interconnects and nano-antennas. The frequency range to be explored is from dc to 220 GHz.
WP4 is divided into 4 tasks. The first one is devoted to the development of adequate substrate technologies including a local porous Si substrate on the Si wafer that can provide efficient RF shielding from the lossy Si substrate. The second task is devoted to the design, fabrication and testing of passive devices and circuits integrated on the local porous Si RF substrate. The third task is devoted to the investigation of the electromagnetic properties of single nanowires or assemblies of nanowires

and the study of nanowire interconnects and nano-antennas and the fourth task is devoted to an exploratory work on novel nanostructured nanocomposite materials for their potential application in RF.

The work performed in the different tasks in the second year of the project is as follows:

Task 4.1

1. At NCSRD/IMEL a detailed study of the dielectric properties at RF of porous Si has been carried out, using co-planar waveguides as test structures. The dielectric permittivity of porous Si was determined using two methods of broadband dielectric characterization:

- Following Conformal Mapping approach and using analytical expressions to correlate S-parameters to the dielectric properties of the substrate.
- Using full-wave 3D simulations for various values of the substrate dielectric parameters and comparing them to the measured S-parameters

The study was performed for porous Si layers of different porosity and morphology.

2. NCSRD/IMEL collaborated with UCL in order to compare two different RF substrates: Local porous Si substrates on the Si wafer and trap-rich high resistivity Si wafers. It was found that both substrates have excellent RF shielding properties that compare well with those of quartz. The advantage of porous Si is that it can be fabricated locally on a low resistivity Si wafer, so as high performance on-chip passives can be integrated on Si together with CMOS.

Task 4.2

FMNT and NCSRD/IMEL collaborated for the development of novel high performance slow-wave co-planar waveguides (s-CPWs) and filters on porous Si. A first batch of samples was fabricated and characterized. New S-CPWs were designed taking into account the available technology. For a proof-of-concept, low-pass step-impedance filters with a cut-off frequency equal to 30 GHz were first designed. In a second step, filters were designed combining the already demonstrated by FMNT/IMEL CPW technology on porous Si and S-CPWs also integrated on porous. This combination aims at (i) increasing the electrical performance of the filters, with a wide rejection bandwidth, and (ii) reducing the filters length because of the high characteristic impedance ratio between CPWs and S-CPWs attributed to the demonstrated high characteristic impedance achievable for CPWs on porous Si. First results demonstrated the superior performance of S-CPWs on porous Si compared with those on low-resistivity Si.

Task 4.3

a) At Tyndall the magnetic properties of different nanomodulated structures of a unique three dimensional configuration have been investigated. These nano modulated structures were fabricated by using different technologies/combination of technologies (electrodeposition, nanoimprint lithography). The different symmetry of these nanomodulated structures were investigated, and then co-related to their magnetic properties and later their potential high frequency applications. It has been observed that a controllable anisotropy can be obtained by unique nanomodulation in a continuous thin ferromagnetic film. A generalized model has been developed for different anisotropy symmetry. Three dimensional nanomodulated structure generates well ordered tunable magnetic dipoles and resists vortex formation. All these important features have been investigated by SQUID magnetometry, MFM imaging and OOMMF micromagnetic simulation.

b) Tyndall and IMEL collaborated for the investigation of the magnetic properties of nano particles embedded in porous silicon with vertical pores. The samples were prepared by IMEL and magnetic properties were thoroughly investigated by SQUID magnetometry in Tyndall.

Task 4.4

A) Al single wire lines. Single Al wire lines in microstrip and CPW configuration were developed at FMNT. A characterisation method was developed for each type of lines, together with corresponding modelling. After characterisation up to 100 GHz, line parameters were extracted. Good agreement between model and measurements was found.

B) Cu single and multiple nanowire. FMNT and NCSRD/IMEL collaborated in designing and fabricating single and multiple copper nanolines on oxidized Si. The first characterisation up to 40 GHz gives interesting results. Nanoline modelling is in progress.

C) Nano antennas. In FMNT nano antennas were studied by simulation.

Some antennas are under design and will be realised.

v) WP5 "Integration and Spreading of Excellence"

Integration activities in Nanofunction are measured through the number of joint processing, characterization and modeling activities organized within each WP/Task as well as cross Task/WP activities. 27 joint activities were launched during this second year. Furthermore, the number of Task/WP as well as cross Task/WP meetings is chosen as an indicator of integration:15 "technical" meetings were organized during this second period, including 3 cross-Task/WP meetings. "Who is Who Guide" was placed on the Nanofunction web-site to inform partners about specific competences available within Nanofunction community, search by "competence" is available. Exchanges of personnel further strengthened the expertise exchange and complementarity between partners. Four calls for exchanges were issued during this second year. 39 weeks of exchanges were selected by Nanofunction Executive and Scientific Committee (E&SC).
Additionally to the integration within Nanofunction, the cooperation with other EU and national projects was stimulated. Screening of the national projects of relevance performed by Nanofunction partners revealed 8 national projects in the fields related to Nanofunction. 8 new projects (both EU and national) launched by Nanofunction members this year demonstrate the high activity level of the network.
Spreading of excellence within and beyond Nanofunction is carried out through the support and organization of workshops/schools/trainings, which are available for a wide scientific community. 15 events were organized by Nanofunction partners during this first year, of which 6 were supported by Nanofunction.
Links with New Member States and Eastern Europe were initiated with the support for the participation of 2 researchers from Poland to the Nanofunction workshop in Helsinki, the International Workshop on Functional Nanomaterials and Devices, which will be held in April 8th-11th, 2013, in Kiev, Ukraine and with the support of an exchange between St Petersburg State Polytechnical University and a Nanofunction partner.
The Virtual Centre of Excellence was strengthened by the integration of a new partner in the More than Moore/Beyond CMOS domains in the Sinano Institute since January 2012. And the Sinano Institute is also strongly involved in the ENI2 initiative (European Nanoelectronics Infrastructure for Innovation) which is now embedded in AENEAS.
Dissemination of knowledge was additionally implemented through the Nanofunction website, issued poster, presentations given by Nanofunction partners at different international scientific events as well publications in high-level international journals:
- 13 publications among which 5 of them are joint.
- 45 conference/workshop presentations, among which 9 were invited presentations and 18 are joint.

Nanofunction web site:
http://www.nanofunction.eu/

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