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Version 0.3

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Notices:

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Change Log

Version	Description of Change
V0.1	Initial Draft of the D6.7
V0.2	Second draft after internal review
V0.3	Third draft including all technical contributions

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1 Introduction

This document summarizes the overall progress of PROXIMA for the second reporting period of the project (corresponding to technical milestone MS3), achieved in the last 18 months of work. This document adopts the structure of the Periodic Progress Report (PPR) provided by the European Commission, following the guidelines described in the Guidance Notes on Project Reporting FP7 Collaborative Projects available on the participants' portal at:
http://ec.europa.eu/research/participants/data/ref/fp7/89692/project-reporting_en.pdf

This document is not the final PPR, which contractually is due 60 days after the end of reporting period. This document has been prepared before the end of month 36. It therefore includes non-final financial data, based on best estimates. However, the reported numbers are as close to reality as possible and form a useful basis to determine the project status, understand and explain any deviation and anticipate corrective action. The final numbers at M36 will be presented in the last project review of the project, to be held in November 2016.

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PROJECT PERIODIC REPORT

Grant Agreement number: 611085

Project acronym: PROXIMA

Project title: "Probabilistic real-time control of mixed-criticality multicore and manycore systems"

Funding Scheme: IP

Date of latest version of Annex I against which the assessment will be made: 2016-07-01

Periodic report: **1st** ☐ **2nd** X **3rd** ☐ **4th** ☐

Period covered: **from** **01 April 2015 (M18) to 30 September 2016 (M36)**

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[1] Usually the contact person of the coordinator as specified in Art. 8.1. of the Grant Agreement.

[2] The home page of the website should contain the generic European flag and the FP7 logo which are available in electronic format at the Europa website (logo of the European flag: http://europa.eu/abc/symbols/emblem/index_en.htm logo of the 7thFP: http://ec.europa.eu/research/fp7/index_en.cfm?pg=logos). The area of activity of the project should also be mentioned.

2 Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate) [3]:

  ☐ has fully achieved its objectives and technical goals for the period;

  ☐ has achieved most of its objectives and technical goals for the period with relatively minor deviations;

  ☐ has failed to achieve critical objectives and/or is not at all on schedule.

- The public website, if applicable

  X is up to date

  ☐ is not up to date

- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 5) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 3.3 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

[3] If either of these boxes below is ticked, the report should reflect these and any remedial actions taken.

Name of scientific representative of the Coordinator: Francisco Javier Cazorla

Date: 30/09/2016

For most of the projects, the signature of this declaration could be done directly via the IT reporting tool through an adapted IT mechanism and in that case, no signed paper form needs to be sent

3 Publishable summary

EU industries developing Critical Real-Time Embedded Systems (CRTES) face relentless demands for increased processor performance to enable the deployment of novel, advanced functionality. This demand reflects the ever-rising proportion of system value delivered in software. At the same time, commercial and economic pressures drive the need for reduced development, verification, certification, and production costs, in order to remain competitive on a world stage.

EU industries developing CRTES (whether safety-, mission- or business-critical) are facing a once-in-a-life-time disruptive challenge caused by the transition to multicore processors and the advent of manycores. This challenge brings about the opportunity to integrate multiple applications onto the same hardware platform, with significant advantages in performance, production costs, and reliability. It also poses a severe challenges in relation to a key problem of CRTES; the need to provide evidence that all software timing (temporal) constraints of consequence are sufficiently satisfied during operation. Current CRTES, based on relatively simple single-core processors, are already extremely difficult to analyse for temporal behaviour. The advent of multicore and manycore platforms exacerbates this problem, rendering traditional timing analysis techniques ineffectual.

PROXIMA has striven to demonstrate that the timing behaviour of mixed-criticality CRTES executing on multicore and manycore platforms can be analysed effectively by combining probabilistic/statistical analysis and defining new hardware and software architectural paradigms that either make resources respond in a jitterless manner or introduce randomization in the timing behavior of those resources. PROXIMA extends this design approaches across the hardware and software stack ensuring that the risks of pathological cases in the time domain are reduced to probabilistically quantifiable and acceptable levels. On top of this, PROXIMA builds a comprehensive suite of probabilistic analysis methods integrated into commercial design, development, and verification tools, complemented by appropriate arguments for certification. PROXIMA provides a complete infrastructure: harnessing the full potential of new processor resources, demonstrating and supporting effective temporal analysis, bringing the probabilistic approach to a state of technological readiness, and priming multiple EU industry sectors in its use via a number of case studies.

PROXIMA aims to respond to two complementary challenges:

C1. to pursue the industrialization of the method and tools that enable the use of high-guarantee probabilistic timing analysis in development; not only for PTA-conformant processor architectures, but also for COTS hardware;

C2. To break new research ground in facing, with probabilistic/statistical techniques, the challenges posed in analysing the timing behaviour of complex applications of mixed-criticality levels.

PROXIMA considers COTS technology at both FPGA and RTOS level to address the disruption caused to the tightness and robustness of PTA bounds by non-PTA-conformant components. PROXIMA also investigates how the principles of PTA extend to manycore systems and propose the PTA-conformant design of new manycore processors.

PROXIMA sets forth the following objectives:

O1. To develop new probabilistic analysis techniques. Invention of new probabilistic analysis techniques capable of providing efficient (tractable) and effective (tight) probabilistic

guarantees on the timing behaviour of complex, industrial-sized, mixed-criticality, real-time systems.

O2. To develop probabilistically analysable SW architectures. Implementing SW architectural components, both in terms of system software (operating system, virtualisation, and communication layers) and compiler facilities that support end-to-end PTA-conformant timing behaviour for mixed-criticality applications running on multicore and manycore HW platforms. Specific software solutions will also be developed to achieve the maximum possible degree of PTA-conformance on COTS HW.

O3. To develop probabilistically analysable multicore and manycore processor HW architectures. Delivering hardware designs for multicore and manycore processors that can provide probabilistically analysable time isolation and time composability for applications operating at different criticality levels.

O4. To reduce costs associated with verifying timing behaviour of mixed-criticality applications. Developing SW and HW components that provide for timing composability by bounding the effect that applications at the same criticality level can have on one another via provable probabilistic bounds, obtained from abstractions of the hardware platform and simple interfaces describing each application.

O5. To produce an industry-ready tool-chain for software production and probabilistic analysis of mixed-criticality applications running on multicore and manycore processors. Providing high-TRL support tools for probabilistic timing analysis, accompanied by solid scientific and methodological evidence that can be successfully used in certification arguments. These will be supplemented by run-time monitoring and verification tools, including those built into the virtualisation and operating system layers that are needed to verify correct timing and scheduling behaviour with respect to applications of different criticality levels.

O6. To produce arguments for domain-specific standardisation and certification processes. Deliver evidence and arguments that can be used in the certification and safety processes of each industrial domain.

O7. To validate the industrial viability of the PROXIMA approach by representative case studies. Collect and deliver evidence from industrial-scale case studies. A case study will be provided to cover the project-related needs in each domain (aerospace, space, railway and automotive). The specification of each case study will be devised to produce verification evidence in support of arguments of conformance with respect to the appropriate standard.

3.1 Expected final results and potential impact and use

PROXIMA challenges the state of the art in the timing analysis of high-integrity software systems, which dreams of retaining much of the analysis methods applied to simple single-core systems. PROXIMA proposes an entirely new method for measurement-based timing analysis of complex software running on complex multicore processors that use high-performance features such as caches or multi-core hardware, which is an unprecedented result in this domain. In this conservative and cautious industry, which is suffering a radical shift in systems architecture, from single-core to multi-core, the impact of PROXIMA helps users find a viable course in their transition.

The short-term impact of the project is a host of 22 exploitable technologies, which together form a framework for software performance and timing analysis of high integrity embedded systems. Some components are already available on the market, whereas exploitation plans exist for many others. The individual technologies range from the design of on-chip processor components, operating system architectures, through to high-level timing analysis tools for single and multi-core platforms and tool qualification/certification IP.

The markets addressed by the project include aerospace, space, rail and automotive. With industrial partners in each such market, PROXIMA had good guidance and feedback on how to tune and adapt the project technologies to fit the needs of each sector. The resulting framework of interoperable solution components allows users to select the items that best fit their use scenario.

PROXIMA has made good progress in bringing the various technologies to the market; there are already opportunities for technology companies including Rapita, Sysgo, Cobham, and Ikerlan to develop new products and services based on the project outcomes and to expand their market. PROXIMA has given all those partners additional technology that increase the value of their portfolio and their standing in the market. The academic/research institutions are continuing to benefit from being at the forefront of technology research and new opportunities for industrial relationships with major technology companies.

The successful acquisition of Rapita (formerly a SME, and now part of a larger organization) is due, in part, to the success of this and other research projects by enhancing its reputation and ability to recruit the best staff.

Fourteen (14) “success stories” have been reported in the project, where consortium members have formed successful partnerships, business relationships, or created opportunities for further research and funding. These include partnerships to exploit technology items and opportunities for industrial and research cooperation. Consortium members plan to continue their effort, working with industrial partners and customers to supporting the success of the European software industries. Several commercial and research activities are on-going, working with early adopters to bring PROXIMA technologies into industrial use. Some exploitable technologies are already being used or adapted in industry. The RapiTime tool qualification and a variant of the multi-core tracing technology are both in use in avionics. Plans for the micro-benchmark technology (and the related pTC-VICI) and FBI-VICI are in place to support the automotive and avionics industries, the hardware randomization technology continues to be explored in the Space industry.

The mid-term impact of the project is primarily supporting the adoption of multi-cores. The large companies in the consortium including Airbus, Airbus Defence and Space, Infineon, Ikerlan, as well as the members of the Industrial Advisory Board, will receive benefit in the medium-term as they begin to unleash the potential of novel multi-core hardware platforms on new projects.

Gains will be reaped through the cost-effective use of multi-core hardware in critical systems. Probabilistic timing analysis is expected to develop and become common practice – the key technologies (MBPTA, FBI and pTC) are currently the most viable methods of performing software timing analysis on advanced multi-core hardware. Rapita, for example, will support probabilistic timing analysis in its commercial analysis tools, based on the PROXIMA work, for selected customers, working with BSC, INRIA and UoY for technical support.

In the long-term, the PROXIMA project is expected to have benefits for the European real-time industry as a whole. The long-term aspiration of PROXIMA is for key elements of the technology to be in mainstream use in commercial products in at least three out of the four key industries covered in the project, avionics, space, railway, and automotive by 2023. In particular, enabling efficient and lighter weight computer technology for space and aerospace remains an important driver for users of PROXIMA.

Overall, these results and plans will enable EU industry to reinforce its technological and market leadership with the ability to develop cost-effective, high-performance critical real-time systems.

3.2 Work performed to date

The results achieved at the end of reporting Period 1 (MS2) at M18, were as follows: a) release of a first version of the PROXIMA execution stack for the FPGA; b) the release of a partial version of the tool chain for the AURIX; and c) the release of a preliminary version of the manycore platform. Initial software-only solutions were developed to help achieving PTA conformance. The RTOS and run-time libraries also include support for data tracing that feeds the PROXIMA timing analysis tools. Experiments for timing characterization of the FPGA and the AURIX platforms with application kernels were carried out to consolidate the respective toolchains. The domain specific mixed-criticality applications on avionics, space and railway have been ported to the PROXIMA environment and these are ready for the following case-study experimentation phase.

The results that the project achieved at the end of reporting Period 3 (corresponding to technical milestone MS3) at M36, on a per-platform basis are as follows:

a) release and use of the final, stable version of the PROXIMA execution stack for the FPGA in both variants, HW-Rand and COTS with SW-Rand;
b) release and use of the final, stable version of the tool chain for the AURIX processor;
c) release and use of an initial version of the tool chain for the P4080 processor;
d) release and use of the final version of the manycore processor simulator, ready for integration with its dedicated software execution stack (RTOS and trace logger) and tool chain.

The evaluation conducted by WP4 on the case studies allowed determining:

1) the coverage of the success criteria;
2) the user-friendliness, the level of automation, and the presence of restrictions and constraints in the use of the PROXIMA technology solutions for all three multicore platform baselines;
3) the real-time performance of all processor platforms and associated execution stacks, in terms of guaranteed and achieved timing behavior.

In terms of the individual elements of the PROXIMA toolchain, we note the following:

a) Hardware solutions were consolidated for the FPGA HW-Rand platform to handle multicore contention jitter in such a way that no change was required on the MBPTA application process.
b) The impact incurred on the execution time of software programs running on COTS and MBPTA-compliant hardware features has been studied.
c) Software randomization solutions were for the FPGA SW-Rand, the AURIX and, to a lesser extent, the P4080 processor boards, to help achieve PTA conformance, for the sources of jitter caused by caches in COTS architectures.
d) RTOS support was provided for all the involved execution tasks and all HW platforms. This included the reinforcement of time-composability features and MBPTA support on PikeOS BSP and guest OSes for the FPGA and P4080, and an adaptation of Erika Enterprise for the AURIX.
e) Support for data tracing was consolidated with RTBx to feed RVS and the PROXIMA timing analysis.
f) Timing analysis for the FPGA SW-Rand and the AURIX was extended to deal with multicore contention. Both solutions were integrated into RVS. For the FPGA HW-Rand, the Extended Path Coverage (EPC) solution was fully integrated on top of RVS.
g) The port of mixed-criticality applications on the corresponding avionics, space and railway platforms was completed.
h) Experiments with case studies of the FPGA, AURIX and P4080 platforms were carried out.
i) Certification arguments (augmented with a description of the safety techniques/measures associated to PTA) were consolidated. To that end it was produced railway and automotive case study safety-concepts which were positively assessed by an independent certification authority

(TÜV Rheinland) and the analysis of the certification dossiers by AIRBUS and AIRBUS Defense and Space certification experts.

On the research side of the project, we had 56 papers accepted for publication in high-tier conferences and journals. Moreover, project partners took part in no less than 68 dissemination events (43 in the academia and 25 in the industry).

3.3 PROXIMA website

The PROXIMA website has been built and published at: ***www.proxima-project.eu***

4 Core of the report for the period: Project objectives, work progress and achievements, project management

4.1 Project objectives for the reporting period

The main objectives set forth for the project at M36 are specified next on a per-platform basis.

- The FPGA line of work had proceed in M18-M36 with the so-called "*variable inter-core interference*" (VICI) phase, i.e. with focus on multicore where tasks can have variable latency across runs. Two versions of the FPGA multicore platform, one with PTA conformance obtained by hardware design, the second with COTS hardware and software-only solutions had to be finalized.
  - For the FPGA HW-Rand, the goals were:
    - First, having consolidated hardware support to enable MBPTA on both CICI and VICI setups. This includes the consolidation and integration with PikeOS of the random modulo placement function in L1 caches and the hash-based random placement in the L2 cache, and the development of probabilistically analysable bus arbitration policies for the on-chip bus.
    - Second, putting in place hardware support to reduce the overhead of instrumentation and increase bandwidth of the tracing facility.
    - Third, providing support to the PROXIMA case studies and the IAB familiarization case studies.
  - For the FPGA SW-Rand, the goals were to have a consolidated software-only (i.e. software randomization techniques) tool chain to control cache jitter in an MBPTA-conformant way for all RTOSes targeting the FPGA platform. At the timing analysis level, a solution was proposed to factor in multicore contention in an MBPTA-conformant manner. Tracing support was further consolidated to adapt to multicore execution. At the RTOS level, specific support for the initialization and handling of random seeds provided by PikeOS for software-only techniques has been consolidated.
- A major objective for the final period was to improve and finalize the integration of the Extended Path Coverage (EPC) approach on top of the RVS tool chain for the FPGA HW-Rand. At M18, EPC was implemented as a set of external scripts, only marginally relying on the RVS framework for instrumentation. Our goal was to move EPC within the RVS ecosystem (RVS comprises a set of tools that interact to perform the analysis) at the end of the project.
- The plan for the AURIX board required having a final release of the technology (hardware platform, RTOS, timing analysis and software-randomization solutions) ready so that the evaluation with the PROXIMA automotive case study and the IAB case studies could be carried out. The software solutions available at M36 for the AURIX platform were expected to warrant full PTA conformance
- The work on the P4080 COTS multicore platform, including time-composable RTOS, timing analysis, SW-only solutions for PTA conformance and application porting was expected to produce a final release by M36, developed in parallel with user-feedback from case-study experiments.
- The work on the manycore simulator, aimed at having an initial simulator ready by M18, with two processor features (intra-cluster NoC by M12 and inter-cluster NoC by M18) rendered PTA-conformant by design. At M18, the porting will start of the timing analysis tool, the RTOS, the associated tool chain, and the chosen benchmarks. In the period from M18 to M24, another feature (new intra-cluster NoC designs specialized for mixed-criticality systems) of the

manycore processor architecture will be made PTA conformant. From M30, attention will shift toward comparing deterministic (a-la parMERASA) manycores and the PROXIMA manycore. The hardware design will be continue to be refined until the end of the project. The prototype implementation of the manycore RTOS to be installed on the manycore processor should be finalized around M24 to allow for the evaluation of its features on synthetic benchmarks and then undergo a refinement phase.

- Also on the hardware front and building upon the manycore simulator, the timing impact of two COTS and/or MBPTA-compliant features had to be analysed. The main target was the effect of caches since they are deemed as the hardware resource creating higher variability across executions.
- The work on certification/qualification had to mature during M18-M36 period. Whereas in the railway case-study safety concept, MBPTA, SW-Rand and HW-Rand solutions were positively assessed by an independent certification authority, an additional automotive case-study safety concept will be submitted to independent evaluation in the final period of the project.

Results with the case studies and the IAB familiarization case studies will allow assessing the coverage of the success criteria; the readiness of the toolchain and the real-time performance in terms of guaranteed and achieved timing behaviour. In summary, the project goal at MS3 was to deliver complete toolchains enabling the execution of the PROXIMA industrial case studies.

4.2 Recommendations from MS2 review (November 2015)

During the MS2 review held in Brussels in November 2015, several recommendations were made by the PO and the external experts. Below we recall them, together with a description of the actions we carried out to address them.

a) Identification of the factors of variation
   - "Efforts for validating a sufficient coverage of environmental conditions at run-time by input samples should continue."
   - "Project partners have designed techniques which identify major factors affecting execution times. This is a big step forward which can be used other contexts as well. However, predictions still come with outliers. Linked to this, reviewers see the need to cover during sampling difficult to predict run-time scenarios. Reviewers appreciate the fact that this issue is explicitly discussed in an open attitude."

Significant effort has been devoted to understand the variability arising from the execution platform underneath the application. To that end, numerous runs were performed in isolation with exactly the same initial conditions for input and system state. In the FPGA board, this allows detecting some variations due to "other activities" occurring in the processor. Yet, the magnitude of these variations (which were ascertained to be in the order of few tens of cycles) was so tiny to have no impact on the obtained predictions. Further discussion on this matter in the context of the FPGA can be found in D4.8. Related to this, D1.10 provides some further analysis of how to address the challenge of ensuring representativeness of input samples in the presence of time-randomized features, whether in hardware or in software. While such work needs to be further extended to provide a definitive answer, it already shows that such an answer does indeed exist, owing to the probabilistic nature of events that yields "meaningful" variability (i.e., one that can be studied mathematically) in execution time.

Analyses were also performed to isolate the impact stemming from the different sources of time randomization. D2.12 explains the impact of cache randomization in the AURIX. D4.8 breaks down the impact from on-core jittery resources (FPU; first level instruction and data caches; and instruction and data TLBs) and off-core jitter resources (bus).

c) Multicore results and COTS hardware

- "More results should be available for multi-core systems."

The central focus of the second phase of the project was set on multicore processors. The work performed progressed along the following three main lines.

- In the HW-Rand FPGA platform, several hardware randomization techniques have been proposed to control, in an MBPTA-friendly manner, the jitter caused by parallel contention on access to hardware resources shared across cores.
- For the COTS platforms, several timing analysis techniques have been proposed to add to the baseline MBPTA technology, to address the jitter caused by parallel contention on access to shared hardware resources. A technique called partially Time Composable (pTC) analysis was proposed for the SW-Rand FPGA platform, and a technique called FBI (short for Forecast-Based Interference) was proposed for the AURIX and the P4080. Evaluations with case studies were performed for the FPGA and AURIX board, bud could not be completed in time for the P4080.
- For the many-core simulator, we focused on different types of NoCs (on-chip network interconnects) and performed, to the best of our knowledge, the first comparison of multi-/many-core designs with strictly deterministic versus randomized timing behavior. This comparison allowed us to deepen our understanding of the performance impact that different shared hardware resources present in the architecture of a multi-/many-core processor can cause on the application level.

e) Impact and Exploitation

- "more effort should be planned to realize an effective exploitation and pre-industrialization of the PROXIMA results."
- "The impact and the exploitation of the PROXIMA results could be significant in the next years. Some actions seem necessary: increasing the involvement and the commitment of all partners to address promising and emerging exploitable use cases; considering certification issues, including the process-related ones".

The industrial partners had a dominant role in the third year of the project. In particular, they were exposed to a series of prototype releases that implemented the technology solutions proposed by the research partners for the timing analysis of the processor platforms of interest to PROXIMA, and returned user feedback on them, while also incrementally completing the implementation and evaluation of their use cases. This progressive exposure was a fundamental facilitator to constructing exploitation routes within each industrial partner in the project. The incremental feedback obtained from the end users was in turn essential for the solution providers to improve the efficiency (for degree of automation) and usability (for understandability of the analysis process and its output) of their technology. This proved an expensive, challenging and never-ending task that yet has seen good and satisfactory progress. The differences that exist in the elements and operation of the proposed PROXIMA solutions between the space and automotive platforms provide some indication of the magnitude of the problem addressed by the project, and of the technical differences between the relevant industries (for types of applications, use needs, and execution platforms).

Technical workshops were held to encourage and promote partner engagement in the mid- to long-term adoption of the PROXIMA technology. This has resulted in a number of opportunities to exploit various technologies in the project, and a range of "success stories" consisting of partnerships and specific opportunities, which are described in D5.10.

e) Success Stories

- "The objectives for the coming period are still relevant. The consortium has the abilities to aspire to a "success story". A way forward is to enhance in the evidence, including demonstration, of the use of random hardware in the (critical) systems taken under study. "
- "Industrial partners should be involved in this action [to realise a "success story"] outlining go-to-market actions."

At the end of the project, 14 "success stories" were single out, as specific, concrete opportunities to exploit the results of the project. Many of them are industrially focused, involving the industrial partners in the project, some also involving external companies.

Two of them are particularly relevant, as they motivate short-term and long-term furthering of the PROXIMA technologies.

Success story 1, in addition to being a short-term success, reports a partnership between BSC and Rapita to perform consultancy based on the multi-core micro-benchmarks, which will require further development and integration of some PROXIMA technology into the customer processes. This partnership focuses on the analysis tool technologies on COTS platforms. A workshop with Airbus has already taken place, successfully, to explore next steps.

At the other end of the execution platform, success story 2 between BSC and Cobham, aims to exploit the hardware randomization in future aerospace platforms. Cobham is promoting the technology and looking to include the hardware modifications in its future processors.

f) Customized hardware
   - "Strengthening the exploitation and sharpening the importance of custom HW for which the envisaged exploitation impact is deemed to be high compared to COTS for which the impact is considered medium"
   - "To have an effective exploitation, BSC could consider creating, or finding an existing, startup to transfer their results."

On the one hand, we have increased the exploitation impact for COTS, as this increases market opportunities and exploitation opportunities. On the other hand, BSC, in coordination with CG, has followed a low-overhead exploitation strategy by offering customized hardware as a product through the CG website. In fact, both BSC and CG will continue the development of enhanced a-la-PROXIMA customized hardware designs beyond the end of the project within the context of an already running project funded by the ESA. Moreover, specific IP libraries with only BSC IP are also ready for distribution and exploitation.

Reaching large-volume markets with customized hardware is a goal that cannot be realistically achieved in the short term. Acknowledging that, we are working to a continuous progression that:

1. allows end users to familiarize with this technology through joint BSC/CG test hardware designs;
2. grants time for other individual technologies (needed or convenient for customized hardware) to be introduced in the market such as multicore analysis and time-composable RTOS;
3. augments the maturity of this technology by reaching ESA prototypes and further developing hardware components. All these steps increase the chances of adoption of the PROXIMA customized hardware by end users first in internal studies, and subsequently in real products.

g) Certification
   - "The deliverable then provides a very good approach and relevant results. However, to exploit the PROXIMA results in a given domain, it is necessary to be compliant to the standards tailored to the considered domain"

The consortium has taken a specific action to take into consideration the certification issue on each of the considered four industrial domains. Additionally to the safety-concept for the railway use-case considering domain specific IEC-61508 and EN-5012x standards, a new safety concept has been elaborated on the automotive domain (w.r.t. ISO-26262 standard) considering specific PROXIMA issues and challenges. An independent certification authority (TÜV Rheinland) has positively assessed the technical compliance of PROXIMA technology with respect to these two domains. Such a private independent certification figure does not exist on the Aerospace domain, but an effort has been done by certification expert on AIRBUS and AIRBUS Defense and Space to elaborate a dossier for Avionics and Space domains considering the technical documentation in PROXIMA and the aforementioned two safety-concepts.

h) Deterministic architectures
   - "The first comparison against the deterministic hardware studied in the parMERASA project. Partners were able to demonstrate advantages for their probabilistic approach. This is a big step forward. This comparison is not yet included in the deliverables."
   - "-O0 required due to cache flushing. There may be code overhead and this could potentially impact a comparison with static WCET analysis, which has not yet been performed."

D1.12 discusses the required comparison and provides quantitative results. While a number of items have been improved for a fair comparison w.r.t. the preliminary numbers presented in the past, quantitative evidence confirms the advantages of the probabilistic approach that were anticipated with those preliminary results.

The "-O0" compilation flag, which was earlier indicated as a requirement for the use of the PROXIMA solutions, and caused concerns to the reviewers, turned *not* to be a requirement. However, it has been preserved for the sake of the specific implementation of SW-Rand, which depends on specific versions of the LLVM compiler. Thus, by preserving the same compilation environment, direct HW-Rand vs. SW-Rand comparisons have been possible in the project. Then, for consistency, this flag has been preserved also in the many-core simulator experiments. Since this is not really a requirement for any of those technology solutions, we believe that it creates no disadvantage for the probabilistic approach. Moreover, lessons learned from the comparison between deterministic and probabilistic approaches reveal that advantages of the probabilistic approach relate to the fact that it obtains WCET estimates relatively close to the average behavior (a bit above) rather than assuming systematically the worst scenario. This characteristic is independent of the particular set of compilation flags, which can, at most, affect the actual value of the gains, but not the fact that they exist and are meaningful.

i) WP2
   - "WP2 software maturity levels are diverse"

As acknowledged in the MS2 review, the maturity of the software-randomization solutions is lower than their hardware-randomization counter parts. This reflects the fact that Cobham Gaisler acts as the industrial expert on the FPGA platform and therefore provides the highest possible competence and savoir-faire on the design and implementation of HW-Rand solutions. In contrast with that, WP2 had to address a much wider span of technologies, cross-compilers, build chains, and RTOSes, which fed the research-path of the project scope in addition to the industrial path, which was served primarily by SYSGO's suite of PikeOS-based products. A number of technical issues (which included the IP nature of SYSGO's technology, the obvious rigidity of their architecture and packaging, their restrictive dependence on para-virtualization, and their not being available for the AURIX and the manycore prototype) caused a proliferation of execution stacks to be attended by WP2. This situation did not allow reducing the gap in software maturity across the proceeds of WP2.

Yet, it served well the purpose of ensuring that execution experiments, data collection and analysis could be performed for all processors considered in the project.

In spite of there being no industrial expert in compilation technology in the PROXIMA consortium, the base software randomization solution has been ported to all the COTS platforms that were used in the PROXIMA industrial use cases. This included developing a totally novel software-randomization technique for the AURIX, in which memory placements have to be kept static at all times during execution. This novel solution (nicked TASA) was experimented with success in the automotive use case that used the CONCERTO application.

j) Infineon involvement
   - "INFINEON could better use its resources if organise internal meeting with some PROXIMA partners and Infineon teams (in the same unit and in other units)"
   - "Infineon can better contribute to the "PROXIMA success story", for example by organising internal meetings with other internal teams/departments to promote the PROXIMA approach and developed technologies."

Infineon will organize a web seminar on the PROXIMA solutions, with special focus on their applicability to the automotive domain, in the October-November period. The seminar will cover:

- The overall PROXIMA approach
- The hardware changes proposed in PROXIMA for MBPTA compliance.
- The work done, for vision, accomplishments and results, on the AURIX platform.

Infineon staff from the Bristol and Munich premises shall attend the seminar.

k) WP3 - UoY
   - "work that has been done is in line with the expectations of the DoW and progresses mostly according to plan (with the exception of WP 3, which is delayed)."
   - "Increasing in the involvement and commitment of the University of York. If needed, it is suggested considering changing the WP3 leader"
   - "The University of York provides signs of underperformance and lack of commitment". "We highlight a deviation in the involvement and commitment of the University of York. It has an impact on the overall WP3 effort, which is higher than expected, because other partners should supply the missing work. There is not an evident agreement between the declared effort and the commitment of the University of York. If needed, it is suggested considering changing the WP3 leader. "

Following the contingency actions defined in the third version of management plan, presented in the D6.6 resubmission in November 2015, the coordinator prepared a reporting template to use specifically for tracking the minute progress of WP3. WP3L used this template from December 2015 until February 2016 inclusive, to report progress items and issues to the coordinator.

In February 2016, a PROXIMA Workshop was held at Airbus Defense and Space Facilities in Toulouse. In that meeting, the coordinator detected further important delays in the progress of WP3 that deflected from the plan established in D6.6 and were not accompanied by acceptable mitigation actions. At that point, the General Assembly of PROXIMA decided to change WP3L. This change was especially aimed to address the concern of the industrial end users in WP4 and the solution providers in WP1 and WP2, with the negative impact caused by the WP3 delay on the required per-platform technology integrations and the execution and evaluation of the due use cases.

The PROXIMA GA proposed UPD, and in particular Tullio Vardanega (already lead of WP2) to take the lead of WP3, in place of Iain Bate from UoY. This proposal was officially voted and accepted with 10 votes in favor and 1 abstention.

At the request of the new WP3L, a new action plan was proposed in which:

- BSC took full responsibility of the timing analysis of the FPGA board (which previously was task assigned to UoY), thus allowing UoY to concentrate on the development of VICI analysis for the COTS processors of interest to the project, first for the AURIX and then for the P4080.
- New, proactive and collaborative mechanisms were used to improve the internal communication and the technical understanding within WP3, and between WP3 and the other WPs.

With these changes, BSC assumed a very high technical risk to perform the multicore timing analysis for the FPGA SW-Rand platform in only a few months, without suffering delays in other BSC tasks as stipulated in the DoW. BSC also assumed a high financial risk to fit this extra effort in its assigned budget. This resolution also burdened UPD considerably, and caused some non-critical technical tasks to be put in the background to give priority to steering WP3 to completion. UPD's long exposure to the vision underpinning the project and vast experience in technical coordination resulted in better monitoring of the progress of the critical tasks and quicker identification of technical and strategic solutions.

These changes allowed mitigating the negative effect the WP3 cumulated delays on the project as a whole, and enabled completing the integration, use and evaluation of the analysis solutions for the two FPGA platforms (HW-Rand and SW-Rand) and the AURIX, which also facilitated the launch of the familiarization case with DENSO. Work on the P4080 reached sufficient maturity and stability to allow WP4 to experiment with the PROXIMA solutions for the platform for single-core setups (multi-core setups were not covered owing to lack of time). The time that was left for those experiments was however insufficient to instigate improvement cycles with the WP2 and WP3 technology and to dig deeper in the analysis results.

In spite of the considerable improvements achieved since last February, the delays cumulated by WP3 inevitably resulted in several changes in the overall project schedule, with far shorter periods granted for the integration of the various constituents of the PROXIMA tool chains. As noted above, this situation created serious difficulties for the solution providers and for the preservation of resources at the industrial users.

4.3 Work progress and achievements during the period

In the last 18 months of the project (M19-M36), there has been intense collaboration among partners to consolidate the tool chains, collect and analyze the results. The product of the work performed can be summarized as follows:

- In the FPGA, the work covered the consolidation and integration with PikeOS of hardware randomization (FPGA HW-Rand platform) and software randomization (FPGA SW-Rand Platform) to enable the use of MBPTA. Tracing support and support to the case studies was provided as required.
- For the FPGA HW-Rand platform:
    - Hardware has been developed according to plan, including PTA-conformant cores (especially dealing with FPU jitter, first level caches and TLBs), PTA-conformant bus design with randomization-based designs; randomized partitioned L2; and upper-bounded memory controller. Notably, for some of the hardware features (like the L1 caches and the PTA-conformant bus) we have gone beyond our commitments and developed designs such as random-modulo for the L1 cache placement and a credit-based bus arbiter that overcome the limitations of current state-of-the art PTA conformant designs under the specific conditions set by the RTOS, the compilation constraints for a fair HW-Rand / SW-Rand comparison, and the case studies.

- We have also developed support for high-speed multicore event tracing. Complete memory access trace (instructions and data) tracing has been implemented to support EPC. Support was provided to the external case study by providing a bitstream fitting the application requirements of the European Space Agency.
- The FPGA platform was integrated with the timing analysis framework via support for tracing execution-time data. In this manner, the FPGA execution stack and tool chain was fully ready for the VICI-phase experiments.
- EPC has been ported and consolidated in the FPGA toolchain. EPC releases the user from heavy and often untenable path coverage obligations on a multi-path program, as it synthetically extends the set of collected measurements to provide the equivalent of full path coverage. Originally implemented as a set of external scripts, EPC has been fully integrated on top of RVS as an additional set of automated tools that interact with it and extend its features. The basic infrastructure for MPTA, inclusive of EPC, on the FPGA has been made available to the end users first in a bare-metal setting and then extended to account for the presence of the RTOS

- For the FPGA SW-Rand platform:
  - Randomization was implemented at the software level. A rich suite of solutions has been developed, all equipped with software-only randomization capabilities: a) a bare-metal solution, intended for initial timing characterization; b) a hypervisor-based solution that uses PikeOS as host and PikeOS Native, PikeOS APEX as guest; c) a hypervisor-free solution that enables RTEMS to run on a symmetric multiprocessor with partitioned scheduling and support for global shared resources. Moreover, the software randomization implementation has been improved in order to provide lower pWCET estimations and memory consumption.
  - A technique was proposed to handle multicore contention jitter in an MBPTA friendly manner. The proposed approach uses as input only performance monitoring counter readings of the application in isolation, i.e. it does not require applications to be run in parallel, which reduces experimentation time and provides results which are independent of the co-runners of the application at deployment.
- For the AURIX:
  - Facilitated by UPD, active collaboration was established with the CONCERTO project (http://www.concerto-project.org/) so that CONCERTO would provide an automotive application targeted from the AURIX from their automotive partner and PROXIMA would adapt it to the PROXIMA analysis solution for that platform and return the analysis results to CONCERTO. This collaboration was very successful and allowed the project to cover the automotive domain for the application part as well as for safety-related considerations.
  - In order to alleviate the burden of having to make a large number of observation runs for every program of interest, the PROXIMA analysis framework for the AURIX had to enable a high level of automation in the instrument-build-deploy-run-trace-dump-analyse process cycle. It also had to ensure that the RTOS activity would not disturb the analysis experiments causing unpredictable effects on the execution time of the application (by local or global interference). To this end, a time-composable adaptation of the OSEK-compliant Erika Enterprise[4] RTOS was developed for the AURIX and fit in the build automation framework integrated in the VICI analysis infrastructure.

[4] http://erika.tuxfamily.org/drupal/

- The evidence of this application running on target and of its integration in the cited automation infrastructure facilitated the launch of a familiarization case study with DENSO, an automotive member of PROXIMA's IAB, which reused all of the AURIX infrastructure and only ported their own application to it in place of CONCERTO's.
- The static software randomization technique nicked TASA, developed specifically for AURIX and prototyped during the previous reporting period, was refined to better fit Erika's compiler, the instrumentation needs, Erika itself, the CONCERTO application, and the VICI analysis infrastructure.
- Experiments were made to ascertain that TASA was able to produce sufficient time randomization to satisfy the MBPTA requirements. The target of those experiments was the cache, exercised in single-core mode, where it was the only source of execution-time jitter in the AURIX hardware architecture. The results were positive and allowed integrating TASA in the build process prior to the launch of the analysis.
- An initial, qualitative, timing characterization of the AURIX was completed by M6 to single out the hardware resources that exhibit the jitteriest timing behavior. Those resources are referred to as *sources of execution time variability* (SETV). Further analysis of COTS NoC implemented on the manycore processor simulator was carried out to better understand the behavior of the NoC in the AURIX processor.
- A novel solution for Variable Inter-Core Interference (VICI) analysis was designed to model, in an automated way, the effects of a variable amount of interference generated by competing activity running in parallel on other cores than the program under analysis. An implementation of this technique was provided for the AURIX, and was successfully integrated in the overall automation framework. This enabled the execution of as many observation runs to obtain the VICI interference prediction and then pass the observation data to MBPTA to obtain the sought pWCET results.

- For the P4080:
  - Two applications, one from the avionics domain and the other for railway, were ported to the P4080, equipped with its PikeOS (native) environment, by AIF and Ikerlan respectively. The port depended on the availability of the processor boards, their integration with the instrumentation framework, and the integration of the latter with the PikeOS compilation and runtime libraries. This caused a chain effect in the scheduling of the respective activities, which reduced the time available for each involved partner to refine their artifacts, and prevented the finalization of the research-oriented RTOS and its use by the industrial partners.
  - The SW-Rand solutions, refined from use with the FPGA, were ported to the P4080, and integrated with the PikeOS build chain of interest to the industrial users.
  - The VICI analysis solution, now denominated FBI, that was first developed for the AURIX was ported to the P4080 and integrated (including its automation scripts) with the build chain for that processor, which allowed the industrial users to make observation runs with a sufficient degree of automation. pWCET analysis results were not obtained in any of the case studies, owing to the late delivery of the timing analysis toolchain. Yet we do not foresee any technical block for the adoption of the VICI-FBI model in the P4080
- For the manycore platform:
  - The manycore simulator has been extended with new tree-based NoC designs for the intra-cluster NoC providing higher controllability for mixed-criticality environments. A comparison between time-deterministic (a la parMERASA) and time-probabilistic (a la PROXIMA) manycore designs has been conducted revealing interesting trends that show that time-randomized designs effectively bring the pWCET close to the average

behavior for NoCs. This motivated the design and implementation of MBPTA-compliant mesh NoCs, which provide huge performance advantages w.r.t. time-deterministic ones. Finally, we have assessed how MBPTA-compliant cache designs improve also reliability by mitigating some sources of aging.
    - With respect to the RTOS support, the simulator has been improved to provide cluster-wide and system-wide interrupt support. This facility can be used by the RTOS to signal individual cores in the manycore and to synchronize tasks running in different cores.
    - The implementation of the ManyCOS prototype could not be finalized owing in part to technical difficulties that severely slowed down its on-target verification, and to project-wise considerations that suggested shifting resources to more critical tasks in the project.
- For the analysis of the timing behavior of COTS and MBPTA-compliant hardware features, we have analyzed the impact on execution time distributions of both, hardware-randomized and software-randomized cache memories, and related that impact to the representativeness of execution time samples provided to MBPTA. We have also analyzed the probabilities to observe cache placements affecting noticeably execution time for hardware and software random placement, with either homogeneous or arbitrary cache access patterns. These analyses illustrate that the minimum number of runs needed to have representative data samples for MBPTA can be determined based on probabilistic reasoning. Finally, we have assessed under what conditions the execution time impact of timing anomalies can be regarded as irrelevant.
- Improved Measurement-Based PTA (MBPTA):
    - Techniques have been consolidated to analyse independent and dependent timing data.
- Work was done to consolidate the certification argument and the associated evidence. This effort built on the positive outcome obtained from the first round-trip interaction with TÜV for review of the conformance of the railway case study against the EN-50128/IEC61508 standards. In the first reporting period, the project the certification task devoted most effort to the railway domain and to the cross-domain argumentation. In the M18-M36 period, a certification dossier was produced to consider PROXIMA technology certification challenges on the aerospace domain. For that, several certification experts on AIRBUS and AIRBUS Defense and Space have carefully evaluated technical documentation of the project together with the aforementioned safety-concept documentation. The main certification arguments and challenges are identified for the final industrialization phase of the PROXIMA technology are discussed in D2.13. For the Automotive domain, we followed the same approach as for the railway domain, which had a positive outcome after a review meeting with TÜV. To this end, a mixed-criticality automotive application safety concept, compliant with ISO-26262 has been defined for the CONCERTO application on top of the AURIX. This safety concept was reviewed by TÜV and a positive assessment was obtained.
- The IAB has been significantly engaged into the project by fluent interactions and early characterizing familiarization case studies (face-to-face discussion, questionnaires, etc.).

The result of the work for MS3 is presented in deliverables: D1.10, D.1.11, D1.12, D2.10, D.2.11, D2.12, D2.13, D3.8, D3.9, D3.10, D.3.11, D.4.8, D.4.9, D5.9, D5.10, D.6.7 and D.6.8

WP1

In the first 18 months developments in the FPGA and the many-core simulator have been performed as planned to i) provide MBPTA compliances and ii) provide support the upper layers of the PROXIMA execution stack: system software (WP2), timing analysis tools (WP3) and case studies (WP4). COTS features have been studied in the simulator to better understand how they can affect SW-only solutions (WP2) as well as timing analysis methods (WP3). Overall, progress has occurred as scheduled.

In this period, we have consolidated the FPGA HW-Rand platform for MBPTA compliance. In that respect, we have put significant effort on the integration of random placement in the L1 data cache due to the complexities introduced by the cache coherency support and on the development of a transparent (no-interference) real-time tracing support able to get traces from all the cores simultaneously at high speed. Since the focus of this period was on the ability to capture multicore interferences we have also devoted a significant amount of time for the development of PTA-amenable arbitration policies enabling competitive WCET estimates.

In the manycore platform we completed all expected developments. The majority of the effort has been put on the development of PTA-conformant NoC designs suitable to deal with intra- and inter-cluster communications since we tested that arbitration policies proposed for the bus also work well for the memory controller, as well as on a fair comparison between time-deterministic and time-randomized manycore designs. More COTS and MBPTA-compliant features have been analyzed mostly focusing on cache behavior and timing anomalies, and how these features influence execution time distribution and representativeness of execution time samples used by MBPTA.

On a per-task basis, contributions have been as follows:

- T1.6 focuses on the analysis of MBPTA-compliant and non-MBPTA-compliant (COTS) hardware features. Impact on execution time distribution of hardware- and software-randomized cache memories have been studied and related to representativeness of execution time samples. Also, the probabilistic nature and execution time impact of random cache placements, either produced by hardware-only or software-only means, have been assessed for both homogeneous and heterogeneous memory access patterns. Finally, the impact of timing anomalies on execution time distributions has also been assessed.
- T1.7 focuses on the FPGA multicore board. We have completed the missing modifications and produced a PTA-conformant multicore design. After m18 significant effort was still required to complete the integration of the random placement in the L1 data cache and in the L2. Both integration tasks were successfully completed after introducing some extra non-planned modifications in the platform. As planned, the focus remained to be on the modifications required to achieve VICI MBPTA-compliance. To that end, the support for L2 cache partitioning was implemented and different PTA compatible bus arbitration policies were designed, integrated, and tested in the final platform. The result of this task, a fully-featured Leon3-based multicore PTA processor design, has been completed adequately.
- T1.8 focuses on the many-core simulator platform. The manycore platform has been completed. The developed platform includes the support for heterogeneous guarantees and support the integration of tasks of different criticality. These features are provided by PTA NoC designs that include trees, meshes, and crossbars. Moreover, time-deterministic and time-randomized manycore designs have been compared on an equal basis.

On a **per-platform basis**, the achievements can be summarized as follows:

- FPGA HW-rand: random modulo and hash-based random placement have been successfully consolidated and integrated in DL1, IL1 and L2 caches Bus arbitration has been made compatible with PTA with existing solutions, and new bus arbitration schemes have been

devised, implemented and integrated for increased efficiency. In summary, all elements needed to have a fully-featured PTA compliant multicore platform have been completed. Furthermore, tracing support capabilities have been noticeably enhanced. Those unique tracing capabilities have been seamlessly integrated with the RapiTime timing analysis flow.

- FPGA SW-rand: no development had to occur for this platform in WP1. However, all tracing, debug and I/O-related developments contribute to this platform also.
- AURIX: the impact of cache memories and timing analysis on execution time distributions and representativeness of execution time samples supports SW-only solutions and timing analysis methods.
- P4080: this platform benefits from the same contributions of WP1 as the AURIX one.
- Manycore simulator: The platform has been completed. The developed manycore has been made PTA-conformant, with alternative and highly-flexible designs, and provides the support needed by the system software and RTOS. Moreover, the manycore simulator has been enhanced to allow a fair comparison between time-deterministic and time-randomized setups.

The **main outcomes** of WP1 include:

(1) PTA-conformance of the FPGA HW-rand platform for CICI and VICI setups;
(2) tracing, debug and I/O support for both the FPGA HW-rand and SW-rand platforms as needed by the SW layers;
(3) analysis of the timing impact of COTS and MBPTA-compliant caches, NoCs and timing anomalies in a simulator to support SW-only solutions and timing analysis methods;
(4) PTA-conformant intra-cluster and inter-cluster NoC designs for many-core clustered processors supporting mixed criticalities, as well as the assessment against time-deterministic setups and the study of reliability effects of time-randomization.

The table below will present the consolidated effort spent in the following workpackage and the explanation of the deviations:

	PM (M18)	PM M36	Total Planned (DoW)	Explanation of deviations
BSC	46,12		92,00	
RPT	3,08		6,00	
SYS	3,00		3,00	
UPD	1,50		2,50	
INRIA	1,00		2,00	
CG	21,00		39,00	
AIF	0,32		1,00	
UoY	0,11		3,00	
ADS	0,12		3,00	
IKR	0,00		0,00	
IFX	0,20		1,00	
Total	76,45		152,50	

WP2

In the first 18-month period, WP2 met the initial set of software-level needs to support for PROXIMA timing analyses and enable their application on industrial case studies. This effort included: the provision of working execution stacks for the different platforms (RTOSes and tool chains) with a first set of time-composable RTOS features already made available (though limited to the ARINC653 personality); and the porting of SW-only techniques to the FPGA platform (bare-metal and RTEMS settings), a preliminary study of its application on the P4080 and prototyping of a novel SW-only solution for the AURIX platform. WP2 was also active in the certification front and was able to develop a safety concept on the use of PTA in a fail-safe railway system and to have it approved by an independent certification authority. On the more research-oriented line of work, WP2 provided a high-level characterization and design of the manycore prototype RTOS for the PROXIMA manycore platform.

In the subsequent 18-month period, WP2 continued to develop the software-level solutions required by the PROXIMA analyses for all the processor platforms of interest, to enable the start of the WP4 experiments, especially the port of the use-case applications, the implementation of tracing, and the automation of the measurement runs. Important effort was devoted to developing and improving the certification argument to support PROXIMA. The development of the manycore prototype RTOS neared completion, but could not be finalized owing to technical difficulties of integration with the processor simulator and project-level decision to devolve residual resources to other critical tasks.

On the industrial RTOS front, the time-composability features in PikeOS, previously limited to selected elements of the ARINC-653 personality, were refined and extended. On the FPGA side, ad-hoc modifications were also required to refine the custom BSP support for the FPGA platform, which required several incremental and bug-fixing releases of PikeOS. On the P4080 side, PikeOS had to accommodate the needs of the SW-Rand solution, but – thanks to its abstraction layer – could directly inherit the time-composability features developed for the FPGA.

For the research-oriented RTOSes, the required time-composable extensions were completed for RTEMS SMP and Erika Enterprise, for the FPGA and the AURIX respectively. Both prototypes were evaluated on synthetic benchmarks to finesse their features and release them to the project at M24. Owing to lack of resources in WP4 and schedule delays at project level, RTEMS SMP was not used by the intended industrial user in PROXIMA, but was experimented with in study projects funded by the European Space Agency, which allowed to fully consolidate its codebase. The time-composable version of Erika Enterprise was instrumental instead to enabling the execution of the automotive use case on the AURIX as well as in the launch of the familiarization case study with DENSO, member of PROXIMA's Industrial Advisory Board. Considerable effort was devoted to adapting the automated build utilities of Erika to serve the VICI analysis process.

The SW-Rand solutions were fully integrated with PikeOS for both FPGA platforms, in particular, with PikeOS Native (used by the Railway case study), PikeOS APEX, (used in the Avionics case study), and PikeOS RTEMS (candidate for use by the Space case study). Improvements over the limitations identified in the refinement phase regarding pWCET estimations and memory consumption have been designed and implemented.

The SW-Rand solutions were subsequently ported to the P4080, inheriting all the improvements made to their FPGA correspondents.

The SW-Rand solutions designed for the AURIX platform, denominated TASA and applied at compilation (as opposed to at execution), was finalized and integrated with the Erika build chain, the VICI instrumentation, and the CONCERTO application.

On the certification front, WP2 concentrated on two parallel directions. It refined the cross-domain certification argument, and it prompted certification experts of the space and avionics partners to elaborate a certification dossier for their own application domain. For the automotive domain, WP2 elaborated an automotive safety-concept (akin to the railway one already completed and approved by TUV) based on the AURIX and the CONCERTO application, for assessment against ISO-26262, which passed the independent review of TUV.

On a per-task basis, the following contributions were made:

- T2.5: The work on the manycore prototype RTOS has advanced following a modular approach were small RTOS modules were developed in isolation and later integrated according to the overall design. Some technical difficulties in integrating the RTOS in the processor simulator (especially slowness of execution, which made debug runs extremely time consuming) and the transfer of residual resources to serve more critical tasks in the project, caused this line of work to suffer additional delays. As the integration with the processor simulator could not complete in time, there currently is no stable version of the RTOS prototype. A description of the development status and of what it takes to bring it to completion is provided in D2.10.
- T2.6: this task takes on the outcomes of T2.3 and T2.4 to provide a refined and consolidated set of software-level solutions to support MBPTA on multicore processor, including (i) RTOS support for the whole set of target processors and (ii) SW-only solutions for COTS platforms. On the RTOS side, refined versions of set of RTOSes with improved time-composability features have been made available for the PROXIMA FPGA (PikeOS and RTEMS SMP) and the COTS platforms (PikeOS for the P4080 and Erika Enterprise for the AURIX). SW-Rand solutions were integrated on all platforms. Dynamic SW-Rand solutions were successfully ported to the P4080 and further consolidated on the FPGA. A static SW-Rand solution was developed for the AURIX and successfully integrated in the VICI analysis framework. The outcomes of this task are reported in D2.11, for PikeOS, and D2.12 for all the rest.
- T2.7: The safety concept based on the railway case study and EN-50128/IEC61508 standards discussed and approved by TÜV has been further refined so that to serve a reference for the other industrial domains directly involved in PROXIMA. A common certification argument has been elaborated based on the outcomes of the safety concept. This line of work has been conducted in tight dialogue with the industrial users operating in WP4 and representatives from the DREAMS consortium, which is part of the mixed-criticality cluster, in a view to define a common certification approach. A certification dossier has been elaborated by certification experts within each partner organization to capture domain specific concerns. For the automotive domain an automotive safety-concept similar to the railway one already completed and approved by TUV has been defined. All outcomes of this task are reported in deliverable D2.13 and related appendices.

On a **per-platform basis**, the achievements can be summarized as follows:

- FPGA HW-rand: a complete software execution stack has been provided for both the industrialization and research lines. The PikeOS PROXIMA BSP and relevant guest OSes include time-composable features and fully support the PROXIMA HW randomization features (e.g., random seed initialization). An RTEMS SMP port to the PROXIMA FPGA with support to the HW randomization features has been made available to industrial users.

  FPGA COTS with SW-Rand: all features provided for the HW-Rand FPGA were reused for this platform. SW-Rand solutions were ported to the FPGA platform, with and without RTOSes. The early version of the SW-Rand solution incurred excessive overhead the first time a function call was performed, which complicated timing analysis. This one-time overhead has been moved to the initialization phase of the execution, therefore not impacting the pWCET estimation. The early version of the SW-Rand solution also consumed excessive memory, which prevented the large application of AIF to be executed. Owing to the late identification of the issue and the high

development cost of its fix, the improved version was not implemented for the FPGA (which did not need the fix).

- AURIX: the original codebase of Erika Enterprise was modified to inject time composability in the most critical RTOS services from the perspective of the application of MBPTA. The Erika build chain was modified and expanded to allow automating the MPBTA process. This process needed the construction of multiple binaries of the application, their instrumentation for tracing, and the execution of multiple observation runs per binary, and therefore would be too effort intensive for a human to perform. A specific version of the SW-Rand solution (nicked TASA) was developed and integrated in the VICI analysis framework and subsequently refined for performance and automation.
- P4080: the PikeOS baseline, already made available to the industrial users from early on in the project, was realigned to include the improvements obtained in the FPGA line of work. The SW-Rand solution was successfully ported to the P4080 and integrated into the VICI analysis framework for it. Enhancements to the FPGA SW-Rand solutions such as reduced pWCET estimations and low memory consumption were implemented for the P4080. The latter improvement allowed the execution of the large avionics application of AIF. The SW-Rand toolchain was integrated with PikeOS Native (used by the railway case study) and PikeOS APEX (used by the avionics one).
- Manycore simulator: the implementation effort on the RTOS prototype for the manycore simulator from WP1 produced a set of major RTOS building blocks (scheduler, timers, and synchronization mechanisms) but did not achieve final integration with the processor simulator owing to reasons of *force majeure*, further discussed in D2.10.

The **main outcomes** of WP2 include:

(1) Software-level support to all the industrial case studies (CICI and VICI phase)
(2) Refinement and injection of time composable features in the RTOS baselines for all platforms
(3) Port of the SW-Rand solutions to the FPGA and P4080
(4) Refinement of the SW-Rand solutions for the FPGA and the P4080
(5) Elaboration and integration of a specific incarnation of SW-Rand for the AURIX (TASA)
(6) Nearly completed implementation of the manycore RTOS prototype
(7) Elaboration of a certification argument for the PROXIMA approach
(8) Elaboration of domain-specific certification dossiers for avionics and aerospace domains
(9) Elaboration of safety concepts for the railway and automotive domains.

The table below will present the consolidated effort spent in the following workpackage and the explanation of the deviations

	PM (M18)	PM M36	Total Planned (DoW)	Explanation of deviations
BSC	26,61		36,00	
RPT	12,27		24,00	
SYS	12,06		39,00	
UPD	33,50		50,00	
INRIA	3,75		4,00	
CG	0,00		0,00	
AIF	0,60		2,00	
UoY	1,08		17,50	
ADS	0,00		1,00	

IKR	11,32		14,00	
IFX	0,20		0,50	
Total	101,39		188,00	

WP3

In the first 18 months, development of the EVT-based analysis has proceeded. EPC, a form of MBPTA has been developed to deal with different input paths (presently for the FPGA platforms only). Some characterization of the use-case platforms has been done. Experiments have been performed to establish the conditions for MBPTA to work in the context of certification cases. Some deviations are detected with respect to D6.3 and the proper counter measurements are proposed.

In the subsequent 18-month period, WP3 devoted a great of effort at studying how to adapt the EVT method concern to the PROXIMA needs. The statistical tests employed in the EVT calculations require appropriate test values: those values were studied and refined in the reporting period. The latest version of the EVT calculations is able to capture the low variability in execution time that some programs may experience in spite of the randomization injected by the modified execution platforms. The resulting analysis method is exploitable, after testing against real industrial programs, but its current R implementation does not offer adequate robustness to industrial use.

Two variants of the VICI analysis were finalized, integrated with RVS and released to WP4, one for the FPGA SW-Rand, denominated Partially Time-Composable (pTC) and Fully Time Composable (fTC), and the other AURIX and the P4080, denominated Forecast-Based Interference (FBI) VICI. The solutions for the FPGA and the AURIX were used and evaluated in industrial case studies, while the ones for the P4080 were not, owing to lack of time and energy in WP4 (end users).

EPC, the PROXIMA method to automatically extend the representativeness of MBPTA results, was finalized and integrated with RVS. We also implemented tool support for the automated generation of synthetic measurements, which was not fully automated in the prototype version of the tool.

RVS and the associated instrumentation framework were ported to all the platforms of interest and formed the integration basis for all platform-specific analysis and build tool chains.

On a per-task basis, the following contributions were made:

- T3.2 – Analysis for Mixed-Criticality on Multicore. Benchmarks and synthetic contenders were developed for all PROXIMA platforms. Detailed evaluations were performed for the FPGA, the AURIX (with internal and external users) and the P4080. The EVT analysis has been evolved with the progress of our understanding of how to compute valid pWCET estimations that ensure both reproducibility in the presence of all statistical properties of relevance, and representativeness of statistical tests. The voting procedure was also integrated in the identically-distributed tests and appropriate check values were identified.
- T3.3 – Analysis for Mixed-Criticality on Manycore. Benchmarks and synthetic contenders were developed for the manycore simulator platform, alongside a framework for the evaluation of the VICI analysis on the bare metal platform. This includes modifications to the instrumentation infrastructure to collect additional statistics from the simulator. The evolution of the EVT analysis was extended to cover the needs of the manycore processor.
- T3.4 – Probabilistic analysis support for case studies. Substantial work was performed on integrating numerous PROXIMA-developed tools into an overall analysis framework. On the AURIX, TASA was modified to support the C99 language version needed to support the applications, a companion tool to TASA was introduced, and instrumentation mechanisms were integrated with Erika-TC, so that they reliably allowed reading out run-time parameters from during observation runs. The application build toolchain was refined to include the different technology items, and then the overall analysis framework (RTOS, TASA, MBPTA and VICI) integrated, tested and evaluated. On the P4080, instrumentation mechanisms were integrated

with PikeOS to reliably read out run-time parameters from observation runs, and then the overall analysis framework (RTOS, MBPTA and VICI-FBI) integrated, tested and submitted to initial evaluation. For EPC, a set of scripts have been developed to automate the application of EPC (both in bare-metal and on top of PikeOS) building on top of the RVS environment. For the FPGA, every access to shared hardware resources were measured and models developed to capture inter-task interference and enable the development of fTC/pTC analysis. For the EVT method, continuous interaction was had with the industrial users, to adapt the method to meet their needs. One of the major modification made in the reporting period was to provide a solution to the small variability of execution time observed in some experiments.

- T3.5 – Industrial-strength analysis tool development. RVS was enhanced by several modules, provided by WP3 partners, to support additional types of analysis. Some modules are tightly integrated to the RapiTime tool, e.g. EVT/MBPTA, while others (EPC and pTC/fTC, FBI-VICI) are supported by providing an API to access internals or simply by modifying the input or output of particular stages of analysis. This has allowed certain key parts of RapiTime (instrumentation, tracing, etc.) to provide a robust framework to achieve reliable analysis tools. EPC was integrated with RVS by means of minor extensions to the internals of RVS and the development of a set of specific bridging tools. The pTC/fTC analysis technique was developed to determine the multi-core jitter occurring in the FPGA, and return an increment factor to measured execution times, dependent on the number and type of accesses to shared hardware resources made by the software program under analysis. Analogous tools and techniques for multi-core interference (VICI) analysis, prototyped in tasks T3.3 and T3.4, were refined for use and evaluation in the industrial case-study applications running the AURIX and the P4080. The AURIX effort included successful delivery to and evaluation by DENSO, from the Industrial Advisory Board. The current implementation of the EVT method use R, which has proven unfit for industrial use, owing to the fact that multiple, distinct implementations of the same function are allowed to appear in several installation packages of R, causing the application to behave differently. We have minimized the impact of this flaw by re-coding some critical packages, but we reckon that a different language implementation should be made to make the EVT calculation engine fit for industrial use.
- T3.6 - Industrial strength integration tool enhancement. All timing analysis tools and methods developed in the project were integrated, via RVS, in their respective tool chain, resulting in technology frameworks specialized per platform, covering from instrumentation to presentation of complete pWCET estimates. Each platform solution was evaluated through a dedicated use case conducted by internal industrial partners (for the AURIX, P4080 and FPGA platforms), or Denso, an external partner from the Industrial Advisory Board, on the AURIX.

On a **per-platform basis**, the achievements can be summarized as follows:

- FPGA HW-Rand and SW-Rand – Every type of contending access to the system bus has been characterized and measured with high accuracy, and the sources of inter-task interference have been determined. This allowed the implementation of the fTC/pTC analysis techniques for the SW-Rand platform and their integration with RVS. The EPC method and tool chain were finalized for the HW-Rand platform, and integrated with RVS. All those analysis solutions were released to WP4 and evaluated in industrial case studies.
- AURIX – Integration of MBPTA and VICI with RVS and the Erika-TC build automation (including TASA) was completed, along with target integration and instrumentation, allowing run-time parameters to be captured during observation runs and feed VICI analysis with them.
- A case study using the CONCERTO platform was fully analysed. Initial results were obtained from the DENSO familiarization case study.

- P4080 – Integration with RVS was completed, allowing run-time parameters to be captured during observation runs and feed VICI-FBI analysis with them. The integration had two parts: one for instrumentation, which caused RVS' compiler wrapper to be installed on top of PikeOS's codeo development environment, and a number of extra features to be added on top of PikeOS itself (for tracing, for selectively configuring the read-outs, for inclusion of TASA).
- Manycore simulator – Instrumentation was provided for integration with RVS. The processor platform was characterized for timing. Analysis to reduce contention effects were performed.

The **main outcomes** of WP3 include:

1) Controlled experiments to support the certification arguments
2) RVS-PROXIMA - software timing analysis tool (RapiTime) modified RapiTime to support the other four analysis tools
3) MBPTA tool for providing pWCET of probabilistic platforms and its extensions to deal with dependencies
4) EPC – extended path coverage tool, to supplement MBPTA for multiple paths.
5) pTC (Partially Time Composable) and fTC (Fully Time Composable) tools - technique that provide multi-core analysis for the COTS-FPGA software randomized platform
6) FBI-VICI – Forecast Based Interference analysis tool analysing multi-core timing interference on randomized and non-randomized platforms.

The table below will present the consolidated effort spent in the following workpackage and the explanation of the deviations.

	PM (M18)	PM M36	Total Planned (DoW)	Explanation of deviations
BSC	7,70		8,00	
RPT	16,91		31,00	
SYS	4,10		12,00	
UPD	18,30		23,00	
INRIA	21,50		55,00	
CG	0,00		0,00	
AIF	0,30		1,00	
UoY	46,57		53,50	
ADS	0,00		0,00	
IKR	4,11		6,00	
IFX	0,00		0,00	
Total	119,49		189,50	

WP4

In the first 6 months, WP4 achieved the definition of the case studies for all industrial domains and the gathering of the requirements that these applications generate to the rest of technical work packages. This definition covers the choice of the hardware platform to be used in each case study as well as the selection of the software stack and the use constraints in the timing analysis tools and tracing support. Additionally, the porting of the case studies to the FPGA board was started, reaching the integration of the application subset for the CICI phase. To this end, the whole tool-chain was integrated, including the hardware randomization features expected to this period, the different OS personalities and the tracing support for the FPGA. This resulted in a number of interactions with the rest of the work packages were feedback was forwarded and some issues solved. To validate the whole tool-chain and ensure that all partners running the case studies are on the same page before starting with the CICI phase, a set of experiments based on benchmarks (PAKs) that exercise different features of the platform were defined and executed. Additionally to the industrial partners in the consortium, good progress has been achieved with the engagement and familiarization case-study strategy with the IAB members.

In this period (M18-36), a final and mature set of PROXIMA tools (consolidated FPGA bitstream for HW randomization, SW randomization code, PikeOS, RVS versions, MBPTA and VICI analysis tools etc.) have been integrated into all the PROXIMA supported platforms (FPGA, AURIX and P4080 scenarios) together with the three industrial use-case applications. This has required intense coordination activities between technology and tool providers on the one hand and industrial end-users on the other hand. This has resulted in consolidated tools, technologies and use cases thanks to strong collaborative spirit. In this integration phase, WP4 experiments served to identify a number of issues and limitations that did not arise in the technical WPs when testing their technology in isolation. As a results, WP1, WP2 and WP3 tools were fixed (at different moments in time and with different frequency) and new enhanced approaches developed (e.g. credit based arbitration in the HW-Rand FPGA). Thanks to that, a final set of results has been documented in D4.8, including insight of the different technologies and analyses of the results on the 4 targeted domains (Avionics, Space, Railway and Automotive). These experiments have also served to allow the end users to evaluate the overall effort required to apply MBPTA in a real system development process and to identify its drawbacks. Additionally, the engagement with IAB has resulted in good advice and direction plus the undertaking of two familiarization case studies, which have demonstrated the PROXIMA technology outside the consortium, as documented in D4.9.

On a per-task basis, contributions have been as follows:

- T4.3 “Execute and analyze experiments”: after finalizing T4.2 “Application Development and Porting, and Preliminary Experiments” during the previous 18 months period, within this final Task 4.3 consolidated experiments have been performed after strong interaction with the other technical workpackages. This execution and analysis of experiments has involved continuous interaction with technical WPs for debug and support purposes. At the end, the complete set of MBPTA tools have been successfully integrated within all the target industrial domains (Avionics, Space, Railway and Automotive) and MBPTA results have been obtained for all the developed platforms (i.e., hardware and software platforms stated in the plan).
- T4.4 “Support for IAB familiarization Case Studies and management of the interaction with IAB”: The interaction with IAB members has been frequent and supportive, with regular IAB meetings throughout the project, including an automotive focused on and a successful industrial workshop. Two familiarization case studies have been carried out: one at the European Space Agency was successful and produced good results; the other with DENSO, an automotive partner, is still on-going after struggling with some technical issues.

On a **per-platform basis**, the achievements can be summarized as follows:

- FPGA with HW-rand: within this platform experiments have been processed and results have been collected and analyzed in several scenarios. First, the industrial applications have been evaluated in isolation, in a platform configuration that managed all features inside cores (i.e., time-randomized caches and upper-bounded FPU latencies), but not those outside the cores (i.e., time-randomized bus). These first results served as a reference to evaluate the impact of multicore contention in the next deliveries that considered different bus arbitration policies (Random Permutation and Credit based). The evaluation of the Random Permutation approach on the case studies revealed a high pessimism in the results, mainly caused by the compilation options used to make the results comparable with SW Randomization results. Even if a high pessimism was expected before running WP4 experiments, the effect of the SW rand Toolchain was not observed when evaluating the random permutation approach with benchmarks and as a result WP1 decided to improve the arbitration by developing the credit based approach. After executing the experiments with the credit-based approach, the case studies have also been evaluated executing the complete mixed-criticality applications, where real applications on each domain are used as contenders in the other cores. Railway, Space and Avionics domain use-cases have been integrated and evaluated within the different configurations of this platform.
- FPGA with HW-rand and EPC: EPC was ported to the FPGA HW-Rand. This technology integration has been automated within WP2 and WP3 to automatically manage execution path related jitter without increased end user effort in terms of path coverage, and evaluated in the Railway and Avionics case studies within WP4. This platform enables extending the analysis to paths not traversed during the observation runs, using a genuine and sound PROXIMA method. Integration in WP4 has been done incrementally, starting with bare metal experiments first and moving to PikeOS in the last phase of the project. Collected results and performed analyses confirm this technology direction.
- FPGA with SW-Rand: in addition to using hardware modifications, the software-only approach of PROXIMA technologies has been also experimented within WP4 in Railway, Space and Avionics case studies. Analogous to the hardware approach, execution time measurements are done by running the unit of analysis in isolation and then an analysis of the multicore contention is done by applying different contention models (fully Time Composable, Partially Time Composable and parameterized partially Time Composable). For validating the approach, the complete mixed-criticality uses cases have been analysed then, using real case study applications as contenders in the other cores. This allowed concluding that the bounds obtained with the multicore models are valid.
- AURIX: The CONCERTO application, which came from an industrial supplier of automotive software, was used as a benchmark for the AURIX tools developed in PROXIMA, namely: the time-composable RTOS, developed in WP2; TASA, developed by WP2 and WP3 to inject software-based randomization in the application subject to timing analysis, to conform with the MBPTA requirements; VICI-FBI, developed in WP3 to quantity the contention overhead generated by parallel execution on the AURIX processor.
- P4080 with SW-Rand: The avionics and railway case studies were ported by AIF and Ikerlan the processor and integrated with the tracing infrastructure, the software randomization utilities and the VICI-FBI analysis tools for this platform. The experiments suffered considerably shortage of time and effort resources owing to the late arrival of the PROXIMA technology. The reasons for this delay are discussed elsewhere in this data package. The effect of the delay however was the inability of WP4 to perform a full round of experiments, that is, to collect all the observations required to first feed VICI-FBI and

then submit the results to MBPTA. Only partial experiments were conducted to completion, which yet produced a vast amount of data for WP4 to reflect on and draw initial ideas on the implications of applying the PROXIMA solutions to their applications running on the P4080.

- For the manycore, WP4 is not involved in any work for this period.

The **main outcomes** of WP4 include:

(1) Technologies and tools developed within the project time have been integrated and consolidated together with representative industrial use cases of the targeted Avionics, Space, Railway and Automotive domains.
(2) All the platforms defined in the project plan have been exercised and industrial promising results have been obtained.
(3) The engagement of the IAB into the project by early characterizing familiarization case studies has been concluded on a successful manner.

The table below will present the consolidated effort spent in the following workpackage and the explanation of the deviations.

	PM (M18)	PM M36	Total Planned (DoW)	Explanation of deviations
BSC	3,56		7,00	
RPT	5,15		11,00	
SYS	0,22		1,00	
UPD	7,00		9,00	
INRIA	1,00		8,00	
CG	0,00		0,00	
AIF	9,20		18,50	
UoY	0,08		8,00	
ADS	9,32		23,50	
IKR	17,00		32,00	
IFX	0,95		4,00	
Total	53,48		122,00	

WP5

The dissemination to academia and industry are both successful based on an important number of accepted papers (55), dissemination events (7 keynotes out of the 43 academic events, impressive web impact with more than 11.000 visits of PROXIMA pages during the lifetime of the project).

The project is well on its way to successful exploitation, with some of the 20 technologies already commercially available, 2 patents (one applied, one planned) and a number of partnerships/success stories being actively developed to support on-going industrial transfer.

All objectives have been fulfilled and there are no deviations with respect to the Description of Work. WP5 has five tasks active during this period of the project (and five associated deliverables):

- T5.1. External communication (dissemination) strategy definition: this task has been fulfilled by the detailed dissemination strategy presented at M4 in the deliverable D5.1. Moreover the project had a strong 18 months on the dissemination part with:
    - 94 papers submitted, 55 papers accepted including:
    - 7 high-quality journal papers including: IEEE Micro and the Journal of Real-Time Systems.
    - 38 papers accepted for publication in important conferences (RTSS, ECRTS, DAC, DATE, ETFA, RTNS);
    - 10 Workshop papers (e.g. WCET Analysis Workshop)
    - Most recently the project has organized and sponsored the following:
        - Ada-Europe PROXIMA Tutorial session –June 2015, Madrid, Spain.
        - Sponsoring of the WCET 2015 workshop to be held in Lund, Sweden, 2015.
        - Sponsoring of the De-CPS 2015 workshop, again during Ada-Europe 2015
        - The first three editions of WMC at RTSS
        - The first edition of a Dagstuhl seminar on mixed-criticality
    - Participation in the MultiPARTES project advisory board
    - Part of the panel at Challenges of Timing Analysis of Many-core Platforms, HiRES 2015 workshop.
    - Invited talk during the “Towards Platforms for Mixed Criticality Systems” workshop at the ARTEMIS/ITEA co-summit 2015.
    - A joint booth with DREAMS and CONTREX projects at the ARTEMIS/ITEA co-summit 2015.
- T5.2. Dissemination tools: this task has been fulfilled and two deliverables contain these contributions:
    - D5.2 concerns the project public website, which is now online and available at http://www.proxima-project.eu. This website has been continually updated with news, events and publications.
    - D5.3 concerns dissemination tools, which have been made available as follows: a project slideshow, a poster, brochure on use cases and a project description leaflet (factsheet) which has been kept current with progress in the project.
- T5.3 Press releases: during the entire projects the participants have released 11 news items.
- T5.5 Technology transfer and exploitation: this task has been responsible for the creation of D5.7, a market trend analysis report in conjunction with members of the IAB. This includes a SWOT analysis to assess the opportunities for exploitation. At the end of the project, 22 exploitable technology items have been developed, each accompanied by the statement of opportunities and exploitation plans. There are also 14 success stories to report (for partnerships, customer relations, etc.). All of that is presented in D5.10.

- T5.6 IPR Management detailed the first IPR proposition detailed in D5.5. This has been extended to include an IPR register. The IPR register has been used to track the exploitable technology items, patents and sharing of background IP.

The table below will present the consolidated effort spent in the following workpackage and the explanation of the deviations.

	PM (M18)	PM M36	Total Planned (DoW)	Explanation of deviations
BSC	2,80		4,00	
RPT	5,16		10,00	
SYS	0,42		1,00	
UPD	1,25		2,00	
INRIA	2,00		6,00	
CG	0,30		2,00	
AIF	0,30		1,00	
UoY	0,94		2,00	
ADS	0,00		1,00	
IKR	1,94		3,00	
IFX	0,00		0,00	
Total	15,11		32,00	

WP6

In the first 18 months of the project, WP6 focused on further defining the management plan initially described in the Description of Work and executing on this plan in order to drive the project forward according to the plan of record. This work largely consisted of setting up the organizational structure of the project, determining the most effective internal communication strategy for the project partners, establishing the appropriate quality assurance procedures and implementing the tools required for tracking project progress. The result per task were the deliverables D6.1, D6.2, D6.3 and D6.4, as explained in 6-Month Project Report in MS1 and D6.5 and D6.6 in MS2

In this period of the project, WP6 focused on the implementation and refinement of all previously defined processes. All details are explained in 3.3 Project Management during the period.

On a per-task basis, contributions have been as follows:

- T6.3 Technical management progress tracking: The output of this task is in the several meeting minutes generated in all the meetings. The list of meetings is below in section 3.3. Moreover, project risks were closely monitored according to the project policy established and related contingency mitigation actions were prepared. The QA procedure for the submission of all deliverables was established and followed. Some KPI's indicating the success:

    - 18 regular monthly plenary telcos were held
    - 51 per-WP monthly telcos for empowering WP leaders to lead the internal WP coordination
    - 33 specific topic telcos
    - 3 workshops (technical workshop/GA in Barcelona, extraordinary case study driven Workshop / GA in Toulouse, Project Industrial Workshop / Technical / IAB/ GA in Leiden and Noordwijk, in ESA premises)
    - 8 formal F2F meetings in partner premises and 3 F2F held during conferences
    - 3 major dissemination workshops – IAB AURIX Industrial day (Munich, BMW premises), PIW Industrial Workshop (Noordwijk, ESA premises), Final MCC workshop (BSC Premises)
    - QA process for 6 deliverables in M24 + 18 deliverables in M36.

  A refined version of D6.6 was presented in the intermediate review M24, which was accepted after the intermediate reviews. The objectives of the task have been fully fulfilled upon acceptance of this D6.7 progress report and D6.8 final report

- T6.4. Effort and financial tracking. This task as complementary of T6.3 Project Reports.

    - Intermediate interim financial and effort tracking was done in M24 and M29 to check evolution of numbers per partner.
    - Final numbers in M36 and related explanations are included in this report.

  The objectives of the task have been fully fulfilled upon acceptance of D6.7 (progress report) and D6.8 (final report).

The table below will present the consolidated effort spent in the following workpackage and the explanation of the deviations.

	PM (M18)	PM M36	Total Planned (DoW)	Explanation of deviations
BSC	9,67		18,00	
RPT	0,75		1,50	
SYS	0,99		2,00	
UPD	0,75		1,50	
INRIA	0,75		1,50	
CG	0,80		1,50	
AIF	0,60		1,00	
UoY	0,97		2,00	
ADS	0,82		1,50	
IKR	0,85		1,50	
IFX	0,06		0,50	
Total	17,01		32,50	

Summary Table on the use of resources:

	WP1		WP2		WP3		WP4		WP5		WP6		TOTAL	
PARTNER	Actual	Planned	Actual	Planned	Actual	Planned	Actual	Planned	Actual	Planned	Actual	Plan.	Actual	Planned
BSC		92,00		36,00		8,00		7,00		4,00		18,0	0,00	165,00
RPT		6,00		24,00		31,00		11,00		10,00		1,50	0,00	83,50
SYS		3,00		39,00		12,00		1,00		1,00		2,00	0,00	58,00
UPD		2,50		50,00		23,00		9,00		2,00		1,50	0,00	88,00
INRIA		2,00		4,00		55,00		8,00		6,00		1,50	0,00	76,50
AG		39,00		0,00		0,00		0,00		2,00		1,50	0,00	42,50
AIF		1,00		2,00		1,00		18,50		1,00		1,00	0,00	24,50
UoY		3,00		17,50		53,50		8,00		2,00		2,00	0,00	86,00
AST		3,00		1,00		0,00		23,50		1,00		1,50	0,00	30,00
IKR		0,00		14,00		6,00		32,00		3,00		1,50	0,00	56,50
IFX		1,00		0,50		0,00		4,00		0,00		0,50	0,00	6,00
Total		152,50		188,00		189,50		122,00		32,00		32,5	0,00	716,50

Global explanation of per-partner deviations:

	PM (M18)	PM M36	Total Planned (DoW)	Explanation of deviations
BSC	96,46		165,00	
RPT	42,66		83,50	
SYS	20,79		58,00	
UPD	63,00		88,00	
INRIA	29,75		76,50	
CG	22,10		42,50	
AIF	11,25		24,50	
UoY	45,85		86,00	
ADS	8,75		30,00	
IKR	35,85		56,50	
IFX	1,40		6,00	
Total	377,86		716,50	

4.4 Project management during the period

This section summarises management of the consortium activities during the period as indicated in Articles II.2.3 and Article II.16.5 of the Grant Agreement. Project management was done within the Work Package 6 tasks –as described above, consisting of the Coordination and Project Management of the PROXIMA Project, is the shared responsibility of the Project Manager (Xavier Salazar) and the Technical Manager (Francisco J. Cazorla); however, it also includes the active participation of all project partners through the Management Board and the General Assembly, which is integral to the successful management of the project.

- Financial administration

Pre-payment of financial contribution to beneficiaries was distributed at the start of the project as explained in D6.4 progress report. As explained in D6.5 there was an interim tracking of progress in M12. Financial forms for the first period P1 covering the first 18 months of the project and the related PPR's were prepared and presented in M20. Second payment of financial contribution was distributed to the partners' right after the acceptance from European commission of MS2. Payment was distributed according to the cost claim accepted for each of the partners, up to the limits defined in the Grant Agreement (including 10% limit and the guarantee fund).

Moreover, the interim tracking of progress for M24 was presented in the extra review in Brussels, and upon the decision of the General Assembly the expected interim report of M30 was advanced to M29 –to make sure the needed changes in the consortium could be backed financially. INRIA preferred to wait till the end of the project to present the progress numbers due to changes in their support personnel.

- Management and Organizational Structure:

The main change in organizational structure during this period was the change of WP3 Leader following EC recommendation after 3rd Review, due to extra delays detected during the Case Study Driven Workshop in Toulouse. The change of WPLeader was formally voted in a GA meeting – votes were sent anonymously by e-mail by each of General Assembly representatives during the 24th and 25th of February 2016 to a notary subcontracted by BSC.

- Co-ordination activities during the period in question, such as communication between beneficiaries:

During MS1, all communication processes and tools were implemented as explained in D6.4. During MS2 they were expanded to as explained in D6.5. During MS3 communication measures were kept and some further measures had to be introduced, mostly aiming to recover the delays in WP3, mitigate the impact to other WPs and to facilitate the specific challenges of the final part of the project. For that reason, it was decided to hold an extra meeting – a case study driven workshop in Toulouse (premises of Airbus and Airbus Defence and Space). This helped with the integration of the different platform and empowered the end-users to drive the interaction with the other partners. Moreover, a number of specific topic telcos was encouraged by WP6 in order to make sure all those technical discussions and presentations and clarifications which would not fit in regular telcos are covered.

The consortium kept on the regular plenary monthly teleconferences to evaluate progress against project plans, identify major problems and co-ordinate project-related interactions among the WP Leaders and WP Industrial Advisors. The Work Package Leaders provided technical status and were encouraged to hold intra WP- or specific topic additional meetings. Dedicated WP-mailing lists and monthly WP-Telcos were also kept for their internal coordination.

During MS2, there were 3 GA/MB Technical Workshops – in addition to the 3 face to face Workshop meetings in M1 and M6 and M14 - consisting of 2-4 days of technical discussions between the Work Package Leaders, during which a half-day General Assembly meeting was held. These meetings facilitated collaboration among the project partners ensuring that the project has progressed according to the plan of record.

Partners also used the opportunity of common dissemination events to meet face to face (RTSS, HiPEAC. This is a very efficient way to profit both from the fact that dissemination of the project is done and to advance in several inter and intra work package issues.

- The following table lists all meetings in this reporting period:

GENERAL ASSEMBLY / MANAGEMENT BOARD / TECHNICAL MEETINGS			
DATE	**MEETING**	**DURATION**	**LOCATION**
23 April 2015	WP2 Teleconference		Teleconference
23 April 2015	WP4 Teleconference		Teleconference
28 April 2015	Plenary GA/MB/Technical		Teleconference
30 April 2015	WP3 Teleconference		Teleconference
05 May 2015	MCC Telco		Teleconference
06 May 2015	WP4-Case Study Characterization Telco 1		Teleconference
12 May 2015	WP4-Case Study Characterization Telco 2		Teleconference
18 May 2015	WP3 Teleconference		Teleconference
19-21 May 2015	2nd Cluster Review + Rehearsal + MCC Workshop	2,5 days	Milano, Italy
26 May 2015	WP2 Teleconference		Teleconference
27 May 2015	EPC Implementation in RVS Telco		Teleconference
28 May 2015	Plenary GA/MB/Technical		Teleconference
03 June 2015	EPC Requirements		Teleconference
03 June 2015	WP1 FPGA m24 Telco		Teleconference
04 June 2015	WP4-Case Study Characterization Telco 3		Teleconference
04 June 2015	WP2-WP3 Aurix Instrumentation		Teleconference
11 June 2015	EPC Meeting		Teleconference
18 June 2015	WP3 Teleconference		Teleconference
19 June 2015	WP4 Teleconference		Teleconference
25 June 2015	WP2 Teleconference		Teleconference
30 June 2015	Plenary GA/MB/Technical		Teleconference
02 July 2015	Definitions of Dependent		Teleconference

02 July 2015	BSC-IKR Pre-Automotive Telco		Teleconference
16 July 2015	MCC Telco		Teleconference
17 July 2015	WP3 Teleconference		Teleconference
17 July 2015	WP4 Teleconference		Teleconference
21 July 2015	WP2 Teleconference		Teleconference
23 July 2015	Plenary GA/MB/Technical		Teleconference
21 August 2015	WP3 Teleconference		Teleconference
25 August 2015	WP2 Teleconference		Teleconference
25 August 2015	WP4 Teleconference		Teleconference
26 August 2015	Plenary GA/MB/Technical		Teleconference
01 September 2015	MCC Telco		Teleconference
02 September 2015	Certification Approach Teñcp		Teleconference
14 September 2015	D2.8 Telco I		Teleconference
16 September 2015	BSC-CONTREX Meeting	2 days	Barcelona, Spain
22 September 2015	WP4 Teleconference		Teleconference
22 September 2015	WP3-F2F RPT-UoY		York, UK
24 September 2015	D2.8 Telco II		Teleconference
25 September	WP3/WP5-F2F RPT-UoY		York, UK
27-30 September 2015	3rd Workshop GA/MB/Technical Meeting	3,5 days	Barcelona, Spain
15 October 2015	WP2 Teleconference		Teleconference
16 October 2015	WP4 Teleconference		Teleconference
21 October 2015	WP3-D3.4 Telco		Teleconference
21 October 2015	Plenary GA/MB/Technical		Teleconference
27 October 2015	CICI_FPGA_Results Discussion I		Teleconference
30 October 2015	D2.8 Certification Telco III		Teleconference
02 November 2015	WP3 Teleconference		Teleconference
03 November 2015	Case Study CICI Results Discusion II		Teleconference
03 November 2015	MCC Telco		Teleconference
16-17 November 2015	3rd Review & Rehearsal	1,5 days	Brussels, Belgium
20 November 2015	WP3 Teleconference		Teleconference
23 November 2015	WP4 Teleconference		Teleconference
23 November 2015	WP2 Teleconference		Teleconference

25 November 2015	F2F WP3 RPT-UoY		York, UK
25 November 2015	Video Preparation Telco		Teleconference
26 November 2015	Plenary GA/MB/Technical		Teleconference
03 December 2015	F2F UPD-UoY –RTSS Conference		RTSS Conference, San Antonio, USA
10 December 2015	WP2 Teleconference		Teleconference
11 December 2015	WP3 Teleconference		Teleconference
14 December 2015	WP4 Teleconference		Teleconference
15 December 2015	Plenary GA/MB/Technical		Teleconference
08 January 2016	F2F WP3 RPT-UoY		York, UK
10-18 January 2016	BSC-AIF-ADS-Integration Visit in Toulouse	4 days	Toulouse, France
19 January 2016	WP3 Teleconference		Teleconference
20 January 2016	F2F UPD-BSC - HiPEAC Conference		HiPEAC Conference, Prague, Czeck Republic
21 January 2016	WP4 Teleconference		Teleconference
22 January 2016	Plenary GA/MB/Technical		Teleconference
26 January 2016	WP2 Teleconference		Teleconference
7-9 February 2016	Case Study Driven Workshop GA/MB/Technical	2,5 days	Toulouse, France
18 February 2016	WP4 Teleconference		Teleconference
22 February 2016	WP2 Teleconference		Teleconference
23 February 2016	FPGA_VICI_Integration Telco		Teleconference
24 February 2016	GA Teleconference		Teleconference
07 March 2016	WP3 Teleconference		Teleconference
10 March 2016	MCC Telco		Teleconference
March 2016	F2F RPT-UoY – Various Meetings on Aurix Integration		York, UK
15-16 March 2016	F2F RPT-INRIA-UoY	2 days	York, UK
23 March 2016	WP4 Teleconference		Teleconference
23 March 2016	WP2 Teleconference		Teleconference
29 March 2016	Plenary GA/MB/Technical		Teleconference
13 April 2016	EPC Open Issues Telco		Teleconference
14 April 2016	P4080 VICI Analysis Telco		Teleconference
18 April 2016	MBPTA Open Issues Telco		Teleconference
19 April 2016	PROXIMA-TUV Certifiaction Meeting	1 day	Mondragon, Spain
21 April 2016	WP4 Teleconference		Teleconference

22 April 2016	WP2 Teleconference		Teleconference
24 April 2016	Aurix Industrial IAB day	1 day	Munich, Germany
26 April 2016	Plenary GA/MB/Technical		Teleconference
03 May 2016	MCC Telco		Teleconference
13 May 2016	Aurix IAB Telco		Teleconference
17 May 2016	CONCERTO_Telco		Teleconference
19 May 2016	WP4 Teleconference		Teleconference
24 May 2016	1st INRIA Tutorial on (in)dependence		Teleconference
24 May 2016	BSC-ESA- Telco on PIW Logistics		Teleconference
25 May 2016	WP2 Teleconference		Teleconference
27 May 2016	Plenary GA/MB/Technical		Teleconference
13 June 2016	WP3 Teleconference		Teleconference
16 June 2016	2nd INRIA Tutorial on (in)dependence		Teleconference
16 June 2016	WP4 Teleconference		Teleconference
20 June 2016	WP2 Teleconference		Teleconference
23 June 2016	Plenary GA/MB/Technical		Teleconference
27-30 June 2016	PROXIMA Industrial Workshop PIW/IAB/GA/MB/Techical	3,5 days	Leiden & Noordwijk, Holland
04 July 2016	P4080 & Aurix Telco		Teleconference
05 July 2016	MCC Telco		Teleconference
18 July 2016	WP3 Teleconference		Teleconference
21 July 2016	WP4 Teleconference		Teleconference
22 July 2016	WP2 Teleconference		Teleconference
27 July 2016	Plenary GA/MB/Technical		Teleconference
29 July 2016	WP3 Teleconference		Teleconference
29 August 2016	WP4 Teleconference		Teleconference
31 August 2016	Plenary GA/MB/Technical		Teleconference
06 September 2016	MCC Telco		Teleconference
19 September 2016	WP4 Teleconference		Teleconference
26 September 2016	Plenary GA/MB/Technical		Teleconference
21-24 November 2016	Final Cluster Review + MCC Workshop + Rehearsal	3,5 days	Barcelona, Spain

- Other management procedures

After MS1, we have established a risk management procedure in order to better track all those elements that could endanger the correct development of the project. Seeding from risks envisioned in the DoW we established a mechanism for permanent tracking as follows:

- We have general risks register – in our shared folders for all to access
- In any monthly GA/MB telcos. WP leaders / WPIA are encouraged to raise any new risks / or notify any status change of every item, new mitigation action, etc.
- In GA / technical workshops risks a carefully in-depth review is triggered (it has been done in Workshop in Barcelona 2015, Toulouse 2016 and Leiden 2016)
- On the atomic level, we carefully reviewed the list of technical requirements (D6.3) in order to maintain a trace of requirements that are not being satisfied and proposed related to mitigation actions. A refined version of D6.6 v1.2 was presented in m24 in order to cover all the mitigation actions to recover the delays in WP3.

Other management procedures that have been carefully discussed and reviewed during this first period the IPR and publication processes –in order to stimulate partners' exploitation and dissemination of the project results, and therefore ensure PROXIMA project has a maximum impact. Due to this tracking, in order to ensure the IP protection of one of INRIA's technologies INRIA's part of D3.4 has been separated in a separate confidential annex.

- Co-operation with other projects/programmes:

Positive collaboration with other European projects has been pushed in the first 18 month of the project and this trend will continue as PROXIMA technology matures.

- During this period we defined the terms of collaboration with parMERASA on various technical and non-technical issues – further details are in D4.3 "ParMERASA Collaboration Agreement".
- The relation with the FP7 MultiPARTES project has been strengthened by the attendance of the PROXIMA Technical co-ordinator to the MultiPARTES final dissemination event.
- In the last FP7 P-SOCRATES project workshop celebrated in Zurich, probabilistic timing analysis concepts developed in PROXIMA where discussed and pushed by BSC (partner in both P-SOCRATES and PROXIMA projects) to be incorporated as a research line in the P-SOCRATES roadmap. Although this discussion is in an early state, we expect to increase the collaboration in the near future.
- Several joint cluster workshops have been organized with the DREAMS and CONTREX IP projects.
    - We held a workshop as part of the first cluster review in Brussels in June 2014
    - During the DATE Conference the MCC cluster organized a joint Workshop in March 2014
    - In January 2015, the MCC organized joint workshop as part of the HiPEAC conference in Amsterdam.
    - In January 2015, PROXIMA was presented to the TACLe COST action which brings togeter
    - During the Co-Summit 2015 Event the MCC prepared an MCC booth that help reaching other European projects in the area.
    - In addition, MCC Telcos are organized every 2 months in order to coordinate all cluster activities.

These events have enabled discussion between the projects and promote results to external research and industrial partners.

Relation with other Research Programmes (other than the CONCERTO project, which is discussed earlier in this report):

- H2020 SAFEPOWER - IK4-IKERLAN has been coordinating the project since January 2016, as a continuation on the work performed in PROXIMA on the certification, multicore and mixed-criticality domain and which opened a new research path for IK4-IKERLAN.
- BGLE DEPARTS – French funded project that has INRIA as partner. INRIA extends its EVT methodology against rare events simulators used for automotive industry.
- LEOC Capacites – French funded project that has INRIA and Airbus as partners. INRIA tests its EVT methodology on different use cases from avionics and space.
- ESA P4S - An ESA funded research project that is looking to exploit Probabilistic Timing Analysis Technology and Scheduling of Multi-Core applications. The PROXIMA participants Rapita, BSC, Cobham Gaisler and UPD and Airbus Defense and Space are all partners in this project.
- ESA MoSATT-CMP - An ESA funded research project that is looking to establish a novel design framework and a set of recommendations for the design of real-time applications on high-performance multi-cores, with specific focus on spacecraft systems. Rapita is providing specialist timing analysis support to this project. Cobham Gaisler are providing hardware platforms and expertise.
- FUI Waruna - French industry-oriented funded project with Inria as partner. This project looks into integration of probabilistic description for model-driven approaches with an intended integration in the POLARSYS framework and the Thales toolchain.
- FUI Céos - French industry-oriented funded project with Inria as scientific leader and Thales industry leader (with Sysgo as sub-contracting). This project uses the probabilistic approaches as an interface between communicating systems with different time criticalities.

5 Deliverables and milestones tables

5.1 Deliverables

TABLE 1. DELIVERABLES										
Del. no.	Deliverable name	Version	WP no.	Lead beneficiary	*Nature*	Dissemination level[5]	Delivery date from Annex I (proj month)	Actual / Forecast delivery date	Status No submitted/ Submitted	Comments
D1.1	Multicore processor requirements	1	WP1	AG	R	RE*/PU	6	31/03/ 2013	submitted	Accepted
D1.2	Manycore processor requirements	1	WP1	BSC	R	RE*/PU	6	31/03/ 2013	Submitted	Accepted
D1.3	COTS Multicore board requirements	1	WP1	BSC	R	RE*/PU	6	31/03/ 2014	Submitted	Accepted

[5] **PU** = Public

PP = Restricted to other programme participants (including the Commission Services).

RE = Restricted to a group specified by the consortium (including the Commission Services).

CO = Confidential, only for members of the consortium (including the Commission Services).

Make sure that you are using the correct following label when your project has classified deliverables.

EU restricted = Classified with the mention of the classification level restricted "EU Restricted"

EU confidential = Classified with the mention of the classification level confidential " EU Confidential "

EU secret = Classified with the mention of the classification level secret "EU Secret "

D1.4	PROXIMA baseline multicore FPGA	1	WP1	AG	P	RE	6	31/03/ 2014	Submitted	Accepted
D1.5	PROXIMA baseline simulator	1	WP1	BSC	P	RE	6	31/03/ 2014	Submitted	Accepted
D1.6	PROXIMA Baseline COTS Multicore	1	WP1	BSC	P	RE	6	31/03/ 2014	Submitted	Accepted
D1.7	Multicore partially PTA-conformant processor designs on FPGA	1	WP1	AG	P+R	RE*/PU	18	31/03/ 2015	Submitted	Accepted
D1.8	Manycore partially PTA-conformant processor designs	1	WP1	BSC	P+R	RE*/PU	18	31/03/ 2015	Submitted	Accepted
D1.9	Initial multi- and manycore processor with COTS-features	1	WP1	BSC	R	RE*/PU	18	31/03/ 2015	Submitted	Accepted
D1.10	Final multi- and manycore processor with COTS-features designs		WP1	BSC	R	RE*/PU	36	31/09/ 2016	Submitted	
D1.11	Refined multicore PTA-conformant processor designs on FPGA		WP1	AG	P+R	RE*/PU	36	31/09/ 2016	Submitted	
D1.12	Refined manycore PTA-conformant processor designs		WP1	BSC	P+R	RE*/PU	36	31/09/ 2016	Submitted	
D2.1	Interim user manual for the RTOS	1	WP2	SYS	R	RE*/PU	6	31/03/	Submitted	Accepted

	baselines to be used in the industrial case studies							2014		
D2.2	Design report of the proposed PTA-support system software features	1	WP2	UPD	R	RE	6	31/03/ 2014	Submitted	Accepted
D2.3	Certification needs in the target industrial domains	1	WP2	IKR	R	PU	6	31/03/ 2014	Submitted	Accepted
D2.4	Initial designs of the innovative RTOS features for manycore processors	1	WP2	UoY and UPD	R	PU	12	31/10/ 2014	Submitted	Accepted
D2.5	Design of the innovative RTOS features for manycores (with evaluations)	1	WP2	UPD	P+R	PU	18	31/03/ 2015	Submitted	Owner was UoY, and was transferred to UPD Accepted
D2.6	Lessons learned from industrial case studies (initial capture)	1	WP2	UPD	R	RE	18	31/03/ 2015	Submitted	Accepted
D2.7	Analysis of benchmark-based evaluation for COTS multicore solutions	1	WP2	BSC	R	PU	18	31/03/ 2015	Submitted	Accepted
D2.8	Preliminary certification safety arguments	1	WP2	IKR	R	PU	18	31/03/ 2015	Submitted	Accepted

D2.9	Certification approach supported by DREAMS and PROXIMA	1	WP2	IKR	R	PU	18	31/03/ 2015	Submitted	Accepted
D2.10	Consolidated designs of the innovative RTOS features for manycores (with evaluations)		WP2	UPD	P+R	PU	36	31/09/ 2016	Submitted	
D2.11	Final user manual for the industry-ready RTOS multicore solutions		WP2	SYS	P+R	PU	36	31/09/ 2016	Submitted	
D2.12	Evaluation report on research-oriented software-only multicore solutions		WP2	BSC	P+R	PU	36	31/09/ 2016	Submitted	
D2.13	Consolidated certification arguments		WP2	IKR	R	PU	36	31/09/ 2016	Submitted	
D3.1	Report on abstract models	1	WP3	UPD	R	PU	6	31/03/ 2014	Submitted	Accepted
D3.2	Initial industrial analysis tools.	1	WP3	RPT	P+R	RE	6	31/03/ 2014	Submitted	Accepted
D3.3	PROARTIS achievements summary	1	WP3	INRIA	R	RE	6	31/03/ 2014	Submitted	Accepted
D3.4	Interim report on probabilistic analysis for mixed criticality	3	WP3	INRIA	R	PU	18	30/06/ 2016	Submitted	Accepted

	on multicore.									
D3.5	Interim report on probabilistic analysis for mixed criticality on manycore.	2	WP3	UoY	R	PU	18	30/10/ 2015	Submitted	Accepted
D3.6	Interim industrial analysis tools.	1	WP3	RPT	P+R	PU	18	31/03/ 2015	Submitted	Accepted
D3.7	Initial report for integration tool time checker	1	WP3	SYS	P+R	RE	18	31/03/ 2015	Submitted	Accepted
D3.8	Final report on probabilistic analysis for mixed criticality on multicore.		WP3	INRIA	R	PU	36	31/09/ 2016	Submitted	
D3.9.	Final report on probabilistic analysis for mixed criticality on manycore		WP3	UoY	R	PU	36	31/09/ 2016	Submitted	
D3.10	Analysis lessons learnt from the case studies		WP3	UoY	R	PU	36	31/09/ 2016	Submitted	
D3.11	Final industrial analysis tools.		WP3	RPT	R+P	RE	36	31/09/ 2016	Submitted	
D4.1	Case studies application requirements	1	WP4	AIF	R	RE	6	31/03/ 2014	Submitted	Accepted
D4.2	Terms of Reference of IAB participation	1	WP4	RPT	R	RE	6	31/03/ 2014	Submitted	Accepted

D4.3	Collaboration agreement with parMERASA	1	WP4	BSC	R	RE	6	31/03/ 2014	Submitted	Accepted
D4.4	Interim Case Studies	1	WP4	AST	R	RE	18	31/03/ 2015	Submitted	Accepted
D4.5	Interim case studies experiments results	1	WP4	AST	R	RE	18	31/03/ 2015	Submitted	Accepted
D4.6	Specification of the IAB case studies	1	WP4	RPT	R	RE	18	31/03/ 2015	Submitted	Accepted
D4.7	Final definition of State of Play in the use of Multicores in Real-Time Industry	2	WP4	IFX	R	PU	18	30/10/ 2015	Submitted	Accepted
D4.8	Final case studies experiments results		WP4	AIF	R	RE	36	31/09/ 2016	Submitted	
D4.9	Report on the results of familiarization case studies		WP4	RPT	R	RE	36	31/09/ 2016	Submitted	
D5.1	Dissemination strategy	1	WP5	RPT	R	CO	4	31/01/ 2014	Submitted	Accepted
D5.2	Project Public Website	1	WP5	BSC	O	PU	6	31/03/ 2014	Submitted	Accepted
D5.3	Dissemination Tools	1	WP5	RPT	O	PU	6	31/03/ 2014	Submitted	Accepted
D5.4	Initial Press Release	1	WP5	RPT	R	PU	6	31/03/ 2014	Submitted	Accepted

D5.5	Initial Exploitation Strategy	1	WP5	RPT	R	CO	6	31/03/ 2014	Submitted	Accepted
D5.6	Period 1 Dissemination and Use Report	2	WP5	INRIA	R	CO	18	31/10/ 2015	Submitted	Accepted
D5.7	Market Trend Analysis	1	WP5	RPT	R	PU	18	31/03/ 2015	Submitted	Accepted
D5.8	Tutorials and Training	1	WP5	BSC	R	RE	24	30/09/ 2015	Submitted	Accepted
D5.9	Period 2 Dissemination and Use Report		WP5	INRIA	R	CO	36	30/09/ 2016	Submitted	
D5.10	Technology Transfer and Exploitation Strategy		WP5	RPT	R	CO	36	30/09/ 2016	Submitted	
D 6.1	Project portal	1	WP6	BSC	O	RE	2	30/11/ 2013	Submitted	Accepted
D6.2	Project Management Handbook	1	WP6	BSC	R	PU	4	31/01/ 2014	Submitted	Accepted
D6.3	Project Requirements and Success Criteria	1	WP6	BSC	R	PU	6	31/03/ 2014	Submitted	Accepted
D6.4	6-Month Project Report	1	WP6	BSC	R	PU	6	31/03/ 2014	Submitted	Accepted
D6.5	Period 1 Project Report	1	WP6	BSC	R	PU	18	31/03/ 2015	Submitted	Accepted
D6.6	Refined Requirements and	1	WP6	BSC	R	PU	18	31/03/	Submitted	Accepted

	Success Criteria							2015		
D6.7	Period 2 Project Report		WP6	BSC	R	PU	36	30/09/ 2016	Submitted	
D6.8	Final Report		WP6	BSC	R	PU	36	30/09/ 2016	Submitted	

5.2 Milestones

The table of milestones as specified in Annex I to the Grant Agreement is cumulative, which means that it should always show all milestones from the beginning of the project.

TABLE 2. MILESTONES	

Milestone no.	Milestone name	Work package no	Lead beneficiary	Delivery date from Annex I dd/mm/yyyy	Achieved Yes/No	Actual forecast	Comments
MS1	Overall research objectives defined, research and development infrastructures established, requirements identified and success criteria defined	WP1, WP2, WP3, WP4	**BSC**	**M6**	**Yes**	**N/A**	By this Milestone, the detailed research and development objectives of PROXIMA have been defined, and the requirements for the tool-chain infrastructure, on which we base the PROXIMA developments, identified. Thus, the complete experimental baseline tool-chain and corresponding requirements has also been defined. The tool-chain includes the multicore FPGA, the manycore simulator, the COTS board, software randomisation tools, the RTOS layers and tools, and tracing and timing analysis tools. Case study applications and kernels will also be identified, along with the main certification requirements, standards and safety techniques of the target industrial domains associated with them. Finally, the metrics to measure the success criteria of the different PROXIMA platforms (based on multicore FPGA, COTS hardware and manycore simulator) have also been defined. This Milestone is achieved through deliverables D1.1, D1.2, D1.3, D1.4, D1.5, D1.6; D2.1, D2.2, D2.3; D3.1, D3.2, D3.3; D4.1, D4.2 and D4.3.

MS2	Initial integrated PROXIMA platforms, some case study application components and kernels ported, and early results obtained on these kernels/benchmarks for the multicore platforms	WP1, WP2, WP3, WP4	**BSC**	**M18**	**Yes**	**N/A**	By Ms2 a) release of a first version of the PROXIMA execution stack for the FPGA multicore processors for the scenario in which contending cores inject constant interference; b) the release of a partial version of the tool chain for the AURIX multicore processor; and c) the release of a preliminary version of the manycore platform, ready for initial integration with the software execution stack and associated tool chain. For the COTS multiprocessors instead, starting with the AURIX, initial software-only solutions have been developed to help achieve PTA conformance. The RTOS and run-time libraries for those platforms also include support for data tracing that feeds the PROXIMA timing analysis tools, so that meaningful observation data can be produced for all runs. Experiments for timing characterization of the FPGA and the AURIX platforms, which use the concept of "PROXIMA Application Kernel", were carried out (almost to completion for the FPGA, only initially for the AURIX), which also served the purpose of consolidating the respective toolchains. The domain specific mixed-criticality applications on avionics, space and railway have been ported to the PROXIMA environment and these are ready for the following case-study experimentation phase. The experience gained in the work to MS2 will be the basis for the construction of certification arguments (equipped with a description of the safety techniques/measures associated to PTA) applicable to the industrial domains of interest. This effort will build on an initial set of certification arguments already constructed for the Railway domain against a cross-domain safety standard, and sustained in the face of a certification authority. This Milestone is achieved through deliverables: D1.7, D1.8, D1.9, D2.4, D2.5, D2.6, D2.7, D2.8, D2.9, D3.4, D3.5, D3.6, D3.7; D4.4, D4.5, D4.6 and D4.7.

MS3	Optimised PROXIMA platforms, full set of results for case studies and kernels, and certification arguments for PROXIMA technology	WP1, WP2, WP3, WP4	**BSC**	**M36**	**Yes**	**N/A**	The result of the work for MS3 is achieved through the presented D1.10, D.1.11, D1.12, D2.10, D.2.11, D2.12, D2.13, D3.8, D3.9, D3.10, D.3.11, D.4.8, D.4.9, D5.9, D5.10, D.6.7 and D.6.8

6 Explanation of the use of the resources and financial statements

Financial statements have to be provided within the Forms C for each beneficiary together with an "Explanation of use of resources" requested in the Grant Agreement for personnel costs, subcontracting, any major costs (ex: purchase of important equipment, travel costs, large consumable items) and indirect costs, to be done within the Forms to be uploaded in the Participant Portal[6]. Since the participant's portal is closed yet for that, our internal tracking tables have been pasted below.

As well, same as with effort numbers since this deliverable has to be submitted at month 36 (instead of 60 days after as usual progress reports) numbers are not final and may be adjusted as they are presented in the review.

[6] In the past, the explanation of use of resources requested in the Grant Agreement was done within a table in this section. The merge of this table within the Forms C was a measure of simplification aimed at avoiding duplication and/or potential discrepancies between the data provided in the table 'Explanation of use of resources' and the data provided in the Forms C.