- About
- Courses
- Seminar DVDs
- Partners
- Contact
- Booking

DIDACTIC SEMINARS

The seminars and lab exercises below are available for download by filling in this form.
This agreement allows you to use the IDESA tutorials in your academic program and prohibits commercial use. By requesting access you agree to conform to the conditions of use mentioned above.

SEMINARS

1	Low Power Digital Design in Sub-90nm CMOS Technologies by Wim De Haene (KULeuven)	1 2 3	325Mb
2	Component matching: best practices and fundamental limits by Marcel Pelgrom and Maarten Vertregt (NXP Research)	1 2 3 4	284Mb
3	Automotive Interferences: EMC and Transients by Herman Casier	1 2	300MB
4	Reliability of future advanced CMOS circuits and technologies by Guido Groeseneken (IMEC)	1 2 3	286MB
5	Two important transistor innovations: strained silicon and FinFETs by Geert Eneman - Nadine Collaert (IMEC)	1 2 3	555MB
6	Risk free, 65 nm and beyond, digital low power design by François Thomas (Cadence)	1 2	334MB
7	Variability Aware Modeling and Yield Aspects by Bart Dierickx (IMEC)	1 2	244MB
8	Variability and Litho-aware digital implementation by François Thomas (Cadence)	1 2	230MB
9	Leakage physics and modeling by Wieslaw Kuzmicz (Warsaw University of Technology)	1 2	159MB
10	Techniques to control leakage power at technology and device level : application to a fully power aware SoC design by Edith Beigné (CEA)	1 2	277MB
11	Compact models for DSM by Christian Enz (EPFL)	1 2	260MB
12	Statistical Static Timing Analysis and Optimization - François Thomas (Cadence)	1 2	174MB
13	CMOS front-end design at millimetre wave frequencies - Alexandre Siligaris (CEA LETI)	1 2	236MB
14	Analog design in scaled technologies - Andrea Baschirotto (University of Lecce)	1 2	261MB
15	Design of ADC in advanced technologies - Andrea Baschirotto (University of Lecce)	1 2	286MB
16	Design of analog filters in advanced technologies - Andrea Baschirotto (University of Lecce)	1 2	251MB
17	Low power CMOS 65 and 45 nm industrial technologies - Thomas Skotnicki (STMicroelectronics)	1 2	329MB
18	ESD and Latchup - Fabrice Blanc (ARM)	1 2	270MB
19	DFT to meet Nanometer Test Challenges - Philippe Rossant (Synopsys)	1 2	260MB
20	Ultra-low Voltage Analog Circuit Design - Christian Enz (CSEM SA, Neuchatel - EPFL, Lausanne)	1 2	343MB
21	Advanced circuit design in ermerging 2D & 3D SOI technologies - Thierry Poiroux (CEA LETI)	1	135MB
22	SOI and multiple gate transistors - Thierry Poiroux (CEA LETI)	1	88MB
23	Thermal issues in nanoscale VLSI devices and circuits - Nicolo Rinaldi (University of Naples)	1 2 3 4	357MB

24	Statistical Memory Analysis for robust SRAM design - Paul Zuber, Petr Dobrovolny (imec)	1 2	526MB
25	Metric Driven Verification - Hans Zander (Cadence)	1	360MB
26	Assertion-based verification - Kawe Fatouhi (Cadence)	1	1.4GB
27	A guided tour of the Interconnect road map from 90 nm down to 32 nm designs in the analog and digital domains - Roberto Suaya	1 2 3	242MB
28	Electrostatic discharge protection for DSM RF circuits - Dimitri Linten	1 2	190MB
29	Fundamentals of digitally-assisted RF - Robert Staszewski	1 2 3	249MB
30	SOC in 65 nm and below. Concepts, design, implementation and application - Fabien Clermidy, CEA-LETI	1	247MB
31	Heterogeneous Design - Nicolas Delorme, Asygn	1 2	235MB
32	Millimeter-wave Design in Silicon Technologies - Didier Belot (STMicroelectronics)	1 2	261MB
33	CMOS Radio Wave Design for MM-Wave applications - Piet Wambacq	1 2	260MB
34	Nonlinear distortion analysis in circuits and systems - Prof. dr. ir. Gerd Vandersteen – Dr. ir. Ludwig De Locht (Vrije Universiteit Brussel)	1 2 3 4	331MB
35	On-chip Passive Components and Deep Submicron RF IC Design - John R. Long (Delft University of Technology)	1 2	244MB
36	Integrated LC oscillators - Pietro Andreani (EIT)	1 2	235MB

LAB EXERCISES

Analog Design in scaled technologies (A. Baschirotto – Univ. Milan-Bicocca, S. D'Amico - Univ. Salento)

Leakage physics and modeling (Wieslaw Kuzmicz - Warsaw University of Technology)

CMOS Physics using MASTAR (Thomas Skotnicki - STMicroelectronics)