SEVENTH FRAMEWORK PROGRAMME
Call FP7-ICT-2009-4 Objective ICT-2009.8.1
[FET Proactive 1: Concurrent Tera-device Computing]

Project acronym: **EURETILE**
Project full title: **European Reference Tiled Architecture Experiment**
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WP9 – Training, Exploitation and Dissemination
D9.1 – First Report on Training, Exploitation and Dissemination

Lead contractor for deliverable: INFN
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Dissemination Level: CO	
PU	Public
PP	Restricted to other programme participants (including the Commission Services)
RE	Restricted to a group specified by the consortium (including the Commission Services)
CO	Confidential, only for members of the consortium (including the Commission Services)

Table of Contents

This is the first deliverable of WP9, therefore we present results obtained in 2010 and 2011. During this period, this Workpackage produced two main results:

- A set of publications and presentations describing the EURETILE results, listed by the first sections of this document;
- the CASTNESS'11 workshop (Roma, 17-18 January 2011). Twenty speakers, representing the four Teradevice Computing projects (EURETILE, TERAFLUX, TRAMS and SooS) presented their activities to about 60 researchers. The last section of this document details the lists of presentations and participants.

1. Presentations

ETHZ

- Iuliana Bacivarov, Thermal-Aware Design of Real-Time Multi-Core Embedded Systems, Invited talk at Mapping Applications to MPSoCs, Jun. 2011.
- Iuliana Bacivarov, Temperature Predictability in Multi-Core Real-Time Systems, Invited talk at DAC Workshop on Multiprocessor System-on-Chip for Cyber Physical Systems: Programmability, Run-Time Support, and Hardware Platforms for High Performance Embedded Applications, Jun. 2011.
- Iuliana Bacivarov, Distributed Application Layer – Towards Seamless Programming of Many-Tile Architectures, CASTNESS 2011, 17 and 18 January 2011, Rome, Italy,http://euretile.roma1.infn.it/mediawiki/img_auth.php/8/88/EURETILE-2-IulianaBacivarov.pdf.
- Iuliana Bacivarov, Distributed Operation Layer: An Efficient and Predictable KPN-Based Design Flow, invited talk at Workshop on Compiler-Assisted System-On-Chip Assembly 2010, in conjunction with Embedded Systems Week, Scottsdale, AZ, US, October 2010, http://www12.cs.fau.de/ws/casa10.
- Iuliana Bacivarov, Efficient Execution of Kahn Process Networks on CELL BE, invited talk at Summer School on Models for Embedded Signal Processing Systems at Lorentz Center, Leiden, Netherlands, 30 Aug - 3 Sep 2010, http://www.lorentzcenter.nl/lc/web/2010/427/presentations/Iuliana-cell.pdf.
- Iuliana Bacivarov, Distributed Operation Layer: A Practical Perspective, tutorial at Summer School on Models for Embedded Signal Processing Systems at Lorentz Center, Leiden, Netherlands, 30 Aug - 3 Sep 2010, http://www.lorentzcenter.nl/lc/web/2010/427/presentations/Iuliana-demo.pdf.

- Iuliana Bacivarov, Distributed Operation Layer: Efficient Design Space Exploration of Scalable MPSoC, invited talk at Combinatorial Optimization for Embedded System Design workshop 2010 in conjunction with CPAIOR2010, 7th International Conference on Integration of Artificial Intelligence and Operations Research techniques in Constraint Programming, Bologna, Italy, June 2010, http://www.artist-embedded.org/artist/Overview,2022.html.
- Iuliana Bacivarov, invited talk at Efficient Execution of Kahn Process Networks on MPSoC, Mapping Applications to MPSoCs 2010, June 29-30, 2010, St. Goar, Germany, http://www.artist-embedded.org/artist/Program,1822.html.

RWTH

- Jovana Jovic, Simulation Challenges in the EURETILE Project, CASTNESS 2011, January 17-18, 2011, Rome, Italy
- Special session at DATE 2011: Virtual Manycore Platforms: Moving Towards 100+ Processor Cores, organized by R. Leupers and G. Martin
- R. Leupers, H. Meyr: Embedded Processor Design, Block lecture, ALARI, Lugano, Feb 2011
- ICT Technology Transfer Workshop targeting Horizon 2020, Brussels, Apr 2011, organized by R. Leupers
- S. Yakoushkin: Advanced Simulation Techniques, Joint RWTH/TU Tampere Seminar, June 2011
- R. Leupers: SoC Design Research in the UMIC Excellence Cluster, Seminar, TU Berlin, Sep 2011
- Juan Eusse: Hybrid Simulation Technology for Extensible Cores and Full System Simulation of Complex MPSoCs, Nov 2011 (Presentation at HiPEAC Computing Systems Week)
- Rainer Leupers, HiPEAC Cluster Meeting (Design and Simulation Cluster), October 2010, Barcelona, Spain
- Rainer Leupers, MPSoC Design for Wireless Multimedia, Tutorial, MIXDES, June 2010, Wroclaw, Poland
- Rainer Leupers, Cool MPSoC Design, ASCI Winter School on Embedded Systems, March 2010, Soesterburg, Netherlands
- Rainer Leupers, Design Technologies for Wireless Systems-On-Chip, Huawei ESL Symposium, September 2010, Shenzhen, People's Republic of China
- Rainer Leupers, Embedded Procesor Design and Implementation, course in MSc in Embedded Systems track at ALaRI Institute, March 1-4, 2010, University of Lugano, Switzerland
- Stefan Kraemer, Advanced Simulation Techniques for Virtual Platforms, May 26, 2010, Imperial College London, London, United Kingdom
- Christoph Schumacher, Stefan Kraemer and Rainer Leupers, demonstration at DAC 2010 exhibition: parSC: parallel SystemC simulation, deterministic, accurate, fast, June 14-16, 2010, Anaheim, USA
- Christoph Schumacher, Virtual Platform Technologies for Multi-core Platforms, UMIC Day, 19 October, 2010, RWTH Aachen

INFN

- P. Vicini, QUonG: A GPU-based HPC System Dedicated to LQCD Computing - Symposium on Application Accelerators in High-Performance Computing, Knoxville, TN - USA, July 2011http://doi.ieeecomputersociety.org/10.1109/SAAHPC.2011.15
- D. Rossetti, Remote Direct Memory Access between NVIDIA GPUs with the APEnet 3D Torus Interconnect - SC11 - International Conference for High Performance Computing, Networking, Storage and Analysis - Seattle, WA http://nvidia.fullviewmedia.com/fb/nv-sc11/tabscontent/archive/304-wed-rossetti.html
- P.S. Paolucci, EURETILE: Brain-Inspired many-tile SW/HW Experiment, CASTNESS 2011, 17 and 18 January 2011, Rome, Italy,http://euretile.roma1.infn.it/mediawiki/img_auth.php/3/3a/EURETILE-1-PierStanislaoPaolucci.pdf
- P. Vicini, EURETILE: The HPC and Embedded Experimental HW Platform, CASTNESS 2011, 17 and 18 January 2011, Rome, Italy,http://euretile.roma1.infn.it/mediawiki/img_auth.php/6/69/EURETILE-6-PieroVicini.ppt
- R. Ammendola, apeNET+: a 3D toroidal network enabling petaFLOPS scale Lattice QCD simulations on commodity clusters, Lattice 2010, THE XXVIII INTERNATIONAL SYMPOSIUM ON LATTICE FIELD THEORY, Villasimius, Italy, June 2010, http://agenda.infn.it/contributionDisplay.py?contribId=335&sessionId=70&confId=2128
- D. Rossetti, apeNET+ Project Status, Lattice 2010, THE XXIX INTERNATIONAL SYMPOSIUM ON LATTICE FIELD THEORY, Squaw Village, Lake Tahoe, CA, USA, July 2011 - to be published on https://latt11.llnl.gov/html/proceedings.php

Target

- W. Geurts, G. Goossens, "Ideas for the Design of an ASIP for LQCD", CASTNESS 2011, Rome (Italy), January 17-18, 2011,http://euretile.roma1.infn.it/mediawiki/img_auth.php/3/3c/EURETILE-5-WernerGeurts.ppt
- G. Goossens, “Why Compilation Tools are the Catalyst for Multicore SoC Design”, Electronic Design and Solutions Fair, Yokohama (Japan), January 27-28, 2011.
- G. Goossens, “Why Compilation Tools are a Catalyst for Multicore SoC Design”, Third Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Design Automation and Test in Europe (DATE-2011), Grenoble (France), March 18, 2011.
- G. Goossens, P. Verbist, “Enabling the Design and Programming of Application-Specific Processors”, Sophia-Antipolis Micro-Electronics Conference (SAME-2011), Sophia-Antipolis (France), October 12-13, 2011.
- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Electronic Design and Solutions Fair, Yokohama (Japan), November 16-18, 2011.
- P. Verbist, “Building software-programmable accelerators for ARM-based subsystems”, ARM Technical Symposium, Taipei and Hsinchu (Taiwan), November 17-18, 2011.

- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Intl. Conf. on IP-Based SoC Design (IP-SoC-2011), Grenoble (France), December 7-8, 2011.
- G. Goossens, “Design Tools for Building Software-Programmable Accelerators in Multicore SoCs”, Workshop on Tools for Embedded System Design, Sint-Michielsgestel (Netherlands), December 13, 2011.
- G. Goossens, E. Brockmeyer, W. Geurts, “Application-Specific Instruction-set Processors (ASIPs) and related design tools for tiled systems”, CASTNESS 2012, Paris (France), January 26, 2012.
- G. Goossens, "How ASIP Technology can Make your RTL Blocks More Flexible", Electronic Design and Solutions Fair, Yokohama (Japan), January 28-29, 2010.
- S. Cox, G. Goossens, "Hardware Accelerator Performance in a Programmable Context: Methodology and Case Study", Embedded Systems Conference, San Jose (CA, USA), April 26-29, 2010.
- G. Goossens, "Design of Programmable Accelerators for Multicore SoCs", First Artemis Technology Conference, Budapest (Hungary), June 29-30, 2010.

2. Papers - Posters - Technical Press – Newsletters

ETHZ

- K. Huang, W. Haid, I. Bacivarov, M. Keller, L. Thiele. Embedding Formal Performance Analysis into the Design Cycle of MPSoCs for Real-time Streaming Applications. ACM Transactions in Embedded Computing Systems (TECS Journal), ACM, 2012.
- L. Schor, I. Bacivarov, H. Yang, and L. Thiele. Worst-Case Temperature Guarantees for Real-Time Applications on Multi-Core Systems. Proc. IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Apr. 2012.
- P. Kumar, J.-J. Chen, and L. Thiele. Demand Bound Server: Generalized Resource Reservation for Hard Real-Time Systems. Proc. Int'l Conference on Embedded Software (EMSOFT), pages 233-242, Oct. 2011.
- L. Schor, H. Yang, I. Bacivarov, and L. Thiele. Worst-Case Temperature Analysis for Different Resource Availabilities: A Case Study. Proc. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Lecture Notes on Computer Science (LNCS), Springer, Vol. 6951, pages 288-297, Sep. 2011.
- P. Kumar, J.-J. Chen, L. Thiele, A. Schranzhofer, and G. C. Buttazzo. Real-Time Analysis of Servers for General Job Arrivals. Proc. Intl. Conf. on Embedded and Real-Time Computing Systems and Applications (RTCSA), pages 251-258, Aug. 2011.
- L. Thiele, L. Schor, H. Yang, and I. Bacivarov. Thermal-Aware System Analysis and Software Synthesis for Embedded Multi-Processors. Proc. Design Automation Conference (DAC), pages 268-273, Jun. 2011.
- D. Rai, H. Yang, I. Bacivarov, JJ. Chen, L. Thiele. Worst-Case Temperature Analysis for Real-Time Systems. In Proceedings of Design, Automation and Test in Europe (DATE), Grenoble, France, March 2011.

- S. Perathoner, K. Lampka, L. Thiele. Composing Heterogeneous Components for System-wide Performance Analysis. In Proceedings of Design, Automation and Test in Europe (DATE), Grenoble, France, March 2011 (invited paper).
- Bacivarov, H. Yang, L. Schor, D. Rai, S. Jha, L. Thiele, Poster: Distributed Application Layer - Towards Efficient and Reliable Programming of Many-Tile Architectures. Design, Automation and Test in Europe (DATE) Friday Workshop, Grenoble, France, March 2011.
- K. Huang, L. Santinelli, JJ. Chen, L. Thiele, and G. C. Buttazzo. Applying Real-Time Interface and Calculus for Dynamic Power Management in Hard Real-Time Systems. Real-Time Systems Journal, Springer Netherlands, Vol. 47, No. 2, pages 163-193, Mar. 2011.
- Schranzhofer, JJ. Chen, L. Thiele. Dynamic Power-Aware Mapping of Applications onto Heterogeneous MPSoC Platforms. IEEE Transactions on Industrial Informatics, IEEE, Vol. 6, No. 4, pages 692 -707, November, 2010.

RWTH

- S. Kraemer, Design and analysis of efficient MPSoC simulation techniques, dissertation, 2011, Aachen, Germany (http://darwin.bth.rwth-aachen.de/opus3/frontdoor.php?source_opus=3769&la=de)
- J. Castrillon, A. Shah, L. Murillo, R. Leupers, G. Ascheid: Backend for Virtual Platforms with Hardware Scheduler in the MAPS Framework, 2nd IEEE Latin America Symp. on Circuits and Systems, Feb 2011, Bogota (Colombia)
- R. Leupers, G. Martin, N. Topham, L. Eeckhout, F. Schirrmeister, X. Chen: Virtual Manycore Platforms: Moving Towards 100+ Processor Cores, Design Automation & Test in Europe (DATE), Mar 2011, Grenoble (France)
- L. Murillo, W. Zhou, J. Eusse, R. Leupers, G. Ascheid: Debugging Concurrent MPSoC Software with Bug Pattern Descriptions, System, Software, SoC and Silicon Debug Conference (S4D), Oct 2011, Munich (Germany)
- S. Kraemer, R. Leupers, D. Petras, T. Philipp, A. Hoffmann: Checkpointing SystemC-Based Virtual Platforms, International Journal of Embedded and Real-Time Communication Systems (IJERTCS), vol. 2, no. 4, 2011
- J. Jovic, S. Yakoushkin, L. Murillo, J. Eusse, R. Leupers and G. Ascheid: Hybrid Simulation for Extensible Processor Cores, Design, Automation and Test in Europe (DATE '12), accepted for publication
- Schumacher, R. Leupers, D. Petras and A. Hoffmann. parSC: Synchronous Parallel SystemC Simulation on Multi-Core Host Architectures. In proceedings of CODES/ISSS '10, October, 2010, Scottsdale, Arizona, USA (http://dx.doi.org/10.1145/1878961.1879005)

TIMA

- Chagoya-Garzon, N. Poste, F. Rousseau, Semi-Automation of Configuration Files Generation for Heterogeneous Multi-Tile Systems, Computer Software and Application Conference (COMPSAC 2011), Munich, Germany, 18-21 July 2011.
- H. Chen, G. Godet-Bar, F. Rousseau, F. Petrot, Me3D : A Model-driven Methodology expediting Embedded Device Driver Development, International Symposium on Rapid System Prototyping (IEEE RSP 2011), pp. 171-177, May 2011, Karlshrue, Germany.

INFN

- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto, Piero Vicini - QUonG: A GPU-based HPC System Dedicated to LQCD Computing - Application Accelerators in High-Performance Computing, Symposium on, pp. 113-122, 2011 Symposium on Application Accelerators in High-Performance Computing, 2011 [[1]]
- Pier Stanislao Paolucci - FP7 EURETILE Project: EUropean REference TILed architecture Experiment - HipeacInfo, Quarterly Newsletter, Number 24, page 11, October 2010 (http://www.Hipeac.net/newsletter) File:PaolucciEuretileHipeacInfo24October2010.pdf
- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Paolucci, Roberto Petronzio, Davide Rossetti, Andrea Salamon, Gaetano Salina, Francesco Simula, Nazario Tantalo, Laura Tosoratto, Piero Vicini - APEnet+: a 3D toroidal network enabling Petaflops scale Lattice QCD simulations on commodity clusters - High Energy Physics - Lattice 2010 (hep-lat); Distributed, Parallel, and Cluster Computing (cs.DC) arXiv:1012.0253v1 [hep-lat] (proceedings)
- R. Ammendola, A. Biagioni, O. Frezza, F. Lo Cicero, A. Lonardo, P.S. Paolucci, D. Rossetti, A. Salamon, G. Salina, F. Simula, L. Tosoratto, P. Vicini - apeNET+: High Bandwidth 3D Torus Direct Network for PetaFLOPS Scale Commodity Clusters, International Conference on Computing in High Energy and Nuclear Physics (CHEP), October 2010, Taipei, Taiwan - Proceedings on J. Phys.: Conf. Ser. 331 052029 doi:10.1088/1742-6596/331/5/052029
- R. Ammendola, A. Biagioni, O. Frezza, F. Lo Cicero, A. Lonardo, P.S. Paolucci, D. Rossetti, A. Salamon, G. Salina, F. Simula, L. Tosoratto, P. Vicini - Mastering multi-GPU computing on a torus network - GPU Technology Conference 2010 (GTC) - http://www.nvidia.com/content/GTC/posters/2010/I09-Mastering-Multi-GPU-Computing-on-a-Torus-Networki.pdf (poster)
- R. Ammendola, A. Biagioni, G. Chiodi, O. Frezza, A.Lonardo, F. Lo Cicero, R. Lunadei, D. Rossetti, A. Salamon, G. Salina, F. Simula, L. Tosoratto, P. Vicini - High speed data transfer with FPGAs and QSFP+ modules - Topical Workshop on Electronics for Particle Physics, Aachen, Germany / September 20-24, 2010 - Proceedings on JINST 5 C12019 doi:10.1088/1748-0221/5/12/C12019
- R. Ammendola et al. - High speed data transfer with FPGAs and QSFP+ modules - Nuclear Science Symposium Conference Record (NSS/MIC) 2010 IEEE, Publication Year: 2010, Page(s): 1323 1325, November 2010, Knoxville, Tennesse. DOI: 10.1109/NSSMIC.2010.5873983

3. Books/Book Chapters

ETHZ

Book chapter: I. Bacivarov, W. Haid, K. Huang, L. Thiele. Methods and Tools for Mapping Process Networks onto Multi-Processor Systems-On-Chip. Handbook of Signal Processing Systems, Springer, pages 1007-1040, October, 2010.

RWTH

Book: R. Leupers and O. Temam (Eds.), Processor and System-On-Chip Simulation, Springer, September 2010, ISBN 978-1441961747
Book: T. Kempf, G. Ascheid, R. Leupers: Multiprocessor Systems on Chip: Design Space Exploration, Springer, Feb 2011, ISBN 978-1441981523

TIMA

Katalin Popovici, Frederic Rousseau, Ahmed A. Jerraya, Marilyn Wolf: Embedded Software Design and Programming of Multiprocessor System-on-Chip, Simulink and SystemC Case Studies, Springer, April 2010, ISBN 978-1-4419-5566-1
Book chapter: Xavier Guerin, Frederic Petrot, Operating System Support for Applications targeting Heterogeneous Multi-Core System)on-Chip in the book Multi-Core Embedded Systems, CRC Press, Chapter 9, 24 pages, April 2010.

4. CASTNESS'11

A key action conducted during this period in the framework of WP9 has been the organization of the CASTNESS'11 Workshop (Computer Architectures, Software tools and nano-Technologies for Numerical and Embedded Scalable Systems), hosted in Roma on 17-18 January 2011 at the Frentani Conference Center.
http://www.congressifrentani.it

Twenty speakers, representing the four Teradevice Computing projects (EURETILE, TERAFLUX, TRAMS and SooS) presented their activities to about 60 researchers.
An archive, hosting all the presentations, is available for public access, hosted on the http://www.euretile.eu web site.

4.1 Agenda

Monday 17 January 2011: Day 1					
Event	**Speaker Name**	**Affiliation**	**Duration**	**Start**	**End**
REGISTRATION			00:40	13:00	13:40

OPENING and WELCOME	Speranza Falciano	INFN Roma	00:20	13:40	14:00
SOOS: Scaling Issues in Current OS Architectures and Approaches to Overcome them	Daniel Rubio Bonilla	USTUTT-HLRS, Stuttgart	00:20	14:00	14:20
SOOS: Composition vs Concurrency	Mihai Letia	EPFL, Lausanne	00:20	14:20	14:40
SHORT BREAK			00:20	14:40	15:00
SOOS: Issues in Large Scale Scheduling of Distributed Applications	Tommaso Cucinotta	Scuola Superiore Sant'Anna, Pisa	00:20	15:00	15:20
SOOS: Resource Discovery and Modelling in Heterogeneous Computing Environnments	Christiaan Baaij	University of Twente	00:20	15:20	15:40
SHORT BREAK			00:20	15:40	16:00
TRAMS: Introduction to the TRAMS Project Objectives	Antonio Rubio	UPC Barcelona	00:20	16:00	16:20
TRAMS Variability at Device Level	Andrew Brown	University of Glasgow	00:20	16:20	16:40
COFFEE BREAK			00:30	16:40	17:10
TRAMS: New Tools and Methods in Robust SRAM Design	Paul Zuber	Imec	00:20	17:10	17:30
TRAMS: Temperature, Voltage and Process Variations in SRAMs	Shrikanth Ganapathy	UPC Barcelona	00:13	17:30	17:43
TRAMS: Robustness of SRAM Memories	Ioana Vatajelu	UPC Barcelona	00:13	17:43	17:56
TRAMS: Carbon Nanotub Technology an Alternative in Future RAM Memories	Carmen Garcia	UPC Barcelona	00:14	17:56	18:10
SOCIAL DINNER				20:30	

Tuesday 18 January 2011: Day 2					
Event	**Speaker Name**	**Affiliation**	**Duration**	**Start**	**End**
EURETILE: Brain-Inspired many-tile SW/HW Experiment	Pier S. Paolucci	INFN Roma	00:20	09:00	09:20

EURETILE: Distributed Application Layer - Towards Seamless Programming of Many-Tiles Architectures	Iuliana Bacivarov	ETH Zurich	00:20	09:20	09:40
EURETILE: Simulation Challenges in the EURETILE Project	Jovana Jovic	RWTH Aachen	00:20	09:40	10:00
COFFEE BREAK			00:30	10:00	10:30
EURETILE: Communication Synthesis in Low Level Software for Hierarchical Heterogeneous Systems	Frederic Rousseau	TIMA/UJF Grenoble	00:20	10:30	10:50
EURETILE: Ideas for the design of an ASIP for LQCD	Werner Geurts	TARGET Leuven	00:20	10:50	11:10
SHORT BREAK			00:20	11:10	11:30
EURETILE: The HPC and Embedded Experimental HW Platform	Piero Vicini	INFN Roma	00:20	11:30	11:50
TERAFLUX: Intro	Roberto Giorgi	Università di Siena	00:20	11:50	12:10
TERAFLUX: OS	Doron Shamia	Microsoft	00:20	12:10	12:30
LUNCH			01:40	12:30	14:10
TERAFLUX: On Transactional Memory in TERAFLUX	Berham Khan	University of Manchester	00:20	14:10	14:30
TERAFLUX: On Computational Models	Salman Khan	University of Manchester	00:20	14:30	14:50
SHORT BREAK			00:20	14:50	15:10
TERAFLUX: On State-of-the-art and Plans on the Loop Nest Optimization	Konrad Trifunovic	INRIA Saclay, France	00:20	15:10	15:30
FET Plans	Jean-Marie Auger	EU FET Officer	00:20	15:30	15:50
CLOSURE				15:50	

4.2 Participant List

CASTNESS'11 (1st and 2nd day - 2011, January 17-18)		
Name	**Project**	**Affiliation**
Jean Marie Auger		EU Commission
Speranza Falciano		INFN Roma
Laura Tosoratto	EURETILE	INFN Roma
Pier Stanislao Paolucci	EURETILE	INFN Roma
Piero Vicini	EURETILE	INFN Roma
Andrea Biagioni	EURETILE	INFN Roma
Ottorino Frezza	EURETILE	INFN Roma
Alessandro Lonardo	EURETILE	INFN Roma
Davide Rossetti	EURETILE	INFN Roma
Francesco Simula	EURETILE	INFN Roma
Francesca Lo Cicero	EURETILE	INFN Roma
Frederic Rousseau	EURETILE	TIMA-UJF Grenoble
Rainer Leupers	EURETILE	RWTH Aachen
Christoph Schumacher	EURETILE	RWTH Aachen
Jovana Jovic	EURETILE	RWTH Aachen
Luis Gabriel Murillo	EURETILE	RWTH Aachen
Iuliana Bacivarov	EURETILE	ETH Zurich
Devendra Rai	EURETILE	ETH Zurich
Michela Giovagnoli	EURETILE	INFN Roma
Werner Geurts	EURETILE	TARGET Leuven
Roberto Giorgi	TERAFLUX	UNISI Siena
Konrad Trifunovic	TERAFLUX	INRIA Saclay
Albert Cohen	TERAFLUX	INRIA Saclay
Daniel Goodman	TERAFLUX	University of Manchester
Salman Khan	TERAFLUX	University of Manchester
Ian Watson	TERAFLUX	University of Manchester
Arne Garbade	TERAFLUX	University of Augsburg
Sebastian Weis	TERAFLUX	University of Augsburg
Behram Khan	TERAFLUX	University of Manchester
Ilaria Sbragi	TERAFLUX	UNISI Siena

Laurent Morin	TERAFLUX	CAPS Entreprise
Doron Shamia	TERAFLUX	Microsoft
Avi Mendelson	TERAFLUX	Microsoft
Rania Mameesh	TERAFLUX	UNISI Siena
Zhibin Yu	TERAFLUX	UNISI Siena
Antonio Portero	TERAFLUX	UNISI Siena
Marco Boni	TERAFLUX	UNISI Siena
Lutz Schubert	S(o)OS	USTUTT-HLRS Stuttgart
Tommaso Cucinotta	S(o)OS	Scuola Superiore Sant'Anna
Jan Kuper	S(o)OS	University of Twente
Bruno Santos	S(o)OS	IT Aveiro
Javad Zarrin	S(o)OS	IT Aveiro
Joao Paulo Barraca	S(o)OS	IT Aveiro
Christiaan Baaij	S(o)OS	University of Twente
Daniel Rubio Bonilla	S(o)OS	USTUTT-HLRS Stuttgart
Mihai Letia	S(o)OS	EPFL Lausanne
Juri Lelli	S(o)OS	Scuola Superiore Sant'Anna
Giulio Mancuso	S(o)OS	Scuola Superiore Sant'Anna
Antonio Rubio	TRAMS	UPC Barcelona
Andrew Brown	TRAMS	University of Glasgow
Ramon Canal	TRAMS	UPC Barcelona
Shrikanth Ganapathy	TRAMS	UPC Barcelona
Carmen Garcia	TRAMS	UPC Barcelona
Ioana Vatajelu	TRAMS	UPC Barcelona
Tanausu Ramirez	TRAMS	Intel
Paul Zuber	TRAMS	Imec