SEVENTH FRAMEWORK PROGRAMME
Call FP7-ICT-2009-4 Objective ICT-2009.8.1
[FET Proactive 1: Concurrent Tera-device Computing]

Project acronym: **EURETILE**
Project full title: **European Reference Tiled Architecture Experiment**
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WP9 – Training, Exploitation and Dissemination
D9.2 – Second Report on Training, Exploitation and Dissemination

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1. CASTNESS'12 WORKSHOP on Computing Architectures Software tools and nano-Technologies for Numerical Embedded and Scalable Systems

During 2012, an important WP9 action has been the contribution to the organization of the CASTNESS'12 Workshop (Computer Architectures, Software tools and nano-Technologies for Numerical and Embedded Scalable Systems).

Twenty speakers, representing the four Teradevice Computing projects (EURETILE, TERAFLUX, TRAMS and SooS) presented their activities.

The CASTNESS'12 workshop has been collocated with the HIPEAC'12 conference (Paris, Jan 23-25th).

This year, according to the TERACOMP plan, the organizational leadership has been assumed by the TERAFLUX project (coordinator Prof. Roberto Giorgi, Università di Siena) and the workshop has been chaired by Rosa Badia (Barcelona Supercomputing Center).

CASTNESS'12 AGENDA

8:00-8:25 Registration
8:25-8:30 **Opening and Welcome**, Rosa M. Badia
8:30-10:45 **TRAMS project**

- *Overview of the TRAMS Project in the second year* , Antonio Rubio (UPC)
- *FinFET variability - TCAD based PDK development*, Si-Yu Liao (UOG)
- *Variability Assessment for 10nm FinFET SRAM*, Miguel MIranda (Imec)
- *Quantitative comparison of proactive and reactive variability compensation technique*, S. Ganapathy, (UPC)
- *System Reconfiguration to Face Multicore Reliability and Variability Challenges*, Tanausu Ramirez (Intel)

- *Panel discussion*

10:45-11:00 Break
11:00-12:45 **EURETILE project**

- *Brain Inspired Many-Tile Experiment: second year overview of EURETILE* , Pier S. Paolucci (INFN)
- *Peer-to-peer GPGPU-APENet+connectivity on HPC EURETILE platform*, Piero Vicini (INFN)
- *Management of process network dynamism in the distributed application layer*, Iuliana Bacivarov (ETHZ)
- *Simulation-based software debugging in many-tile systems*, Luis Murillo (RWTH)
- *The use of communication path formalization for driver synthesis in the context of hierarchical heterogeneous systems*, Frederic Rousseau (UJF-TIMA)
- *Application-Specific Instruction-set Processors (ASIPs) and related design tools for tiled systems*, Gert Goossens (TARGET)
- *EURETILE Specific Questions & Answers*
- *Panel discussion*

12:45-14:00 Lunch Break
14:00-15:45 **TERAFLUX project**

- *TERAFLUX: exploiting dataflow parallelism in teradevice computing - Year 2,* Roberto Giorgi (UNISI)
- *Teraflux Architecture,* Skevos Evripidou (UCY)
- *Reliability aspects in Teraflux,* Theo Ungerer (U. Augsburg)
- *Teraflux, from the programming model to the execution model* Antoniu Pop (INRIA)
- *Panel discussion*

15:45-16:15 Break
16:15-18:00 **SoOs project**

- *Overview & Status of S(o)OS* (HLRS)
- *New approaches to annotating & identifying concurrency and parallelism on code level* (HLRS/UT)
- *Description of resource capabilities using ClASH* (UT)
- *Characterization and analysis of pipelined applications on the Intel SCC* (SSSA)
- *Rethinking Transactional Memory in the Manycore Context* (EPFL)
- *Communication & migration in many-core systems* (IT)
- Panel Discussion

2. Papers - Posters - Technical Press – Newsletters

Here after the list updated to the reporting date.

2.1 ETHZ

2013

- L. Thiele, L. Schor, I. Bacivarov, and H. Yang. Predictability for Timing and Temperature in Multiprocessor System-on-Chip Platforms. ACM Transactions in Embedded Computing Systems (TECS), 2013.

- P. Kumar, D. Chokshi, and L. Thiele. A Satisfiability Approach to Speed Assignment for Distributed Real-Time Systems. Proc. Design, Automation & Test in Europe Conference (DATE), Grenoble, France, Mar. 2013.

2012

- P. Kumar, and L. Thiele. Behavioural Composition: Constructively Built Server Algorithms. Proc. 5th Workshop on Compositional Theory and Technology for Real-Time Embedded Systems, San Juan, Puerto Rico, p. 9-12, Dec. 2012.
- P. Kumar and L. Thiele. Quantifying the Effect of Rare Timing Events with Settling-Time and Overshoot. Proc. IEEE Real-Time Systems Symposium (RTSS), San Juan, Puerto Rico, p. 149-160, Dec. 2012.
- S.-H. Kang, H. Yang, L. Schor, I. Bacivarov, S. Ha, and L. Thiele. Multi-Objective Mapping Optimization via Problem Decomposition for Many-Core Systems. Proc. IEEE Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia), Tampere, Finland, p. 28-37, Oct. 2012.
- L. Schor, I. Bacivarov, D. Rai, H. Yang, S.-H. Kang, and L. Thiele. Scenario-Based Design Flow for Mapping Streaming Applications onto On-Chip Many-Core Systems. Proc. Int'l Conf. on Compilers Architecture and Synthesis for Embedded Systems (CASES), Tampere, Finland, p. 71-80, Oct. 2012.
- D. Rai, H. Yang, I. Bacivarov, and L. Thiele. Power Agnostic Technique for Efficient Temperature Estimation of Multicore Embedded Systems. Proc. Int'l Conf. on Compilers Architecture and Synthesis for Embedded Systems (CASES), Tampere, Finland, p. 61-70, Oct. 2012.
- L. Schor, H. Yang, I. Bacivarov, and L. Thiele. Thermal-Aware Task Assignment for Real-Time Applications on Multi-Core Systems. Proc. Int'l Symposium on Formal Methods for Components and Objects (FMCO) 2011, Turin, Italy, Volume 7542 of LNCS, p. 294-313, Oct. 2012.
- L. Schor, H. Yang, I. Bacivarov, and L. Thiele. Worst-Case Temperature Analysis for Different Resource Models. IET Circuits, Devices & Systems, Volume 6, Issue 5, p. 297-307, Sep. 2012.
- K. Huang, W. Haid, I. Bacivarov, M. Keller, L. Thiele. Embedding Formal Performance Analysis into the Design Cycle of MPSoCs for Real-time Streaming Applications. ACM Transactions in Embedded Computing Systems (TECS Journal), ACM, Volume 11, Issue 1, p. 8:1-8:23, 2012.
- L. Schor, I. Bacivarov, H. Yang, and L. Thiele. Fast Worst-Case Peak Temperature Evaluation for Real-Time Applications on Multi-Core Systems. Proc. IEEE Latin American Test Workshop (LATW), Quito, Ecuador, p. 1-6, Apr. 2012.
- L. Schor, I. Bacivarov, H. Yang, and L. Thiele. Worst-Case Temperature Guarantees for Real-Time Applications on Multi-Core Systems. Proc. IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Proc. IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Beijing, China, p. 87-96, Apr. 2012.
- P. Kumar and L. Thiele. Timing Analysis on a Processor with Temperature-Controlled Speed Scaling. Proc. IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Beijing, China, p. 77-86, Apr. 2012.

- Bacivarov, I. Belaid, A. Biagioni, A. El Antably, N. Fournel, O. Frezza, J. Jovic, R. Leupers, F. Lo Cicero, A. Lonardo, L. Murillo, P.S. Paolucci, D. Rai, D. Rossetti, F. Rousseau, L. Schor, C. Schumacher, F. Simula, L. Thiele, L. Tosoratto, P. Vicini, H. Yang – "DAL: Programming Efficient and Fault-Tolerant Applications for Many-Core Systems" - Poster at HIPEAC12 - Jan 23-25, 2012 Paris, France

2011

- P. Kumar, J.-J. Chen, and L. Thiele. Demand Bound Server: Generalized Resource Reservation for Hard Real-Time Systems. Proc. Int'l Conference on Embedded Software (EMSOFT), pages 233-242, Oct. 2011.
- L. Schor, H. Yang, I. Bacivarov, and L. Thiele. Worst-Case Temperature Analysis for Different Resource Availabilities: A Case Study. Proc. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Lecture Notes on Computer Science (LNCS), Springer, Vol. 6951, pages 288-297, Sep. 2011.
- P. Kumar, J.-J. Chen, L. Thiele, A. Schranzhofer, and G. C. Buttazzo. Real-Time Analysis of Servers for General Job Arrivals. Proc. Intl. Conf. on Embedded and Real-Time Computing Systems and Applications (RTCSA), pages 251-258, Aug. 2011.
- L. Thiele, L. Schor, H. Yang, and I. Bacivarov. Thermal-Aware System Analysis and Software Synthesis for Embedded Multi-Processors. Proc. Design Automation Conference (DAC), pages 268-273, Jun. 2011.
- D. Rai, H. Yang, I. Bacivarov, JJ. Chen, L. Thiele. Worst-Case Temperature Analysis for Real-Time Systems. In Proceedings of Design, Automation and Test in Europe (DATE), Grenoble, France, March 2011.
- S. Perathoner, K. Lampka, L. Thiele. Composing Heterogeneous Components for System-wide Performance Analysis. In Proceedings of Design, Automation and Test in Europe (DATE), Grenoble, France, March 2011 (invited paper).
- Bacivarov, H. Yang, L. Schor, D. Rai, S. Jha, L. Thiele, Poster: Distributed Application Layer - Towards Efficient and Reliable Programming of Many-Tile Architectures. Design, Automation and Test in Europe (DATE) Friday Workshop, Grenoble, France, March 2011.
- K. Huang, L. Santinelli, JJ. Chen, L. Thiele, and G. C. Buttazzo. Applying Real-Time Interface and Calculus for Dynamic Power Management in Hard Real-Time Systems. Real-Time Systems Journal, Springer Netherlands, Vol. 47, No. 2, pages 163-193, Mar. 2011.

2010

- Schranzhofer, JJ. Chen, L. Thiele. Dynamic Power-Aware Mapping of Applications onto Heterogeneous MPSoC Platforms. IEEE Transactions on Industrial Informatics, IEEE, Vol. 6, No. 4, pages 692 -707, November, 2010.

2.2 RWTH

2012

- Schumacher, J. H. Weinstock, R. Leupers, G. Ascheid, L. Tossorato, A. Lonardo, D. Petras, T. Groetker. "legaSCi: Legacy SystemC Model Integration into Parallel

SystemC Simulators". 1st Workshop on Virtual Prototyping of Parallel and Embedded Systems (ViPES), 2013, Boston, USA (accepted for publication).

- Schumacher, J. H. Weinstock, R. Leupers and G. Ascheid: Cause and effect of nondeterministic behavior in sequential and parallel SystemC simulators. IEEE International High Level Design Validation and Test Workshop (HLDVT'12). Nov 2012, Huntington Beach (California-USA).
- Schumacher, J. H. Weinstock, R. Leupers and G. Ascheid: Scandal: SystemC Analysis for NonDeterminism AnomaLies. Forum on Specification and Design Languages (FDL '12), Sep 2012, Vienna (Austria)
- L. G. Murillo, J. Harnath, R. Leupers and G. Ascheid: Scalable and Retargetable Debugger Architecture for Heterogeneous MPSoCs. System, Software, SoC and Silicon Debug Conference (S4D '12), Sep 2012, Vienna (Austria)
- L. G. Murillo, J. Eusse, J. Jovic, S. Yakoushkin, R. Leupers and G. Ascheid: Synchronization for Hybrid MPSoC Full-System Simulation. Design Automation Conference (DAC '12), Jun 2012, San Francisco (USA)
- R. Leupers: More Real Value for Virtual Platforms. Design, Automation and Test in Europe (DATE '12), Mar 2012, Dresden (Germany)
- J. Jovic, S. Yakoushkin, L. G. Murillo, J. Eusse, R. Leupers and G. Ascheid: Hybrid Simulation for Extensible Processor Cores. Design, Automation and Test in Europe (DATE '12), Mar 2012, Dresden (Germany)

2011

- S. Kraemer, R. Leupers, D. Petras, T. Philipp, A. Hoffmann: Checkpointing SystemC-Based Virtual Platforms. International Journal of Embedded and Real-Time Communication Systems (IJERTCS), vol. 2, no. 4, 2011
- L. G. Murillo, W. Zhou, J. Eusse, R. Leupers, G. Ascheid: Debugging Concurrent MPSoC Software with Bug Pattern Descriptions. System, Software, SoC and Silicon Debug Conference (S4D '11), Oct 2011, Munich (Germany)
- R. Leupers, G. Martin, N. Topham, L. Eeckhout, F. Schirrmeister, X. Chen: Virtual Manycore Platforms: Moving Towards 100+ Processor Cores. Design Automation & Test in Europe (DATE), Mar 2011, Grenoble (France)
- J. Castrillon, A. Shah, L. G. Murillo, R. Leupers, G. Ascheid: Backend for Virtual Platforms with Hardware Scheduler in the MAPS Framework. 2nd IEEE Latin America Symp. on Circuits and Systems, Feb 2011, Bogota (Colombia)
- S. Kraemer, Design and analysis of efficient MPSoC simulation techniques, dissertation, 2011, Aachen, Germany (http://darwin.bth.rwth-aachen.de/opus3/frontdoor.php?source_opus=3769&la=de)

2010

- C. Schumacher, R. Leupers, D. Petras and A. Hoffmann. parSC: Synchronous Parallel SystemC Simulation on Multi-Core Host Architectures. In proceedings of CODES/ISSS '10, October, 2010, Scottsdale, Arizona, USA (http://dx.doi.org/10.1145/1878961.1879005)

2.3 TIMA

2011

- Chagoya-Garzon, N. Poste, F. Rousseau, Semi-Automation of Configuration Files Generation for Heterogeneous Multi-Tile Systems, Computer Software and Application Conference (COMPSAC 2011), Munich, Germany, 18-21 July 2011.
- H. Chen, G. Godet-Bar, F. Rousseau, F. Petrot, Me3D : A Model-driven Methodology expediting Embedded Device Driver Development, International Symposium on Rapid System Prototyping (IEEE RSP 2011), pp. 171-177, May 2011, Karlshrue, Germany.

2.4 INFN

2012

- The EURETILE Consortium - Brain Simulation Benchmark: Inspiring and benchmarking the scalability and fault-tolerance of future many-tile systems - Poster at HIPEAC12 - Jan 2012 Paris, France
- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto, Piero Vicini - APEnet+: a 3-D Torus network optimized for GPU-based HPC Systems - Poster at CHEP 2012, New York, NY - Proceedings on 2012 J. Phys.: Conf. Ser. 396 042059 doi:10.1088/1742-6596/396/4/042059
- R. Ammendola, A. Biagioni, O. Frezza, A. Lonardo, F. Lo Cicero, P. S. Paolucci, D. Rossetti, A. Salamon, F. Simula, L. Tosoratto, P. Vicini, APEnet+: a 12x34 Gbps data transmission system with FPGAs embedded transceivers and QSFP+ modules - Poster at NSS-12 Nuclear Science Symposium - Anaheim, California, October 29 – November 3, 2012 - [TO BE PUBLISHED]
- R Ammendola, A Biagioni, O Frezza, F Lo Cicero, A Lonardo, PS Paolucci, D Rossetti, F Simula, L Tosoratto, P Vicini - APEnet+: a 3D Torus network optimized for GPU-based HPC Systems - Journal of Physics: Conference Series - 396 042059 doi:10.1088/1742-6596/396/4/042059
- S. Amerio, R. Ammendola, A. Biagioni, D. Bastieri, D. Benjamin, O. Frezza, S. Gelain, W. Ketchum, Y. K. Kim, F. Lo Cicero, A. Lonardo, T. Liu, D. Lucchesi, P. S. Paolucci, S. Poprocki, D. Rossetti, F. Simula, L. Tosoratto, G. Urso, P. Vicini, and P. Wittich - Applications of GPUs to online track reconstruction in HEP experiments - NSS-MIC 2012 Proceedings [TO BE PUBLISHED]
- Bacivarov, I. Belaid, A. Biagioni, A. El Antably, N. Fournel, O. Frezza, W. Geurts, G. Goossens, J. Jovic, R. Leupers, F. Lo Cicero, A. Lonardo, L. Murillo, P. S. Paolucci, D. Rai, D. Rossetti, F. Rousseau, L. Schor, C. Schumacher, F. Simula, L. Thiele, L. Tosoratto, P. Vicini and H. Yang - EURETILE: Unified Networking Infrastructure for Embedded and HPC many-tile platforms - Poster at HIPEAC12 – 25 Jan 2012 Paris, France

2011

- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto, Piero Vicini - QUonG: A GPU-based HPC System Dedicated to LQCD Computing - Application Accelerators in High-Performance Computing, Symposium on, pp. 113-122, 2011 Symposium on Application Accelerators in High-Performance Computing, 2011

- APEnet+ project status - XXIX International Symposium on Lattice Field Theory - July 2011 Squaw Valley, Lake Tahoe, CA

2010

- Pier Stanislao Paolucci - *FP7 EURETILE Project: EUropean REference TILed architecture Experiment* - HipeacInfo, Quarterly Newsletter, Number 24, page 11, October 2010 (http://www.Hipeac.net/newsletter)
- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Paolucci, Roberto Petronzio, Davide Rossetti, Andrea Salamon, Gaetano Salina, Francesco Simula, Nazario Tantalo, Laura Tosoratto, Piero Vicini - *APEnet+: a 3D toroidal network enabling Petaflops scale Lattice QCD simulations on commodity clusters* - High Energy Physics - Lattice 2010 (hep-lat); Distributed, Parallel, and Cluster Computing (cs.DC) arXiv:1012.0253v1 [hep-lat] (proceedings)
- R. Ammendola, A. Biagioni, O. Frezza, F. Lo Cicero, A. Lonardo, P.S. Paolucci, D. Rossetti, A. Salamon, G. Salina, F. Simula, L. Tosoratto, P. Vicini - *apeNET+: High Bandwidth 3D Torus Direct Network for PetaFLOPS Scale Commodity Clusters*, International Conference on Computing in High Energy and Nuclear Physics (CHEP), October 2010, Taipei, Taiwan - Proceedings on J. Phys.: Conf. Ser. 331 052029 doi:10.1088/1742-6596/331/5/052029
- R. Ammendola, A. Biagioni, O. Frezza, F. Lo Cicero, A. Lonardo, P.S. Paolucci, D. Rossetti, A. Salamon, G. Salina, F. Simula, L. Tosoratto, P. Vicini - *Mastering multi-GPU computing on a torus network* - GPU Technology Conference 2010 (GTC) - http://www.nvidia.com/content/GTC/posters/2010/I09-Mastering-Multi-GPU-Computing-on-a-Torus-Networki.pdf (poster)
- R. Ammendola, A. Biagioni, G. Chiodi, O. Frezza, A.Lonardo, F. Lo Cicero, R. Lunadei, D. Rossetti, A. Salamon, G. Salina, F. Simula, L. Tosoratto, P. Vicini - *High speed data transfer with FPGAs and QSFP+ modules* - Topical Workshop on Electronics for Particle Physics, Aachen, Germany / September 20-24, 2010 - Proceedings on JINST 5 C12019 doi:10.1088/1748-0221/5/12/C12019
- R. Ammendola et al. - *High speed data transfer with FPGAs and QSFP+ modules* - Nuclear Science Symposium Conference Record (NSS/MIC) 2010 IEEE, Publication Year: 2010, Page(s): 1323 1325, November 2010, Knoxville, Tennessee. DOI: 10.1109/NSSMIC.2010.5873983

3. Presentations

3.1 ETHZ

2012

- Iuliana Bacivarov, System-Level Thermal Aware Design of Real-Time Embedded Systems, Lecture at Design and Test Summer School 2012, Oct. 2012, Puebla, Mexico.
- Iuliana Bacivarov, Distributed Application Layer: Scenario-Based Design Flow for Mapping Streaming Applications onto On-Chip Many-Core Systems, Invited talk at Thales Paris, Aug. 2012, Paris, France.

- Iuliana Bacivarov, EU FP7 project EURETILE - EUropean REference TILed architecture Experiment (2010-2013): Distributed Application Layer, in Special Session on Ongoing EU Projects at ASAP 2012, Jul. 2012, Delft, Netherlands.
- Iuliana Bacivarov, Distributed Application Layer: Efficient Programming of Reliable Many-Core Systems, Invited talk at TU Delft, Jun. 2012, Delft, Netherlands.
- Iuliana Bacivarov, Distributed Application Layer: Mapping Dynamic Streaming Applications onto Many-Core Systems, Invited talk at Map2MPSoC/SCOPES, May 2012, Schloss Rheinfels, St. Goar, Germany.
- Iuliana Bacivarov, Management of Process Network Dynamism in the Distributed Application Layer, CASTNESS 2012, Jan. 2012, Paris, France.

2011

- Iuliana Bacivarov, Thermal-Aware Design of Real-Time Multi-Core Embedded Systems, Invited talk at Mapping Applications to MPSoCs, Jun. 2011.
- Iuliana Bacivarov, Temperature Predictability in Multi-Core Real-Time Systems, Invited talk at DAC Workshop on Multiprocessor System-on-Chip for Cyber Physical Systems: Programmability, Run-Time Support, and Hardware Platforms for High Performance Embedded Applications, Jun. 2011.
- Iuliana Bacivarov, Distributed Application Layer – Towards Seamless Programming of Many-Tile Architectures, CASTNESS 2011, 17 and 18 January 2011, Roma, Italy, http://euretile.roma1.infn.it/mediawiki/img_auth.php/8/88/EURETILE-2-IulianaBacivarov.pdf.

2010

- Iuliana Bacivarov, Distributed Operation Layer: An Efficient and Predictable KPN-Based Design Flow, invited talk at Workshop on Compiler-Assisted System-On-Chip Assembly 2010, in conjunction with Embedded Systems Week, Scottsdale, AZ, US, October 2010, http://www12.cs.fau.de/ws/casa10.
- Iuliana Bacivarov, Efficient Execution of Kahn Process Networks on CELL BE, invited talk at Summer School on Models for Embedded Signal Processing Systems at Lorentz Center, Leiden, Netherlands, 30 Aug - 3 Sep 2010, http://www.lorentzcenter.nl/lc/web/2010/427/presentations/Iuliana-cell.pdf.
- Iuliana Bacivarov, Distributed Operation Layer: A Practical Perspective, tutorial at Summer School on Models for Embedded Signal Processing Systems at Lorentz Center, Leiden, Netherlands, 30 Aug - 3 Sep 2010, http://www.lorentzcenter.nl/lc/web/2010/427/presentations/Iuliana-demo.pdf.
- Iuliana Bacivarov, Distributed Operation Layer: Efficient Design Space Exploration of Scalable MPSoC, invited talk at Combinatorial Optimization for Embedded System Design workshop 2010 in conjunction with CPAIOR2010, 7th International Conference on Integration of Artificial Intelligence and Operations Research techniques in Constraint Programming, Bologna, Italy, June 2010, http://www.artist-embedded.org/artist/Overview,2022.html.
- Iuliana Bacivarov, invited talk at Efficient Execution of Kahn Process Networks on MPSoC, Mapping Applications to MPSoCs 2010, June 29-30, 2010, St. Goar, Germany, http://www.artist-embedded.org/artist/Program,1822.html.

3.2 RWTH

2012

- R. Leupers. Multicore Platform Design: Tackling a Grand Challenge in Embedded Computing. Keynote at the 15th Euromicro Conference on Digital System Design (DSD '12), Sep 2012, Izmir, Turkey
- R. Leupers. Embedded Multicore Design Technologies: The Next Generation. Keynote at the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP '12), Jul 2012, Delft, The Netherlands
- R. Leupers. Design Technologies for Wireless Multiprocessor Systems-on-Chip, PhD course, University of Pisa, Jul 2012, Pisa, Italy
- Christoph Schumacher. Virtual EURETILE Platform: a Platform for Many-tiled Systems Simulation. Joint RWTH/TU Poznan Seminar, May 2012, Poznan, Poland
- R. Leupers (session chair). Workshop at DATE 2012: "Quo Vadis, Virtual Platforms? Challenges and Solutions for Today and Tomorrow". Mar 2012, Dresden, Germany
- R. Leupers (organized by). Special session at DATE 2012: "Virtual Platforms: Breaking New Grounds". Mar 2012, Dresden, Germany
- R. Leupers, H. Meyr. Embedded Processor Design, Block lecture ALaRI, Feb 2012, University of Lugano, Lugano, Switzerland
- R. Leupers. What's hot on Embedded System Design. Keynote at the Embedded Technology Conference (ETC '12), Feb 2012, San Pedro, Costa Rica
- Luis Murillo. Simulation-based software debugging in many-tile systems. CASTNESS 2012, January 26, 2012, Paris, France

2011

- Juan Eusse. Hybrid Simulation Technology for Extensible Cores and Full System Simulation of Complex MPSoCs. Presentation at HiPEAC Computing Systems Week, Nov 2011, Barcelona, Spain
- R. Leupers. SoC Design Research in the UMIC Excellence Cluster, Seminar, TU Berlin, Sep 2011, Berlin, Germany
- S. Yakoushkin. Advanced Simulation Techniques, Joint RWTH/TU Tampere Seminar, June 2011, Tampere, Finland
- R. Leupers (organized by). ICT Technology Transfer Workshop targeting Horizon 2020, Apr 2011, Brussels, Belgium
- R. Leupers and G. Martin (organized by). Special session at DATE 2011: Virtual Manycore Platforms: Moving Towards 100+ Processor Cores, March 2011, Grenoble, France
- R. Leupers, H. Meyr. Embedded Processor Design, Block lecture ALaRI, Feb 2011, University of Lugano, Lugano, Switzerland
- Jovana Jovic, Simulation Challenges in the EURETILE Project, CASTNESS 2011, January 17-18, 2011, Rome, Italy

2010

- Christoph Schumacher, Virtual Platform Technologies for Multi-core Platforms, UMIC Day, 19 October, 2010, RWTH Aachen, Germany

- Rainer Leupers, HiPEAC Cluster Meeting (Design and Simulation Cluster), October 2010, Barcelona, Spain
- Rainer Leupers, Design Technologies for Wireless Systems-On-Chip, Huawei ESL Symposium, September 2010, Shenzhen, People's Republic of China
- Christoph Schumacher, Stefan Kraemer and Rainer Leupers, demonstration at DAC 2010 exhibition: parSC: parallel SystemC simulation, deterministic, accurate, fast, June 14-16, 2010, Anaheim, USA
- Rainer Leupers, MPSoC Design for Wireless Multimedia, Tutorial, MIXDES, June 2010, Wroclaw, Poland
- Stefan Kraemer, Advanced Simulation Techniques for Virtual Platforms, May 26, 2010, Imperial College London, London, United Kingdom
- Rainer Leupers, Cool MPSoC Design, ASCI Winter School on Embedded Systems, March 2010, Soesterburg, Netherlands
- Rainer Leupers, Embedded Procesor Design and Implementation, course in MSc in Embedded Systems track at ALaRI Institute, March 1-4, 2010, University of Lugano, Switzerland

3.3 INFN

2012

- R. Ammendola, apeNET+: a 3D toroidal network enabling petaFLOPS scale Lattice QCD simulations on commodity clusters, Lattice 2010, THE XXVIII INTERNATIONAL SYMPOSIUM ON LATTICE FIELD THEORY, Villasimius, Italy, June 2010, http://agenda.infn.it/contributionDisplay.py?contribId=335&sessionId=70&confId=2128
- D. Rossetti, Leveraging NVIDIA GPUDirect on APEnet+ 3D Torus Cluster Interconnect - GTC 2012 - GPU Technology Conference - May 2012 - San Jose, CA, [[8]]
- R. Ammendola, Comunicazioni Peer to Peer tra GPU remote con APENet+ - E4 Workshop 2012 - Sept 2012 - Bologna, Italy [[9]]
- D. Rossetti, Multi GPU simulations: status and perspectives - New Frontiers in Lattice Gauge Theory, GGI Firenze, Italy - [[10]]
- Davide Rossetti, Breadth First Search on APEnet+ - talk at IA^3 Workshop on Irregular Applications at SC12 conference, 10 Nov 2012. Presentation available here
- Pier Stanislao Paolucci, Brain Inspired Many-Tile Experiment: second year overview of EURETILE, CASTNESS'12, 26 January 2012, Paris, France
- P. Vicini, Peer-to-peer GPGPU-APENet+connectivity on HPC EURETILE platform, CASTNESS'12, 26 January 2012, Paris, France

2011

- D. Rossetti, apeNET+ Project Status, Lattice 2010, THE XXIX INTERNATIONAL SYMPOSIUM ON LATTICE FIELD THEORY, Squaw Village, Lake Tahoe, CA, USA, July 2011 - to be published on https://latt11.llnl.gov/html/proceedings.php
- P. Vicini, QUonG: A GPU-based HPC System Dedicated to LQCD Computing - Symposium on Application Accelerators in High-Performance Computing, Knoxville, TN - USA, July 2011 http://doi.ieeecomputersociety.org/10.1109/SAAHPC.2011.15

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3.4 Target

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2011

- G. Goossens, “Why Compilation Tools are the Catalyst for Multicore SoC Design”, Electronic Design and Solutions Fair, Yokohama (Japan), January 27-28, 2011.
- G. Goossens, “Why Compilation Tools are a Catalyst for Multicore SoC Design”, Third Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Design Automation and Test in Europe (DATE-2011), Grenoble (France), March 18, 2011.
- G. Goossens, P. Verbist, “Enabling the Design and Programming of Application-Specific Processors”, Sophia-Antipolis Micro-Electronics Conference (SAME-2011), Sophia-Antipolis (France), October 12-13, 2011.
- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Electronic Design and Solutions Fair, Yokohama (Japan), November 16-18, 2011.
- P. Verbist, “Building software-programmable accelerators for ARM-based subsystems”, ARM Technical Symposium, Taipei and Hsinchu (Taiwan), November 17-18, 2011.
- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Intl. Conf. on IP-Based SoC Design (IP-SoC-2011), Grenoble (France), December 7-8, 2011.
- G. Goossens, “Design Tools for Building Software-Programmable Accelerators in Multicore SoCs”, Workshop on Tools for Embedded System Design, Sint-Michielsgestel (Netherlands), December 13, 2011. W. Geurts, G. Goossens, "Ideas for the Design of an ASIP for LQCD", CASTNESS 2011, Rome (Italy), January 17-18,

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- S. Cox, G. Goossens, "Hardware Accelerator Performance in a Programmable Context: Methodology and Case Study", Embedded Systems Conference, San Jose (CA, USA), April 26-29, 2010.
- G. Goossens, "Design of Programmable Accelerators for Multicore SoCs", First Artemis Technology Conference, Budapest (Hungary), June 29-30, 2010.