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"Towards Zero Power ICT" Proactive Scheme

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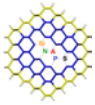

Executive Summary (publishable)

Silicon nanowire (SiNW) field effect transistors (FET) have been widely investigated as biological sensors for their remarkable sensitivity due to their large surface to volume ratio (S/V) and high selectivity towards a myriad of analytes through functionalization. The aim of Task 3.2 (deliverable D3.4) is to investigate junctionless nanowire transistors (JNT) through 3D Technology Computer Aided Design (TCAD) simulations performed as a function of geometrical dimensions and channel doping concentration N_d for a p-type tri-gated structure. Our goal is to provide useful guidelines for the design of junctionless FET silicon nanowire sensors that can be integrated into miniaturized, low power biosensing systems that would aid in future fabrication endeavours. JNT having a uniform and usually highly doped source/channel/drain can provide high drain currents and a tunable threshold voltage. The operation regime (threshold voltage V_{th}) and electrical characteristics of JNTs can be directly tuned by the careful design of the NW/Fin FET. This is of particular importance as device sensitivity has been found to be dependent on the operating point at which sensor measurements are carried out with the subthreshold having optimal sensitivity (highest conductance response). Though we may set the operation point (for maximum sensitivity) by back-gating (BG) this is not appropriate for low-power device applications as high voltages are needed in order to induce inversion, accumulation or depletion through the backgate insulator. In this work, we seek to tune the operation point of a JNT sensor for maximum sensitivity by the careful design of the NW/Fin geometrical dimensions, doping concentration and gate insulator. In this work, we propose a long channel (L > 500 nm) junctionless nanowire transistor (JNT) SiNW sensor based on a highly doped, ultrathin body field-effect transistor with an organic gate dielectric $\varepsilon_r = 1.7$. Two different materials, namely, an oxide and an organic monolayer, with varying dielectric constants ε_r provide surface passivation. Mildly doped $N_d = 1x10^{19}$ cm^{-3}, thin bodied structures (fin width $F_w < 20$ nm) with an organic dielectric ($\varepsilon_r = 1.7$) were found to have promising electrical characteristics for FET sensor structures such as $V_{th} \sim 0$ V, high relative sensitivities in the subthreshold regime S > 95%, high transconductance values at threshold $g_{m,Vfg=0V} > 10$ nS, low subthreshold slopes SS ~ 60 mV/dec, high saturation currents $I_{d,max} \sim$ 1-10 μA and high $I_{on} / I_{off} > 10^4$ - 10^{10} ratios.

1 Introduction

1.1 The NW Sensor

The ISFET (ion sensitive field effect transistor) introduced by Bergveld in 1970 [1-3] is analogous to a MOSFET (metal oxide semiconductor field effect transistor) except that the gate channel is exposed to a solution and therefore ions or charged molecules at the surface of the channel act as a gate [4]. In comparison to a MOSFET where the gate electrode has direct contact with the gate dielectric, a reference electrode V_{ref} or local gate V_{lg} electrode is instead typically inserted into the analyte contacting the gate. Ions in solution or charged molecules influence the gate potential so that they can exert electrostatic control on the source to drain current I_d [4]. When charged analyte molecules adsorb on a NW an electric field created on the surface exerts an effect both inside and outside of the semiconductor channel. Nanosensor structures such as SiNWs have the potential to provide fast, low cost, low power, label free detection, real time response, high throughput analysis and insight into biological processes while not requiring large sampling quantities [5, 6]. Due to the small size (large S/V) of SiNWs the presence of a few charged biological molecules on their surface can modulate the carrier distribution over their entire cross sectional conduction pathway making the devices highly sensitive compared to the traditional planar sensor that Bergveld introduced [7]. It has also been found that decreasing the size of the nanowire decreases the electrostatic capacitances that provides for faster response times [8].

The reference electrode is normally an indispensable part of the ISFET measurement set-up. Its function is to provide a stable electrical contact to the test electrolyte and define the electric potential of the sensing liquid. It must also provide for an electrode-electrolyte interface potential that does not vary with electrolyte composition so that changes in I_d of the ISFET are a measure only of changes in its electrolyte-insulator interface [9]. Device

sensitivity is also dependent on the operating point at which sensor measurements are carried out. The subthreshold region has been found to have the optimal sensitivity (highest conductance response) for enhancement mode NW sensors [10, 11]. In this regime, the NW is nearly depleted of carriers with a much larger screening length λ_D in comparison to its radius R allowing for molecular gating to occur throughout the whole cross section of the structure [10, 11]. Commercial reference electrodes (*i.e.:* Ag/AgCl or calomel) though stable, they are bulky, expensive and their inclusion in sensing measurements prohibits the successful integration of FET sensors into miniaturized, portable, low cost systems. Therefore use of a noble metal pseudo reference electrode (V_{gate}) integrated into a differential pair (ISFET/REFET) circuit has been previously explored [3, 9, 12] for example. The differential ISFET/REFET pair configuration allows for the use of a solid state noble metal local electrode that can be patterned by photolithography on chip vs. the use of an external, large and intrusive reference electrode. We may also set the operation point (for maximum sensitivity) by back-gating (BG) [13, 14], but is also not appropriate for low-power device applications as high voltages are needed in order to induce inversion, accumulation or depletion through the backgate insulator. The JNT has been found to have a tunable threshold voltage [15] dependent on NW dimensions, type of gate insulator and doping concentration therefore, in this work we seek to tune the operation point of a JNT sensor by the careful design of the NW/Fin.

1.2 The Junctionless Nanowire Transistor

JNTs are said to be junctionless because the source and drain extensions have the same type and doping concentration as the conduction channel (*i.e.:* P^+-P^+-P^+, N^+-N^+-N^+) [16-19]. They have high doping channel concentrations and with no p-n junctions or doping gradients they are essentially resistors with a gate electrode that controls the carrier density [15, 16, 20-

22]. The operation of the JNT is based on the depletion or accumulation of carriers in the highly doped semiconductor channel [17, 19]. JNTs feature bulk conduction as opposed to surface conduction [18, 23] making them an interesting candidate for NW FET biosensor devices with high S/V ratios. Having no doping concentration gradients greatly simplifies the fabrication process, reduces variability and relaxes thermal budget requirements since there is no impurity diffusion during thermal processing steps [21, 23, 24]. Furthermore, the threshold voltage can be easily varied by changing different parameters such as the width, height, doping and surface passivation/dielectric characteristics. These are all advantageous qualities for the fabrication of miniaturized sensor devices and their heterogeneous integration with other components.

1.3 The Sensing Interface

Another aspect that deserves some thought when designing a sensor structure is the surface passivation material which acts as a gate dielectric. The SiNW-dielectric interface is important for the electrical stability of the device. SiO_2 is not the best pH selective material as it does not provide a stable contact between the liquid and the sensor [1]. Since protons can penetrate the Si-oxide layers leading to large leakage current, different dielectrics (*i.e.:* Alumina) have been deposited in order to efficiently suppress this issue [10]. The protection layer should be as thin as possible in order to maintain the sensitivity of the device. It has been found in literature that the passivation of the silicon surface *via* strong covalent Si-C bonds can provide well defined and stable monolayers with insulating properties superior to that of native oxide [25, 26]. Two different dielectric materials have been investigated in this study. First, the dielectric constant ε_r = 1.7 of the organic monolayer $SiC_{16}H_{33}$ passivating an oxide free silicon surface as determined by Faber *et al.*,[25] and thickness t_d = 1.78 nm were utilized in the simulation. This mimics the functionalization scheme to be employed in future

work by Tyndall (Task 2.2) assuming that the dielectric properties of this organic monolayer are similar to the functionalization of interest. SiO_2 as a gate dielectric material (ε_r = 3.19) was also investigated.

2 TCAD Simulation Study

Different junctionless transistor devices have been studied by 3D TCAD simulations. Fig. 1 shows the top side view of the meshed simulated structure. The geometric parameters (fin height F_h, fin width F_w and channel length L indicated in Fig. 1) as well as the junctionless channel doping concentration N_d, have been varied in order to find the optimal device characteristics for a low power and high sensitivity sensor. The dielectric thickness t_d, source/drain (S/D) extensions, and buried oxide (BOX) are also displayed in the schematic. The JNT is gated from the front and from the sides, in a tri-gate FET architecture.

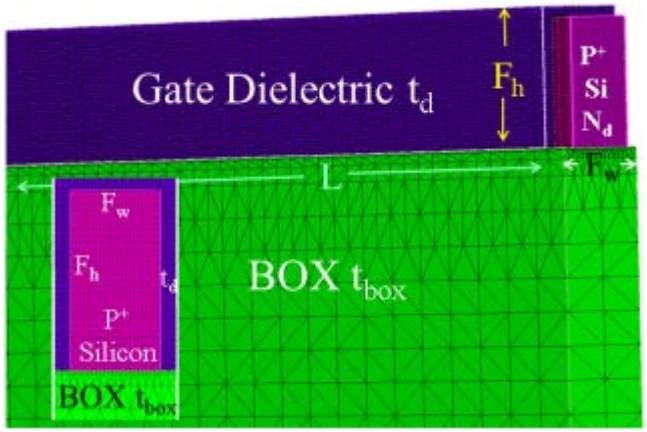

Figure 1. 3D and cross section of simulated tri-gate junctionless structure.

3D TCAD simulations using Sentaurus Device e.2010.12 have been performed as a function of gate dielectric constant (ε_r = 1.7, 3.9), geometrical dimensions (fin channel length L = 0.5, 1, 2 µm, fin height F_h = 10, 20, 30, 45 nm and width F_w = 10, 20, 30 nm) and doping concentration (boron B, $N_d = 10^{18}$ cm^{-3}, 10^{19} cm^{-3}, 2x10^{19} cm^{-3}) for a p-type Si-NW/fin tri-gated junctionless FET. The fin width F_w, height F_h, channel L, dielectric thickness t_d, and source/drain (S/D) extensions are displayed in the schematic of Fig. 1. For sensing applications, long channels L > 100 nm are necessary to guarantee biological interaction with the NW surface and are therefore also studied here. The simulations were built to include 145

nm of buried oxide (BOX) (displayed in the schematic of Fig. 1) with varying silicon fin heights and widths to resemble the silicon on insulator (SOI) FinFET based structure currently being fabricated. The lateral S/D extensions are 10 nm on each side of the gate channel. The S/D contacts are simulated as ohmic. The junctionless transistor is gated from the front-side resembling a tri-gate FET (multigate fin). The front gate voltage V_{fg} is swept keeping the back-gate grounded V_{bg} = 0 V for high and low drain voltage potentials of V_d = -1 V and -50 mV. The gate electrode was simulated as N^+ polysilicon ($2x10^{20}$ cm^{-3}, workfunction φ = 4.1 V). The drain current I_d is iteratively computed by solving the Poisson's and hole continuity (majority carrier) equations throughout the cross-section of the fin. The drift-diffusion model is used for the carrier transport in the semiconductor without impact ionization. A mobility degradation model is also being implemented for carrier scattering effects in highly doped semiconductors. A doping dependent carrier mobility model was also included as well as an electric field dependent model with Shockley-Read-Hall (SRH) carrier recombination/generation.

3 Results and Discussion

3.1 Transfer and output characteristics of simulated devices

Simulated drain current curves as a function of front gate voltage (I_d-V_{fg}) at low (V_d = - 50 mV) and high drain bias (V_d = - 1 V) are presented in Fig. 2a (left -axis) for a structure with F_w = 10 nm, F_h = 45 nm, ε_r = 1.7, N_d = 10^{19} cm^{-3}, and L = 500 nm. The right axis shows the calculated transconductance $g_m = \left(dI_d/V_{fg}\right)$ which can be indicative of device sensitivity. This figure illustrates the different JNT conduction regimes: (i) $V_{fg} >> V_{th}$ for flatband V_{fb}, the point at which the current is $I_d = q\mu N_d(F_w F_h)V_d/L$ (q: charge and μ: hole mobility) and the JNT becomes a simple resistor, (ii) $V_{fg} < V_{fb}$ accumulation, (iii) $V_{fg} = V_{fb}$ flatband, (iv) $V_{fb} < V_{fg} < V_{th}$ partial channel depletion, and (iv) $V_{fg} = V_{th}$ threshold. Fig. 3b shows the I_d-V_d output characteristics for devices with F_w = 10 nm, F_h = 45 nm, L = 500 nm, N_d = 10^{18} cm^{-3} and two different gate dielectrics ε_r = 1.7 (organic monolayer) and ε_r = 3.9 (SiO_2). We can see the normal operation of a p-type junctionless device transitioning from linear to saturation regimes as the drain voltage increases toward more negative values. As expected, below threshold ($V_{fg} > V_{th}$) the p-doped device is off and the drain current I_d drops to very low values. As the gate voltage increases the channel becomes depleted of majority carriers (holes) and shuts off even for increasing negative drain voltages. Above V_{th}, as the drain voltage is increased (towards higher negative drain voltage values) the height of the potential barrier that impedes carriers' flow (hole conduction current) through the channel is decreased and the current increases in a linear fashion with increasing V_d until saturation is reached. At saturation, the drain current I_d reaches a constant value independent of the drain bias V_d. The gate potential efficiently modulates the channel conductance and shuts-off the

JNT device for both dielectrics. Fig. 2 curves are representative of all simulated devices to be presented here.

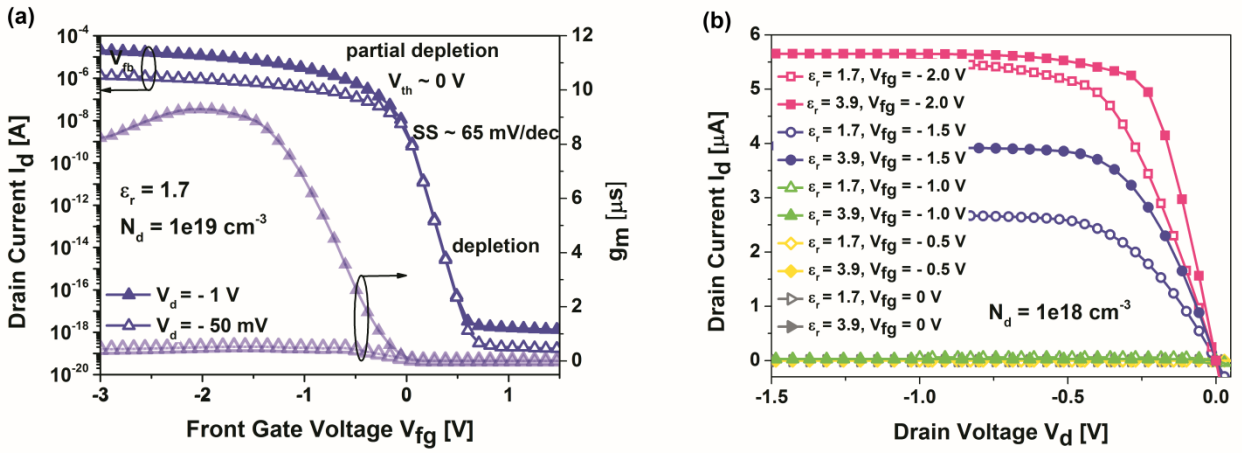

Figure 2a I_d-V_{fg} (left) and g_m (right) at low (V_d = - 50 mV) and high (V_d = -1 V) drain potentials for a device with F_w = 10 nm, F_h = 45 nm $N_d = 10^{19}$ cm^{-3}, ε_r = 1.7 and L = 500 nm. **3b**. I_d-V_d output characteristics for V_{fg} = -2, -1.5, -1, -0.5, and 0 V for a devices with F_w = 10 nm, F_h = 45 nm L = 500 nm for $N_d = 10^{18}$ cm^{-3} for different gate dielectrics.

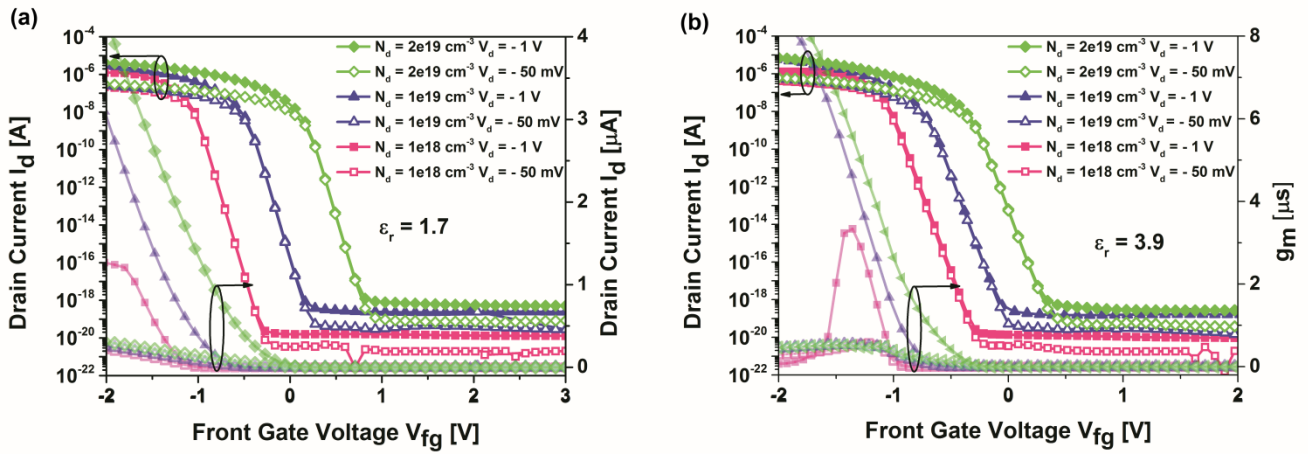

Figure 3. I_d-V_{fg} curves (log scale left) at low (V_d = - 50 mV) and high (V_d = -1 V) drain potentials for a device with $F_w = F_h$ = 10 nm, L = 500 nm and increasing N_d for a device with ε_r = 1.7 **(a)**, ε_r = 3.9 **(b)**. The right axes of **(a)** shows the respective linear I_d-V_{fg} curves and **(b)** the transconductance g_m.

The simulated I_d-V_{fg} for structures with $F_w = F_h$ = 10 nm, length L = 500 nm and different channel doping concentrations $N_d = 10^{18}$ cm^{-3}, 10^{19} cm^{-3}, 2x10^{19} cm^{-3} are shown for two different gate dielectrics ε_r = 1.7 (Fig. 3a) and for SiO_2 ε_r = 3.9 (Fig. 3b). The right axes (light

shade) shows the linear I_d-V_{fg} curves (Fig. 3a) and calculated transconductance (Fig. 3b) respectively.

3.2 Sensitivity

Enhancement mode SiNW/Fin FET-based sensors have been found to be extremely sensitive to surface charge perturbations and their sensitivity changes as a function of F_w, F_h and L dimensions [27-32]. In particular, the sensitivity of these structures increases as a function of increasing surface to volume ratio [33]. For such devices, when the cross sectional dimensions are comparable to the screening length λ_D molecular gating is more efficient and better control of the conducting channel is achieved. Nanometer-scale cross-sections lead to depletion or accumulation of carriers in the bulk of the device when a charged biomolecule binds to the surface, versus surface-only modulation for ISFET planar sensor [33-36]. As the channel doping concentration determines the Debye length ($\lambda_D \propto \sqrt{1/N_d}$) for these NWs it has been shown in literature that lightly doped channels exhibit greater sensitivities than highly doped or undoped [28-30].

Typically, sensitivity is defined as the relative variation of current (or conductance G) $S = (I_{d\psi 0} - I_{d\psi 1})/\, I_{d\psi 0}$ due to a difference in the external potential (here, $\Delta\Psi = (\Psi_1 - \Psi_0) = 110\, mV$). Fig. 4a shows S and I_d as a function of overdrive voltage $V_{OV} = V_{fg} - V_{th}$ for different junctionless channel doping concentrations and $F_w = F_h = 10$ nm, $\varepsilon_r = 1.7$, L = 500 nm. In this figure we can see that high sensitivities (S ~ 98 %) are possible with junctionless devices with the relative sensitivity being the highest in the subthreshold regime (S > 98%). Furthermore, it is still possible to have high sensitivities (S > 80%) and measure high output currents (I_d > nA) above threshold. In this figure we can see that for devices with small cross sections (10 x 10 nm^2) the relative sensitivity does not change significantly with increasing doping concentration and the same S_{max} is observed at subthreshold. Fig. 4b also

shows that the S_{max} for thin fin devices (F_w = 10 nm) is almost unchanged with increasing F_h and only when the doping channel concentration increases to N_d = 2x19 cm^{-3} the sensitivity changes noticeably (reduction) with F_h. The maximum sensitivity for all thin F_w = 10 nm structures is still high and greater than 98%.

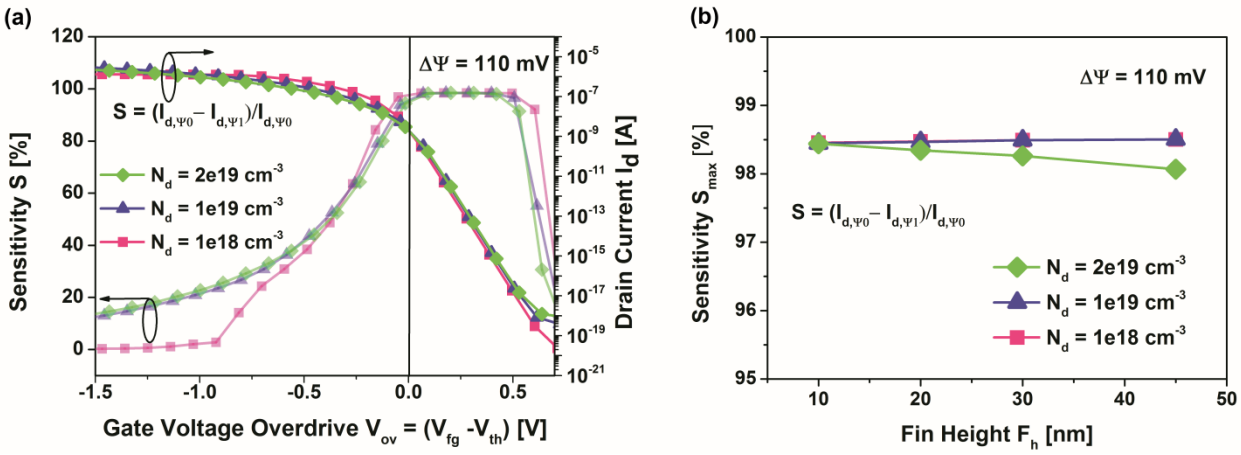

Figure 4. (a) Relative sensitivity S for junctionless devices with increasing N_d, F_w = F_h = 10 nm, ε_r = 1.7, L = 500 nm when V_d = -1 V as a function of V_{OV} (left axis) and corresponding I_d-V_{ov} (right). **(b)** Maximum sensitivity S_{max} as function of increasing F_h for different N_d with constant F_w =10 nm, ε_r = 1.7, L = 500 nm, V_d = -1 V.

Fig. 5(a) shows S and I_d as a function of V_{ov} with increasing F_w and for F_h = 10 nm, ε_r = 1.7, L = 500 nm Figure 5(b) shows the S_{max} as function of increasing F_w for different N_d when F_h = 10 nm, ε_r = 1.7, L = 500 nm. One can see from these figures that again the maximum sensitivity does not change significantly with increasing F_w except when the doping concentration increases to N_d = 2x10^{19} cm^{-3}. When N_d = 2x10^{19} cm^{-3} the S_{max} decreases considerably with increasing F_w (S_{max} = 68% for F_w = 30 nm, when N_d = 2x10^{19} cm^{-3}).

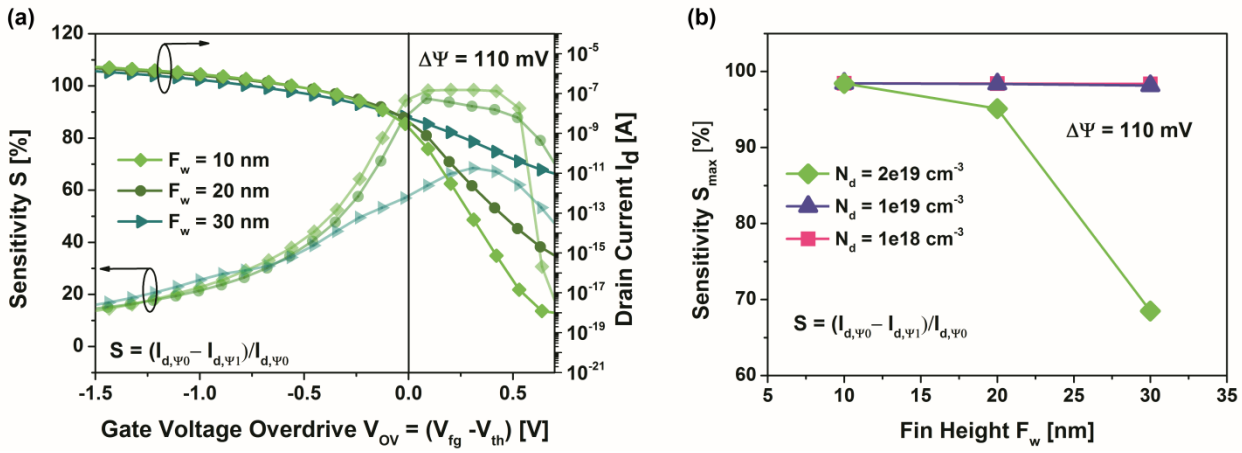

Figure 5. (a) Relative sensitivity S for junctionless devices with increasing F_w, high doping concentration N_d = 2x19 cm^{-3}, F_w = 10 nm, ε_r = 1.7, L = 500 nm, V_d = -1 V as a function of V_{OV} (left axis) and corresponding I_d-V_{ov} (right). **(b)** Maximum sensitivity S_{max} as function of increasing F_w for different N_d with constant F_h =10 nm, ε_r = 1.7, L = 500 nm, V_d = -1 V.

3.3 Threshold Voltage

In this work the threshold voltage V_{th} was defined as the voltage for which the drain current reaches a value of $I_d = (100\,nA * F_w/L)$ as it is typically defined in industry [24]. Fig. 6 shows the extracted V_{th} values for the simulated devices as a function of increasing F_h values for different N_d and with a gate dielectric constant of ε_r =1.7 (Fig. 6a) and ε_r = 3.9 (Fig. 6b) while keeping constant F_w = 10 nm. Similarly, Figs. 7a and 7b show the V_{th} for different doping concentrations with increasing F_w and increasing junctionless channel length respectively (ε_r = 1.7 and F_h = 10 nm).

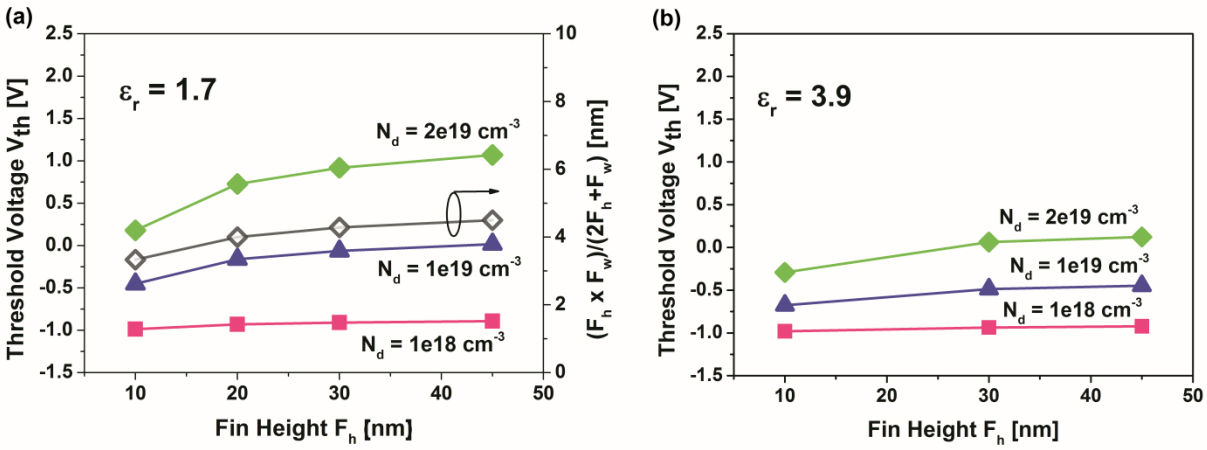

Figure 6. V_{th} variation as a function of F_h for different N_d for devices with constant F_w = 10 nm, L = 500 nm, V_d = -1 V for an insulator dielectric ε_r = 1.7 **(a)** ε_r = 3.9 **(b)**. The right axis (open symbols) in **(a)** shows the corresponding fin cross sectional area to effective width ratio $(F_w F_h)/(2F_h + F_w)$ as a function of F_h.

For good electrostatic control, the cross section area $(F_h F_w)$ needs to be small enough to allow depletion of carriers and efficiently turn-off the JNT [17]. Figs. 6 and 7a show that for increasing doping concentrations it is harder to turn off the device for a given F_w and F_h. The threshold voltage increases and goes from negative towards more positive values as the fin height and doping concentrations increase in agreement with literature results [37]. For low doping concentrations the V_{th} variation is minimal nevertheless for all F_h, F_w, L and it changes the most when $N_d = 2x10^{19}$ cm^{-3}. When $N_d = 10^{18}$ cm^{-3}, and ε_r = 1.7, the threshold voltage shift is ΔV_{th} = 0.093 V with increasing F_h from 10 to 45 nm, whereas when $N_d = 2x10^{19}$ cm^{-3} ΔV_{th} = 0.890 V (Fig. 7a). For low doping levels, the side gates are enough to completely deplete the channel; the top gate does not have any impact, which translates into V_{th} depending only on F_w. With a high doping level, the side gates are not enough to deplete completely the channel, which translates into V_{th} depending more on the height (relates to the thickness that the top gate has to deplete in order to turn off the device). The V_{th} variation with F_h and F_w is not as pronounced for devices with SiO_2 dielectric constants

(ε_r = 3.9, Fig. 6b and S1 in the supporting information), *i.e.*: when $N_d = 2x10^{19}$ cm^{-3}, ΔV_{th} = 0.414 V as the F_h is increased from 10 to 45 nm (Fig. 6b), almost 50% less than when ε_r = 1.7 (Fig. 6a). Though threshold voltage variation increases with doping concentration, it is also not as pronounced for devices with fin widths of 10 nm in accordance with previous literature results that have shown that for small cross section structures (< 10x10 nm^2) the V_{th} change with doping concentration is almost negligible [38]. It is therefore possible to reduce threshold voltage variability because device layer thickness reproducibility is not an issue: current SOI technology allows for the manufacture of wafers with ultra-thin silicon device layers (below 50 nm) with tight uniformity specifications within a few Angstroms (6 sigma range of less than 1 nm), below 2% [39]. The variation in the width highly depends on process variation (lithography, etching), and could therefore be more problematic than the thickness variation.

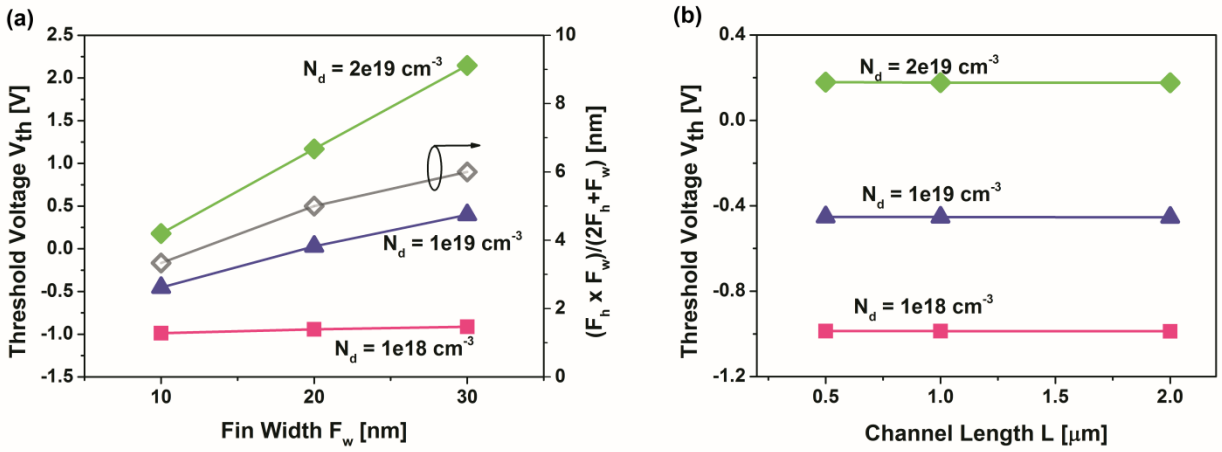

Figure 7. V_{th} variation as a function of increasing F_w **(a)** with constant F_h = 10 nm, L = 500 nm, V_d = -1 V and increasing L **(b)** with constant F_w = F_h = 10 nm, V_d = -1 V for different N_d and gate insulator dielectric ε_r = 1.7. The right axis of **(a)** shows the corresponding fin cross section area to effective width ratio $(F_w F_h)/(2F_h + F_w)$ as a function of increasing F_w.

The effect of F_w and F_h on the threshold voltage of a JNT has previously been investigated in literature. For example, Doria *et al.*,[15], and de Souza *et al.*,[37] derived an analytical

model that relates the threshold voltage to the fin cross sectional area ($F_w F_h$) and effective width ($2F_h + F_w$) from a 2D solution of the Poisson equation for a gate-all-around structure. Eq. 2 shows de Souza's derivation for V_{th} of a junctionless transistor. Here, $\hbar$ is the normalized Plank's constant, m* is the effective carrier mass, ϕ_{MS} is the work function difference between the gate material and silicon, ε_{si} is the silicon permittivity, q is the electron charge, C_{ox} is the gate dielectric capacitance per unit length and c is a fitting parameter that characterizes the corner capacitances [15, 37]. We can see that the geometrical characteristics of the device greatly influence the operation regime as found throughout our simulation results. In particular, it is worth noticing that the V_{th} is strongly influenced by the fin width due to the quadratic dependence of the second part of the equation shown below. Fig. 6a and 7a show the $(F_w F_h)/(2F_h + F_w)$ ratio as a function of F_h and F_w (right axes) respectively. In agreement with our results the threshold voltage depends on the F_w, F_h, N_d, C_{ox} (Eq. 1) and ϕ_{MS}.

$$C_{ox} = \varepsilon_r \left(\frac{F_w + 2F_h}{t_d} + c \right) \quad (1)$$

$$V_{th} = \phi_{MS} - qN_d \left(\frac{F_w F_h}{C_{ox}} + \frac{1}{\varepsilon_{Si}} \left(\frac{F_w F_h}{2F_h + F_w} \right)^2 \right) + \frac{\pi^2 \hbar^2}{2qm^*} \left(\frac{1}{{F_h}^2} + \frac{1}{{F_w}^2} \right) \quad (2)$$

Nonetheless as can be seen in Fig. 8a, the V_{th} trend as a function of F_w does not seem to correlate well with the model. Our results show a much greater V_{th} shift as the fin width increases from 10 to 30 nm in particular for high N_d. For $N_d = 10^{18}$ cm^{-3} the threshold voltage shift with increasing F_w is $\Delta V_{th} = 0.075$ V and when $N_d = 2\text{x}10^{19}$ cm^{-3} $\Delta V_{th} = 1.967$ V in comparison to the V_{th} shift as the fin height increases from 10 to 30 nm $\Delta V_{th} = 0.739$ V when $\varepsilon_r = 1.7$.

Since the working principle of a junctionless transistor is quite different from that of a typical inversion or accumulation mode device, it is not surprising that the definition of

threshold voltage should as well be different. One definition that can still be used is the gate potential at which mobile charge density Q_m is cancelled. With this definition in mind, from a charge based analytical model for a JNT double gate MOSFET (DG MOSFET) Sallese *et al.*,[17] derived Eq. 3 for V_{th} which includes both linear and logarithmic contributions on the doping concentration (influencing the V_{th} in opposite ways) and a linear dependence on the thickness of the semiconductor T_{si}. Here, $U_T = kT/q$, n_i is the intrinsic doping concentration.

$$V_{th} = \phi_{MS} + U_T \cdot ln\left(\frac{N_d}{n_i}\right) - q \cdot N_d T_{Si} \cdot \left(\frac{1}{2C_{ox}} + \frac{1}{8C_{Si}}\right) \quad (3)$$

This equation illustrates the unusual non-monotonic variation of the threshold voltage with doping concentration N_d for junctionless transistors that can also be seen in the I_d-V_{fg} curves in Figs. 6 and 7. One can also see that it is possible to find the best doping density N_d and thickness combination for a given V_{th} and dielectric which makes junctionless NWs attractive for biosensor applications.

Holtij *et al.*,[40] investigated the V_{th} variation as a function of increasing L. They found that the threshold voltage decreases considerable with decreasing L for L < 100 nm with the change being particularly drastic for channel gate lengths below 22 nm. Our simulation results do not show a strong V_{th} dependence with increasing gate length L for the long channel devices investigated here (0.5 – 2 μm) as shown in Fig. 7b. Holtij *et al.*,[40] defined the threshold voltage as the gate bias at which the value of the minimum potential equals the value of the Fermi potential at which point the mobile charge density equals the fixed charge density. At this point, a neutral region forms inside the channel and current begins to flow from source to drain in the bulk. From this assumption they derived an expression for the

threshold voltage V_{th} and found analogous trends as the ones presented here for their n-type devices [40]. The same trends for V_{th} were found for low drain potentials V_d = - 50 mV.

3.4 Drive Current

When comparing devices with the same geometry and channel doping concentrations but different gate insulator materials we can see that when ε_r = 1.7 (Fig. 8a shows the I_{on}/I_{off} ratio as function of increasing F_w with constant F_h = 10 nm, Figure S3a in the supporting information shows the I_{on}/I_{off} as a function of increasing F_h with constant F_w = 10 nm with different doping concentrations) only devices with a doping concentration of $N_d = 10^{18}$ cm^{-3} or with a sufficiently small channel cross section ($F_w = F_h$ = 10 nm) can be efficiently turned off at V_{fg} = 0 V ($I_{on}/I_{off} > 10^{13}$). I_{off} (off-state, drain-leakage) is the current I_d at V_{fg} = 1e-10 V. The on-state current I_{on} is defined as the value of the drain current at $V_{fg} = -3$ V. All other devices with ε_r = 1.7 are normally on at V_{fg} = 0 V or have a much smaller I_{on}/I_{off} current ratios $< 10^4$ (10^6 for F_w = 10, F_h = 20 nm, for high drain potentials V_d = - 1 V and $N_d = 10^{19}$ cm^{-3}). When the insulator dielectric constant is increased to ε_r = 3.9 (Figure 9b shows I_{on}/I_{off} as a function of increasing F_h with constant F_w = 10 nm with different doping concentrations) devices can be turned off at V_{fg} = 0 V even for higher doping concentrations of $N_d = 10^{19}$ cm^{-3} as the higher gate capacitance offers better electrostatic control and the electric field from the gate is capable of completely depleting the channel of carriers.

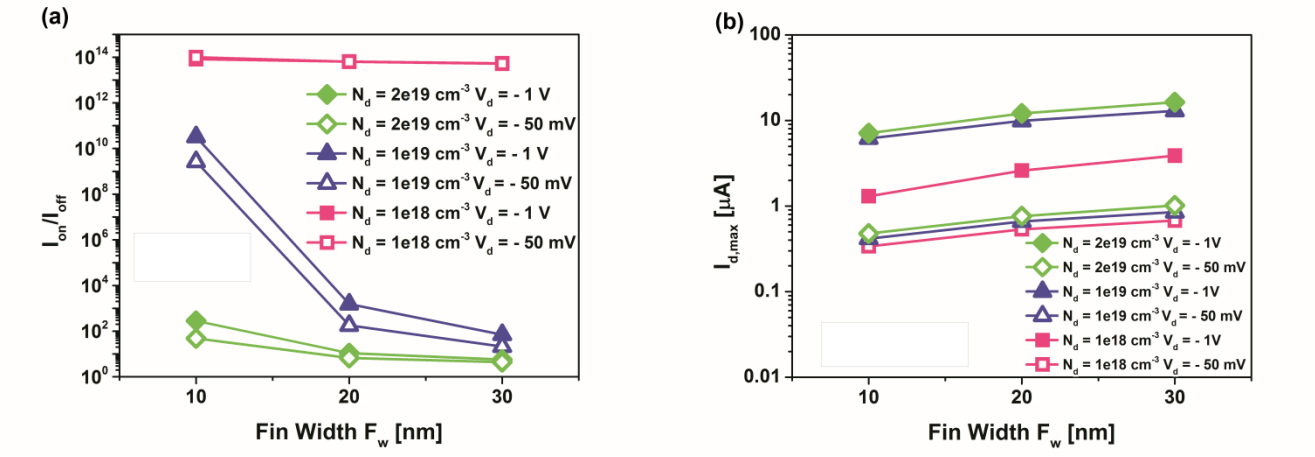

Figure 8. I_{on}/I_{off} **(a)** and $I_{d,max}$ **(b)** variation as a function of increasing F_w for different doping concentrations for devices with gate insulator dielectric ε_r = 1.7, constant F_h= 10 nm, L = 500 nm.

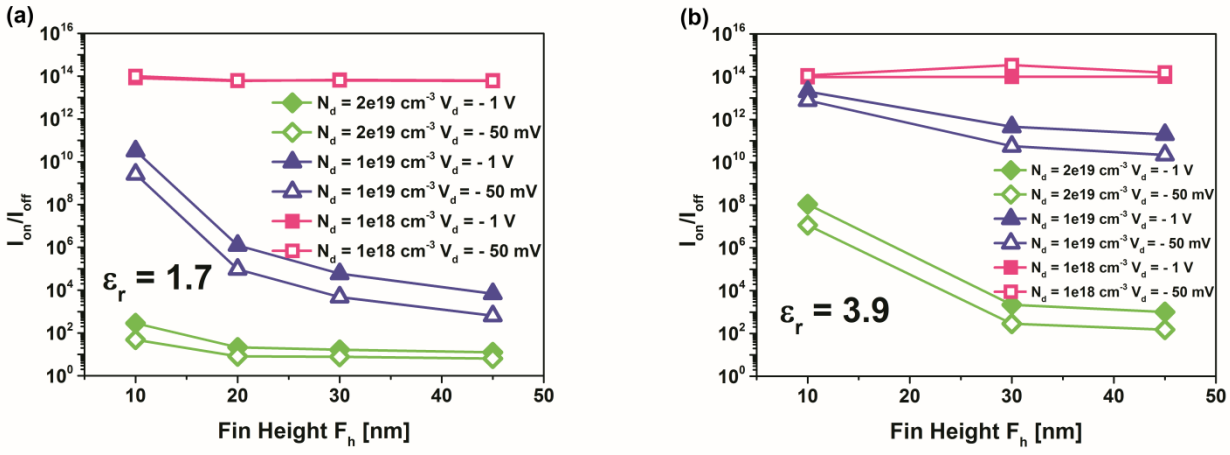

Figure 9. I_{on}/I_{off} variation as a function of increasing F_h for different doping concentrations constant F_w = 10 nm, L = 500 nm for devices with gate insulator dielectric ε_r = 1.7 **(a)** and ε_r = 3.9 **(b).**

As a general trend, the maximum current $I_{d,max}$ increases with increasing doping concentration N_d (Fig. 9b), F_h (Figure 9a shows the $I_{d,max}$ as a function of increasing F_h for different doping concentrations with constant F_w = 10 nm, L = 500 nm and ε_r = 1.7) and F_w (Figure 9b). The $I_{d,max}$ also decreases for increasing channel lengths L (Figure 9b shows the $I_{d,max}$ as a function of increasing L for different doping concentrations with constant F_w = F_h = 10 nm, and ε_r = 1.7) as expected due to the higher total resistance of higher channel lengths.

3.5 Short Channel Effects

The drain induced barrier lowering (DIBL) is the induced reduction in threshold voltage at high drain voltages. The DIBL occurs when the height of the energy barrier that impedes carrier's flow through the channel for a gate potential below threshold is reduced by the electric field induced by the drain potential. Higher drain bias decreases the potential barrier and a conduction channel will form at lower gate potentials therefore decreasing the threshold voltage. The DIBL is defined as $DIBL = \frac{V_{th}|_{V_{d,low}} - V_{th}|_{V_{d,high}}}{V_{d,low} - V_{d,high}}$ with $V_{d,high}$ = -1 V and $V_{d,low}$ = -50 mV. The DIBL for all junctionless transistors overall was found to be relatively small (< 100 mV) which has been attributed to the absence of doping junctions for much shorter effective channel devices (< 20 nm).[55] As can be seen in Fig. 10, the DIBL increases with increasing junctionless channel doping concentration and increasing F_w. Small DIBL values (< 40 mV) can be achieved for low doping concentrations and small channel cross sections 10x10 nm^2. The DIBL variation with increasing fin width is particularly pronounced for high doping concentrations, increasing from 18 to 107 mV as the F_w increases from 10 to 30 nm with a constant F_h =10 nm for ε_r = 1.7. In comparison, the DIBL seems to be quite insensitive to increasing F_h (when F_w =10 nm) with constant DIBL values of 7, 15 and 17 mV for N_d = 1x10^{18} cm^{-3}, 1x10^{19} cm^{-3} and 2x10^{19} cm^{-3} respectively.

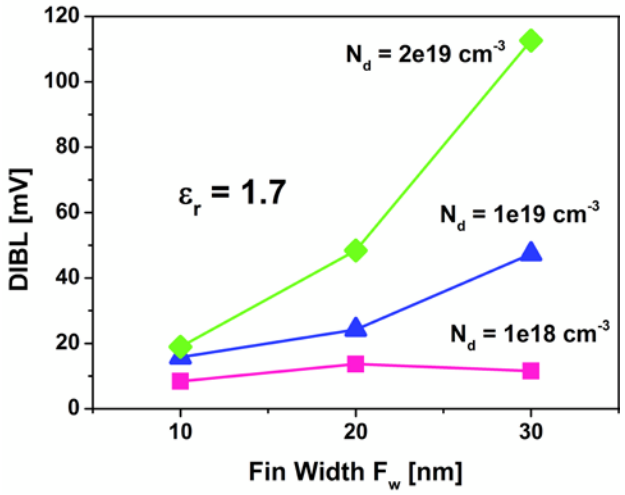

Figure 10. DIBL variation as a function of increasing F_w for different doping concentrations for devices with gate insulator dielectric $\varepsilon_r = 1.7$, $F_h = 10$ nm, $L = 500$ nm, $V_d = -1$ V.

3.6 Subthreshold Slope

The subthreshold slope SS (Eq. 4) gives us an idea of the switching capabilities of a transistor. As the depletion width W_{dm} extends through the bulk of the semiconductor channel the capacitance ratio $C_{dm}/C_{ox} \sim (\varepsilon_{si} t_{ox}/\varepsilon_r W_{dm})$ should be relatively small making the SS small as well (60 mV/dec at room temperature is the minimum value for standard transistors).[53] From Eq.4 one can see that the SS is also affected by the gate insulator dielectric constant.[54] The SS is slightly degraded for devices with a gate insulator $\varepsilon_r = 1.7$ (Fig. S5a) *vs*. $\varepsilon_r = 3.9$ (Fig. S5b) as expected.

$$SS = \frac{kT}{q}\left(\frac{d(log_{10} I_d)}{dV_G}\right)^{-1} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \quad (4)$$

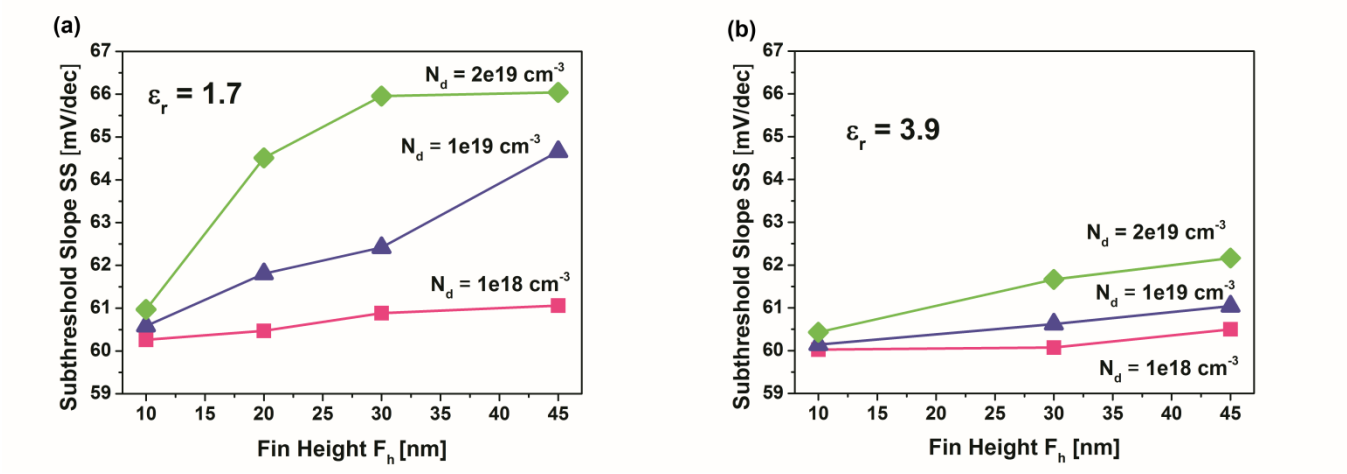

Figure 11. Subthreshold slope SS as a function of increasing F_h for different doping concentrations for devices with gate insulator dielectric ε_r = 1.7 **(a)** and ε_r = 3.9 **(b)** with constant F_w = 10 nm, L = 500 nm, V_d = -1V.

As can be seen in Figs. 11 and 12, the subthreshold slope (from $SS = dV_G/d(\log_{10} I_d)$) reaches the thermal limit of MOSFETs for all studied structures with a fin width F_w = 10 nm (SS < 67 mV/dec). It degrades with increasing F_h (Fig. 11), F_w (Fig. 12a), L (Fig. 12b), and doping concentration. This effect is less pronounced for structures with a silicon dioxide gate dielectric ε_r = 3.9 as anticipated. The SS changes most dramatically as the F_w is increased from 10 (SS = 60.97 mV/dec) to 30 nm (230.07 mV/dec) for high channel doping concentrations $N_d = 2x10^{19}$ cm^{-3} and ε_r = 1.7. The subthreshold slope also increases slightly with increasing channel lengths (Fig. 12b shows the SS as a function of increasing L for different doping concentrations when $F_w = F_h$ = 10 nm, ε_r = 1.7, V_d = -1V). The SS degradation is much more pronounced for structures with higher doping concentrations $N_d = 10^{19}$, $2x10^{19}$ cm^{-3}. This is understandable as the higher the doping concentration the stronger the induced electric field for channel carrier depletion and efficient turn-off. This is in accordance with previous literature results. Not surprisingly, we find analogous changes in the sensitivity with F_h and F_w, degrading in the same fashion as the subthreshold slopes as previously discussed.

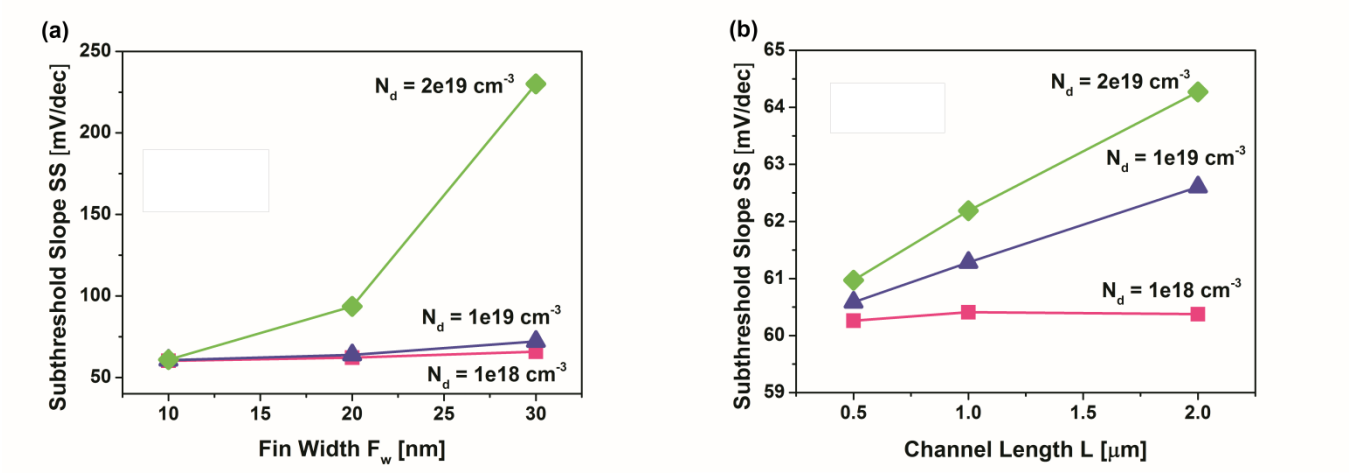

Figure 12. Subthreshold slope SS as a function of increasing F_w **(a)** and increasing L **(b)** for different doping concentrations and V_d = -1V for devices with gate insulator dielectric ε_r = 1.7.

3.7 Transconductance

The maximum transconductance $g_{m,max}$ and transconductance values at V_{fg} = 0 V, $g_{m,Vfg=0V}$ were extracted from the simulated I_d *vs.* V_{fg} curves for high and low drain potentials. The transconductance reaches a maximum and then decreases (Fig. 2a shows this graphically), but in comparison to inversion mode devices the decrease in transconductance with gate voltage is not as pronounced.[30] This is because of the reduced transverse electric field to the current flow that characterizes junctionless devices. The maximum transconductance increases with F_h (Fig. 13a), generally with F_w (Fig. 14a) except for high N_d and decreases with increasing channel length (Fig. 14b). The effect of doping concentration in the maximum transconductance is not as straight forward, Fig. 13a and 14a show this. At low drain bias (V_d = 50 mV) the maximum transconductance increases with decreasing N_d. For high drain bias (V_d = -1 V) the highest maximum transconductance values happens at $N_d = 10^{19}$ cm^{-3}. The scattering rate is dominated by impurity scattering in the heavily doped channels of the junctionless transistor.[49] For low drain bias carrier scattering is more pronounced for channels with higher doping concentrations and hence the lower maximum transconductance. The

same effect can be seen for longer channels as there is a greater chance for carrier recombination, hence the lower transconductance values.

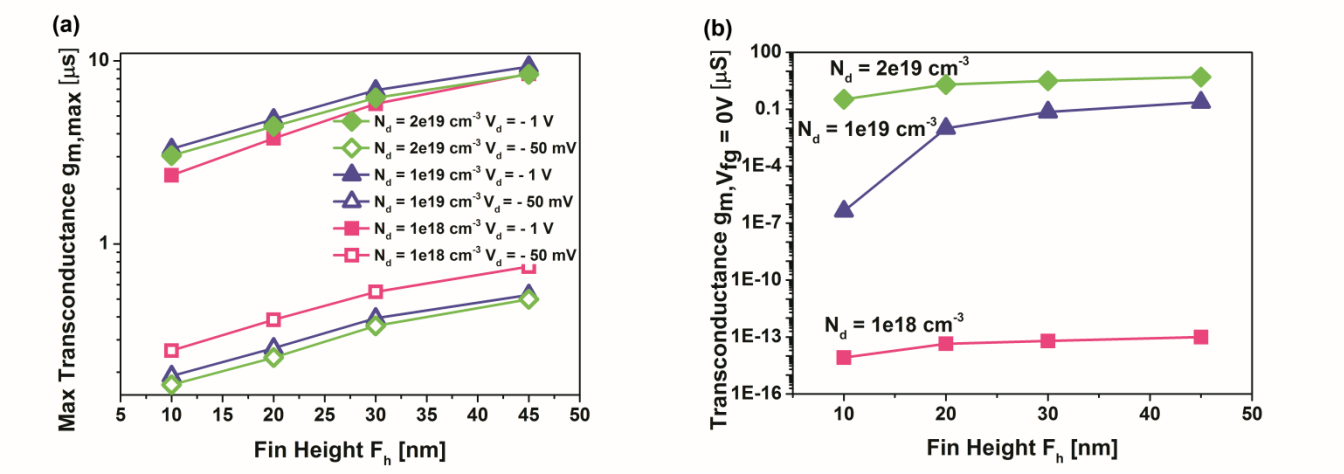

Figure 13. Maximum transconductance values $g_{m,max}$ **(a)** and transconductance values when V_{fg} = 0 V, $g_{m,Vfg=0V}$ **(b)** as a function of increasing F_h for different N_d for devices with gate insulator dielectric ε_r = 1.7, F_w =10 nm, L = 500 nm.

The transconductance $g_m = (dI_d/dV_{fg})$ is a measure of the sensitivity to surface charges. A high transconductance value means a bigger change in drain current for a given change in surface charge which can translate to higher device sensitivities. Transconductance values when V_{fg} = 0 V could be of particular importance for this study as we seek to eliminate the reference electrode needed to establish a liquid potential for high sensitivity. Fig. 13b and 14b show $g_{m,Vfg=0}$ as a function of increasing F_h increasing F_w respectively for different doping concentrations for devices with gate insulator dielectric ε_r = 1.7. The highest transconductance values when V_{fg} = 0 V are achieved when ε_r = 1.7, $N_d > 10^{19}$ cm^{-3}, high F_h and thick F_w.

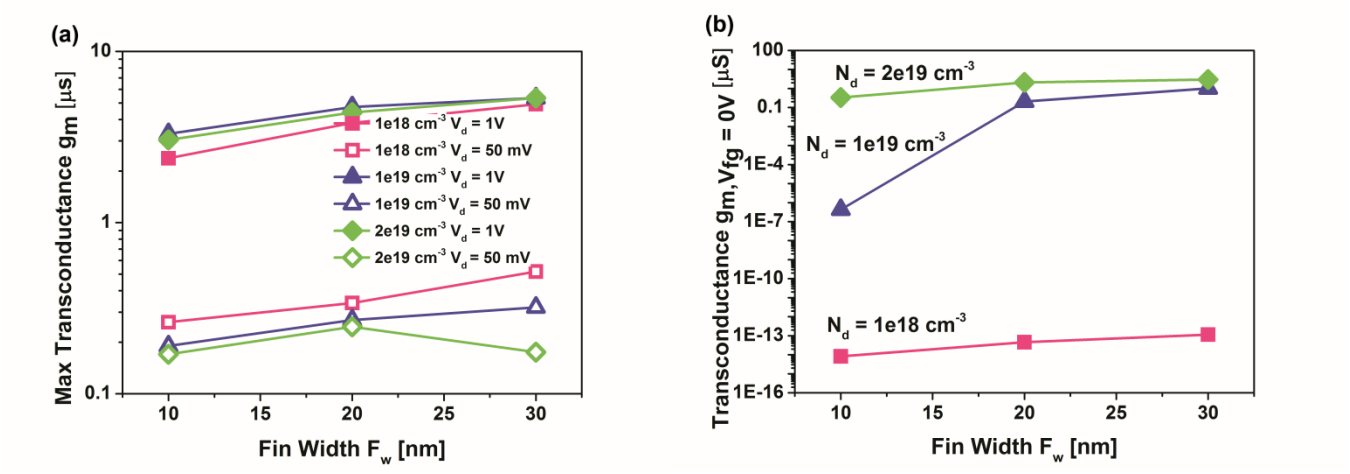

Figure 14. Maximum transconductance values $g_{m,max}$ **(a)** and transconductance values when V_{fg} = 0 V, $g_{m,Vfg=0V}$ **(b)** as a function of increasing F_w for different N_d for devices with gate insulator dielectric ε_r = 1.7, F_h =10 nm, L = 500 nm.

4 Conclusions

Silicon nanowire FET based sensors have great potential for the direct and specific measurement of biological entities at ultra-low concentrations in completely miniaturized, low power, possibly implantable systems. Junctionless nanowire sensors may allow the successful integration of such devices into a myriad of systems due to their tunable electrical characteristics. Also, having no doping concentration gradients simplifies the fabrication process, reduces variability and thermal budget requirements since there is no impurity diffusion during thermal processing steps. The use of heavily doped channel devices is also advantageous due to the inherent reduction of dopant fluctuations that will therefore reduce variations in the electrical characteristics of the junctionless device.

It is important when designing the next generation of junctionless FET sensors to select the device geometry and doping concentration that can be made reproducibly. Also, to select the device that allows for high drain currents, high transconductance g_m values in the absence of a local/reference electrode potential (when V_{fg} = 0V), that leads to the operation of the FET in the high sensitivity regime (subthreshold) around V_{fg} = 0 V with a V_{th} value ~ 0 V for the dielectric gate insulator of interest. From the simulations conducted here we found a few choices that meet all of these requirements for each dielectric. For ε_r = 1.7 the most interesting devices are the ones with fin width F_w = 10 nm and height F_h = 30 and 45 nm, doping concentration of N_d = $1x10^{19}$ cm^{-3} and length L = 500 nm. They have high transconductance values of $g_{m,Vfg=0V}$ of 71 and 233 nA/V, respectively, V_{th} ~0V for high sensitivities with high output currents. Devices with the same geometries are also interesting for ε_r = 3.9 except that a higher doping concentration of N_d = $2x10^{19}$ cm^{-3} is necessary to have V_{th} around ~ 0 V, increasing at the same time the drain current. Looking at a broad parameter

space our results provide useful guidelines for tuning the design of FET nanowire sensors in the low-power and high-sensitivity operation regime.

5 Outlook and Planned Activities in Task 3.2

To complete the work in Task 3.2, the following activities are foreseen

- N-type enhancement SiNW devise is currently being investigated by 3D TCAD simulations for comparison purposes.
- TCAD device simulations to provide guidelines (geometrical dimensions, doping concentrations) for future fabrication endeavours of SiNW JNT sensor by WP2 partners.
- Further development of the atomic-scale simulators, extraction of the work function and relation to the threshold voltage as a figure of merit.
- Publications in progress.

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