3.1 Publishable summary

Project content and objectives

In the last years, the NVM market has been characterized by a continuous growth in term of units shipped and of revenues for semiconductor companies. This large increase of the demand of solid-state, low power non-volatile devices is related to the huge development of mobile applications and portable equipments that are becoming a large part of the sold electronic systems.

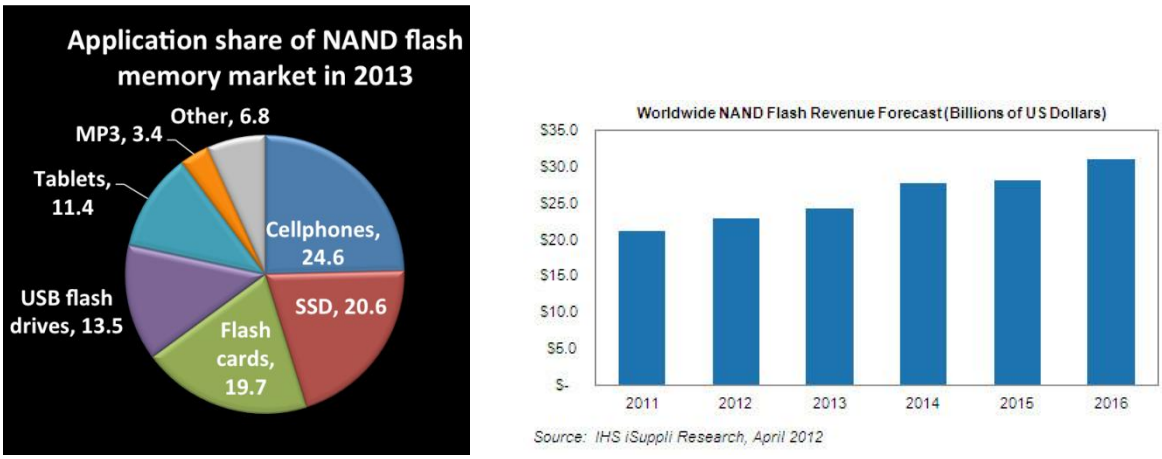

Fig. 1: NAND flash memory by application (http://blog.virtium.com/samsung-and-toshiba-retain-nand-flash-market-share-leadership-in-2012/) on the left hand side. On the right side forecast revenue for NAND flash market.

In the last period, the non-volatile memory market is characterized by an average growth rate of about 15% per year, mainly due to the request for data storage devices. In fact, the NOR Flash market, mainly related to the code storage applications, has shrunk in the last years, while NAND Flash technology has continued to grow despite the difficult economic environment. This different growth rate is mainly related to the fact that NAND Flash represents the mainstream technology for data storage applications, thus being driven by the huge amount of storage memory required in today's applications for digital photos, tablet, MP3 and digital data in general. Moreover, this trend is expected to continue in the next years, mainly driven by the diffusion of digital video system and high definition devices, with the resulting increase of the amount of stored data in the electronic devices. According to this scenario, in the next years the non-volatile memory market will be thus dominated by those technologies that will be able to guarantee the lowest cost per Gbit improving their performance. However NAND technology is very low performer and it is usually used coupled with a fast high performance DRAM to ensure a quick communication with the bus and the processor. In this context, the concept of storage class memory (SCM) is coming up as an intermediate solution between performance and cost as reported in Fig. 2, being a good compromise between the two and coming very close to the universal memory concept. In particular latency time (time required to read a bit in random access mode) plays a major role in enhancing the performance at the system level. NAND has a latency time of about 50 µs, while DRAM is about 20 ns. Phase change memory is the ideal candidate to be used featuring an intermediate latency time in the range of 50 ns -100 ns, thus being able to fill this gap. However, today PCM are limited by the high programming current required that has several implication on cost, performance and reliability. The PASTRY project aims to the investigation of a novel kind of non-volatile memory device, featuring low power consumption if compared with standard chalcogenide-based memories

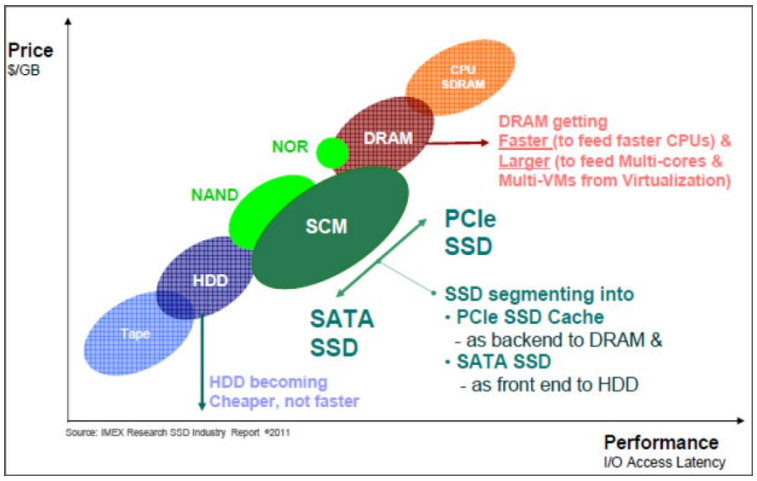

Fig 2: SCM allow lower cost than DRAM but better performance of NAND, filling the existing gap and improving the system performance.

(PCM). The new memory concept is based on engineered Chalcogenide SuperLattices (CSL) that should allow realizing the memory switching with a modification in the bonding nature instead of the energy expensive melting process, leading to a significant reduction of both transition times and programming currents.
A significant lowering of the programming current and time implies:

- Smaller or less performing selecting transistors, thus reducing the cell size in embedded application (smaller MOS selector width), in high-density bipolar transistors-selected PCM and in ultra-high density
- Cross-point products with 3D stacking and diode selectors integrated in the back-end; allowing a multi-stack memory with a cell size of $(4/n)F^2$, where n is the number of layers.
- Improved array efficiency due to a significantly reduced width of the MOS column and row decoders
- Faster program/erase operation, in the range of few ns;
- Higher programming throughput, since the programming parallelism is limited by the program current and time needed by each cell;
- Extended reliability, reducing the temperature inside the cell and the program pulse duration, with significant improvements of endurance and thermal cross-talk disturb.

Despite the experimental evidence reported in literature [1,2,3] the physical mechanism is not yet understood. The physical mechanisms reported [3,4] are not yet fully convincing and a clear atomistic model of the phenomenon, useful for device engineering, is still missing.
The main objectives of the project are:

- A complete understanding of the nature of the switching phenomenon in CSL materials by detailed optical and structural measurements and atomistic simulations
- The development of an optimized CSL and its integration in a PCM device that allows to fulfill the "universal memory specification"
- Demonstration of the performances achieved in a fully functional 2x nm large size array and of the readiness of CSL PCM for the state-of-the-art lithographic technology node and array density
- Demonstration of the concept scalability in 1xnm functional CSL PCM cell

Universal Memory key attributes	Flash NAND	Flash NOR	DRAM	CSL PCM Universal Memory
Cell size	$2F^2$(*)	$10F^2$	$6F^2$	$4F^2$
Write-Erase	200ms/page- 2 ms/block	1 ms- 1 s/sector	20 ns	Few ns
Retention	85 C 10 y	125 C 10 y	Volatile	85C 10 y
Endurance	10^4	10^4	10^{15}	$>10^{12}$
Latency time	~50 us	60 ns	20 ns	20 ns
Bit granularity	Page	Sector	Bit	Bit
Power consumption	Low (tunnel effect)	Low (tunnel effect)	High (refresh)	Low
Readiness for production	Now	Now	Now	2016
Scalability	> 16 nm	>45 nm	>20 nm	> 10 nm

Table I: Benchmark between charge storage-based memories and CSL-based "universal memory". (*) 2bit/cell configuration

The expected advantages of the proposed solution are reported in Table I. Latency time is very low and comparable to the DRAM one. Also the cell size is very aggressive similar to the NAND single level. Performances are intermediate between NAND and DRAM, with an improved cycling compared to the first one and better retention with respect to the second one (DRAM in volatile). This set of characteristics makes the proposed solution very close to a universal memory and hence an ideal candidate for the storage class memory; the low cost, ensured by the reduced cell size, make CSL an interesting solution to make storage class memory a reality.

References:

[1] Shintani Tominaga et al., "Phase Change Meta-materials and device characteristics", E/PCOS 2010
[2] Toshimichi Shintani at al., "Properties of Low-Power Phase-Change Device with GeTe/Sb2Te3 Superlattice Material", E/PCOS 2011
[3] E Simpson, P Fons, A Kolobov, M Krbai, T Yagi, J Tominaga, "Interfacial Phase-Change Memories", Nature Nanotechnology vol. 6, pp. 501-505 (2011)
[4] Takaura, N at all., "Charge injection super-lattice phase change memory for low power and high density storage device applications", VLSI 2013

Work performed and main results

During the first year of the project, the activity was mainly related to three fields: material development (WP2), single test vehicle development (WP3) and physical model understanding of CSL structured material (WP4).
Concerning work package 2, a lot of work has been done on the deposition side by PDI and RWTH aiming to develop a suitable material. PDI focused the efforts in developing a Molecular Beam Epitaxial technique (MBE) for chalcogenide superlattice deposition (CSL). Samples were prepared on flat silicon wafer with (111) orientation. Alternation of GeTe layer and Sb_2Te_3 layers were grown with different thicknesses and deposition conditions obtaining high quality films in terms of roughness and texture. Multilayers with both GeTe and Sb_2Te_3 as a first layer were grown. The role of a first layer of antimony has been also explored to improve the texture of the film and the quality of the epitaxial layer, enabling very good quality film growth also when CSL starts with GeTe

layer. Good CSL has been grown with a number of layers up to 20 and thicknesses down to few nanometers. RWTH was, on the other hand, focused on the Plasma Vapour Deposition technique. Also in this case several samples have been realized with different numbers of layers and thicknesses. At the beginning of the project, films were deposited at room temperature. To improve the quality of the CSL, the PVD chamber was upgraded to enable high temperature deposition at 250°C improving the texture of the film. Even though the material optimization is not yet completed and it is still in progress, at the end of the first year the consortium developed sufficiently good CSL by both MBE and PVD. The quality evaluation benchmark at this level has been achieved using material metrics (i. e. roughness, minimum thickness of the single layer and texturing of the layer). The obtained layers were considered by the consortium sufficiently good to be suitable for integration in the single test vehicle developed in WP3.

During the first reporting period, work package 3 was mainly devoted to the development of a suitable single cell vehicle for the CSL material electrical evaluation with a cell size of 50 nm x 50nm. The laboratory level deposition tools (available in the consortium) are not compatible with the Fab protocol; as a consequence once the vehicle goes outside the Fab, it cannot come back into the production line after deposition by partners. Some work has thus been devoted to make the single cell vehicle suitable for this purpose, without requiring additional process steps between the CSL deposition and the electrical measurements. The single cell vehicle has thus been fabricated and a protocol for material deposition has been set-up among the partners. This working methodology has been checked depositing conventional GST materials (both by PVD in Aachen and MBE in Berlin) in the single cell vehicle, obtaining results comparable to Fab deposited GST. A study about the possible applications of CSL-based has been also provided, opening the possibility for a high performance storage class memory.

Work package 4 was devoted to the physical understanding of the CSL films. Published literature has been reviewed and a DFT-based molecular dynamics simulation tool has been set-up. Role of tetragonal Ge has been investigated by first principle consideration and simulations are able to qualitatively describe the chalcogenide superlattice behaviour. To support simulation activity, physical analysis has been also carried out. High quality transmission electron microscopy analysis has been performed highlighting the self assembly nature of chalcogenide materials that naturally tend to be in defined stacking sequence. Self assembly as a function of antimony concentration has also been studied in standard GST system. Furthermore a first XAS experiment has been performed at the synchrotron to set-up a proper methodology for characterization of CSL films.

To manage the research activities, during the first year, the project met three times. The kick-off meeting was held in Agrate, Italy in October 2012. An intermediate meeting at 6th month has been performed in Aachen in April 2013 and a first year ending consortium meeting has been held in Berlin in September 2013 after the E/PCOS conference. From scientific point of view, the project activity is aligned to the timeline declared in the document of work (part B of ANNEX I).

Regarding exploitation, the expertise developed during project execution concerns various fields and its use is of great potential interest for industrial application and future research activities of all partners. Possible target applications are identified and a potential process flow for the integration of CSL on current technology was envisaged. Progress on CSL growth by MBE and PVD is interesting not only for microelectronics applications, but also in optical applications, as well as for topological insulator and magnetic applications. First principle studies and simulations of molecular structures are useful for general comprehension of chalcogenide materials already used both in the optical and electronic data storage.

Dissemination of project results is occurring mainly in three different ways:

1) Public website about the project at the following URL: www.pastryproject.eu
2) Publication of results on papers
3) Participation to conference and workshop on the topic

To know more about the project, please contact aredael@micron.com or go to the project website.