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SEVENTH FRAMEWORK PROGRAMME

Network of Excellence

# NEWCOM#

Network of Excellence in Wireless Communications#

## FP7 Contract Number: 318306


## WP2.1 – Radio interfaces for next generation wireless systems

## D21.1 - Description of EuWIn@CTTC technical facilities and interfaces, and preliminary plan of activities

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# Executive Summary

The nature of this initial deliverable of WP2.1 ("Radio interfaces for next-generation wireless systems") is mainly descriptive and its purpose is three-fold. The first goal is introducing the EuWIn lab at large, providing detailed descriptions about its three sites (CTTC, CNIT/Bologna, CNRS/Eurecom), its goals, and the means to achieve them. The second goal is to provide an accurate report on the technical facilities that are available at EuWIn@CTTC and the interfaces through which they can be accessed. More precisely, the main assets of EuWIn@CTTC are: GEDOMIS®, which offers an experimental environment that enables the prototyping of next generation broadband wireless communication systems, which feature bit-intensive PHY-layer techniques possibly combined, if desired, with multi-antenna schemes; GNSS-SDR, which is an open source GNSS software defined receiver addressing the design and implementation of multi-constellation, multi-band GNSS receivers; and OpenInLocation, which is an open experimental environment for research on indoor location composed of a set of extremely low-cost, programmable nodes (together with their wireless interfaces and their corresponding software repository). Finally, the third goal is to present the preliminary plan of activities (first JRA proposals, web portal, web meetings, workshops, training schools, industry liaisons, demonstration activities and experimental tours) together with the lab access policies that depend on the type of applicant: the access will be essentially free and open for Newcom# partners and associated institutions, and decided on a case-by-case basis for external institutions.

The most important outcome that stems from the contents in this deliverable is that EuWIn@CTTC is now ready to start the experimental activities of WP2.1.

# Table of Contents

# 1. Introduction

EuWIn (the European Laboratory of Wireless Communications for the Future Internet) intends to become one of the durable and most successful outcomes of Newcom#. EuWIn fosters excellence in research in the field of wireless communications, and it aims at training a new generation of scientists prone to do research both from the theoretical and the experimental viewpoint.

The general theme of EuWIn is "**Fundamental Research Through Experimentation**". This motto emphasizes that the laboratory is not targeted to demonstration activities (though they might be considered sometimes); rather, the laboratory aims at making theoretical and fundamental research closer to the real world, in terms of adherence to the true problems that any new technology has to face at time of implementation, and of realism of model assumptions. As additional scope, EuWIn will represent a sort of gateway among the community of scientists doing fundamental research in the field of wireless communications, and industry.

Despite the intention to become a long-lasting initiative, EuWIn is described in this document only in terms of its plan of activities to be performed within the Newcom# course. EuWIn represents the experimental Track (Track #2) of Newcom#. EuWIn activities are devised as facilitators for the research performed within Track #1. Some of the EuWIn facilities will support the Joint Research Activities (JRAs) conducted within the Track #1 WPs. Inter-Track JRAs will be defined accordingly. On the other hand, EuWIn aims at creating a durable and self-sustainable environment that will survive after the end of Newcom#; therefore, all means to establish a structured integrated laboratory will be pursued and are described in this Deliverable.

EuWIn is composed of three sites, targeting at separate technologies and fields of experimentation: the laboratories of the research center CTTC of Barcelona (Spain), of CNIT/University of Bologna (Italy), and of the EURECOM institute of Sophia-Antipolis (France). The three institutions had developed experimental facilities in the context of other projects in the past years, and have committed to make them available to other Newcom# partners, through an integrated and open framework.

Additional Newcom# institutions, besides the three that committed towards the creation of an open laboratory context, have expressed the intention to contribute through some local experimental facilities to EuWIn: Bilkent, CNRS, PUT, UCL and UPC (third party of CTTC).

The three EuWIn sites cover aspects related to radio interfaces (mainly based on MIMO and PHY-layer algorithms) and localization techniques, at CTTC, flexible radio technologies over MIMO platforms, at CNRS/EURECOM and Internet of Things (IoT) and Smart City applications, at CNIT/UniBO. Overall, accounting for all institutions participating to Track #2, the experimental activities will deal with aspects of modulation, coding, signal processing, localization, radio channel characterization, routing, topology control.

The main scopes of EuWIn, the tools used to achieve integration within the sites, and the facilities available at each of the three sites, are discussed in Section 2 of this Deliverable. The Section also includes a short presentation of the EuWIn website, which is described in more detail in D36.1. In Section 3 the lab equipment made available at CTTC, is presented, and the objectives of the testbeds are clearly identified; two additional parallel Deliverables report on the details related to the CNIT/University of Bologna and EURECOM sites. The general parts of the three Deliverables are common to emphasize the unique scope and the

integrated strategy, while Section 3 is different for each of the three Deliverables. Section 4 shows the plan of EuWIn activities. It is detailed for the next six months, while the plans for the following two years will be described in the Deliverables due at M12. The Section also presents the policy for access to the lab facilities. The conclusions shortly discuss on the potential role of EuWIn within the scientific community and for the European industry context.

## 1.1 Glossary

| | |
|---|---|
| ADC | Analog-to-digital converter |
| CIR | Channel impulse response |
| DAC | Digital-to-analog converter |
| DDS | Direct digital synthesizer |
| DL | Downlink |
| DoA | Direction of arrival |
| DoD | Direction of departure |
| DSP | Digital signal processor |
| FBMC | Filterbank multicarrier |
| FPGA | Field programmable gate array |
| GLONASS | Global'naya navigatsionnaya sputnikovaya sistema |
| GNSS | Global navigation satellite system |
| GPL | General public license |
| GPS | Global positioning system |
| HDL | Hardware description language |
| HTML | Hypertext markup language |
| IC | Integrated circuit |
| JRA | Joint research activity |
| LTE | Long term evolution |
| LAN | Local area network |
| LNA | Low noise amplifier |
| MIMO | Multiple input multiple output |
| OFDM | Orthogonal frequency-division multiplexing |
| PAPR | Peak-to-average power ratio |
| PCB | Printed circuit board |
| PHY | Physical layer |
| RF | Radio frequency |
| RTF | Rich text format |
| RRM | Radio resource management |
| SDR | Software defined radio |
| SFDR | Spurious free dynamic range |
| SPI | Serial peripheral interface |
| TXCO | Temperature-compensated crystal oscillator |
| UL | Uplink |
| USB | Universal serial bus |
| USRP | Universal software radio peripheral |
| VGA | Variable gain amplifier |
| VSA | Vector signal analyzer |

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|---|---|
| VSG | Vector signal generator |
| WLAN | Wireless LAN |
| XML | Extended markup language |

# 2. EuWIn Scope and Activities

This Section describes the general goals of EuWIn, the types of activities planned and the policy for accessing its facilities. Short introduction to the EuWIn website structure is also given.

## 2.1 Introduction

As mentioned in Section 1, the three EuWIn sites deal with separate technical and scientific topics: Radio Interfaces (CTTC), IoT (CNIT/UniBo), and Flexible Communication Terminals (CNRS/EURECOM). However, the scope of EuWIn is to achieve an integrated laboratory able to address under a common environment the various topics of wireless communication technologies for the future Internet. To reach this goal, on the one hand the sites have been identified based on the complementarity of their competencies and facilities; on the other, some technical topics are common to two EuWIn sites, thus facilitating the integration of competencies and procedures: localization techniques are a common topic for CTTC and UniBO; MIMO based platforms for testing purposes are available at both EURECOM and CTTC; heterogeneous architectures and technologies for the IoT are considered both at UniBO and EURECOM sites.

All Newcom# institutions will be allowed to take advantage of this integrated (yet distributed) laboratory, through an open access policy described below. The procedures for the coordinated access to the lab facilities are also introduced in this Deliverable, and implemented through the EuWIn website. Newcom# associate partners will also be allowed to have access under agreed conditions, while institutions external to the Newcom# environment will undergo specific and selective agreements as described below.

The vision of EuWIn can be represented through the spheres shown in Figure 2-1.

The inner sphere includes the three EuWIn sites. The integration of facilities and coordination of activities is under the responsibility of the EuWIn Director, Roberto Verdone (CNIT/UniBO). The three institutions, as detailed later, have been working during the first semester of Newcom# to extend and integrate their pre-existing facilities, creating the tools for their use by the rest of the Network of Excellence.

The second “internal” sphere includes all Newcom# institutions (the figure emphasizes those who, at time of DoW preparation, expressed commitment towards EuWIn. During the three years of Newcom# the set of these institutions might change). All Newcom# institutions have access to the EuWIn facilities, according to the open access policy defined later, free of charge.

The third “internal” sphere includes the associate partners of Newcom#, both those defined at time of DoW preparation (mainly industries) and those accepted by the consortium after project kick off. These institutions have access free of charge to the EuWIn facilities based on a selective process/policy described later.

Finally, the “external” sphere includes all institutions interested in having access from outside Newcom# to the EuWIn facilities. This sphere is based on a case-by-case consideration of the access conditions, which will depend on the type of activity foreseen, the facility/site of interest, etc.

At time of delivery of this document, the following Newcom# partners are involved in potential JRAs targeted at the exploitation of the EuWIn@CTTC facilities: AAU, Bilkent, CNRS, IASA,

PUT, UCL, and VUT. Moreover, the following additional institutions from outside Newcom# have declared strong interest into the EuWIn WP2.1: ACTIX, Agilent, AVEA, U-Blox, NEC Labs, Orange Labs, Renesas Mobile, Samsung, Telecom Italia, Telefonica I+D, and Thales Communications.

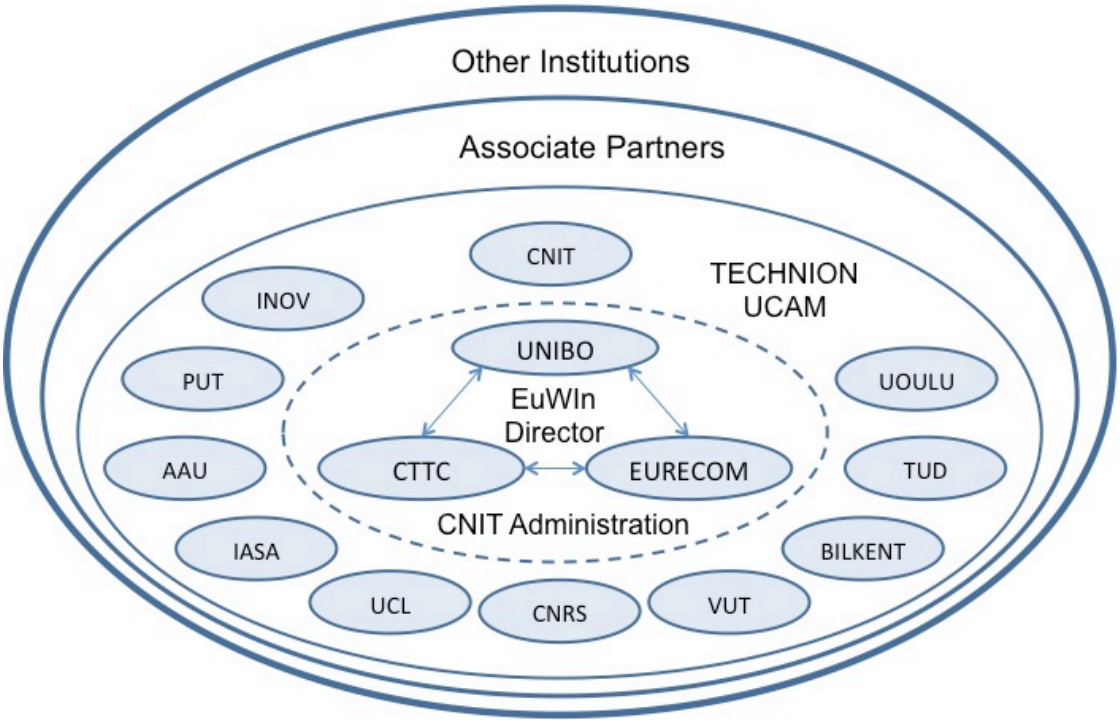



**Figure 2-1: The Newcom# Spheres.**

The EuWIn website will specify and publicize for each sphere the access policy and the procedures for a coordinated exploitation of the laboratory facilities.

## 2.2 EuWIn Goals and Lines of Action

The uttermost goal of EuWIn is the creation of a new generation of scientists willing to perform fundamental research through experimentation. Additionally, EuWIn, being one of the Tracks of Newcom#, aims at an active role within the Network of Excellence as an instrument for dissemination and link with industries.

These goals can be reached in the long term by developing instruments and activities which will allow the involvement, at different levels, of the largest possible number of researchers, from inside and outside Newcom#. EuWIn will therefore pursue its goals through the implementation of several types of actions:

1) **Real world measurements** helpful for fundamental research activities.
2) **Real world performance evaluation** of fundamental research results.
3) **Links with industries**, either associated to NEWCOM# or not.
4) **Dissemination** of NEWCOM# research outcomes.
5) **Durable integration** of resources and activities provided by NEWCOM#.
6) **World contests** open to all researchers, within and outside NEWCOM#.

These lines of action are discussed briefly in the following subsections.

### 2.2.1 Real World Measurements

Real world measurements will be useful in order to extract from them models and parameters to be used in theoretical research. Radio channel characterisation, for instance, is of outmost relevance to scientists studying the link-level performance of wireless systems; human mobility modelling, link-level assessment of the bit error rate against SNR (signal-to-noise-ratio) performance, are examples of research activities which can take advantage of measurement campaigns and are useful to the evaluation of the performance of wireless networks. All the EuWIn sites (and other Newcom# institutions) have facilities which will allow the development of measurement campaigns aimed at the definition of suitable models to be used for the performance of wireless systems, either at link or network level, as specified later. This line of activity indeed will provide *inputs* to the theoretical study of link and network level performance of wireless systems, performed within Track #1, making them more realistic in terms of models used.

### 2.2.2 Real World Performance Evaluation

Real world performance evaluation is a task performed in research either through mathematical modelling, simulation, emulation or experimentation; when the system under analysis is complex, the latter approach is the only one that is feasible. It requires flexible experimental facilities allowing the implementation of the link-level or network-level techniques/algorithms under evaluation. The EuWIn sites have developed facilities that are flexible enough in order to allow implementation of different techniques/algorithms designed by scientists performing theoretical research. This line of action therefore, will take the *outputs* of the research performed within Track #1, and provide assessment of the performance through experimentation.

### 2.2.3 Links with Industries

EuWIn will represent the main Newcom# instrument to create links with industries; the lab facilities will be used as proofs-of-concept of the techniques/algorithms designed, studied and evaluated within Track #1. Representatives from industry will be invited at all EuWIn events, and the researchers involved in the JRAs performed within EuWIn will organise visits at the premises of companies. The industry-academia link, which was missing in its predecessor Newcom++, will be established within Newcom# thanks to the availability of the EuWIn facilities and testbeds.

### 2.2.4 Dissemination

All EuWIn dissemination events, either intended for industry or academia, will have at least one of the EuWIn sites present, showing the facilities, making them available remotely, and reporting on the latest achievements. EuWIn leaflets, posters and video trailers will be generated and made available to all EuWIn researchers with the aim of creating a repository of promotional material to be used for dissemination purposes.

### 2.2.5 Durable Integration

EuWIn intends to create a framework which will go beyond the duration of the Newcom# project. To this aim, all coordination, promotional and dissemination activities will be geared towards a longer horizon than the three years of expected duration of Newcom#. However, durable integration requires financial sources which should be found outside the Newcom# budget. EuWIn will seek for additional sources of funds through the participation of the

EuWIn institutions to competitive EC calls, and from the private sector (industries willing to access the EuWIn facilities).

### *2.2.6 World Contests*

Some of the EuWIn sites (among them, the one at UniBO) will launch international contests to test over the lab facilities techniques/algorithms designed by institutions willing to participate. This will create further visibility to the laboratory, while representing a potential source of incomes for future activities after the end of Newcom#.

## 2.3 EuWIn Activities

The lines of action described in the previous subsection take the form of activities performed within Track #2 as it follows:

1) **A Unique Portal:** facilities, activities and repository of measurements;
2) **Web Meetings,** to coordinate and plan visits of researchers;
3) **Workshops** on experimental research;
4) **Training Schools** on experimental research;
5) **Industry Liaisons**;
6) **Demonstration activities:** at conferences, fairs, etc;
7) **Experimental Tours**: PhD students visiting the three sites in sequence.

Short description of the activities is given in the following subsections.

### *2.3.1 A Unique Portal*

Under the domain euwin.org, a website has been created (properly linked to the Newcom# website). The scope of the portal is to create a unique access to the laboratory, by providing shared documents, description of procedures for getting access to the facilities, and a repository of those measurement data that are shared and can be useful to the researchers involved in EuWIn activities. The website will also provide information on the events generated or participated by EuWIn, the contacts had with industries, etc.

### *2.3.2 Web Meetings*

Besides the usual web meetings held periodically by the three WP Leaders of Track2, EuWIn will organise web meetings open to all EuWIn participants in order to disseminate within the project information regarding the latest development of the lab facilities, to coordinate and schedule the access and the activities of the EuWIn-related JRAs. These web meetings will be called by the EuWIn Director depending on needs and requests, and the dates will be fixed through polls, informing all researchers at least 30 days before the meeting will take place.

### *2.3.3 Workshops*

To foster sensibility towards experimentation, EuWIn will organise workshops, with the contribution of both Newcom# researchers and scientists participating to other projects, which will aim at discussing the benefits of experimental research and compare the approaches toward open access platforms.

### *2.3.4 Training Schools*

One of the most important activities performed within EuWIn, apart from the experimental trials, is the organisation/contribution to training schools. Through the participation of EuWIn key researchers as lecturers and the organisation of experimental sessions at the schools, the attendees will be trained towards experimental research.

### *2.3.5 Industry Liaisons*

Each of the EuWIn sites will establish liaisons with specific industrial labs and companies, identified based on the topic of interest of the site. The EuWIn sites will be then responsible for the organisation of periodic meetings with the industry representatives in order to create stable contacts that might bring to forms of support to the EuWIn activities in the long term.

### *2.3.6 Demonstration Activities*

The achievements got within Newcom# and the development of new facilities, will be demonstrated at fairs, exhibitions and other events participated by many industry representatives.

### *2.3.7 Experimental Tours*

The most challenging objective of EuWIn is the creation of a generation of researchers prone to fundamental research trough experimentation, with competencies spanning over different layers of the protocol stack. This goal can be achieved by letting PhD students get involved into activities performed over the experimental facilities of different EuWIn sites, dealing with separate scientific topics. These activities will be denoted as “experimental tours”, as the students will visit different sites, performing experiments that will be properly coordinated in order to achieve a unique scientific goal through the integration of measurements achieved over separate testbeds.

## 2.4 The Three EuWIn Sites

### *2.4.1 EuWIn@CTTC*

The CTTC site (www.cttc.es) features the following three high performance testbeds, which are the core of the EuWIn@CTTC assets:

a) GEDOMIS® (GEneric hardware DemOnstrator for MIMO Systems): GEDOMIS® is an experimental platform that comprises a complete set of high performance baseband prototyping boards (FPGA and DSP-based), signal generation equipment, high-end RF front-ends, signal analysis instruments, specialized software tools and APIs. A key instrument of the testbed is the EB Propsim C8 channel emulator, which can be configured to provide realistic mobility scenarios of both certified and user-designed channel models. The Propsim C8 operates in real-time and facilitates the verification and testing of system designs prior to field-trials. Hence, GEDOMIS® offers a lab environment that enables the prototyping of next generation broadband wireless communication systems, which feature bit-intensive OFDM PHY-layer techniques possibly combined, if desired, with multi-antenna schemes. Moreover, the prototyping boards of GEDOMIS® feature various energy consumption measurement blocks, which can be used to assess the energy-efficiency for a given hardware implementation.

b) GNSS-SDR (Global Navigation Satellite System - Software Defined Radio): GNSS-SDR is an open source GNSS software defined receiver that adresses the design and implementation of multi-constellation, multi-band GNSS receivers. According to its open nature, the source code is published under General Public License (GPL) v3, which secures

practical usability, inspection, peer-review and continuous improvement by the research community, allowing the discussion based on tangible code and the analysis of results obtained with real signals. In addition to the source code, the project offers a development ecosystem (website, code repository, mailing list, bug tracker) that aims to build a community of researchers, developers and users around the project. The ultimate goal is to provide high-accuracy positioning for the masses, and for free. There are many ways for researchers to contribute to the project, e.g., programming new features (algorithms, receiver architectures, etc.), optimizing existing algorithms, reporting bugs or debugging existing features, among many others. This facility's equipment comprises an RF signal generator (Agilent's Vector Signal Generator E4438C equipped with GPS Personality), an assortment of GNSS antennas, RF measurement equipment (oscilloscope, network analyzer, spectrum analyzer), a set of Universal Software Radio Peripherals (V1 and V2) and USB data grabbers.

c) OpenInLocation (an open lab for research on indoor location): The main objectives of this lab is to drive R&D and innovation in indoor location by evaluating state-of-the-art and commercial technologies in challenging environments, improving them in terms of enabling High-Definition Situation-Aware (HDSA) applications and services, and, finally, fostering collaboration to contribute with new ideas for indoor positioning, to disseminate results and outreach to new audiences beyond Newcom#. This lab is composed of a set of extremely low-cost, programmable nodes that can act either as anchor node or as a mobile node, the wireless interfaces for such nodes (WiFi, Bluetooth, ZigBee, etc.), sensors (in IC form), and the corresponding software repository.

The common features to these three labs is that they promote collaborative research by offering an adequate framework and tools and they are all based on the principle of reproducible research, which enables practical discussions on tangible problems.

### *2.4.2 EuWIn@UNIBO*

The EuWin@UNIBO site provides more than 200 wireless nodes implementing different types of radio interfaces, and deployed according to the following platforms:

Flexible Topology Testbed (FLEXTOP) – 100 nodes equipped with IEEE 802.15.4 radios distributed inside the lab over a regular layout creating an open and flexible platform for emulating several types of network topologies, achieved through proper software setting of the inter-node losses. This platform is based on over-the-air (OTA) implementation of software, meaning that NEWCOM# partners will be given remote access to implement the software;

Data Sensing and Processing Testbed (DATASENS) – An infrastructure of approximately 100 nodes using IEEE 802.15.4 radios deployed inside one of the University buildings, in rooms and corridors, implementing sensors able to monitor/emulate physical instances like light intensity, temperature, current drain, equipped with small LCD screens that will ease the management and control of application tasks. In addition to the nodes composing the fixed infrastructure, approximately 50 battery-supplied mobile nodes (with 802.15.4 devices) carried by people moving around, are part of the testbeds (Roaming Nodes);

Localization Testbed (LOCTEST) - Approximately 50 additional nodes with high-accuracy localization capabilities, using IEEE 802.15.4a or IEEE 802.15.4f Ultra-Wide Bandwidth (UWB) radios, will be deployed in the same building depending on the future commercial availability of low-cost UWB-based devices;

The infrastructure also includes some network coordination nodes equipped with mini-PC boards and different types of gateways (WLAN, LAN) for proper interconnection to the Internet.

### *2.4.3 EuWIn@EURECOM*

EURECOM (www.eurecom.fr) is a research and teaching institute located in the Sophia Antipolis Technopole in the South of France. EURECOM's research activity traditionally focuses on 3 domains which have led to the creation of three research departments: Networking & Security, Multimedia Communications, and Mobile Communications. The Mobile Communications Department has its focus on digital signal processing for mobile communications, information theory, 4th generation and clean-slate cellular radio systems, wireless protocols, mobile ad hoc networks, software radios, and SW and HW prototyping. In addition to fundamental research, the department has strong expertise in open-architecture multi-way real-time radio platforms (www.openairinterface.org) for use in publicly-funded research projects aiming at demonstrating innovations at all protocols layers (RF to applications). The latter is provided to EuWIN for use within the network and afterwards. The OpenAirInterface.org (OAI) development and facilities primarily target cellular technologies (LTE/LTE-Advanced and beyond) and rapidly-deployable mesh/ad-hoc networks. The platform comprises both hardware and software components and can be used for simulation/emulation as well as real-time experimentation. It comprises the entire protocol stack from the physical to the networking layer. The objective of this platform is to provide methods for protocol validation, performance evaluation and pre-deployment system test.

## 2.5 Liaisons with Industries

### *2.5.1 EuWIn@CTTC*

Currently, the CTTC team involved in WP2.1 ("Radio interfaces for next-generation wireless systems") has links with many industry players, among which the most relevant follow:

AT4 Wireless (recently acquired by Agilent Technologies): This collaboration started in 2009, when the CTTC team started to develop, together with the AT4 Wireless team, the test platform E2010, which is designed to perform compatibility tests to LTE terminals. The experience gained through this collaboration has contributed to a knowledge transfer, which is foreseen to be very useful in Task 2.1.4 ("High spectrally-efficient radio interfaces").

AVIAT Networks: This collaboration started in 2012. CTTC is carrying out a series of projects for the Silicon Valley-based company AVIAT Networks. Among these projects, the most relevant for Newcom# is the project where CTTC is providing a baseband processing solution for the improvement of energy efficiency in new generation transmitters for wireless backhauling equipments. This collaboration can have a positive impact on CTTC's participation in Task 2.1.2 ("Low-energy-consumption and low-emission radio interfaces"). Moreover, within this same topic, CTTC has submitted a proposal in the Seventh Framework Programme together with the Slovenian branch of AVIAT Networks.

Nutaq (before Lyrtech RD): This collaboration started in 2012. Nutaq is currently commercializing a software IP that contains the physical layer of the WiMAX standard developed by CTTC, which is named BeMImoMAX (http://nutaq.com/public/files/products/bemimomax/bemimomax.pdf). The CTTC team is now adapting this IP to make it compatible with the LTE standard. If other IPs are obtained as a result of the experimental research performed within Newcom#, CTTC can study together

with Nutaq and the other partners involved in the research the possibility of commercializing them.

### *2.5.2 EuWIn@UniBO*

The EuWIn site in Bologna has links with many industries, owing to the participation to many EC projects and industrial contracts. The main industry links, related to the scopes of EuWIn, are mentioned here:

the FLEXTOP testbed developed within EuWIn is of interest to the research labs of Telecom Italia, with particular reference to IoT applications;

EuWIn@UniBo has a peculiar link with Embit srl, a small Italian company which is design centre for Texas Instruments and Freescale and the provider of all wireless devices implemented within the laboratory;

the EuWIn site in Bologna has a preferred link with Intel labs of Ireland, which also investigate smart city applications of wireless communications.

### *2.5.3 EuWIn@EURECOM*

OAI has explicit links with industrial partners who contribute to its development both within the context of publicly-funded projects and out of mutual interest on specific research subjects. Currently, the main industrial collaborators, which are, incidentally, affiliate members of the NoE, include:

Alcatel Lucent Bell-Labs (Villarceaux, France) contribute to optimized real-time signal processing for SDR, innovative protocol extensions to LTE, emulation tools based on OAI, interfacing of OAI to industrial-grade RF platforms (remote radio-heads - RRH).

Orange Labs (Beijing, China, subdivision of Orange France) contribute to optimized real-time signal processing for SDR, interfacing of OAI to other hardware platforms (custom and USRP).

Agilent (Beijing, China) contribute to optimized real-time signal processing for SDR.

Thales Communications (Gennevilliers, France) contribute to development of multi-hop protocols and resource allocation strategies for rapidly-deployable mesh networks and innovative signal processing for improving RF amplifier efficiency in terminals.

## 2.6 The EuWIn Website

The EuWIn website has been designed using the same platform chosen for the Newcom# portal, i.e., Joomla. This makes their maintenance easier. It has been devised both as an instrument for facilitating cooperation among the institutions involved (through a private part used as repository of shared documents and measurement databases), and as a dissemination tool providing all the information needed to join the laboratory activities.

However, it is important to emphasise that the EuWIn website does not represent a duplication of the information reported in the Newcom# portal, and all official documents related to the project will be found only on the Newcom# portal. Therefore, deliverables and meeting minutes will be posted on the latter, whereas promotional material (leaflets, video

trailers, etc.) and documents describing in detail the lab facilities, will be found on the EuWIn website.

Moreover, the EuWIn website is integrated in the Newcom# portal, as all user credentials made available to Newcom# researchers to access the project portal will be imported on the EuWIn site, so that all Newcom# researchers will be given access to the private area of the EuWIn website under the same credentials.

The structure devised for the EuWIn website is as follows.

HOME — it contains a short welcome message and describes the goals of EuWIn

STRUCTURE — description of the lab structure is given, using contents of this Deliverable
- → Sites — map, link to three institution websites
- → Director — short descript of role, personal welcome message
- → WP Leaders — short descript of roles, personal welcome messages
- → Partners — mention of Newcom# partners active within EuWIn
- → Liaisons — mention of the industries/labs/projects linked to EuWIn activities

FACILITIES — general description of the various platforms
- → Platform#1 (eg GEDOMIS) description
- → Platform#2 (eg FLEXTOP)
- → Platform#3 (eg DATASENS)
- → Platform#4 (eg LOCTEST)
- → …

ACCESS — the general access policy is described
- → Documents — link to public documents
- → Join — forms to be filled for requesting access
- → Visit — forms to be filled for proposing a visit to the laboratory sites

DEMOS — inaugural video and images
- → one per demo realised, with some info (where, who, picture, what facility)

WORKSHOPS — description of the philosophy behind the organisation of workshops
- → one per workshop organised, contributed (where, programme, what facility)

SCHOOLS — description of the philosophy behind the organisation of schools
- → one page per school organised, contributed (where, programme, what facility)

REPOSITORY — a username/password form to be filled for restricted access

CONTACTS

Concerning the repository, whose access will be restricted to Newcom# partners and affiliate institutions, it was agreed by the WP Leaders that it will contain the outcome of the measurement campaigns performed within the Newcom# JRAs, and the documents needed to coordinate/facilitate access to the lab facilities.

The first version of the website, released at M6, will replace the three pages DEMOS, WORKSHOPS, SCHOOLS, with one single page EVENTS. More details regarding the first version of the EuWIn website are found in D3.6.1.

# 3. EuWIn Technical Facilities and Interfaces at CTTC

This Section provides a description of the technical facilities that are available at EuWIn@CTTC together with the necessary interfaces to interact with them. Moreover, some additional facilities and equipments, which other partners intend to use and which are available outside the CTTC premises, are also described, as they are included in WP2.1.

## 3.1 Introduction

The experimental activities performed at the EuWin@CTTC site will address aspects related to low-energy and low-emission radio interfaces (e.g., PAPR reduction algorithms). Moreover, applied research will also focus on novel high spectral efficiency radio interfaces where advanced coding strategies, e.g., polar codes, will be implemented and tested. In parallel to these experimental research activities, channel measurements, models, and databases will also be created and maintained to be able to validate the obtained results with practical channels that exist in real life; this activity will be partly carried out in cooperation with the COST Action IC1004 in which several partners involved in this lab (AAU, UCL, CNIT) participate. Finally, localization techniques will be addressed through the implementation of positioning algorithms in platforms based on inertial sensors, commercial GNSS ICs, etc. This latter activity will be tightly connected to the one performed at the EuWIn@CNIT/Bologna site.

In order to satisfactorily carry out the above mentioned activities, CTTC makes available the three high performance testbeds that have been briefly described in Section 2.4.1: **GEDOMIS®**, **GNSS-SDR**, and **OpenInLocation**. Their detailed description follows:


**Figure 3-1: The GEDOMIS® testbed (left), the GNSS-SDR project webpage (top right), and one Arduino board from the OpenInLocation lab (bottom right).**

## 3.2 GEDOMIS®

### 3.2.1 Description

The GEDOMIS® testbed is an ideal platform to develop, test and validate the PHY-layer of modern wireless communication systems covering the prototyping and verification requirements of advanced solutions that target base stations, smart antennas, MIMO systems, Software-Defined Radio (SDR), geolocation, cognitive radio and high-speed test and measurement campaigns. In the past it has been used to develop and test real-time systems based on the IEEE 802.11, IEEE 802.16 and 3GPP rel. 9 standards. GEDOMIS® is able to host PHY-layer prototypes of multi BSs and multi User Equipments (UEs). A non-exhaustive list of supported PHY-layer development scenarios is given in table 1 (e.g., according to the number of transmitters-receivers, the number of antennas at each end, the transmission scheme and the signal bandwidth). Please note that wherever the signal bandwidth is mentioned to reach up to 10 MHz, it is an approximate calculation which needs to be thoroughly investigated in case the mentioned system is planned to be developed. At the same time, wherever a signal bandwidth of 20 MHz is mentioned, it refers to systems that have already been developed at GEDOMIS®. A schematic representation of GEDOMIS® is given in Figure 3-2, which includes the majority of the hardware equipment and boards used in the default set-up of the testbed. A brief description of its high-end instruments and boards is given in the following section. Detailed specifications are quoted in Appendix 6.1.

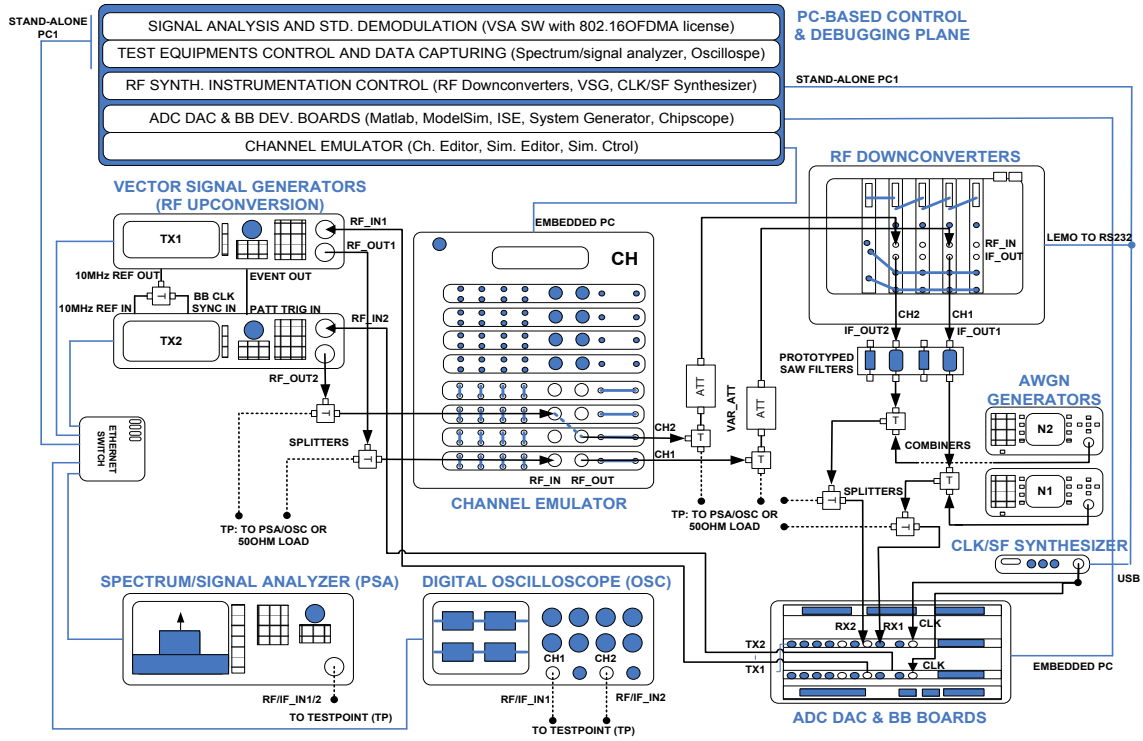



**Figure 3-2: Schematic diagram of the default set-up of the GEDOMIS® testbed.**

| Number of Tx - Rx | Number of antennas Tx- Rx | Antenna Scheme | DL with emulated UL | DL and UL | Bandwidth (MHz) |
|---|---|---|---|---|---|
| 1-1 | 4x4[1] | MIMO | yes | no | up to 10 |
| 1-1 | 2x2 | MIMO | yes | no | 20 |

[1] Using to 2 extra E4438C Vector Signal Generators from Agilent which are not available at GEDOMIS but could be made available (authorization is required since they belong to other research areas at CTTC).

| | | | | | |
|---|---|---|---|---|---|
| 1-1 | 1x2 | SIMO | yes | no | 20 |
| 1-1 | 2x1 | MISO | yes | no | 20 |
| 1-1 | 2x2[1] | MIMO | - | yes | up to 10 |
| 1-1 | 1x2 | SIMO | - | yes | up to 10 |
| 1-1 | 2x1[1] | MISO | - | yes | up to 10 |
| 4-4[1] | 1x1 | SISO | yes | no | up to 10 |
| 2-4 | 1x1 | SISO | yes | no | up to 10 |
| 1-3 | 1x1 | SISO | - | yes (for the Tx) | up to 10 |
| 2-2 | 1x1 | SISO | yes | no | 20 |
| 2-2[1] | 1x1 | SISO | - | yes (for the Tx) | up to 10 |
| 2-2[1] | 2x2 | MIMO | yes | no | up to 10 |
| 1-2 | 1x2 | MISO | yes | no | up to 10 |

**Table 3-1: Indicative PHY-layer development scenarios supported by GEDOMIS®.**

### *3.2.2 Equipment*

**Signal generation HW:**

- Agilent Vector Signal Generators up to 6GHz: The E4438C ESG vector signal generator (VSG) combines outstanding RF performance and sophisticated baseband generation to deliver calibrated test signals at baseband, IF, and RF frequencies up to 6 GHz. It offers an internal baseband generator with arbitrary waveform and real-time in-phase/quadrature (I/Q) capabilities, ample waveform playback and storage memory, and a wide RF modulation bandwidth. By using more than two of these signal generators MIMO transmission is enabled.

- Agilent Baseband Studio digital signal interface module: The N5102A Baseband Studio digital signal interface module provides fast and flexible digital inputs or outputs for the E4438C ESG vector signal generator. In output mode, you can deliver realistic complex-modulated signals directly to digital devices and subsystems. In the input mode, the interface module ports custom digital inputs to the signal generator's baseband system, providing a quick and easy way of upconverting to calibrated analog IF, RF or microwave (μW) frequencies. In both operating modes, the interface module adapts to the specific device with the logic type, data format, clock features, and signalling being required.

- Applied Instruments NS-3 RF Noise sources up to 2.15 GHz: This broadband RF Noise Generator generates an extremely flat AWGN signal from 5 to 2150 MHz. The output level adjusts in 0.1 dB steps over a 30 dB range (-90 dBm/Hz max. output power, ± 2.0 dB flatness over full operating range) and can be ON/OFF pulse modulated. Typical applications: signal/carrier to noise generation (i.e. typically for BER vs SNR system testing), active device loading, interference, RF leakage, frequency response, intermodulation and insertion loss testing.

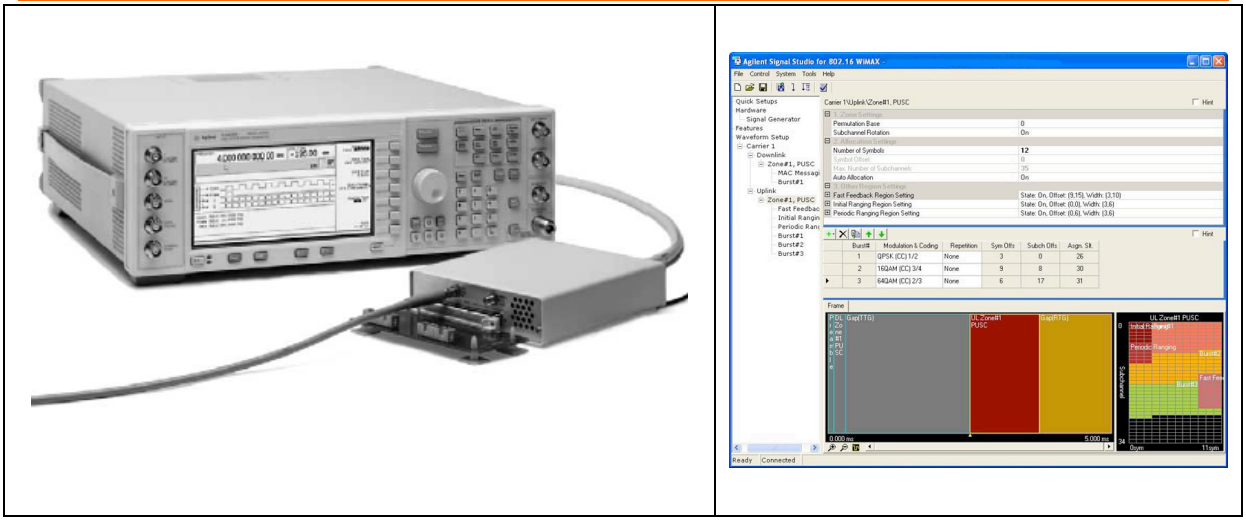


**Figure 3-3: Signal creation HW & SW: Agilent Technologies ESG E4438C Vector signal generator and N5101A Baseband Studio PCI card (left) and Signal Studio SW (right).**

**Signal generation SW:**

- Agilent Signal Studio: Agilent Signal Studio is a suite of flexible, standards-based signal creation software that allows cutting the time spent on signal simulation and provides a validated and performance optimized reference signal to better characterize, evaluate and fine tune designs. The CTTC licensed standard signals are Wireless Local Area Networks (WLAN) IEEE 802.11 a/b/g/j/p, WiMAX (IEEE 802.16-2004, IEEE 802.16e-2005 Wave2), and Digital Video Broadcasting DVB-T/H/C. The software enables the generation of a wide range of application-specific test signals, at baseband, RF, and microwave frequencies using the Agilent ESG vector signal generators available at GEDOMIS®. For downloading custom I/Q waveforms (e.g. MATLAB files) into the signal generators the application Signal Studio Toolkit is used.

- Agilent Baseband Studio: This SW is a suite of digital baseband hardware, software application tools, and accessories that enable digital baseband and RF designers to generate, capture, impair, playback, and emulate real world signal conditions. Baseband Studio applications can be used with the E4438C ESG vector signal generators, and PCs equipped with the N5101A Baseband Studio PCI card (not available in GEDOMIS®).

**Channel Emulation hardware & software:**

- Elektrobit (EB) C8 Channel Emulator: The EB Propsim C8 is a technology-independent radio channel emulator supporting all major wireless standards and signal types in a broad frequency range (350MHz to 6GHz, 70 MHz bandwidth with default option) covering established and future technologies. It allows users to perform realistic and accurate radio channel emulation supporting the development of most demanding wireless applications such as beam forming, 4×4 MIMO, network level testing, software defined radio and aerospace satellite communications.

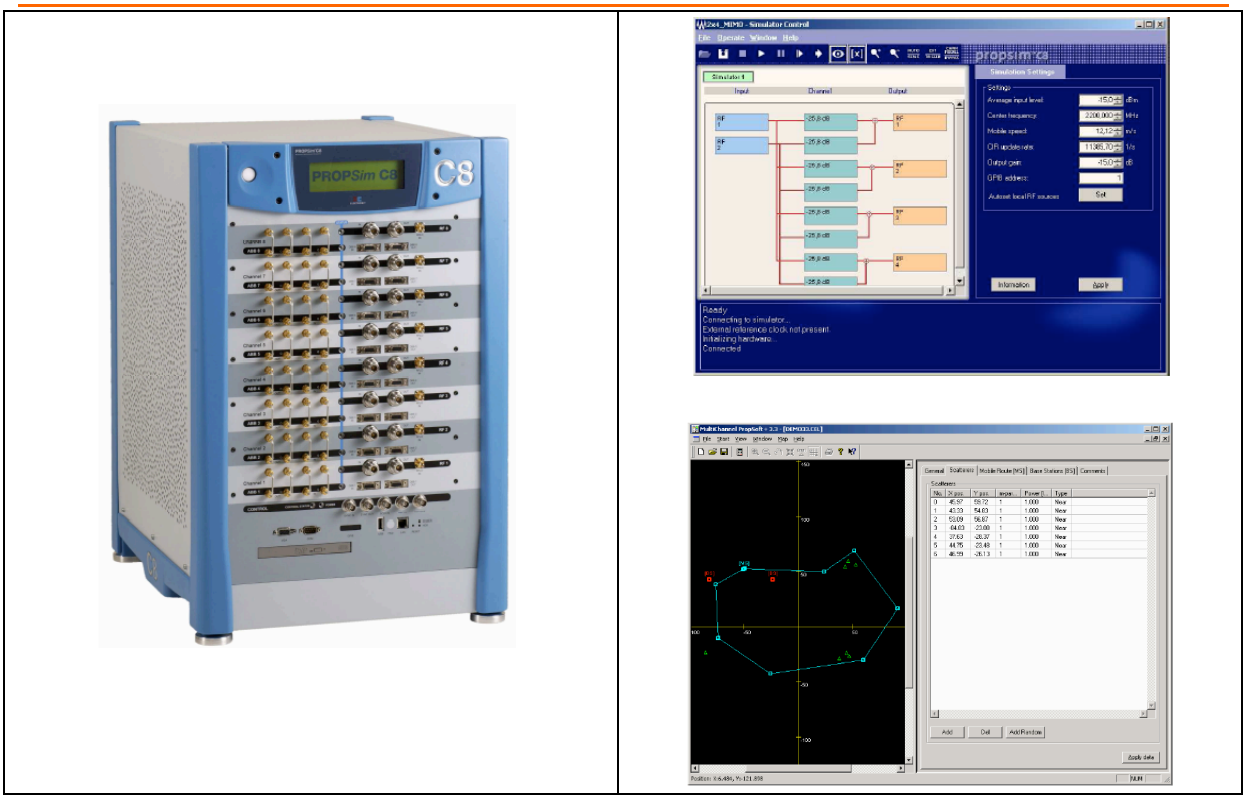



**Figure 3-4: EB Propsim C8 channel emulator (left), Simulator Editor & Propsoft+ GUIs (right).**

The physical radio channel characteristics, such as frequency, multipath propagation, fast fading, dynamic delays, attenuation, noise, interference and shadowing, can be emulated independently on each channel. The user can utilize all major standardized channel models or create its own radio channel models with a set of available versatile channel modelling tools. These tools provide means for modelling MIMO complex correlation or DoA/Direction of Departure (DoD), DoA/DoD spread and antenna geometry based beam forming for smart antenna applications. In addition to statistical and spatial channel models, the user can utilize measured channel data or data collected with various measurement tools (e.g. scanners and drive test tools) supported by EB Wireless Environment Solution. EB Propsim C8 is delivered with Windows 2000 and application software pre-installed including channel model, correlation and simulation editors. The channel emulator is also equipped with Propsoft+, a Channel Impulse Response (CIR) generator software that generates a set of time variant complex channel impulse responses from a user specified propagation environment.

**Signal Analysis HW:**

- Rohde & Schwarz FSQ Signal Analyzer up to 26.5GHz: It offers signal analysis at a demodulation bandwidth of up to 120 MHz with the dynamic range of a high-end spectrum analyzer. The equipment has application firmware for digital demodulation measurements for WLAN (IEEE 802.11 a/b/g/j and IEEE 802.11 turbo mode) and WiMAX (IEEE 802.16-2004, IEEE 802.16e-2005), and for noise figure and gain analysis.

- Agilent Infiniium Oscilloscope: The Agilent 8000B Series Infiniium real-time ultra-high performance oscilloscope is required to meet the needs of engineers designing state of the art high-speed serial communication links and other ultra-high-speed electronic systems. The available scopes support 4 analog channels with up to 10GHz Bandwidth with up to 40

GSa/s sample rate. This instrument can be used as multiple-channel analog front-end to extract data for further processing with the Agilent 89600 VSA software (and thus enabling MIMO reception).

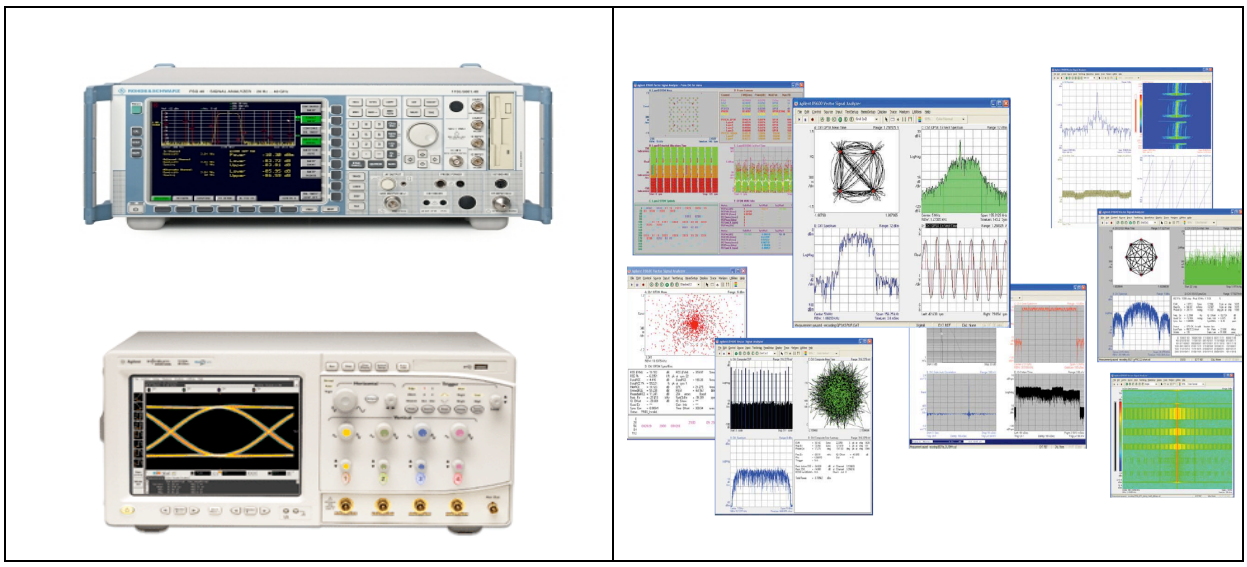


**Figure 3-5: R&S FSQ26 Signal analyzer and Agilent Technologies DSO80804B Infiniium Oscilloscope (left) and 89600 VSA software GUI captures (right).**

**Signal Analysis SW:**

- Agilent 89600 Vector Signal Analysis (VSA): The software provides superior general-purpose and standards-specific signal evaluation and troubleshooting tools. These tools can be used to dig into the signal and gather the data needed to successfully troubleshoot PHY layer signal problems. GEDOMIS® disposes the full set of libraries through the educational license of VSA.

Real-world signals acquired by the 89600 software can be linked to the Agilent Advanced Design System (ADS) simulation environment (which can also load waveforms into the signal generators and thus close the loop) for further processing or mixed-domain and multi-platform verification.

**Synthetic instrumentation:**

- Mercury Computer Systems (MCS) High Performance 4-channel RF Downconverter: The MCS Echotek Series RF 3000 Tuners is a reconfigurable multi-channel platform to down-convert general wireless standard signals from RF to IF. The equipment must be placed within the frame of a complete RF, data acquisition and signal processing platform and performs high dynamic range, wide bandwidth, excellent phase noise, single or multi-channel phase-coherent operation and ultra fast tuning speed. The basic 3000T tuner is comprised of two single-slot VME modules: the 3000RF receiver module and the 3000S synthesizer module (using Direct Digital Synthesizer (DDS) technology). This 2-board 6U VME set functions as an ultra high-performance 20 MHz to 3000 MHz RF-to-IF. The tuner provides both an intermediate frequency at 140 MHz (65MHz bandwidth) and a baseband output suitable for direct input into an external A/D converter. The 3000RF module has a dual RF input, which can be switched for systems that may have high and low antenna array inputs. Alternatively, one RF input can be utilized as a dedicated calibration port. For multi-channel applications, additional 3000RF modules can be integrated with the 3000S synthesizer

module to form a multi-channel fast-tuning radio solution. The system can run in a master/slave configuration, such that the system can be dynamically changed to run in either independently tunable or phase-coherent operation. This allows the system to be cabled up once and reconfigured on the fly via the control software that can be configured for a standard RS-232 or a serial peripheral interface (SPI) port, thereby allowing the unit to be controlled via the front panel in addition to the VME bus. GEDOMIS® features a [4RF+1synthesizer] module-configuration enclosed in a Vector Series 400 6U 21slot VME chassis allowing future expansions and integration of upconverters (for TX) or other 6U ADC/DAC or DSP/FPGA VME boards. The high-performance characteristics are enabling factors for applications such as MIMO wireless communication systems (commercial mobile phone base stations, wireless LAN networks) or diverse multiple-purpose software radio allowing cognitive radio, direction finding and beamforming.


**Figure 3-6: MCS Echotek Series 3000T downconverters (left) and Holzworth Instrumentation HS1001A synthesizer.**

- Holzworth Microwave Source: The Holzworth HS1001C RF Synthesizer is an ultra low phase noise, single channel CW source. Capable of tuning frequencies from 8MHz to 1GHz in 0.001Hz step resolution, this “small form” versatile synthesizer can be controlled directly by the proprietary application software Labview or a preloaded lookup table which enables such functionality as rapid frequency hopping. The device can be either DC powered by using an external AC/DC power supply or by using a custom made dual USB cable (and thus enhancing its portability). The source can be used as (below IEEE L-band) RF synthesizer, or as baseband system clock or ADC sampling frequency generator: CTTC is currently working in many wireless demonstrators for some wireless standards/systems (WiFi, WiMAX, UWB, DVB, GPS/Galileo…) and for certain applications it is required both low jitter and low phase noise (e.g. high-density multi-carrier OFDM systems).

**Lyrtech ADP, signal conversion and baseband processing platform:**

The Lyrtech’s Advanced Development Platform (ADP) comprises a full set of signal conversion and baseband processing boards. Full specifications are given in Appendix 6.2. The VHS-DAC and VHS-ADC (Figure 3-7) signal conversion boards of the ADP are fitted respectively with 4 dual TI DAC5687 Digital to Analogue Converters (DAC) providing up to 8 transmitting channels and 4 dual AD6645 Analogue to Digital Converters (ADC) providing up to 8 receiving channels. These two boards allow the implementation of MIMO systems and other antenna array configurations used in radar or terrestrial-to-satellite communications. Each of the eight phase-coherent channels of the DAC and ADC boards shares a common clock source and includes a digitally controlled Variable Gain Amplifier (VGA). There is also an on-board 104 MHz crystal and external clock and trigger inputs in both boards. The DAC

and ADC boards include a single Xilinx Virtex-4 FPGA device (i.e., XC4VLX160), 128 MB of on-board SDRAM and they are connected to a cPCI chassis through a dedicated backplane connection. Finally, a proprietary full-duplex 1GBps bus (i.e., Rapid Channel) allows the VHS-ADC and VHS-DAC boards to connect with the main baseband processing board.

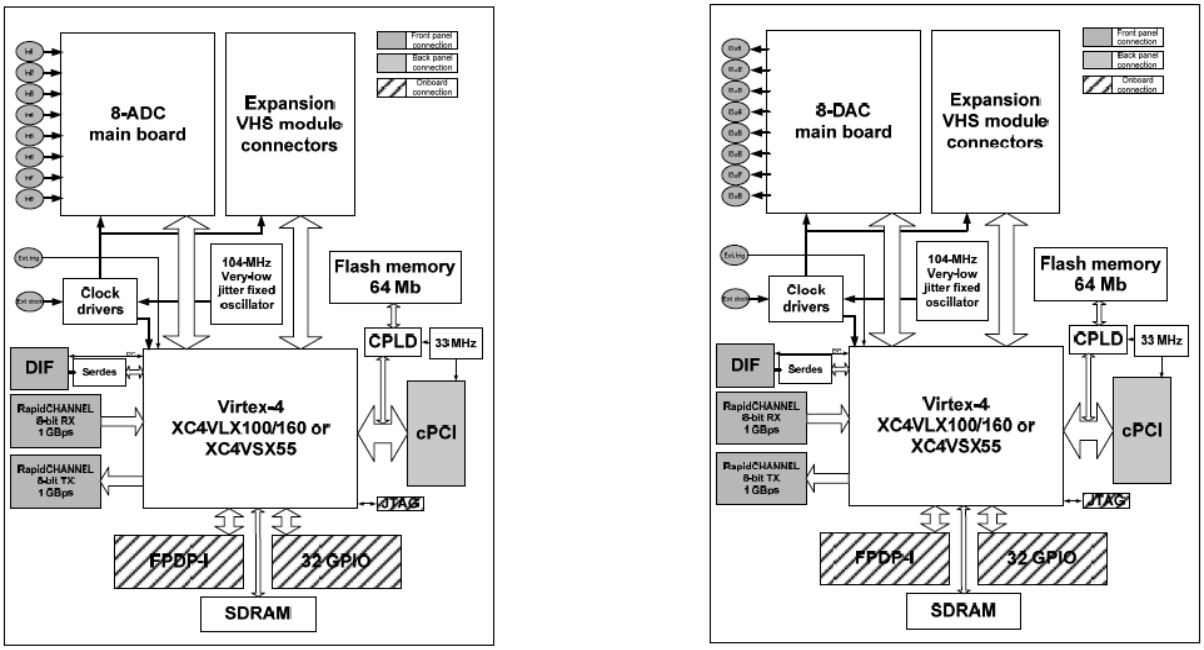



**Figure 3-7: The block diagram of the VHS-ADC (left) and the VHS-DAC (right) boards.**

In order to compare the challenges of wideband bit-intensive baseband operations, the ADP includes another baseband signal processing board, namely the Signal Master Quad (SMQUAD), able to address demanding data loads and DSP operations. As seen in Figure 3-8, this board includes two Xilinx Virtex-4 FPGA devices (i.e., XC4VLX160 in our case) and 4 fixed-point DSP processors from TI (i.e., TMS320C6416 running up to 1GHz in our case). The SMQUAD features 128 MB of SDRAM per FPGA and DSP processor. The inter-FPGA communication is accomplished via a full-duplex 1GBps bus and the FPGA-to-DSP communication is accomplished via a 32-bit wide bus. As in the case of the VHS-DAC and VHS-ADC boards the SMQUAD board is similarly connected to the chassis via the cPCI backplane. The SMQUAD features two additional daughter-boards (DRC), which are connected to the LYRIO+ sites. The DRC boards are connected to the LYRIO+ sites of the SMQUAD board and help the latter to establish full-duplex 1GBps connections with the VHS-ADC and VHS-DAC boards thanks to the on-board Rapid Channel connector. The FPDP and GPIO-32 I/O interfaces are not included. Each DRC boards is fitted with a Xilinx Virtex-4 FPGA device (i.e., XC4VSX35).

Finally, the chassis is fitted with a PC which runs Windows XP 32-bit (i.e., ADP software compatibility prerequisite). The PC is also connected to the cPCI backplane and runs the ADP software and drivers (ADP version 3.0 or 3.2[2]), including dedicated Graphical User Interfaces (GUIs) for controlling and interacting with each board that is connected to the cPCI chassis. Considering that all described boards fitted in the ADP are making use of the same the cPCI bus, the role of the PC is not limited to off-line control functions, but it is also thought to be used for various real-time operations such as waveform record and play-back, programming registers on the FPGA and use of the Real-Time Data Exchange (RTDEx) bus. Figure 3-9 shows a joint representation of the different boards comprising the GEDOMIS® testbed. Note that one of the DRC boards is currently not operating.

[2] These versions of ADP are compatible with the Xilinx ISE 9.2, TI Code Composer 3.3 and Mathwork's Matlab 2007b versions.

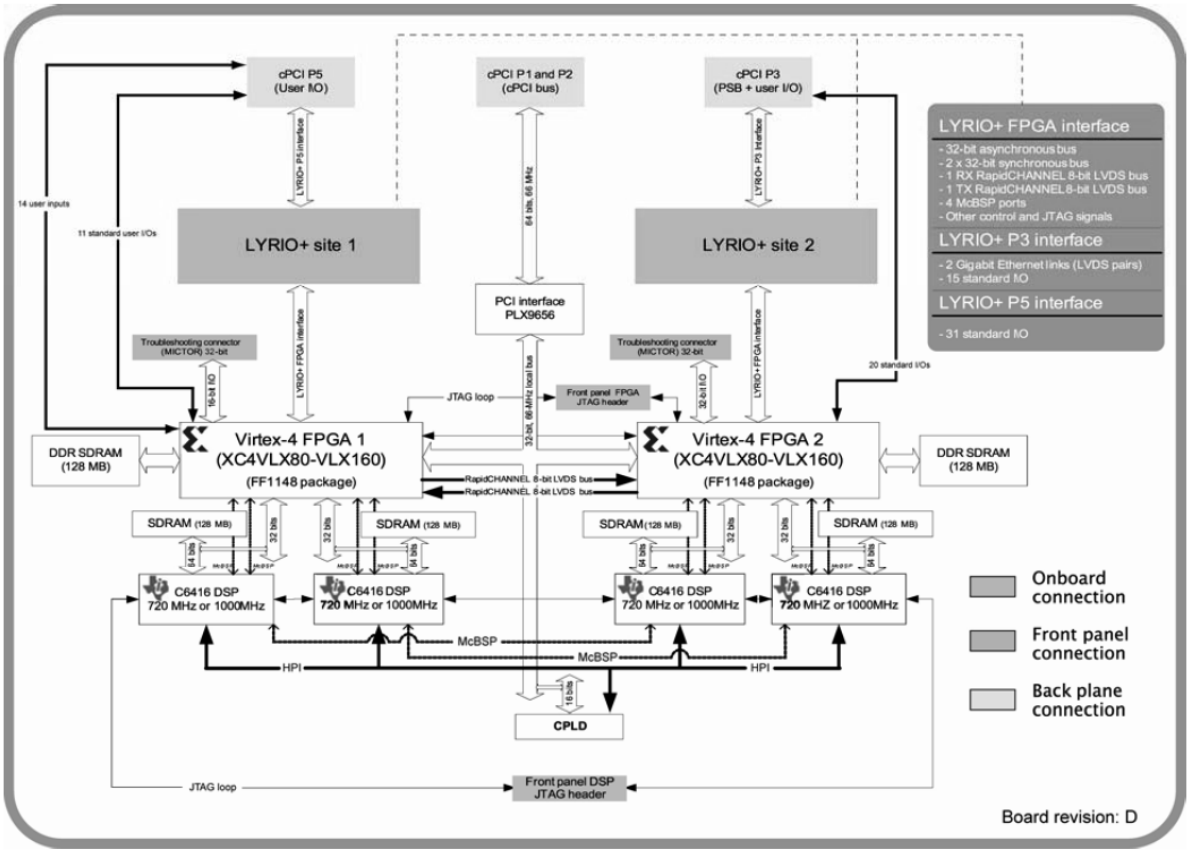



**Figure 3-8**: **The block diagram of the SMQUAD board.**

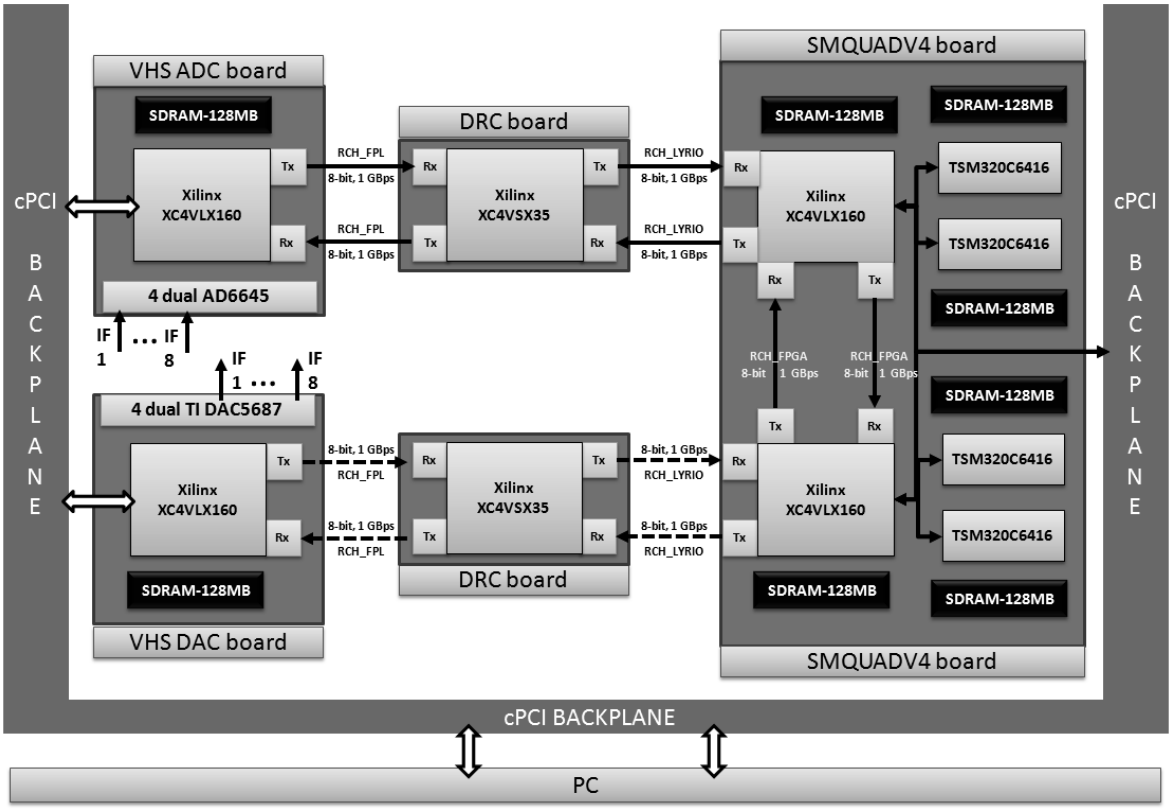



**Figure 3-9: Overview of the ADP solution available at GEDOMIS®.**

### *3.2.3 Interfaces*

The testbed does not offer a unified Graphical User Interface (GUI) to program, control and configure all of its hardware equipment and software. The different equipment, boards and software can be accessed with the means specified hereafter:

- Different web-based GUIs running on a browser of the ADP PC provide access to the:
  - Agilent E4438C VSGs,
  - Rohde & Schwarz FSQ Signal Analyzer and the
  - Agilent 8000B Series Infiniium Oscilloscope
- GUIs running at the ADP PC provide APIs for the:
  - MCS Echotek Series RF 3000 4-channel Downconverters
  - Holzworth HS1001C RF Synthesizer
  - Lyrtech VHS-ADC, VHS-DAC and SMQUAD boards of the ADP
- Instrument programmed exclusively in-situ (no GUI is available):
  - Applied Instruments NS-3 RF Noise sources
- A separate PC (embedded in the instrument) runs a software that provides access to the:
  - Elektrobit C8 Channel Emulator
- A separate PC hosts the (the ADP PC does not meet the performance specs):
  - Agilent VSA

In theory, all the instruments (apart from one), APIs and software of GEDOMIS® that run on a PC can be accessed with different remote desktop sessions (i.e., considering that all PCs run different MS Windows versions). However, configuring and programming GEDOMIS® via remote access is practically impossible, since there has always to be present an engineer with previous exposure in use and manipulation of the instruments and software of GEDOMIS®. Many configuration options will have to be tested and validated in-situ together with the visiting researcher[3]. Also, the large number of User's Manuals and technical documentation makes it anyway practically impossible for someone to rapidly use the testbed without the help of qualified and experienced researchers who have already used GEDOMIS® before; apparently this can be facilitated only with in-situ use. It is also important to note that GEDOMIS® comprises a set of heterogeneous instrumentation and boards; it is thus vital for the instrument-safety to be always supervised in-situ any research and development activity. The same applies when the instruments or components of the testbed must be appropriately configured, connected or tuned to meet specific performance prerequisites or test-scenarios.

GEDOMIS® can be used to develop:

i. Offline testbeds which typically combine Matlab simulations at the two baseband ends - transmitter and receiver- with instrumentation for the signal conversion (DACs, RF up-conversion, channel emulator or antennas, RF downconversion, ADCs). Offline testbeds are typically used to evaluate quasi-static channels.

[3] Setting up and configuring a real-time wireless communication testbed that focuses on PHY-layer algorithm prototyping implies the separate and joint testing of the diverse type of instruments and signal processing boards that form part of it. This allows researchers to achieve the desirable operating conditions and performance, according to the specifications of a certain standard. In order to accomplish this task, certain performance features of the equipment comprising the testbed need to be characterized and analysed, a fact that helps to identify performance bottlenecks at the beginning of the development. Real-time testbeds are commonly having performance stability issues due to the interdependencies among instruments in the signal processing path (baseband, ADC/DAC, RF conversion and channel); it is quite common for example that the power-level of the signal between cabled instruments or hardware boards may unexpectedly variate out of the defined range due to some sort of failure, mismatch or loose connection of cables, adapters, attenuators, on-board connectors or other components. This may significantly change the overall expected performance of the developed baseband transmitter and receiver, making also hard the traceability of the problem during system-debugging.

ii. Real-time testbeds which features an end-to-end full real-time operation able to validate realistic mobility and fast fading channel conditions.

A brief guide that describes the two modes of development and operation of GEDOMIS® is given hereafter:

**Configuring and using GEDOMIS® as an offline testbed:**

- Build in Matlab the Tx baseband output I/Q vectors (stored in a .MAT)
- Use Agilent's Signal Studio Toolkit
  - Upload I/Q vectors to the Agilent's ESG4438C Vector Signal Generators (VSGs)
- Use the two ESG4438C VSGs to produce real RF signals
  - The ESG4438C has a baseband BW of up to 40 MHz for this operation mode
  - The ESG4438C embeds an arbitrary waveform generator and RF signal up-converter circuitry able to provide at real-time signals from 250 kHz to 6 GHz
  - The VSGs can realize 2 independent Tx or a 2-antenna MIMO Tx
- Use the Elektrobit Proposim C8 channel emulator to apply a static channel
  - The emulator supports up to 4 channels, 350 MHz - 6 GHz, 70 MHz bandwidth.
  - Load a standard channel from an existing library
  - Build channels in Matlab and upload them to the emulator (up to 48 taps each)
- OPTION 1: Use the Agilent Infiniium 80000B 4-channel oscilloscope to capture data
  - Up to 10 GHz, sample rates: 2ch @ 40 GSa/s, 4ch @ 20 GSa/s
  - Memory depth per channel: 1M (4ch), 2M (2 ch))
  - The Oscilloscope offers 6.2 effective bits resolution to the captured data
    - Optional step: Use Agilent's VSA to demodulate the signal
    - The channel emulator is by-passed
    - The signal has to be compliant with a standard supported by VSA
    - VSA runs at a PC and takes samples from the Oscilloscope via Ethernet
  - Post-process the captured data in Matlab
  - Develop the Rx in Matlab
- OPTION 2 Achieve a better resolution in the captured data
  - Use the RF donwcoverters (20MHz to 3GHz, Phase-Coherent 4 channel)
  - Use the 8-channel ADC board (105MSPS, 14 bit) featuring an FPGA device
  - Tune the RF down-converters to provide the IF frequency that satisfies the analogue bandwidth and sampling specifications of the ADC devices
  - Apply an empirical back-off margin (e.g., 12 dBs) by modifying the gain of the on-board VGAs (i.e., using a GUI) to avoid the saturation of the ADCs
  - Capture and retrieve the data at the FPGA device of the ADC board using a preconfigured FPGA application and a dedicated GUI

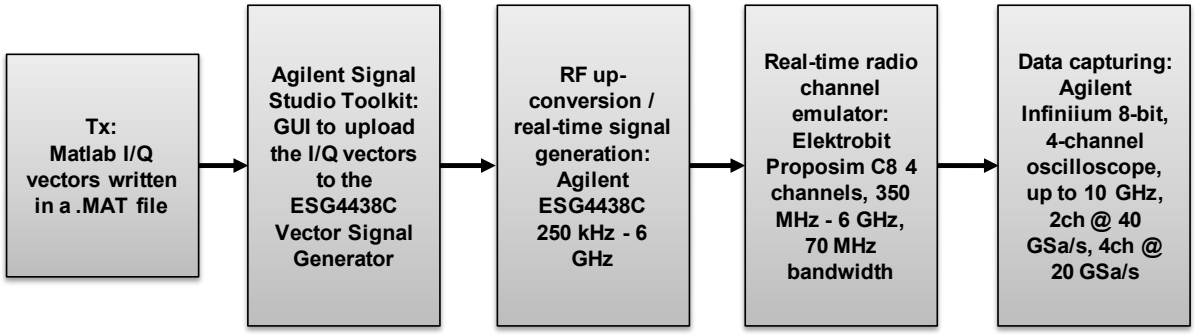



**Figure 3-10: The offline PHY-layer realization flow using GEDOMIS®.**

**Using GEDOMIS® to develop a real time testbed:**

- Develop the Tx in Matlab and capture data that can be used for developing the Matlab model of the Rx following the procedure for offline realizations
- Manually translate the Matlab model of both Tx and Rx to HDL code
- Debug the HDL functional code using proprietary HDL simulation EDA tools
- Implement the RTL code to target the FPGA devices of GEDOMIS®
    - Integrate both Tx and Rx with the firmware of the boards
    - Configure for the DAC devices e.g., filters, interpolation factor, IF signal
    - Implement an AGC algorithm which reconfigures on-the-fly the on-board VGAs
    - Produce the final bitstream(s) and configure the FPGA devices
    - The DSP and signal conversion boards of GEDOMIS® feature
        - FPGAs: 4 Xilinx Virtex LX160 devices, 1 Xilinx Virtex SX35 device
        - DSP processors: 4 TSM320C6416 (fixed point 1GHz)
        - DACs: 4 dual TI DAC5687 D/A (14-bit, 480 MSPS)
        - ADCs: 4 dual AD6645 A/D (14-bit, 105 MSPS)
        - 8 Gbit/s full duplex custom communication bus (board-to-board, FPGA-to-FPGA)
- Use the ESG4438C VSGs of GEDOMIS to upconvert the IF signals
    - Provide at real-time signals with output frequencies from 250 kHz to 6 GHz
    - The VSGs can realize 2 independent Tx or a 2-antenna MIMO Tx
- Use the Elektrobit Proposim C8 channel emulator
    - The real-time implementation of the baseband part of the Tx and Rx allows the validation of both static and mobile channel models.
- Use the Agilent Infiniium 80000B series 4-channel oscilloscope
    - Data visualization, signal testing and debugging
- Use the Rohde & Schwarz Signal Analyzer FSQ26
    - The spectrum analyzer can be used for RF signal testing and debugging purposes
    - 20 Hz to 26.5 GHz. Data capturing feature (IQ 120 MHz analysis bandwidth, 235 Msa IQ memory, Sample rate up to 326.4 MHz)
- Optional step: Use Agilent's Vector Signal Analyzer to demodulate the signal
    - Standard compliancy is verified likewise.

A use-case of GEDOMIS® as 2x2 mobile WiMAX DL transmitter and receiver is included in Appendix 6.3 with full details on the configuration and programming of all the used boards and instruments. Additionally, a short introduction on how to use GEDOMIS® to develop real-time FPGA baseband systems is given in Appendix 6.4.

## 3.3 GNSS-SDR

### *3.3.1 Rationale*

Location has become an embedded feature not only on medium and high-end mobile phones, but also on other portable devices such as digital cameras and portable gaming consoles. This massive deployment of GNSS receivers requires a high level of integration, a low cost, a small size and a low power consumption, which has pushed the leading GPS integrated circuit (IC) manufacturers to offer single-chip solutions easy to integrate in multi-function devices. Thus, the radio frequency (RF) front-end and the baseband processing are

jointly implemented in monolithic ICs, tiny black boxes leaving the user no possibility to interact or to modify the internal architecture or the algorithmics.

This approach is very convenient for location based services and applications, since users and developers are interested in using the location information (eventually taking advantage of complementary information coming from wireless network providers) but not in how the position has been obtained. Good examples of this abstraction can be found in the application programming interfaces (APIs) of two major operating systems for mobile devices: Apple's iOS provides a core location framework with objects that incorporate the geographical coordinates and altitude of the device's location along with values indicating the accuracy of the measurements, when those measurements were made, and information about the speed and heading in which the device is moving. A similar situation is found in Android, which provides a location package that contains classes with descriptive-named methods such as `getLatitude()`, `getLongitude()`, `getAltitude()`, `getSpeed()`, `getAccuracy()` and so on. This abstraction layer simplifies a lot the job of the application developer, but leaves no way to observe or modify any internal aspect of the receiver.

As an opposite driving force, the advent of a number of new GNSS (Galileo, COMPASS), the modernization of existing ones (GPS L2C and L5, GLONASS L3OC) and the deployment of augmentation systems (both satellite-based, such as WAAS in the USA, EGNOS in Europe, and MSAS in Japan; and ground-based, such as WiFi or cellular-network based positioning) depict an unprecedented landscape for receiver designers. In the forthcoming years, many new signals, systems and frequency bands will be available for civil use, and their full exploitation will require a thoughtful redesign of the receiver's architecture and inner algorithms. In addition to being black boxes hidden by an abstraction layer, current mass-market GPS ICs are clearly constrained in terms of configurability, flexibility and the capacity to be upgraded. New available signals pose the challenge of multisystem, multiband receivers' design, including issues such as interference countermeasures, high-precision positioning for the mass-market, assisted GNSS and tight hybridization with other technologies.

These facts have headed receivers' designers to the software radio paradigm, in which an analog front-end performs the RF to intermediate frequency (or directly to baseband) conversion prior to the analog-to-digital converter (ADC). All remaining signal and data processing, including the hybridization with other systems, are defined in the software domain. This approach provides the designers with a high degree of flexibility, allowing full access and possibility of modification in the whole receiver chain.

NEWCOM#, the European Network of Excellence in Wireless Communications, through the European Lab on Wireless Communications for the Future Internet (EuWIn), proudly offers an open source software defined GNSS receiver freely available to the research community. GNSS-SDR provides an open framework for such signal processing, from the interface to commercially available RF front-ends to the computation of code and phase observables, the natural inputs of most geodetic processing software. Thus, users are able to inspect and modify every aspect of the signal processing performed by the receiver, something not possible when working with integrated circuits.

### *3.3.2 Description*

GNSS-SDR is an open source project that implements a global navigation satellite system software defined receiver in C++. With GNSS-SDR, users can build a GNSS software receiver by creating a graph where the nodes are signal processing blocks and the lines represent the data flow between them. The software provides an interface to different suitable RF front-ends and implements the entire receiver's chain up to the navigation

solution. Its design allows any kind of customization, including interchangeability of signal sources, signal processing algorithms, interoperability with other systems, output formats, and offers interfaces to all the intermediate signals, parameters and variables.

The proposed software receiver targets multi-constellation/multi-frequency architectures, pursuing the goals of efficiency, modularity, interoperability, and flexibility demanded by user domains that require non-standard features, such as earth observers or geodesists, and allowing applications such as the observation of the ionosphere, GNSS reflectometry, signal quality monitoring, space weather, and high-accuracy (cm-level) positioning based on carrier-phase navigation techniques. GNSS-SDR is focused on signal processing, understood as the process between the ADC and the computation of code and phase observables, including the demodulation of the navigation message. We purposely omit data processing, understood as the computation of the navigation solution from the observables and the navigation message, since there are a number of well-established libraries and applications for that (also in the open source side, such as GPSTk).

The goal is to provide efficient and truly reusable code, easy to read and maintain, with fewer bugs, and producing highly optimized executables in a variety of hardware platforms and operating systems. In that sense, the challenge consists of defining a gentle balance between level of abstraction and performance, addressing:

- Concurrency (take advantage of multicore processors).
- Efficiency (take advantage of the specific processor architecture).
- Performance (and how to measure it!).
- Portability (should live in a complex, dynamic ecosystem of operating systems and processor architectures).
- Ability to run in real-time or in post-processing (real-time is only for the chosen ones).
- Extendibility (easy addition and test of new algorithms and implementations).

GNSS-SDR runs in a common personal computer and provides interfaces through USB and Ethernet buses to a variety of either commercially available or custom-made RF front-ends, adapting the processing algorithms to different sampling frequencies, intermediate frequencies and sample resolutions. It also can process raw data samples stored in a file. The software performs signal acquisition and tracking of the available satellite signals, decodes the navigation message and computes the observables needed by positioning algorithms, which ultimately compute the navigation solution. It is designed to facilitate the inclusion of new signal processing techniques, offering an easy way to measure their impact in the overall receiver performance. Testing of all the processes is conducted both by the systematic functional validation of every single software block and by experimental validation of the complete receiver using both real and synthetic signals. The processing output can be stored in Receiver Independent Exchange Format (RINEX), used by most geodetic processing software for GNSS, and navigation results can be displayed via the KML open standard, an XML notation for expressing geographic annotation and visualization within Internet-based, two-dimensional maps and three-dimensional Earth browsers.

The source code is released under the GNU General Public License (GPL), thus ensuring the freedom of modifying, sharing, and using the code for any purpose. This secures practical usability, inspection, and continuous improvement by the research community, allowing discussion based on tangible code and the analysis of results obtained with real signals. Hence, GNSS-SDR is also intended to be a framework for algorithm testing and an educational tool, since everybody is allowed to peruse the source code, see how the receiver is actually implemented, and contribute with improvements, bug fixes, and addition of new features.

Although GNSS-SDR is still far from full-featured commercial software receivers, it constitutes a free platform that can be continuously improved by peer-reviewing and contributions from users and developers around the world, unleashing the potential of collaborative research in the field of GNSS software receivers.

### *3.3.3 Project Ecosystem*

Infrastructure for project management, code development and efficient communication among users and developers is a key aspect in every software project. When it comes to open development schemes, project ecosystem becomes crucial in gaining momentum and attracting new people and ideas. GNSS-SDR offers the following resources:

- **Web site**. The website must be well designed in terms of usability, functionality and extendability, ensuring an enjoyable and appealing user experience. We used Drupal as a content management system.The result can be found at http://gnss-sdr.org.The website visitors will be monitored via Google Analytics, a service offered by Google that generates detailed statistics about a website's traffic and traffic sources.
- **Revision control system**. For the source code, an application that automates the process of keeping an annotated history of the project, allowing reversion of code changes, change tracking, and bug tracking is essential. GNSS-SDR uses the service provided by SourceForge based on Subversion, a popular software versioning and revision control system distributed under an open source license. Developers use Subversion to maintain current and historical versions of files. The Sourceforge website for the project is at http://sourceforge.net/projects/gnss-sdr
- **Documentation**. This is of paramount importance for users, developers, testers, software architects and students. GNSS-SDR usesDoxygen, a tool for writing software reference documentation. The documentation is written within the C++ code, in form of comments, and is thus relatively easy to generate (since it can be written along with the source code) and keep up to date. Doxygen scans the code, extracts the documentation and dumps it in HTML, LATEX, RTF or XML formats, cross-referencing documentation and code, so that the reader of a document can easily refer to the actual code.It also automatically generates dependency graphs, inheritance diagrams, and collaboration diagrams. In addition to code documentation, the project web page provides with detailed instructions about the installation, usage, coding style and general information about the program.In addition to the code documentation, GNSS-SDR also offers through its website a number of tutorials and “how-tos” addressing different aspects of the software, from building instructions to detailed procedures about how to contribute to the source code, coding style recommendations, good practices for testing, etc. Those documents can be checked at http://gnss-sdr.org/documents
- **Communication**. An email distribution list uses to be an efficientcommunication tool among developer team members and users. A public mailing list has been set up for this purpose: anyone can freely subscribe to it and put in contact with the developer team and other users jus visiting
  https://lists.sourceforge.net/lists/listinfo/gnss-sdr-developers

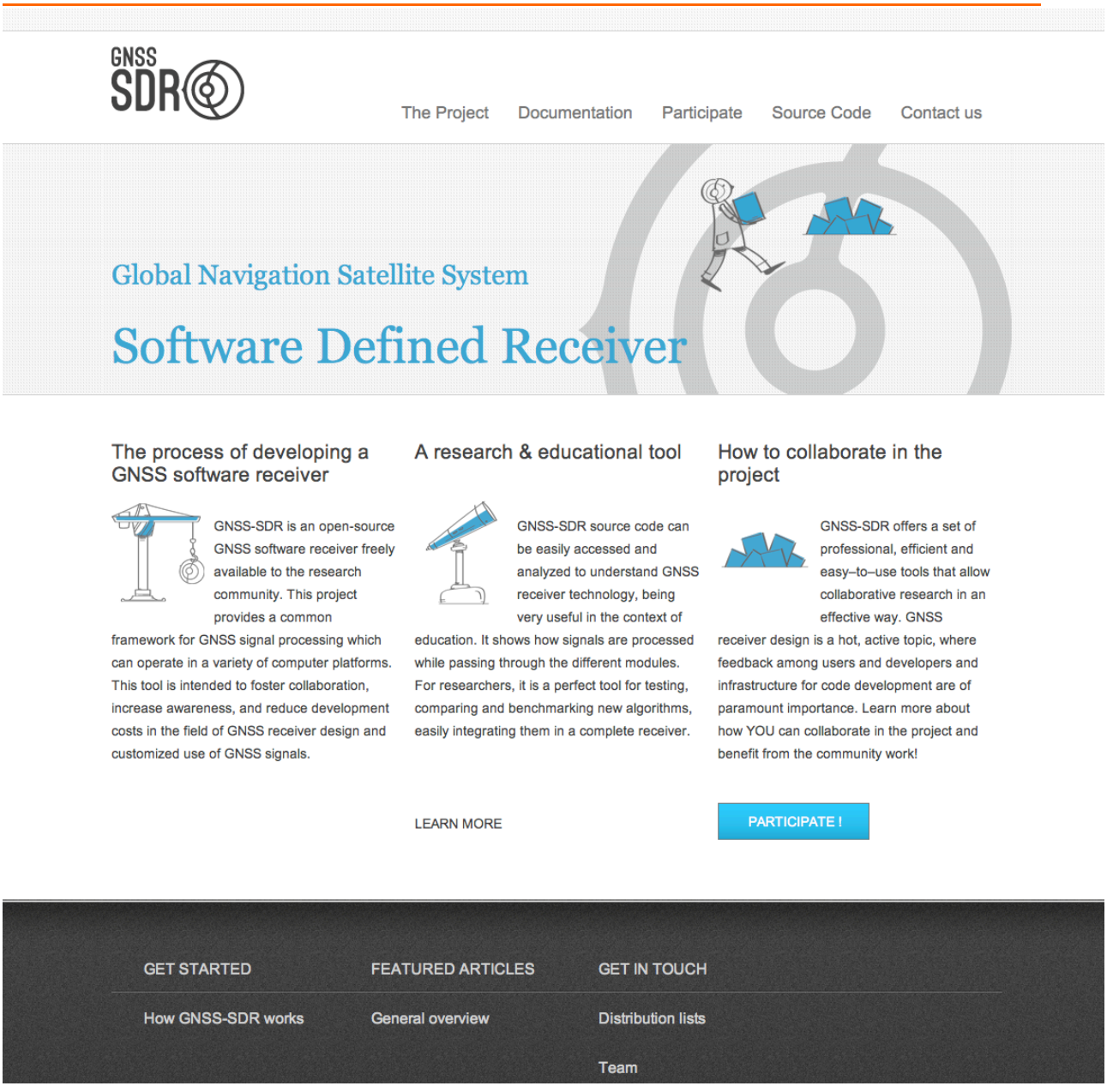



**Figure 3-10: Main page of GNSS-SDR's website, at http://gnss-sdr.org**

### *3.3.4 GNSS-SDR Open Source Software Stack*

Due to the open source nature of this software project, anyone can download and build the package at its own machine. Currently, GNSS-SDR runs in most of the popular Linux distributions (see Table 3-2 for a list of operating system choices) and takes advantage of other third-party open source tools.

| Operating System | Website and logo | Versions tested |
|---|---|---|
| **Ubuntu** | http://www.ubuntu.com/ | • Ubuntu 12.04 LTS (Precise Pangolin). 32 and 64-bit versions.<br>• Ubuntu 12.10 (Quantal Quetzal). 32 and 64- |

| | | |
|---|---|---|
| | ubuntu linux for human beings | bit versions. |
| **Debian** | http://www.debian.org/ debian GNU/Linux | • Debian 6.0.6 (Squeeze) |
| **Fedora** | http://fedoraproject.org/ fedora | • Fedora 18 (Spherical Cow) |
| **Mac OS X** | http://www.apple.com/osx/ Mac | • Mac OS X 10.8 (Mountain Lion) |

**Table 3-2: List of operating systems in which GNSS-SDR has been tested**

Software development, compilation and execution require some external dependencies and software packages that contribute adding features and functionalities. All of them are released with open licenses that allow its free usage by third-party software and users. Table 3-3 summarizes those external software libraries and tools. The fact that all of them can be downloaded, used and redistributed for free ensures practical usability by a wide range of users (students, researchers and practitioners) around the world for a minimal cost (*i.e.*, Internet access).

| Dependency / Software tool | Website and logo | License | Features |
|---|---|---|---|
| **GNU Radio** | http://gnuradio.org GNU Radio | GNU General Public License. | Software development toolkit that provides signal processing blocks to implement software radios. |

| | | | |
|---|---|---|---|
| **Gflags** | http://code.google.com/p/gflags/ | Redistribution and use in source and binary forms, with or without modification, are permitted. | Library that implements commandline flags processing. |
| **Glog** | http://code.google.com/p/google-glog/ | Redistribution and use in source and binary forms, with or without modification, are permitted. | This library provides logging APIs based on C++-style streams and various helper macros. |
| **Googletest** | http://code.google.com/p/googletest/ | Redistribution and use in source and binary forms, with or without modification, are permitted. | Google's framework for writing C++ tests on a variety of platforms. |
| **Armadillo** | http://arma.sourceforge.net/  | The library is open-source software, and is distributed under a license that is useful in both open-source and commercial/proprietary contexts | Armadillo is a C++ linear algebra library (matrix maths) aiming towards a good balance between speed and ease of use. The syntax is deliberately similar to Matlab. |
| **Doxygen** | http://www.stack.nl/~dimitri/doxygen/   | GNU General Public License. | Doxygen is the *de facto* standard tool for generating documentation from annotated C++ sources. |
| **CMake** | http://www.cmake.org/   | Redistribution and use in source and binary forms, with or without modification, are permitted. | Cross-platform, open source build system.CMake is used to control the software compilation process generating native makefiles and workspaces that can be used in any compiler environment. |

| | | | |
|---|---|---|---|
| **Subversion** | http://subversion.apache.org/   | Apache License 2.0 | An open-source, centralized version control system characterized by its reliability as a safe haven for valuable data; the simplicity of its model and usage; and its ability to support the needs of a wide variety of users and projects, from individuals to large-scale enterprise operations. |
| **GCC** | http://gcc.gnu.org/   | GNU General Public License. | The GNU Compiler Collection includes a front-end for C++, as well as the associated GNU Standard C++ Library, best known as libstdc++. |

**Table 3-3: List of software tools and libraries required by GNSS-SDR.**

Some optional features may require other dependencies.

### *3.3.5 Software Features*

GNSS-SDR has been designed with flexibility, modularity and extendibility in mind. It provides a framework for GNSS signal processing, in which each module has well-defined interfaces that the user can populate with his/her own algorithms and then combine them in a custom receiver. Some working examples are already available. Table 3-4 lists the main features and current status of the open source software receiver.

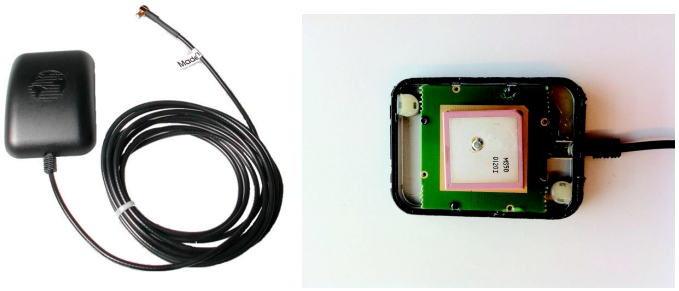
| Feature | Status | Comments |
|---|---|---|
| **Multiplatform** | Functional | Most Linux distributions (32 and 64 bits) and Mac OS X. |
| **Multithreaded** | Mature | Exploits multiple processors when available thanks to the thread-per-block software architecture. |
| **Works with files and several RF front ends** | Mature | Can work with files, any front-end compatible with the Universal Hardware Driver, and some other examples. |
| **Signal acquisition** | Functional | Acquisition of GPS L1 C/A, Galileo E1B and E1C signals, several algorithms available. |
| **Signal tracking** | Functional | Tracking of GPS L1 C/A, Galileo E1B and E1C signals, several algorithms available. |
| **Decoding of navigation message** | Functional | Demodulation of the navigation message GPS NAV. Decoding of Galileo INAV is in progress. |
| **PVT solution** | Functional | Simple PVT solution based on Least Squares. GPS-only. |
| **Standard output formats** | In progress | NMEA, RINEX and KML outputs for easy connection with other software tools. |

**Table 3-4: GNSS-SDR features and current status**

### *3.3.6 Equipment*

By nature, GNSS-SDR is a software tool that anybody can freely install anywhere, and its basic functionality does not require any extra equipment. However, serious experimentation requires the availability of some expensive (and sometimes, heavy) equipment for the controlled generation of radioelectrical scenarios, electromagnetic measurement devices, and electric ancillary for the radiofrequency front-end. Through EuWIn, CTTC is offering the following equipment:

| Equipment | Comments |
|---|---|
| **RF signal generator** | Agilent's Vector Signal Generator ESG 250K-6GHz (Model: E4438C) equipped with GPS Personality that simulates a multisatellite GPS signal for GPS L1/L2 C/A receiver testing. This firmware option provides the capability to verify functionality of embedded GPS chips in mobile consumer products such as cellular phones and handheld receivers. The predefined scenarios can be loaded to the instrument using the scenario files, freely available at Agilent website. An option that provides the following features:<br>• Multi-satellite GPS configuration (1 to 8 satellite capability).<br>• Signal simulates real world scenarios (multiple scenarios available).<br>• Real satellite data (synchronized satellites with Doppler shifts and navigation messages).<br>• Scenario playback duration up to 30 minutes.<br>  <br>**Figure 3-11: Agilent E4438C ESG with GPS Personality option.** |
| **GNSS antennas** | Assortment of GNSS antennas:<br>• **Novatel GPS 600 Active antenna:**<br>The Model 600-G antenna is an active antenna designed to operate at the GPS and GLONASS L1 and L2 frequencies. The slot array antenna element is coupled to a low noise amplifier (LNA). The unit is optimized to receive right-hand-circularly-polarized signals. Its radiation pattern is shaped to reduce signals |

| | |
|---|---|
| | arriving at low elevation angles. These features decrease the errors associated with electromagnetic interference and multipath. The antenna is intended for surveying and other kinematic positioning applications.<br>  <br>**Figure 3-12: Novatel GPS 600 L1 and L2 antenna.**<br>• **Garmin GA27c**<br>The Garmin GA27c is a low cost, low profile active ceramic-patch type antenna with a magnetic mount. It is intended to be used for automotive GPS L1 C/A receivers.<br>  <br>**Figure 3-13: Garmin GA27c GPS L1 antenna.** |
| **Oscilloscope** | Tektronix's TDS7254 Digital Phosphor Oscilloscope 2.5GHz |
| **Spectrum analyzer** | Agilent's E4403B. |
| **Network analyzer** | Rohde & Schwarz's ZVA24-M2 24GHz, 4 Ports Vector Network Analyzer |
| **Universal Software Radio Peripheral** | The EuWIn laboratory at CTTC is equipped with two USRP1 (USB 2.0) mainboards, one of them modified to use an external sampling clock. In addition, two USRP2 (Gigabit Ethernet) mainboards are available on request. This equipment is supported by the GNU Radio toolkit and by the GNSS-SDR software. Table 3-6 and Table 3-7 show the most relevant features of USRP 1 and USRP 2.<br>In order to receive GNSS signals with the USRPs equipment, the laboratory is equipped with two DBSRX2 daughterboards with the features listed in Table 3-8. |
| **SiGe GN3S Sampler v2 +** | The USB GN3S sampler v2 GPS L1 RF front-end dongle is based on the SiGe 4120 GPS IC, that provides a data stream with a sampling frequency |

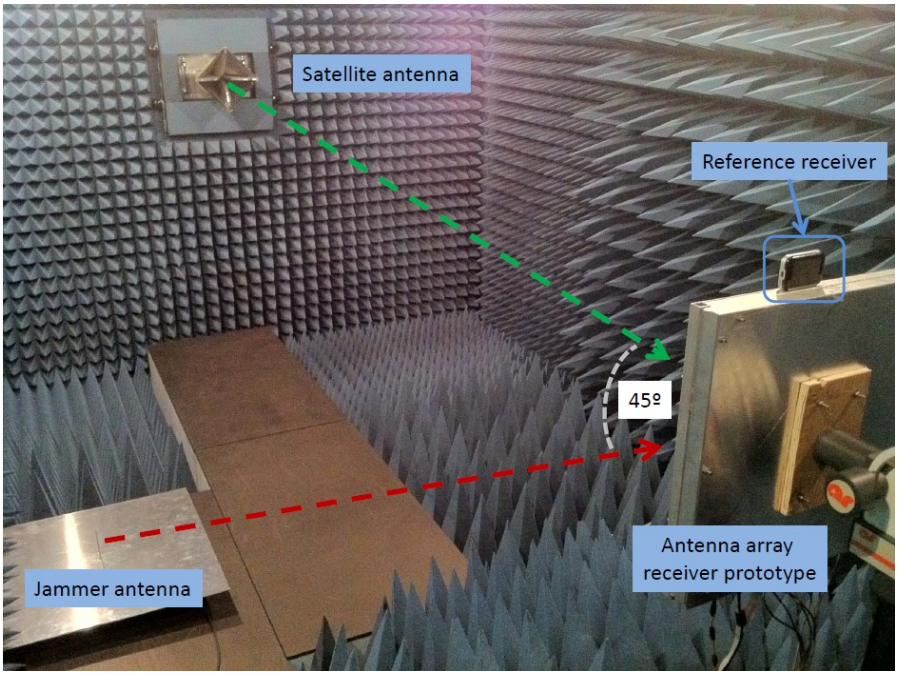
| | |
|---|---|
| **Magnetic mount GPS L1 active patch antenna** | of 16:3676 MHz and a bandwidth up to 4.4 MHz with 2 bits per sample. It is supported by GNSS-SDR as a real-time signal source. |
| **Access to anechoic chamber** | CTTC's anechoic chamber was designed by the group ETS-Lindgren as a turnkey solution for making antenna measurements of wireless telecommunication devices. The system can be used to perform antenna measurements in far-field test distances for more generic antenna properties such as 3D radiation pattern. The measurement setup including multi-axis positioner, positioning controller, commercial software for antenna measurements, and fully anechoic chamber is completely automatic.   **Figure 3-14: GNSS interference experimentin the CTTC anechoic chamber.** |
| **RF ancillary (connectors, cables, power sources, etc.)** | General equipment of a RF Lab is available. |

**Table 3-5: List of equipment available at EuWIn@CTTC for working with GNSS-SDR**

| Feature | Value |
|---|---|
| **Computer interface** | USB 2.0 |
| **ADC** | Two Dual 64 MS/s, 12-bit ADC's |
| **DAC** | Two Dual 128 MS/s, 14-bit DAC's |
| **Onboard TXCO** | 25 ppm TCXO Frequency Reference |
| **External sample clock input** | YES |
| **Dual band operation (dual daughterboard slot)** | YES |

| | |
|---|---|
| **ADC Wideband SFDR** | 85 dBc |
| **DAC Wideband SFDR** | 83 dBc |
| **Host Sample Rate (8b/16b)** | 16/8 MS/s |

**Table 3-6: USRP1 features**

| Feature | Value |
|---|---|
| **Computer interface** | Gigabit Ethernet |
| **ADC** | One Dual 100 MS/s, 14-bit ADC |
| **DAC** | One Dual 400 MS/s, 16-bit DAC |
| **Onboard TXCO** | 5 ppm TCXO Frequency Reference |
| **External sample clock input** | YES |
| **Dual band operation** | NO |
| **ADC Wideband SFDR** | 88dBc |
| **DAC Wideband SFDR** | 80dBc |
| **Host Sample Rate (8b/16b)** | 100/50 MS/s |

**Table 3-7: USRP2 features**

| Feature | Value |
|---|---|
| **Frequency coverage** | 0.8-2.3 GHz. |
| **Analog bandwidth** | 1-60 MHz |
| **Output type** | Analog Baseband (I/Q) |
| **Noise figure** | 5 dB |
| **Gain** | 80 dB |

**Table 3-8: DBSRX daughterboard features**

## 3.4 OpenInLocation

### *3.4.1 Rationale*

It is commonly agreed that GNSS cannot be the unique technology for positioning, especially in indoor scenarios with no line of sight with the GNSS space vehicles. Global navigation systems need to be complemented with other local aids, such as inertial measurement units, external information provided by wireless networks, signals of opportunity or dedicated wireless infrastructure.

In order to explore the potential of several technologies for positioning with a hands-on approach, we propose an open laboratory to drive R&D and innovation in indoor location, evaluating state-of-the-art and commercial technologies in challenging environments (*i.e.*, the presence of strong multipath echoes, non-line-of-sight (NLOS) conditions, high signal attenuation) and improving them in terms of a well-defined objective: to enable High-Definition Situation-Aware (HDSA) applications and services. These include, among others:

- Logistics.

- Augmented reality.
- Security applications: tracking and monitoring of unauthorized persons in secured areas.
- Management: location and tracking of people and key resources.
- Emergency services.
- Search and rescue operations.
- Automotive safety.

During the execution of NEWCOM++, a huge amount of work was devoted to the development of positioning schemes and experimentation with commercial devices. In NEWCOM# we want to take this research further and make it widely available by implementing algorithms in commercial, low-cost devices. Although building testbeds for indoor location will be the first short-term target, OpenInLocation is designed with the aim of going towards the Living Lab concept, where real users will shape development, integrating research and innovation processes through the co-creation, exploration, experimentation and evaluation of innovative ideas, scenarios, concepts and related technological artifacts in real life use cases.

The mission of OpenInLocation is to accelerate the development of cutting-edge indoor location solutions to be used worldwide by fostering collaboration and contributing with new ideas for indoor positioning, disseminating results and outreaching to new audiences beyond NEWCOM#.

### *3.4.2 Description*

The technology mix demanded by indoor location solutions requires a laboratory in which users can access a wide range of interfaces to an heterogeneous set of devices and form factors, and some processing capability to blend those inputs and provide the final output, that is, the device's position. This implies flexibility in the number and type of sources, as well as the possibility to implement low-level algorithms in order to process low data, fast enough to achieve real time. Considering such requirements, we have set an open laboratory with the following main features:

- Hands-on, hardware and software oriented activities.
- Addresses the technology mix required for indoor positioning.
- Promotes collaboration and sharing by using low-cost development platforms.
- Promotes reproducible research.
- Open to industry and institutions beyond NEWCOM# members.

In recent years, we have witnessed the bloom of low cost, credit-card sized computers such as Raspberry Pi or Arduino. Those devices (both are under 50 €) embrace the Open Hardware and Open Software approach, building a community of developers and enthusiastic users around the World. In this approach, hardware design (i.e. mechanical drawings, schematics, bill of materials, PCB layout data, HDL source code and integrated circuit layout data), in addition to the software that drives the hardware, are all released under an open license that permits users to study, change, use and improve it. This creates vibrant ecosystems around those products, providing support, development and promotion of their hardware, software and related resources. Those ecosystems include the supply chain, the support community and the education section. The aim of OpenInLocation is to exploit the synergies already created in those ecosystems and to merge the experience and know-how of the research staff involved in NEWCOM#, contributing with new ideas and

developments and thus expanding the range of tools available to the whole community, both within NEWCOM# institutions as well as to other institutions and the general public.

Using Raspberry Pi, Arduino or similar platforms, this laboratory allows the implementation, experimental validation and/or performance assessment of sensors and radio interfaces in both controlled and real-world environments, providing the user with practical, easy-to-reproduce-at-home hardware setups and software tools that allow focusing in location-related issues instead of spending time and money in building and programming a dedicated platform. In addition to the equipment provided at EuWIn@CTTC for experimentation, this laboratory aims to provide open access to practical information on how the experiments were made, using widely available, low-cost platforms when possible, thus promoting peer-reviewing and collaboration within users with common interests.

### *3.4.3 Equipment*

EuWIn@CTTC OpenInLocation laboratory is equipped with the required hardware to implement positioning algorithms using the following technologies:

- RF RSSI-based positioning
  - WiFi 802.11 B/G
  - Bluetooth 4.0
  - Zigbee
- RFID positioning
  - Active tags
  - Passive tags

The laboratory is composed of a set of programmable wireless nodes that can act either as anchor node or as a mobile node. In addition it is also available the USRP SDR platform for advanced operations such as RF channel characterization and RF fingerprinting measurements.

Two different wireless nodes hardware are available depending on the application and computational requirements:

- **High Performance Node** platform composed of Raspberry Pi, an open-source single-board ARM 11 processor-based computer capable of running Linux O.S, and
- **Low Power Node** platform composed of the Arduino Uno open-source microcontroller board populated with an Atmel ATmega328 MCU.

The RF measurement devices described above for GNSS-SDR will be also available for OpenInLocation activities at EuWIn@CTTC premises.

Hereafter, we provide the specifications for both the high performance and low power platforms.

**High Performance Nodes: Raspberry Pi**

The Raspberry Pi is a credit-card-sized single-board computer developed in the UK by the Raspberry Pi Foundation with the intention of promoting the teaching of basic computer science in schools.

The platform was designed with open source software development in mind. It has a Broadcom BCM2835 system on a chip (SoC), which includes an ARM1176JZF-S 700 MHz

processor (The firmware includes a number of "Turbo" modes so that the user can attempt overclocking, up to 1 GHz, without affecting the warranty), VideoCore IV GPU, and 512 MB of RAM, a microSD slot, and two USB host ports.

| Component | Feature |
|---|---|
| **Processor** | Broadcom BCM2835 700MHz ARM1176JZFS processor with FPU and Videocore 4 GPU. GPU provides Open GL ES 2.0, hardware-accelerated OpenVG, and 1080p30 H.264 high-profile decode. |
| **Operating Voltage** | 5V (microUSB powered) |
| **RAM memory** | 512MB RAM |
| **Storage and OS memory** | SD card socket up to 32 GB. Boots from SD card, running a version of the Linux operating system. |
| **Networking** | 10/100 Base-T Ethernet socket |
| **USB** | 2 x USB 2.0 sockets |
| **HDMI video out socket** | YES |
| **RCA composite video out socket** | YES |
| **Audio** | 3.5mm audio out jack |
| **Video input** | Raspberry Pi HD video camera connector |
| **Size** | 85.6 x 53.98 x 17mm |

**Table 3-9: Raspberry PI model B features.**

**Figure 3-15: Raspberry PI model B board.**

## Low Power Node: Arduino

The Arduino Uno is a microcontroller board based on the ATmega328. It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz ceramic resonator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with an AC-to-DC adapter or battery to get started.

| Feature | Value |
|---|---|
| **Microcontroller** | ATmega328 |
| **Operating Voltage** | 5 V |
| **Input Voltage (recommended)** | 7-12 V |
| **Input Voltage (limits)** | 6-20 V |
| **Digital I/O Pins** | 14 (of which 6 provide PWM output) |
| **Analog Input Pins** | 6 |
| **DC Current per I/O Pin** | 40 mA |
| **DC Current for 3.3V Pin** | 50 mA |
| **Flash Memory** | 32 KB (ATmega328) of which 0.5 KB used by bootloader |
| **SRAM** | 2 KB (ATmega328) |
| **EEPROM** | 1 KB (ATmega328) |
| **Clock Speed** | 16 MHz |

**Table 3-10: Arduino Uno features.**

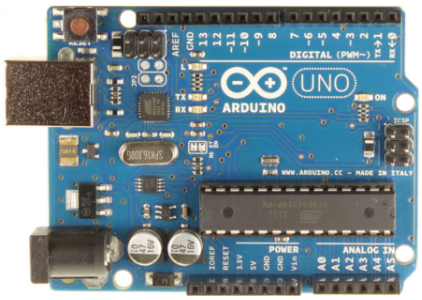



**Figure 3-16: Arduino Uno platform.**

**Sources of information for indoor location**

- **3-axis accelerometer module**

Both platforms can be equipped with a 3-axis accelerometer module to integrate inertial measurements in the positioning algorithm. This module will be upgraded to a complete Inertial Measurement Unit (IMU) featuring also a 3-axis gyroscope. The data connection is established using a simple TTL serial interface and the module power supply is drawn from the node mainboard. Table 3-11 shows the selected accelerometer module for the EuWin laboratory.

| Module | Chipset | Range and measure rate | Link |
|---|---|---|---|
| TRIPLE AXIS ACCELEROMETER BREAKOUT | MMA8452Q | ±2g/±4g/±8g dynamically selectable full-scale Output Data Rates (ODR) from 1.56 Hz to 800 Hz | http://www.cooking-hacks.com/index.php/shop/sensors/triple-axis-accelerometer-breakout-mma8452q.html |

**Table 3-11: 3-axis accelerometer module.**

- **WiFi 802.11 b/g module**

The support for WiFi RSS positioning will be available only in the HPN platform due to the hardware driver requirements. The selected interface to the 802.11b/g chipset is the USB 2.0 to facilitate the integration into the Linux operating system.

The selection criterion for both the chipset manufacturer and model is based on the availability of a complete open-source driver and firmware implementation. It should be supported in the Linux kernel. Currently, the Atheros chipset family is one of the most well documented and supported chipsets. CTTC has previous experience in the development of advanced 802.11 protocol modifications for Atheros PCI chipsets that can be ported to the USB version.

There are several manufacturers that provide a USB WiFi dongles featuring Atheros chipsets. A desirable one should support the ath5k or ath9k kernel driver implementation. A complete list of specific chipset models is available at http://wikidevi.com/wiki/Atheros

- **Bluetooth module**

In order to implement Bluetooth-based networks and to measure the RSS a suitable Bluetooth module will be selected according to the following requirements:

- ✓ Master and slave working modes
- ✓ TTL Serial interface
- ✓ RSS beacon measurements accessible from the AT command operation
- ✓ External antenna connector desirable to use custom antenna designs

Table 3-12 shows the selected Bluetooth modules to be evaluated at the EuWin lab.

| Module | Chipset | Antenna connector | Link | Bluetooth version |
|---|---|---|---|---|
| BT-05 / BTH-07 | CSR BC417 | NO | http://www.elecfreaks.com/store/bluetooth-modem-minimum-passthrough-module-p-229.html | 2.1 |
| BlueGiga WT11i-A | Proprietary | NO | http://www.bluegiga.com/WT11i_Class_1_Bluetooth_Module | 2.1 + EDR |
| Bluetooth X-BEE shell | PBA 31308/2 | SI | http://www.cooking-hacks.com/index.php/shop/arduino/arduino-bluetooth-module.html | 2.1 |
| Panasonic | PAN1326 HCI | NO | http://es.mouser.com/search/refine.aspx?Ntk=P_MarCom&Ntt=117252132 | 4.0 Dual Mode (both normal and low power profiles) |
| Bluegiga BLE113 | Proprietary | NO | http://www.bluegiga.com/BLE113_Bluetooth_Smart_module | 4.0 Dual Mode(both normal and low power profiles) |

**Table 3-12: Bluetooth modules.**

## 3.5 Facilities and Lab Equipment Outside CTTC Premises

In addition to the facilities and lab equipment that are made available at EuWIn@CTTC, other partners involved in WP2.1 will also make use of their own equipment and facilities to carry out joint research activities. In the following subsections, a brief description of these facilities and lab equipment outside the CTTC premises is presented.

### *3.5.1 Facilities and Lab Equipment at Bilkent University*

Bilkent University has TimeDomain PulsOn 410 Monostatic Radar Module (MRM), which is a coherent UWB radar module with 1.4 GHz of RF bandwidth. There are 4 transceiver (radar) units, which can be used to transmit UWB pulses and receive reflections from the objects in the environment. The units operate at a center frequency of 4.3 GHz.

### *3.5.2 Facilities and Lab Equipment at UPC*

The UPC platform for spectrum measurements is composed of a broadband discone-type antenna that covers the frequency range from 75 to 3000 MHz, a filter to remove FM audio broadcast signals, and a high-performance spectrum analyzer, a laptop to record the spectral activity and optionally a GPS. Figure 3-17 shows the measurement platform scheme.

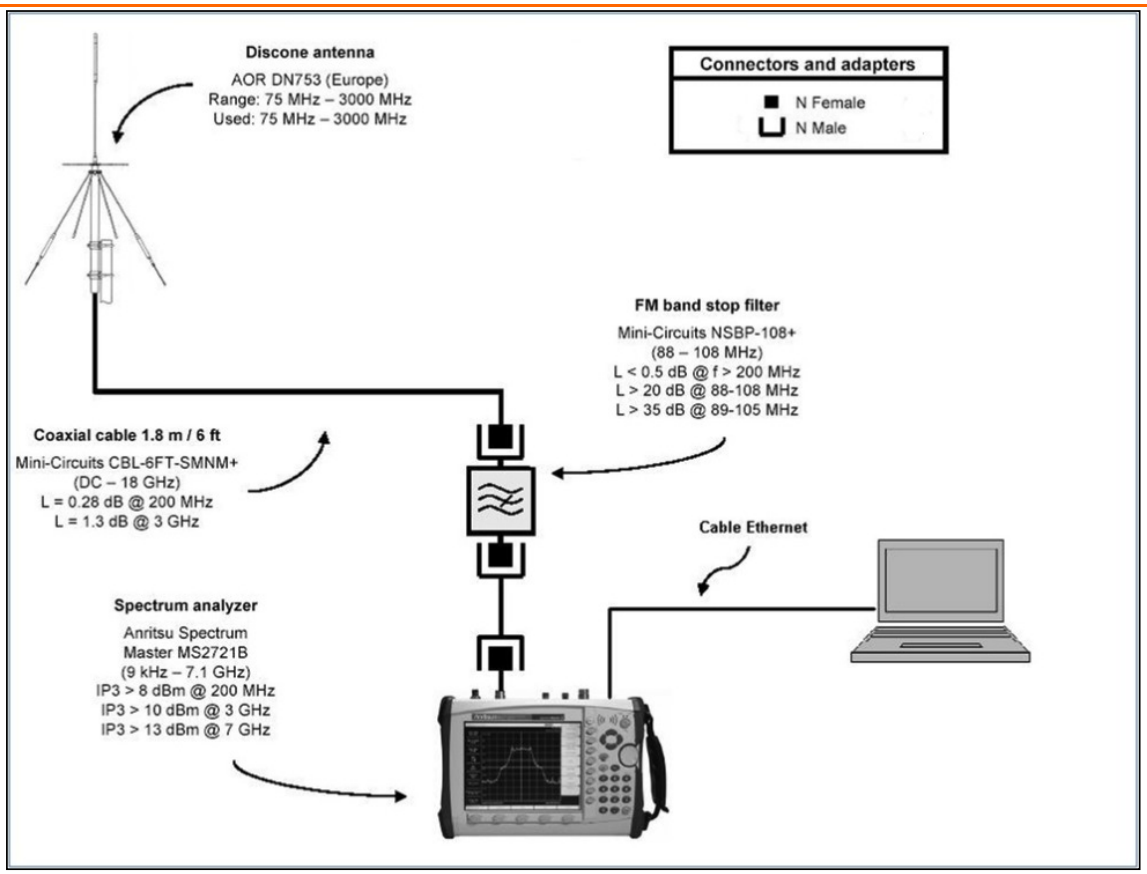



**Figure 3-17: Scheme of the measurement platform without GPS**

The AOR DN753 is a wideband antenna with vertical polarization and omni-directional receiving pattern in the horizontal plane. Even though some transmitters are horizontally polarised, they usually are high-power stations, such as e.g. TV stations, that can be detected even with vertically polarised antennas.

Anritsu Spectrum Master MS2721B is employed to provide power spectrum measurements and record the spectral activity over the complete frequency range Anritsu MS2721B Spectrum Analyser. This spectrum analyzer provides a measurement range from 9 kHz to 7.1 GHz, low noise levels and a built-in pre-amplifier (which facilitates the detection of weak signals), fast sweep speeds automatically adjusted, and various communication interfaces enabling the connection of external USB storage devices as well as controlling instruments. Moreover the handheld, battery-operated design simplifies the displacement of the equipment to different measurement locations.

The control subsystem, shown in Figure 3-18, is in charge of supervising the measurement process, retrieving the measurement data from the spectrum analyzer and saving the results in an appropriate format for off-line data post-processing. The control subsystem is mainly composed of a laptop, which is connected to the spectrum analyzer via an Ethernet interface. The laptop runs a tailor-made script under Matlab's software environment, which controls the measurement process. The control script communicates with the spectrum analyzer by means of the Matlab's Instrument Control Toolbox and making use of commands in SCPI (Standard Commands for Programmable Instruments) format with the VISA (Virtual Instrument Standard Architecture)-TCP/IP interface.

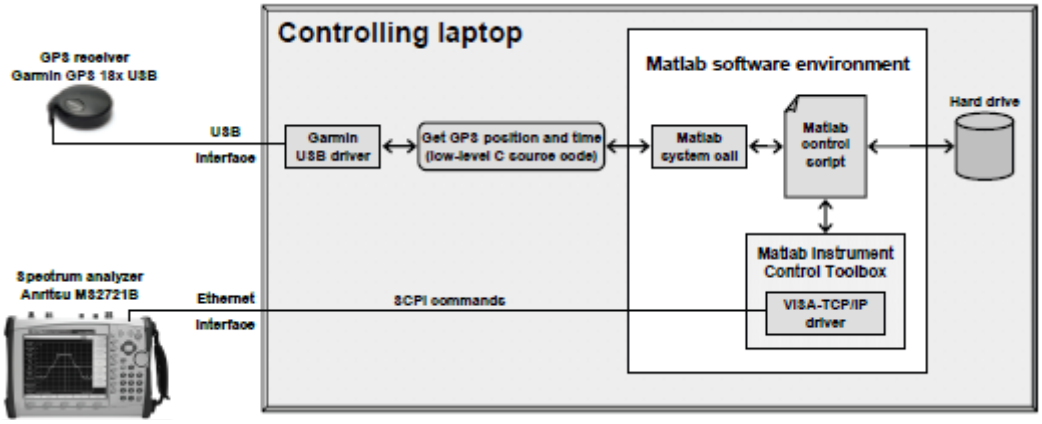



**Figure 3-18: Control Subsystem**

With the above platform, UPC has conducted in the last years a number of spectrum measurements and has developed a tool that records all the spectrum measurements carried out in several buildings and locations of Barcelona and surroundings. This website is located at http://spoc.upc.edu/ and gathers information about the spectrum occupancy behavior of the different relevant frequency bands, such as TETRA, TV, E-GSM, DCS1800, UMTS, etc. It includes results (per individual radio-channel or per the whole band) in terms of:

- Power associated parameters in terms of maximum, minimum, average, mode values or amplitude probability distribution,
- Duty Cycle in terms of Duty cycle of the Primary radio channel, Duty Cycle of the whole frequency band; effective bandwidth per band or relative occupancy,
- Temporal Evolution in terms of Time duration of spectrum holes or time interval between consecutive holes. These parameters can be computed in terms of their maximum, minimum, average, mode or Cumulative Distribution Function (CDF),
- Frequency evolution (contiguous bandwidth of spectral holes in terms of average, minimum, maximum and mode or CDF).

### *3.5.3 Facilities and Lab Equipment at UCL*

The ElektroBit channel sounder available at UCL is composed of two multi-antenna units, as shown in Figure 3-19: a transmitter unit and a receiver unit, which is composed by two modules, one of which is the data acquisition module. Each unit is controlled by the user with a laptop computer through a LAN connection.

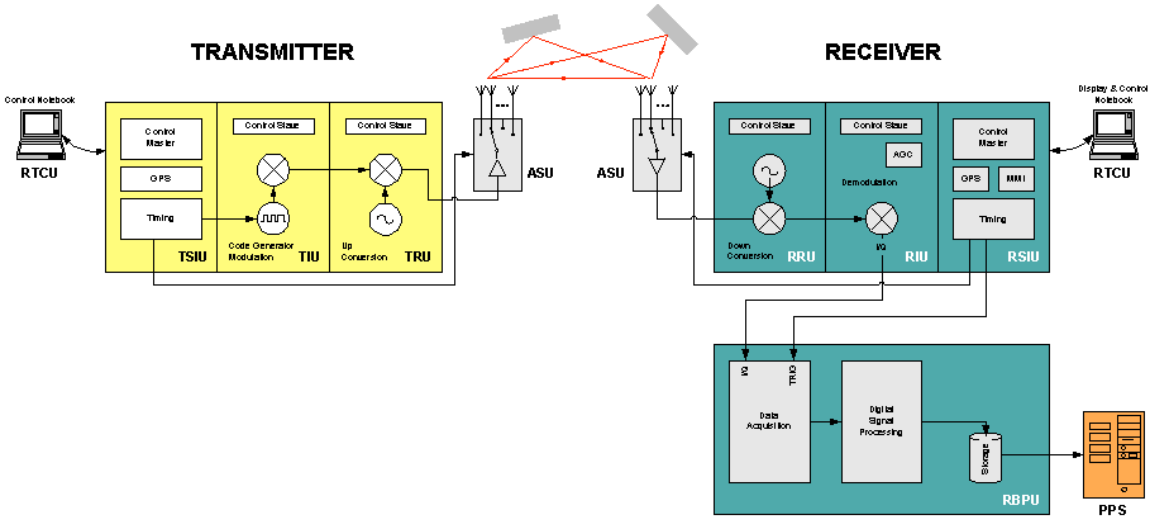



**Figure 3-19: ElektroBit channel sounder picture (above) and block diagram (below)**

At transmit side, a pseudo-noise sequence is generated and used to modulate the transmitted signal that is up-converted to radio frequency from an intermediate frequency. Similarly, at the receiver side, the received signal is down-converted and demodulated into I/Q format. A crucial step in all measurement campaigns where the two units are separated is the synchronization of the local oscillators, which employ Rubidium clocks. In the ElektroBit channel sounder, this consists in two steps: the synchronization in a strict sense, where the relative phase rotation is minimized by tuning the atomic clocks, and the time-tag synchronization, where a common absolute time reference is given to the two units. The synchronization is kept for long time, but phase drifts can be present also after synchronization. These may generate linear phase variations in a static environment, that have to be corrected in post-processing. In Clock-Keep Alive (CKA) mode, it is possible to move the sounder without external power supply and without losing synchronization.

Another important concept is the one of timing. The basic unit is the chip, which represent one symbol of a code. The chip rate is the metric that controls the timing. The higher the chip rate, the better the delay resolution of the measured impulse response. The delay sampling resolution can be evaluated as:

$$\tau_{resolution} = \frac{1}{N_{sc} f_{chip}}$$

where $N_{sc}$ is the number of samples per chip. The chip rate is limited by the bandwidth $B$, as $f_{chip} = B/2$. Each transmitted code is formed by several chips. The length of a code has to be longer than the maximum measurable delay in the propagation scenario but shorter than the Doppler period, i.e. the time for which the channel can be considered constant. Longer

codes also produce higher processing gain, thus improving the dynamic range. The measurable excess delay is:

$$\tau_{excess} = \frac{N_{chip}}{f_{chip}}$$

where $N_{chip}$ is the code length in chips. For each transmitting antenna, a number of codes equal to the receiving antenna plus one is transmitted. The supernumerary code serves as guard, needed to let the transmitter switch to the next antenna in the sequence. When all receive ($N_r$) and transmit ($N_t$) antennas are scanned, the acquisition cycle, which represents the measured channel at a certain time, is concluded. For each acquisition cycle, the number of codes is given $N_t/(N_r + 1)$

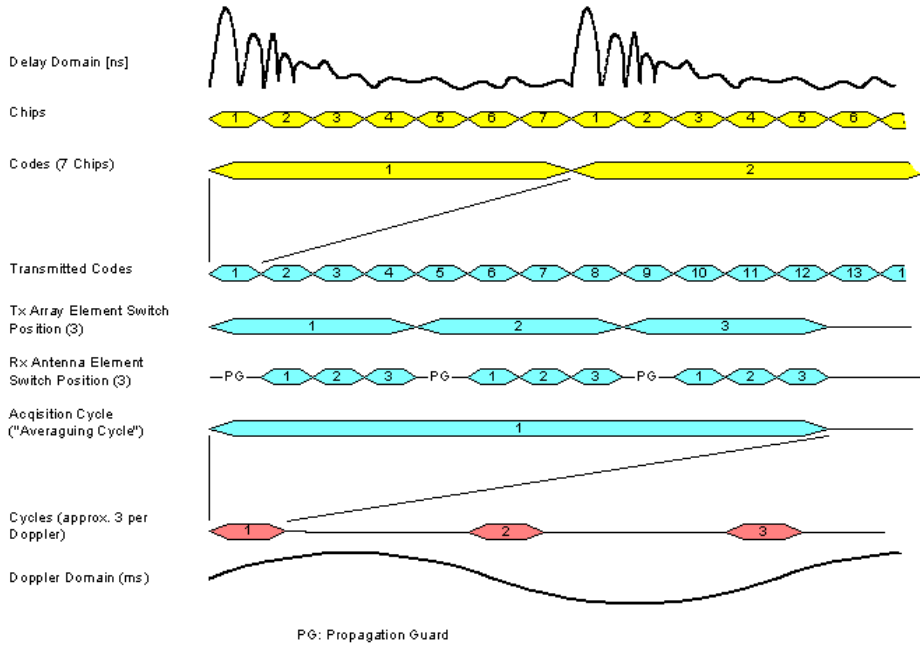



**Figure 3-20: ElektroBit channel sounder timing concepts**

In case of high Doppler scenarios, the cycles can be measured in bursts, i.e. during part of the time cycles are measured and during the rest data are stored on the disk, without taking measurements.

Input parameters can be introduced in the channel sounder via the laptop connection with the help of an easy-to-use set-up wizard.

Before starting the data acquisition, a calibration measurement is required. This consists in measuring a well-known channel that normally is an attenuator of given attenuation back-to-back connected to the units via the measurement cables. This produces the system response that can be used in post-processing to compensate for system and cable losses.
Finally, Table 3-13 presents all input parameters to be defined before the measurements and their acceptable values.

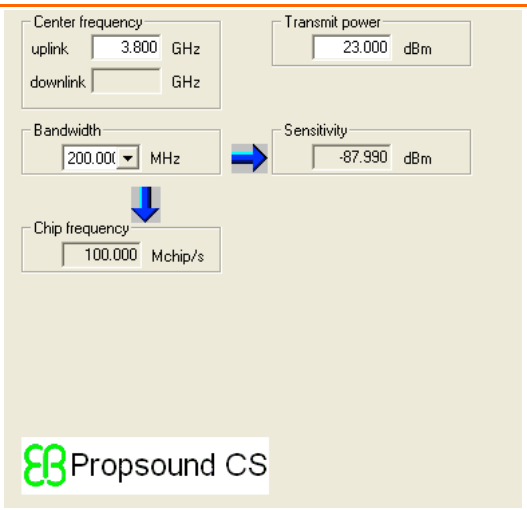



**Figure 3-21: ElektroBit set-up wizard**

| | |
|---|---|
| Carrier frequency | from 3.5 to 4.2GHz |
| Bandwidth | from 1.5 to 200MHz |
| Transmit power | default value 23dBm |
| Number of samples per chip | from 1 to 10 |
| Max. path length | Sets the min. code length in chips |
| Number of Tx antennas | from 1 to 8 |
| Number of Rx antennas | from 1 to 8 |
| Max. mobile/scatterer speed | Sets the min. channel sample rate |

**Table 3-13: Input parameters for ElektroBit channel sounder**

### *3.5.4 Facilities and Lab Equipment at PUT*

In PUT lab following list of equipment will be used:

- USRP N210 devices with WBX/XCVR2450 boards. These devices can be used for the transmission and reception of complex samples in a wide range of frequencies thanks to daughterboard: WBX: 50-2200MHz, XCVR2450: 2.4-2.5 GHz and 4.9-5.9 GHz. The USRPs boards, in case of receiver, are used to convert radio-frequency samples to baseband complex values transmitted to standard PC computer via Gigabit Ethernet interface. In transmitter mode, baseband complex samples generated at computer are frequency shifted and Digital-to-analog converted on the USRP board before being sent to its antenna port. Maximum output power is 100 mW. For baseband processing a number of software radios platforms can be used on a computer, e.g. GNU radio (gnuradio.org) and IRIS (http://www.softwareradiosystems.com/redmine/projects/iris) are considered.

- Rohde & Schwarz FSLv6 spectrum analyzer, 9 kHz to 6 GHz. This device can be used as typical spectrum analyzer, i.e. for power spectral density estimate, but also to analyze, collect or demodulate complex samples (signal bandwidth up to 28MHz). It

can be remotely operated via GPIB or Ethernet interface. Thanks to built-in preamplifier signals of low power can be detected.

- Rohde & Schwarz SMBV 100 A Vector Signal Generator, 9 kHz to 6 GHz. This device can be used for generation of signals following contemporarily used digital standards, e.g. 3GPP LTE FDD, GSM, EDGE, WLAN and DVB-T. Additionally some frontend distortions, e.g. IQ imbalance, local oscillator offset with addition of white noise signal. Output power ranges from -145 dBm to 18 dBm.

# 4. Preliminary Plans of Activities and Policies

This Section gives details regarding the plans of activities for the next six months (M7 to M12), leaving to the annual Deliverables (to be delivered at M12) the definition of the activities planned for the next years. The Section also provides description of the policy agreed to give access to the lab facilities.

## 4.1 Introduction

Track #2 intends to create a framework that will survive to the end of Newcom#. Therefore, on the one hand the plan of activities has been devised as a component of the NoE; on the other, all dissemination and promotional actions are conducted under a more general perspective. For the same reason, the access policy has been discussed under a long-term vision.

## 4.2 Steps Followed

The achievements of Track #2, after the first six months of Newcom# fully dedicated to the lab set-up and the definition of the activity plan, have been reached through the following sequence of steps and actions:

- Set-up of the facilities and creation of the documentation needed for the open access at the individual site premises, since kick-off till M6; it is envisaged that the sites will undergo continuous update during the course of Newcom#;

- Face-to-face meetings among the EuWIn Director and the three WPLeaders to discuss about EuWIn goals and plans, at the Newcom# kick-off meeting (November 2012, Pisa) and the Track #1 meeting (March 2013, Paris);

- Monthly skype meetings among the EuWIn Director and the three WP Leaders to discuss the status of lab set-up and coordinate activity plans;

- First presentation of the EuWIn scopes and facilities in Pisa, during the Newcom# kick-off meeting;

- A Track #2 session dedicated to the discussion of JRAs and presentation of EuWIn facilities in Paris, on March 7, during the Track #1 meeting;

- A Track #2 web meeting held on April 9, discussing among all researchers involved, the access policy and the plan of activities.

## 4.3 Research-Specific Plans of Activities

From a research point of view, Newcom# WP2.1 is divided in four tasks:

Task 2.1.2: Low-energy-consumption and low emission radio interfaces
Task 2.1.3: Hybrid localization techniques for wireless terminals
Task 2.1.4: High specrtally-efficient radio interfaces
Task 2.1.5: Channel measurements, modelling, and databases

The initial Task 2.1.1 “Lab set-up, maintenance, and planning” contains some technical activities, but is lacking a research focus.

The GEDOMIS® tesbed will be the main asset around which research activities for Tasks 2.1.2, 2.1.4, and 2.1.5 will revolve. Regarding Task 2.1.3, the key assets from EuWIn@CTTC will be the GNSS-SDR platform and the OpenInLocation lab.

At time of preparation of this Deliverable, 14 preliminary joint research activities (JRA) have been proposed. The consolidation of these JRAs and, possibly, the addition of new ones will be carried out during the Track 2 meeting that will take place in Bologna in July 2013. A list of these JRA together with their short description follows:

| JRA Title | Enhanced NC-OFDM transmission with reduced spurious emission level |
|---|---|
| Proposer Partner | PUT |
| Related Task | Task 2.1.2 and Task 2.1.4 |
| Description | Reduction of subcarrier spectrum sidelobes and intermodulations (caused by nonlinear power amplifier characteristic and high Peak-to-Average Power Ratio of OFDM signal) in the transmitter (and corresponding reception algorithms in the receiver) will allow for dynamic generation of signal well localized in frequency, i.e. with “clean” power spectrum density plot. Algorithms other than digital filtering are considered as they can provide lower computational complexity and higher flexibility (in choosing set of subcarriers used in non-contiguous [NC] manner) in comparison to typical digital filtering. At PUT we have some basic implementation of Cancellation Carriers + Windowing method operating using USRP hardware. Further development is required to take into account intermodulations caused by hardware imperfections (predistortion or PAPR reduction mechanisms). Tests of algorithms on other frontends are recommended. |

| JRA Title | Practical Implementation of Polar Codes |
|---|---|
| Proposer Partner | CNIT |
| Related Task | Task 2.1.4 |
| Description | Polar codes have proved to achieve capacity under specific conditions. Different algorithms have been proposed for decoding polar codes with different tradeoffs between decoding complexity and performance. This task will address the design of efficient hardware architectures for decoding polar codes. Among the algorithms that will be studied are belief propagation decoding and successive cancellation decoding. |

| JRA Title | Design and experimental validation of algorithms for active and passive indoor positioning |
|---|---|
| Proposer Partner | Bilkent |
| Related Task | Task 2.1.3 and Task 2.2.2 |

| | |
|---|---|
| Description | Indoor localization remains as a challenging problem, the solution of which could trigger a myriad of new services and applications. UWB has been recognized as a feasible technology for solving that problem. However, there are still issues that need to be addressed like the implementation of estimation and tracking algorithms for indoor UWB/RSSI positioning and radar applications or the investigation of cooperation techniques in cloud moving users |

| | |
|---|---|
| JRA Title | Assessment and development of multi-link channel models |
| Proposer Partner | UCL |
| Related Task | Task 2.1.5 |
| Description | Multi-link channels are met in cooperative scenarios, where the correlation between distributed (possibly MIMO) channels may largely impact the performance (throughput, etc.). This JRA aims at exploring the multi-link aspects of radio channels, and to propose models for design and simulation. |

| | |
|---|---|
| JRA Title | Channel models for cooperative positioning |
| Proposer Partner | UCL |
| Related Task | Task 2.1.5 |
| Description | This JRA aims at exploring the multi-link aspects of radio channels for positioning purposes, and at proposing models for design and simulation. The goal is to develop and experimentally validate representations of complex multi-link radio channels for cooperative indoor positioning. |

| | |
|---|---|
| JRA Title | Vehicle-to-X dynamic relay channel modeling |
| Proposer Partner | UCL |
| Related Task | Task 2.1.5 |
| Description | This JRA aims at developing models for relay scenarios in vehicular settings, e.g. V2V2V or V2V2I. The goal is to develop and experimentally validate channel models for relay scenarios in vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) networks, accounting for the non-stationarity in such settings. |

| | |
|---|---|
| JRA Title | PAPR reduction algorithms for OFDM-like systems: An implementation and experimental validation |
| Proposer Partner | CNRS |
| Related Task | Task 2.1.2 |
| Description | Orthogonal Frequency Division Multiplexing (OFDM) signals are characterized by very high Peak-to-Average Power Ratio (PAPR) levels. This characteristic leads the OFDM signals to be very sensitive in nonlinearity of analog circuits of the transceiver, in particular those of the High Power Amplifier (HPA) at the |

| | |
|---|---|
| | emission. A HPA is conceived to operate in its saturation zone which corresponds to its high efficiency region. However, in this zone, the HPA has a severe non-linear behavior. These nonlinearities are sources of In-Band (IB) distortions which can both degrade the link performance in term of Bit Error Rate (BER) and also cause significant Out-Of-Band (OOB) interference products that make it harder for the operator to comply with stringent spectral masks. For these reasons, reducing the PAPR of OFDM signals is increasingly being considered to be very important in maintaining the cost-effectiveness advantages of OFDM in practical systems. Many methods have been proposed to mitigate the OFDM PAPR by acting on the signal itself. An original classification representation for PAPR reduction techniques was studied and proposed by *SUPELEC-IETR*. |

| | |
|---|---|
| JRA Title | High spectrally-efficient radio interfaces |
| Proposer Partner | CNIT |
| Related Task | Task 2.1.4, Task 1.3.1 and Task 2.3.2. |
| Description | Classical high efficiency design techniques for the transmitter power amplifier are well suited with constant or quasi-constant envelope signals, while become less effective when adopted with high PAR modulation schemes.<br><br>Furthermore, the very stringent linearity requirements of such systems, often forces the power amplifier to operate very far from saturation and with additional linearization circuits, both negatively affecting the overall efficiency.<br><br>Our aim is evaluation and test of the envelope tracking technique, a system architecture that offers very good results in terms of power efficiency when operating with high PAR (6-9 dB) modulation schemes. |

| | |
|---|---|
| JRA Title | Compressive sensing for sparse propagation channel estimation |
| Proposer Partner | CNRS |
| Related Task | Task 2.1.5 |
| Description | Mainly due to the relative mobility of the transmitting and receiving equipments, the wireless propagation channel is time varying. Under the assumptions of linearity and time invariance during the measurements, the propagation channel is completely characterized by its Complex Impulse Response (CIR). In order to overcome this time varying property, the wireless telecommunication systems periodically estimate the CIRs. In this framework, we propose to use compressive sensing toward the estimation of the CIR. |

| | |
|---|---|
| JRA Title | Experimentation for multiple source detection, localization, and transmit power estimation |
| Proposer Partner | IASA |

| | |
|---|---|
| Related Task | Task 2.1.3 |
| Description | Experimental assessment of passive localization techniques for cognitive radio applications. The main focus is on RSS based multiple radio source detection, localization and transmit power estimation. Other ranging techniques will be also considered depending on the platforms capabilities. |

| | |
|---|---|
| JRA Title | Integration and experimental validation of the Xilinx LTE channel coding IP combined with a video transmission using the existing LTE-based PHY-layer of CTTC |
| Proposer Partner | CTTC |
| Related Task | Task 2.1.4 |
| Description | The current LTE-based PHY-layer (DL) which is an HDL IP developed at CTTC does not include channel coding. Hence, the JRA will involve FPGA-based simulation, implementation, on-board testing and experimental validation of a channel coding processing block based on a Xilinx IP on top of the in-house PHY-layer. The LTE turbo encoding and decoding IPs (single license) are donated to CTTC for academic purposes. In order to sufficiently contemplate this IP block, an end application will also be included, which in our case is real-time HD video transmission and reception. |

| | |
|---|---|
| JRA Title | Energy profiling of PHY-layer schemes in LTE-based or WiMAX communication systems |
| Proposer Partner | CTTC |
| Related Task | Task 2.1.2 |
| Description | Real-time power consumption measurements of different LTE-based or WiMAX-based PHY-layer configurations (different multi-antenna scheme, different modulation etc) implemented in FPGA devices using an appropriate FPGA power monitoring HDL core, which takes advantages of the FPGA fabric voltage and current sensors. |

| | |
|---|---|
| JRA Title | Spectrum occupation measurements and database exploitation |
| Proposer Partner | CTTC/UPC |
| Related Task | Task 2.1.5 |
| Description | During the last years, and starting in NEWCOM++, UPC has built a semi-public database that contains spectrum occupancy measurements in different bands and locations in the area of Barcelona and neighborhoods.<br><br>Information contained in this database can be exploited by the partners for the development RRM strategies making use of flexible spectrum management.<br><br>Measurements have been obtained by means of a handheld Anritsu MS2721B Spectrum Analyser. |

| | |
|---|---|
| JRA Title | Efficient receiver algorithms based on approximate Bayesian inference for MIMO communications |
| Proposer Partner | AAU |
| Related Task | Task 2.1.4 |
| Description | Approximate Bayesian inference allows for approximating large probabilistic systems by simplified, tractable probabilistic structures over which typical operations (e.g. marginalization or maximization) are feasible to perform. The techniques are often formulated as message-passing algorithms over probabilistic graphical representations.<br><br>We explore the application of message-passing algorithms to the design of iterative receiver processing for high spectrally efficient wireless MIMO communications. The sought receivers iteratively combine channel estimation, MIMO equalization and channel decoding. |

## 4.4 Non-Research-Specific Plans of Activities

At time of preparation of this Deliverable, the following plans have been made. They are presented through the same itemised list reported in subsection 2.3.

1) **A Unique Portal**

   The first release of the website is made public at the end of M6, time of delivery of this Deliverable. The website will be updated every six months, based on the achievements at the end of each period.

2) **Web Meetings**

   Web meetings will be organized based on the request of Newcom# researchers. So, no periodic meetings are planned.

3) **Workshops**

   The first Newcom# Emerging Topic Workshop (ETW) will be dedicated to the theme that represents the motto of EuWIn: “Fundamental Research Through Experimentation”. It will be held in Bologna, at the premises of the EUWIn site, on July 8-9. The TPC of the workshop includes the three Track #2 WP Leaders, the EuWIn Director and Dr. Florian Kaltenberger of EURECOM. It will include three sequential sessions: one will be dedicated to industry speeches, one to presentations given by representatives of other EC funded projects, and the last one to talks given by Newcom# researchers involved in some experimental activities. At time of writing, a list of potential industry speakers and projects has been defined, and the invitations are sent. The final programme will be ready after delivery of this Deliverable, and will be posted on the EuWIn website under “EVENTS”. The workshop intends to group together separate experiences carried out in Europe, showing how experimental testbeds can be useful to fundamental research and the development of new techniques/protocols.

4) **Training Schools**

The first Newcom# Training School will be dedicated to the topic of interference management. It will be held in May 28-31, 2013 in Sophia-Antipolis at the premises of the EuWIn site of EURECOM. One of the four days of the school will be fully dedicated to experimental activities, involving the facilities of EURECOM and CTTC. The programme is available in the EURACON website www.euracon.org (EURACON is the association in charge of administration, logistics and publicity of the School).

The third Newcom# Training School will be dedicated to the topic of experimental research. It will be organized, jointly with the COST Action IC1004, in November 2013 in Barcelona at the premises of the EuWIn site. The school will comprise oral, poster and lab sessions. The programme will be defined before end of summer 2013. The TPC includes the three Track #2 WP Leaders, the EuWIn Director, Dr. Florian Kaltenberger of EURECOM, Prof. Claude Oestges of UCL. The programme will be available in the EURACON website www.euracon.org.

5) **Industry Liaisons**

During the third week of June 2013 (June 17) Newcom# will visit the Orange Labs at Issy-Les-Moulinaux, in France. The three EuWIn sites will present their facilities in that context.

6) **Demonstration activities**

The inaugural event of EuWIn will take place in Bologna, at the premises of the EuWIn site, on July 8, 2013. During this event, all EuWIn facilities will be presented to the public, both through talks and demos/posters. The event will be professionally video recorded in order to prepare two video trailers (one and five minutes, respectively) to be used for promotional purposes later. Industry representatives and researchers from other EC projects will be invited. EC officers will also be invited. The event will be followed (till the morning of the 9$^{th}$) by the Emerging Topic Workshop and (from the afternoon of the 9$^{th}$ till the 10$^{th}$) by the Track #2 meeting, which will include parallel networking sessions and plenary talks to present to all Newcom# researchers the scopes of Track #2 JRAs. The entire event will be a major occasion to show EuWIn facilities to many researchers and industry representatives.

7) **Experimental Tours**
This line of activity deals with PhD students visiting the three sites in sequence to perform measurements that are closely related and that are made toward a unified scope. This kind of activity is planned for the second year of Newcom#.

## 4.5 Access Policy

The policy for access to the EuWIn facilities has been thoroughly discussed by the WP Leaders under the coordination of the EuWIn Director, and the following decisions have been made. The discussion is reported based on the definition of the EuWIn spheres presented in this Deliverable.

**The Newcom# partners.**

They are given free of charge and prioritised access to the facilities (this was a commitment taken at time of DoW approval).

**The Newcom# associate institutions.**

As detailed in the deliverable D43.1 ("The NEWCOM# Handbook), the NoE has two types of Associate Partners: Type I, which are those more interested in conducting dissemination-related activities in collaboration with project partners; and Type II, the main aim of which is to conduct joint research activities in collaboration with project partners. Their number is not defined at time of writing of this Deliverable, since Newcom# can decide to accept new associate partners during its life. Access to EuWin wil be granted to Associate Partners, although in the case that a large number of partners is accepted the EuWIn sites can not commit to provide access to all of them. The general policy is that EuWIn intends to be as much open as possible, given the resource constraints (in terms of space, and availability of researchers for support). Therefore, it is decided that all Newcom# Associate Partners (both Type I and Type II) will have free of charge and open access to all information and data made available through the repository of the EuWIn website. On the other hand, physical access to the lab facilities will be as a rule restricted to Type II partners that have signed a specific agreement of cooperation with the NoE based on requests raised by the associate institutions (with specification of the goals and the mutual benefits), and on the availability of resources. These requests will have lower priority with respect to those coming from Newcom# full partners, and will be processed according to an order which will defined by the WP Leader for each EuWIn site, depending on the mutual benefits expected. Evidence of the access policy above will be given with publication on the (freely accessible) EuWIn website.

Revision of the rules of access to EuWIn will be performed every 12 months after the release of the present document, according to the experience gained during the previous operating period.

A welcome letter will be sent to new associate institutions upon previous agreement with one of the EuWIn WP Leaders, informing about the general policy of collaboration. These institutions will be listed on the EuWIn website for better visibility.

**External Institutions.**

In this case the policy depends on the specific platform and EuWIn site. The WP Leaders will decide whether to provide access to the databases and/or the facilities, and whether free of charge or based on the payment of a fee, on a case-by-case basis, in agreement with the guidelines and the approval of the Executive Board.

# 5. Conclusions

In this deliverable, the EuWIn lab as a whole and the EuWIn@CTTC site in particular have been presented and their initial set of planned activities have been described. Thus, stemming from the contents of this document the following can be concluded:

- The facilities at EuWIn@CTTC (whose main assets are **GEDOMIS®**, **GNSS-SDR**, and **OpenInLocation**) are ready to be utilized by all Newcom# partners participating in WP2.1 and also by the Newcom# associate institutions and external, third parties. The lab facilities that other partners (Bilkent, CTTC/UPC, UCL, and PUT) will utilize for part of their experimental research activities are also ready.

- During these first 6 months of project activity in WP2.1, the main workload has been devoted to the EuWIn@CTTC set-up and description of its facilities and interfaces. However, a remarkable effort has also been devoted to the proposal of initial JRAs where research on cutting edge topics related to next generation radio interfaces will be conducted through experimentation.

- In accordance with the estimation given in Newcom# DoW, the exact plan of JRAs and of other non-research specific activities will be fully detailed in D21.2, which is due in M12. The Track 2 meeting that will be held in Bologna in July 2013 will be instrumental to achieve this objective.

From all that has been said above, it is clear that the activities in WP2.1 are advancing in an appropriate pace and in accordance with the proposed schedule.

# 6. Appendixes

## 6.1 Appendix: GEDOMIS® Testbed HW & SW Specifications

### *6.1.1 Hardware*

| SIGNAL AND ARBITRARY WAVEFORM GENERATORS | | | | |
|---|---|---|---|---|
| **VENDOR** | **PRODUCT NUMBER** | **DESCRIPTION** | **UNITS** | **SHORT DESCRIPTION** |
| Agilent Technologies | E4438C | ESG Vector signal generator | 2U | High-end vector signal generator that combines outstanding RF performance and sophisticated baseband generation to deliver calibrated test signals at baseband, IF, and RF frequencies up to 6 GHz. |
| OPTIONS | E4438C-506 | Frequency range from 250 kHz to 6 GHz | 2U | Maximum frequency range option available. |
| | E4438C-UNJ | Enhanced phase noise performance | 2U | > 15 dB improvement over standard phase noise performance (High stability OCXO frequency reference with a high Q YIG oscillator) |
| | E4438C-005 | 6 GB internal hard drive | 2U | Extends the internal baseband generator's standard storage capacity from 1 MSa to over 1 GSa of non-volatile memory for each I and Q channel. |
| | E4438C-602 | Internal baseband generator, 64 MSa memory with digital bus capability | 2U | Integrates an advanced dual mode internal baseband generator with a state-of-the-art vector signal generator to facilitate complex I/Q modulation at RF frequencies. |
| | E4438C-003 | Enables ESG digital output connectivity with N5102A | 2U | Enables connectivity with the Agilent N1502A digital signal interface module, which provides digital outputs. |
| | E4438C-004 | Enables ESG digital input connectivity with N5102A | 2U | Digital input capability that provides fast, flexible means of upconverting digital baseband signals to a calibrated analog I/Q, IF or RF signal. |
| | E4438C-403 | Calibrated Noise (AWGN) Personality | 2U | Enables flexible stand-alone AWGN generation and for setting signal-to-noise ratios directly within select E4438C ESG signal creation software. The uncorrelated nature of the |

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| | | | | test stimulus is ideal for generating noise interference and is especially important for determining receiver performance. |
| Agilent Technologies | N5102A | Baseband Studio digital signal interface module | 2U | Provides fast and flexible digital inputs or outputs for the E4438C ESG vector signal generator. In output mode, it can deliver realistic complex-modulated signals directly to the digital devices and subsystems. In the input mode, the interface module ports your own digital input to the signal generator's baseband system, providing a quick and easy way of upconverting to calibrated analog IF, RF or µW frequencies. |

**Table 6-1: Vector signal generators option configuration and short description.**

| CHANNEL EMULATOR | | | | |
|---|---|---|---|---|
| **VENDOR** | **PRODUCT NUMBER** | **DESCRIPTION** | **UNITS** | **SHORT DESCRIPTION** |
| Elektrobit | C8 | EB Propsim C8 | 1U | Multi-channel fading emulator designed to fulfill the performance demands of MIMO system testing from 3GPP LTE, WiMAX, Wi-Fi to WCDMA. |
| OPTIONS | C800-1 | Fading Channel (RF and ABB) | 4U | Number of physical channels of emulator. |
| | C804-1 | Internal Local Oscillator 2toX | 1U | 2RF Internal Local Oscillators that provide ease of use to EB Propsim C8 in multichannel emulation as the emulator sets the correct local oscillator frequency automatically based on frequency setting. No external RF signal generators are needed for up and downconversion. |
| | C806 | MIMO Extension | 1U | Allows the emulation of up to 2x2 MIMO scenario within a single device. The MIMO extension option enables the possibility to “split” hardware channels so that two independent fading channels can be emulated by using only one physical channel of emulator. |

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|---|---|---|---|---|
| | C808 | Additional 24 paths/channel | 4U | Multipath propagation setting improvement (from 24 to 48 taps). |

**Table 6-2: Channel emulator option configuration and short description.**

| SPECTRUM / SIGNAL ANALYZER | | | | |
|---|---|---|---|---|
| **VENDOR** | **PRODUCT NUMBER** | **DESCRIPTION** | **UNITS** | **SHORT DESCRIPTION** |
| Rohde&Schwarz | R&S FSQ26 | 20 Hz to 26.5 GHz Signal Analyzer | 1U | The FSQ combines the outstanding spectrum analyzer features and functions of the FSU with a demodulation and analysis bandwidth that has been enhanced to 120 MHz. |
| OPTIONS | R&S FSQ-B72 | I/Q Bandwidth Extension | 1U | Signal analysis with up to 120 MHz bandwidth |
| | R&S FSQ-B100 | I/Q Memory Extension 235 Msamples | 1U | I/Q Memory Extension 235 Msamples |
| | R&S FSQ-K70 | Universal demodulation, analysis and documentation of digital radio signals | 1U | Firmware General Purpose Vector Signal Analyzer: Universal demodulation, analysis and documentation of digital radio signals. |
| | R&S FSQ-K91 | WLAN IEEE 802.11 a/b/g/j TX Application Firmware | 1U | Application firmware that covers standard-related tests as well as further evaluations for in-depth analysis in development for signals in line with the WLAN IEEE 802.11 a/b/g/j standard. |
| | R&S FSQ-K93 | TX measurements on OFDMA signals in line with IEEE 802.16-2004, IEEE 802.16e-2005 | 1U | Application firmware that allows TX measurements on OFDM and OFDMA signals in line with the WiMAX™ IEEE 802.16-2004 and IEEE 802.16e-2005 standards. |
| | R&S FSU-K30 | Application Firmware for Noise Figure and Gain Measurements | 1U | Provides the high-grade analyzers with features otherwise only provided by special noise measurement systems. Requires a noise source. |

**Table 6-3: Spectrum/Signal Analyzer option configuration and short description.**

| OSCILLOSCOPE |
|---|

| VENDOR | PRODUCT NUMBER | DESCRIPTION | UNITS | SHORT DESCRIPTION |
|---|---|---|---|---|
| Agilent Technologies | DSO80804B | Infiniium Oscilloscope - 8 GHz 20/40 GSa/s 4 Ch | 1U | Superior debugging and advanced application analysis in a powerful windows-based lab oscilloscope. |
| OPTIONS | DSO80000-001 | 1-2M Memory/CH Upgrade On Half Channels | 1U | Increases acquisition memory depth to 2M (half channels) |

**Table 6-4: Digital oscilloscope option configuration and short description.**

| RF&MW SYNTHETIC INSTRUMENTS | | | | |
|---|---|---|---|---|
| **VENDOR** | **PRODUCT NUMBER** | **DESCRIPTION** | **UNITS** | **SHORT DESCRIPTION** |
| Mercury Computer Systems | N/A | Echotek Series RF 3000 Multi-Channel Phase-Coherent Tuner | 1U | Ultra high-performance 20 MHz to 3000 MHz VHF/UHF downconverter with low phase noise and ultra fast tuning speed. |
| MODULES | 910-38038 | Echotek Series RF 3000T 140MHz RF w/VHF PRESELECTOR 65 MHz BANDWIDTH | 4U | 6U VME 4 channel downconverters in phase-coherent operation. |
| | 910-38067 | 65MHz BDW 140MHz IF Kit With Cutoff | 4U | 65MHz IF Cutoff SAW filter centered at 140MHz |
| | 910-38090 | Kit, 3000RF LEMO | 4U | LEMO cable+connectors enabling communication between tuner boards in the master/slave and multi-channel configurations. |
| | 910-38051 | Echotek Series RF 3000T 140MHz SYN | 1U | 6U VME Single broadband frequency synthesizer for phase-coherent operation. |
| | 910-38091 | Kit, EI SYN LEMO | 1U | Allows the system to be cabled up once and reconfigured on the fly via the control software that can be configured for a standard RS-232 (RS-232 to LEMO cable + connectors). |
| (Vector Electronics and Technology) | 901-38006 | ADV 3000 & 5000 Series -- 6U, 21 Slot Chassis, 600W (5V@70A, +12V@10A, -12V@3A) | 1U | 6U 21slot VME chassis |
| Holzworth | HS1001A | 8MHz to 1GHz Single Channel RF synthesizer | 1U | Small-factor USB powered Broadband CW source with phenomenal phase noise performance and spectral |

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| | | | | purity, offering precisely incremented tuning resolution. |

**Table 6-5: RF Downconverters and microwave synthesizer modular configuration and short description.**

| DSP/FPGA DEVELOPMENT PLATFORMS | | | | |
|---|---|---|---|---|
| **VENDOR** | **PRODUCT NUMBER** | **DESCRIPTION** | **UNITS** | **SHORT DESCRIPTION** |
| Lyrtech | LSP001-605 | MIMO 4X4 - Advanced - AC | 1U | Mixed-signal and baseband processing platform for MIMO systems |
| MODULES | LSP130-613 | VHS-ADC Virtex-4, LX160-AC-Gain | 1U | High-speed, multichannel acquisition advanced development platform. It is equipped with eight phase-synchronous ADCs that operate at a maximum rate of 105 MHz and a high-capacity Virtex-4 FPGA for high-speed processing |
| | LSP144-603 | VHS-DAC Virtex-4, LX160-AC-Gain | 1U | High-speed, multichannel digital-to-analog conversion advanced development platform. It is equipped with eight phase-synchronous DACs that operate at a maximum refresh rate of 480 MSPS through on-chip interpolation and a high-capacity FPGA for high-speed processing |
| | LSP140-163 | SignalMaster Quad Virtex-4, Advan | 1U | Advanced development platform is specifically designed to help develop and test DSP algorithms through its combination of FPGA and DSP devices. It allows to simultaneously design and test in a real-time environment through its integration to the model-based design software tools for Simulink. |
| | LSP142-611 | DRC V-4 SX55 No FPDP/GPIO | 2U | DRC module Add-ons. Allows feeding and retrieving digital data to and from it at high speeds. |

**Table 6-6: Data acquisition and signal processing platform modular configuration and short description.**

### 6.1.2 Software packages and licenses

| SIGNAL CREATION | | | | |
|---|---|---|---|---|
| **VENDOR** | **PRODUCT NUMBER** | **DESCRIPTION** | **UNITS** | **SHORT DESCRIPTION** |
| Agilent Technologies | N/A | Signal Studio & Embedded Software | N/A | Software to create standard validated & performance optimized reference signals, configure the signals in an easy-to-use application-specific graphical interface and validate your 3rd party interoperability. The software is used with the two Radiocommunications Laboratory properly licensed ESG E4438C vector signal generators. |
| LICENSES | N7615A | Signal Studio for 802.16 OFDMA | 2 | Software to create waveforms that comply with WirelessMAN-OFDMA PHY in the IEEE 802.16-2004 and 802.16e standards. The software's intuitive graphical user interface provides convenient access to the physical and basic MAC layer parameters, including bandwidth, cyclic prefix ratio (G), and frame length, providing the versatility required to configure waveforms for both component and receiver design verification and testing. |
| | N7615A-101 | License E4438C with internal baseband generator | 2 | Connect to E4438C signal generator, transportable, perpetual. |
| | N7615B-RTP | Advanced 802.16Rev2 OFDMA | 2 | Supports mixed Matrix A and Matrix B bursts in a single DL-PUSC or DL-AMC zone for both regular and HARQ bursts, incremental redundancy HARQ allocations in both downlink and uplink zones (including IR CC and IR CTC), cyclic delay diversity (CDD) for 2 Tx antennas, creating frequency domain duplex (FDD) and half-duplex FDD (H-FDD) frames, new permutation types and STC/MIMO in DL AMC zone (1x6 and 3x2 for non-STC mode, 2x6 for STC mode), configuring mixed normal and band AMC allocation modes |

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| | | | | within one sounding symbol, and support user-defined channel correlation matrix in the MIMO channel configuration |
| | N7613A | Signal Studio for 802.16-2004 WiMAX | 2 | Software to create spectrally correct Fixed WiMAX reference signals for component test and modify physical (PHY) layer signal parameters to verify performance under various signal conditions. For receiver test, enables setting up fully coded MAC layer signals and configuring bursts and MAC PDUs with or without a header and CRC. The software automatically creates FCH and broadcast messages (DL-MAP, UL-MAP, DCD, UCD). To verify receiver robustness, I/Q impairments and real-time AWGN can be added to the test signal. |
| | N7613A-101 | License ESG E4438C with internal baseband generator | 2 | Connect to E4438C signal generator, transportable, perpetual. |
| | N7617A | Signal Studio for 802.11 WLAN | 2 | Create standards-based BB and RF reference signals for testing 802.11a/b/g/j/p/n WLAN receivers and components with ESG E4438C signal generators. For receiver test, the application provides full channel coding for BER/BLER/FER. For component test, the application provides partially coded, statistically correct waveforms for stimulus/response testing. |
| | N7617A-203 | Basic 802.11a/b/g/j/p WLAN | 2 | OFDM (10MHz/20MHz Bandwidth), DSSS-OFDM, DSSS/PBCC/CCK and ERP-PBCC (PBCC 22 and PBCC 33) modulation types, multi-carrier support (up to 3 carriers), baseband I/Q Impairments, multipath (20 paths), data source type (all zeros, PN9, PN15, user-defined file) and multiframe control. |
| | N7617A-213 | Advanced 802.11a/b/g/j/p WLAN | 2 | Channel Encoder ON/OFF: Scrambler ON/OFF, convolutional Encoder |

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|---|---|---|---|---|
| | | | | ON/OFF, OFDM Scrambler and Reserved Service Bits (for 802.11a/j/p, 802.11g OFDM), PBCC Encoder ON/OFF, DSSS Scrambler (For 802.11b and 802.11g DSSS). |
| | N7617A-101 | Connect to E4438C signal generator | 2 | Connect to E4438C signal generator, transportable, perpetual. |
| | N7623A | Signal Studio for DVB | 2 | Software to create DVB-T, DVB-H, and DVB-C waveforms and specify channel coding and modulation parameters, OFDM frame structure, and TPS information to create DVB signals that meet the specific receiver and component test requirements |
| | N7623A-101 | License ESG, E4438C, with internal baseband generator | 2 | Connect to E4438C signal generator, transportable, perpetual. |
| Agilent Technologies | N7622A | Signal Studio Toolkit | N/A | Free custom I/Q waveform download utility for use with ESG signal generators. Different I/Q data files formats are supported (MATLAB "MAT File 5", ASCII, Agilent 16-bit and 14-bit, etc). |

**Table 6-7: Signal creation software, licensing configuration and short description.**

| SIGNAL ANALYSIS | | | | |
|---|---|---|---|---|
| **VENDOR** | **PRODUCT NUMBER** | **DESCRIPTION** | **UNITS** | **SHORT DESCRIPTION** |
| Agilent Technologies | 89600 | Vector Signal Analysis Software | N/A | The Agilent 89600 vector signal analysis software enables characterizing complex, time-varying signals with detailed and simultaneous spectrum, modulation and time waveform analysis, in RF/wireless communications applications. |
| LICENSES | 89601B | Floating license | 15 | Educational license including all packages |
| | 89601AN | Floating License | 1 | Perpetual floating license capability allows many users to share licenses. A license installed on the network is available to any PC that is connected to the network. |

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|---|---|---|---|---|
| | 89601AN-200 | Basic Vector Signal Analysis (no HW connectivity) | 1 | License to analyze time, frequency, and amplitude domain behavior and more with a complete set of vector and scalar analysis measurements including: time, gated time, spectrum, power spectral density, CCDF and CDF, auto-correlation and coherence. |
| | 89601AN-300 | Hardware connectivity | 1 | With this option, VSA can be linked to Agilent instruments, including CTTC spectrum analyzers, oscilloscopes, logic analyzers. VSA functionality is provided within the signal acquisition capabilities of the platform with which it is working. |
| | 89601AN-AYA | Digital Modulation Analysis | 1 | Demodulates a wide range of standard communication formats, such as GSM, EDGE, and EDGE Evolution. It also offers a wide range of demodulators for FSK, BPSK, QPSK, offset QPSK, QAM, APSK, and VSB, all with variable filter type and alpha, symbol clock rate, and bandwidth. Proprietary filtering can be applied by providing the filter's impulse or frequency response. |
| | 89601AN-B7R | WLAN modulation analysis | 1 | It offers IEEE 802.11a/b/g standards-based testing and modulation analysis of IEEE 802.11a OFDM, IEEE 802.11b DSSS/CCK/PBCC, IEEE 802.11g, IEEE 802.11p DSRC, IEEE 802.11j 10 MHz. |
| | 89601AN-B7S | IEEE 802.16-2004 OFDM modulation analysis | 1 | Provides coverage for all IEEE 802.16-2004 modulation formats, including BPSK, QPSK, 16QAM, and 64QAM, TDD, FDD, and H-FDD, uplink and downlink, bursted and continuous, all frame lengths, guard intervals, and sampling factors and demodulation down to the raw bit level. It also provides traditional error analysis measurements (Band power, carrier-to-noise, peak-to-average power CCDF, amplitude, group delay) and 802,16-2004 OFDM specific (Relative constellation error in % or dB, RCE vs. symbol number, RCE vs. subcarrier |

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| | | | | number, equalizer frequency and impulse response, error vector spectrum/time including RMS error vector, quadrature skew, gain imbalance, I-Q offset, frequency error, symbol clock error and common pilot error. |
| | 89601AN-B7Y | IEEE 802.16 OFDMA modulation analysis | 1 | Provides analysis of: PUSC, OPUSC, FUSC, OFUSC, AMC zones including dedicated pilot option for PUSC and AMC beamforming, uplink and downlink, all bandwidths from 1.25 MHz through 28 MHz, all FFT sizes from 128 to 2048, DL-PUSC signals using 2-antenna matrix A or B transmission schemes for STC/MIMO, UL-PUSC signals containing data bursts with collaborative spatial multiplexing (SM) enabled, CDMA ranging regions to aid with troubleshooting network entry, IQ impairment compensation allows RCE measurements to be made even in early design phases or prior to calibration, downlink signals employing Cyclic Delay Diversity. |
| | 89601AN-105 | Dynamic link to EEsof ADS/SystemVue | 1 | Enables tight, interactive integration with Agilent EEsof's advanced design system to analyze computational data from a simulation. ADS/SystemVue simulation results can be used to create signals and output them via the Agilent ESG signal generator to source a prototype hardware. This is useful when a) the signal type involves a new standard or modulation format; b) when it is required to understand what changes to the previous hardware design stage imply to the next; or c) when one hardware stage is physically realized before others are available. Once it physically exists, hardware can be measured with the 89600 VSA software connected to a supported measurement platform, and compared to the simulation if desired. |

**Table 6-8: Signal analysis software, licensing configuration and short description.**

# SYSTEM SIMULATION, DESIGN AND VERIFICATION

| VENDOR | PRODUCT NUMBER | DESCRIPTION | UNITS | SHORT DESCRIPTION |
|---|---|---|---|---|
| Agilent Technologies | | | | |
| LICENSES | E8900M | ADS Family Media (Design Environment) | 1 | Graphical user interface for schematic entry and simulation setup within the Advanced Design System (ADS). All schematic RF, system and DSP designs are captured within the Design Environment including the configuration of simulation and optimization, setting variables, viewing libraries, and running Design Guides. |
| | E8811L | MMIC Designer Pro (ads_datadisplay, ads_layout, ads_schematic, mom_opt, mom_vis, momentum, mom_obj, sim_harmonic, sim_linear, trans_gdsii) | 1 | This bundle provides Provides essential RF and microwave design capabilities in a highly productive enterprise schematic design environment. Fast linear simulation, comprehensive filter and passive circuit synthesis. Provides analysis of non-linear circuits excited with multi-tone sources, and extensive, preconfigured simulation setups useful in amplifier, RF, microwave, oscillator and custom circuit designs. 3-D planar electromagnetic (EM) simulator used for passive circuit analysis. Also includes modules for animating current flow in conductors and slots, circuit optimization and analytical modeling. |
| | E8854L | RF Systems Models (mdl_systemlib) | 1 | E8854A RF System Models provides gain blocks, mixers, modulators and demodulators and PLL components. In addition, verification model extractors and verification models for RF system-level analysis and verification are included. |
| | E8885L | Convolution Simulator (sim_convolution) | 1 | This is an advanced time-domain simulator that extends the capability of E8884A High Frequency SPICE by accurately simulating frequency-dependent |

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| | | | | components (distributed elements, S-parameter data files, transmission lines, etc.) in a time-domain simulator. |
| | E8883L | Circuit Envelope Simulator (sim_envelope) | 1 | This is an efficient simulation technique for the complex digitally modulated RF signals found in today's wireless circuits.Typical analyses and measurements include: Pseudo-random digitally modulated RF solutions, ACPR, EVM, PAE simulation and optimization, transient RF solutions, PLL frequency vs. time analysis (lock time), AGC, PLL transient response (ringing, settling, overshoot, etc.) simulation and optimization and high order (5th, 7th, 9th) mixer inter-modulation product analysis. |
| | E8823L | Agilent Ptolemy Simulator (sim_systime) | 1 | System-level simulation and design solution based on a hybrid of synchronous and timed synchronous dataflow technologies:-Provides hybrid dataflow and time domain design and simulation capability for mixed DSP, analog and RF systems,-Extensive DSP, RF, communications, baseband analog model libraries and user-defined C++ models to architect reference system quickly to provide accurate specs and verification environment for DSP, RF and baseband block designers, -Co-simulation with RF (Circuit Envelope) and analog (Transient Convolution) circuit simulators to enable transistor level blocks, such as amplifiers, mixers and oscillators, to be designed, optimized and verified against system level specs, -Co-simulation with Circuit Envelope enables accurate non-linear X-parameter behavioral models from measurement or simulation to be used in system simulation, -Co-simulation with HDL digital simulators (Cadence NC-SIM, Verilog XL and Mentor Modelsim) enables HDL development and verification against system |

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| | | | | specs for error-free ASIC/FPGA implementation, -Co-simulation with Matlab enables Matlab scripts IP reuse for sophisticated DSP algorithm development, |
| | | | | -Fixed point implementation analysis and optimization enables fixed point math, bit-width and quantization effects to be accounted for and optimized to the original ideal floating point design with 13 powerful optimizers,-Connected Solutions with Agilent instruments enables progressive system integration between virtual and available real hardware by synthesizing and using real signals for one pass final system implementation success,-Provides the simulation foundation for wireless standards verification with Agilent Wireless Libraries (to be acquired) for the latest 3G, 4G cellular and data networking standards such as LTE, WiMax™ and VWAN. |
| | E8884L | High Frequency Spice (sim_transient) | 1 | Non-linear, time-domain simulator for analyzing very large base-band circuits, startup transients, oscillators, and high-speed digital and switching circuits. |
| | E8905L | DXF Translator (trans_dxf_hier) | 1 | Provides bi-directional translation to/from layouts in the DXF file format. |
| | E8880L | Spice netlist license (trans_spice_netlist) | 1 | Spice netlist translator |

**Table 6-9: System simulation/design/verification software, licensing configuration and short description.**

## 6.2 Appendix: Specifications of the ADP Signal Conversion and Baseband Processing Platform

| VHS-ADC | VHS-DAC | SMQUAD-4 | DRC (x2) |
|---|---|---|---|
| **ADCs:**<br>▪ AD6645 (8x) sampling rate 105 MSPS, 14-bit resolution<br>**Analogue inputs:**<br>▪ 50-Ohm MMCX connectors<br>▪ AC coupled, with gain<br>○ 0.2-200 MHz input BW<br>○ -18 to 4 dBm input scale<br>**Sampling clocks:**<br>▪ Onboard 104-MHz clock<br>▪ 50-Ohm ext. clock source<br>**Control & pre-processing:**<br>▪ Virtex-4 XC4VLX160 FPGA<br>▪ 128-MB SDRAM<br>**Off-board I/O:**<br>▪ RapidCHANNEL TX & RX, 1 GBps, full-duplex<br>▪ 400 MBps external FPDP<br>▪ DIF LVDS serdes, 105 MBps<br>▪ 32-bit, 33-MHz ext. PCI port<br>▪ 32-bit GPIO-32 header<br>▪ I2C interface | **DACs:**<br>▪ DAC5687 (4x) sampling rate 480 MSPS (14-bit resolution)<br>**Analogue inputs:**<br>▪ 50-Ohm MMCX connectors<br>▪ AC coupled, with gain<br>○ 0.3-240 MHz input BW<br>○ -21 to 2.9 dBm output BW<br>**Sampling clocks:**<br>▪ Onboard 104-MHz clock<br>▪ 50-Ohm ext. clock source<br>**Control & pre-processing:**<br>▪ Virtex-4 XC4VLX160 FPGA<br>▪ 128-MB SDRAM<br>**Off-board I/O:**<br>▪ RapidCHANNEL TX & RX, 1 GBps, full-duplex<br>▪ 400 MBps external FPDP<br>▪ DIF LVDS serdes, 105 MBps<br>▪ 32-bit, 33-MHz ext. PCI port<br>▪ 32-bit GPIO-32 header<br>▪ I2C interface | **FPGA devices:**<br>▪ 2 Xilinx Virtex-4 XC4VLX160<br>**DSP microprocessors:**<br>▪ 4 TMS320C6416 DSPs<br>**SDRAM memories:**<br>▪ 128MB per DSP/FPGA<br>**Off-board I/O:**<br>▪ RapidCHANNEL TX & RX, 1 GBps, full-duplex<br>▪ 400 MBps external FPDP<br>**On-board inter-FPGA bus:**<br>▪ LYRIO 1-GBps (1 RX , 1 TX)<br>**Backplane connections:**<br>▪ I/O pin direct to FPGA 1 (14x)<br>▪ I/O pin to LYRIO+ site 1 (31x)<br>▪ I/O pin to LYRIO+ site 2 (15x)<br>▪ Gigabit Ethernet to LYRIO+<br>**cPCI interface**<br>▪ cPCI bus: 64 bits, 66 MHz<br>▪ cPCI local bus:32bits,66 MHz | **FPGA devices (in both DRCs):**<br>▪ 2 Xilinx Virtex-4 XC4VSX35<br>▪ Onboard flash PROM<br>**Off-board I/O:**<br>▪ RapidCHANNEL TX & RX, 1 GBps, full-duplex<br>▪ 400 MBps external FPDP<br>▪ 32-bit GPIO-32 header<br>**On-board inter-FPGA bus:**<br>▪ LYRIO 1-GBps (1 RX , 1 TX) |

**Table 6-10: The ADP platform hardware specifications.**

## 6.3 Appendix: Configuration, Test and Validatation of an Implemented 2x2 Mobile Real-time WiMAX DL Transmitter and DL Receiver Using the GEDOMIS® Testbed

The current setup is prepared for the transmission of 2x2 Mobile WiMAX custom signals (i.e. .mat files loaded into the signal generators with Signal Studio Toolkit, SSToolkit from now on). This signal is not fully compatible with the IEEE802.16e-2005 standard since it is not including features like channel coding, but is fully valid for technological validation and application of research concepts. The main downlink signal specification is detailed below:

- Air interface → OFDMA
- Duplex mode → TDD
- BW = 20 MHz (fixed)
- Sampling frequency → Fs = 22.4 MHz (28/25*20MHz) (fixed)
- FFT size = 2048 points (fixed)
- Modulation type = QPSK (fixed)
- Cyclic prefix = ¼ useful OFDM symbol length (fixed)
- MIMO schemes → STBC
- Subchannelization → PUSC zone supported (with optional AMC for the SISO configuration)
- Data are not be channel encoded (i.e. randomization, no encoding, no interleaving)
- Number of bursts: only 1 burst in each zone (no multi-user capabilities)
- DL-MAP and FCH will not be decoded at the receiver

### *6.3.1 Signal Creation*

- The first step is to open two instances of SSToolkit SW. Each instance will be configured to download the two different generated waveform bitstreams (one per antenna) into each signal generator (e.g. mimo1v1 and mimo2v1 will be downloaded into GEDOMIS® ESG1 and GEDOMIS® ESG2 respectively). In order to proceed faster, load the following SSToolkit setup files: “MIMO_TX1_docon.tk” and “MIMO_TX2_docon.tk” that can be found in the folder labeled as “SSToolkit” at GEDOMIS® PC1 Desktop Folder.

- **SSToolkit Configuration parameters:**

- Verify that each SSToolkit instance is pointing at different vector signal generators. To select the signal generator the user has to click on the “System Menu” and select “Change Hardware Connections”. The wizard is quite straightforward if the Agilent IO Expert has been successfully installed in the computer and all the instruments are properly connected and configured for Ethernet use (for the current case).

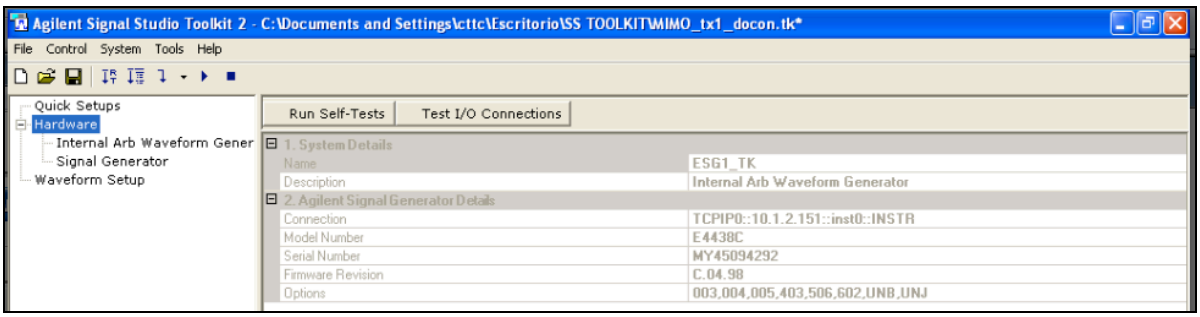


**Figure 6-1: SSToolkit Hardware communication configuration (for GEDOMIS® ESG1).**

In the Menu shown in Figure 6-2 for the Internal Arbitrary Waveform Generator, the “Sample Clock” is set to four times the sampling frequency of the signal (i.e. 22.4MHz). This is not mandatory to use such an oversampling. The ESG utilizes an interpolator filter in the

conversion of the digital I and Q baseband waveforms into analog waveforms with a clock that is four times that of the baseband clock (and thus smoothing out the waveform appearance). This filter sometimes has overshoots that provoke a DAC overrange error. If that error occurs during playback of the waveform, a reduction of "Runtime Scaling" may be applied. The default runtime scaling of 70% guarantees that a data over range cannot occur.

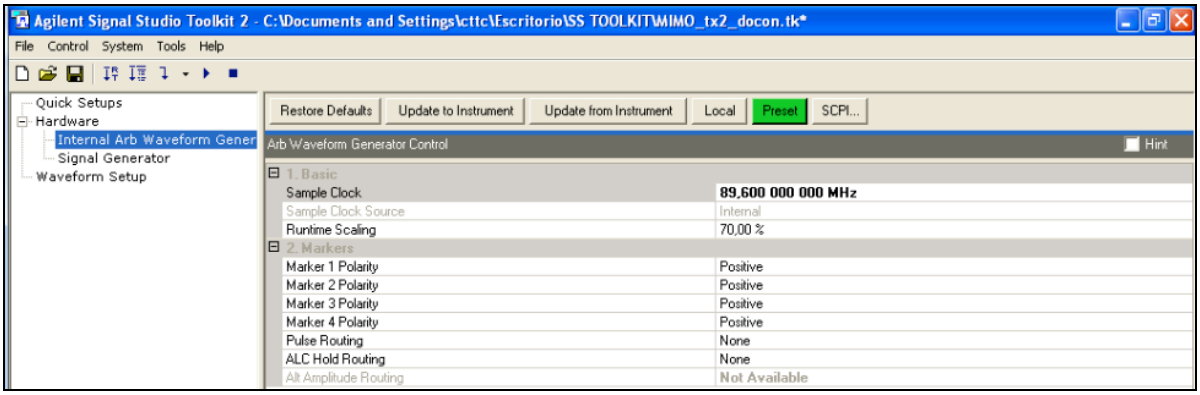


**Figure 6-2: SSToolkit Hardware Internal Arbitrary Waveform Generator configuration (for the two GEDOMIS® ESGs).**

The markers in the waveform file can be used to synchronize other instruments with the played waveform, as a trigger signal to start a measurement at a given point on a waveform, or to drive the pulse modulator to achieve a greater on/off ratio than is provided by the I/Q. The Arb waveform files can have up to four makers depending on the waveform format. The program allows independently setting the polarity of each marker and the routing in order to enable functions like "RF Blanking" (to blank the RF output) or "ALC Hold" (the RF output power of the signal generator is constantly monitored and controlled by the automatic leveling control (ALC) circuit).

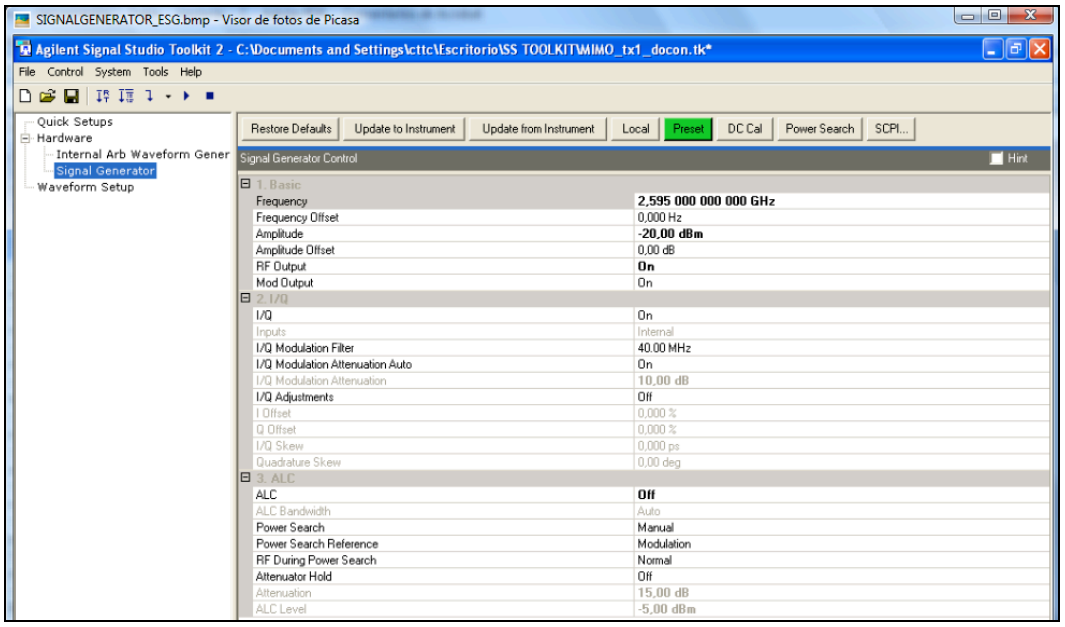


**Figure 6-3: SSToolkit configuration (for the two GEDOMIS® ESGs).**

As it can be seen in Figure 6-3, the next step is to configure the signal generator operating frequency, amplitude, and tune the I/Q interface parameters (e.g., if we would like to introduce I/Q gain and phase imbalances) or the ALC activation if required (Note: With ALC

Hold enabled, the output power leveling does not respond to changes to the signal amplitude and there are some modulation conditions the ALC circuit cannot handle properly that lead to output level errors).
Finally, within the "Waveform Setup" Menu, each instance of SSToolkit is loaded with the corresponding Matlab file (one per TX channel or antenna) including the I and Q double data format components as it can be seen in Figure 6-4. Markers to enable/disable advanced functionalities of the signal generators can be included in the MATLAB file as an additional vector with the same length as the I and Q vectors (with '0' or '1' values to activate/deactivate the markers at each sample position when the introduced waveform sample rate equals the Arbitrary Waveform Generator sample clock). This Menu also includes a spectrum mirroring option (to use in those upconverters where frequency spectrum inversion is produced), and enables the entry of user-defined sample clock rates (e.g. 22.4MHz for a 20MHz bandwidth mobile WiMAX signal).

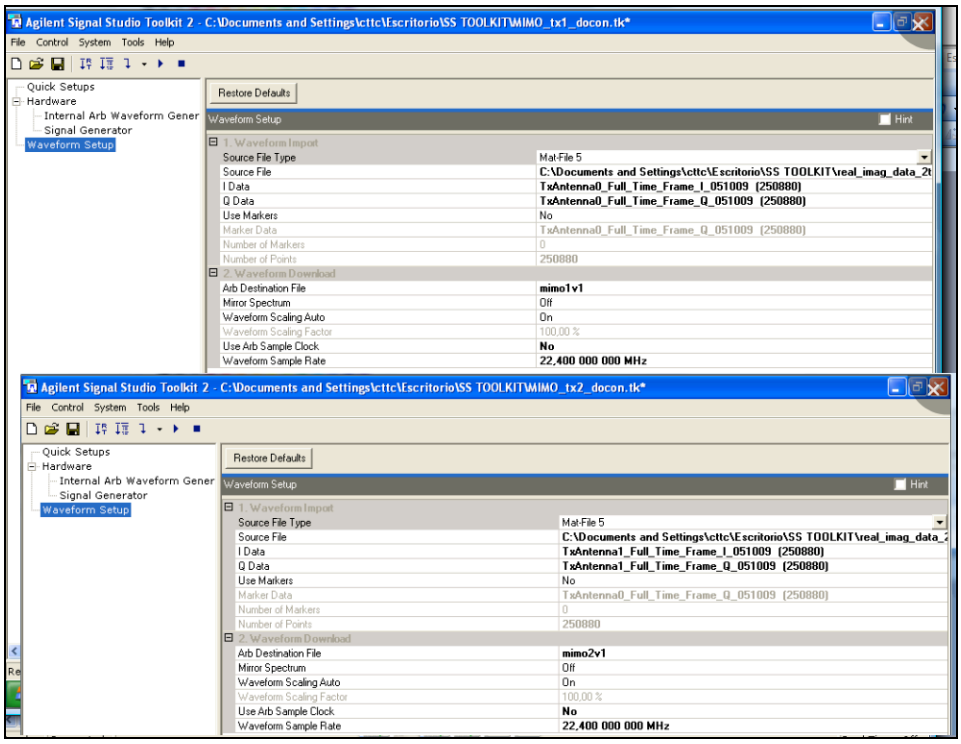


**Figure 6-4: SSToolkit Waveform Setup for the GEDOMIS® ESG1 (upper side) and the GEDOMIS® ESG2 (lower side).**

Before downloading the signal into the ESG vector signal generator (via LAN, after selection of "Control" Menu and "Download & play"), ensure that the signal generators are not connected to the RF Downconverters or the channel emulator: While generating the signal the carrier frequency at the output may have a very high value that could saturate/damage the following stages. After this step, click the "Control Menu" and select "Download and Play" to load each signal into the selected generators.

- **Specific setup of the signal generators for MIMO operation:**

- One signal generator is used as MASTER while the other signal generator is used as SLAVE. In order to synchronize them not only clock synchronization between the baseband signal generators is required, but also the use of a trigger signal activated when the frame of the master signal starts being transmitted. The Back Panel HW

connections (BNC cables and splitters between the signal generator Back Panel connectors) are done as illustrated in Figure 6-5:

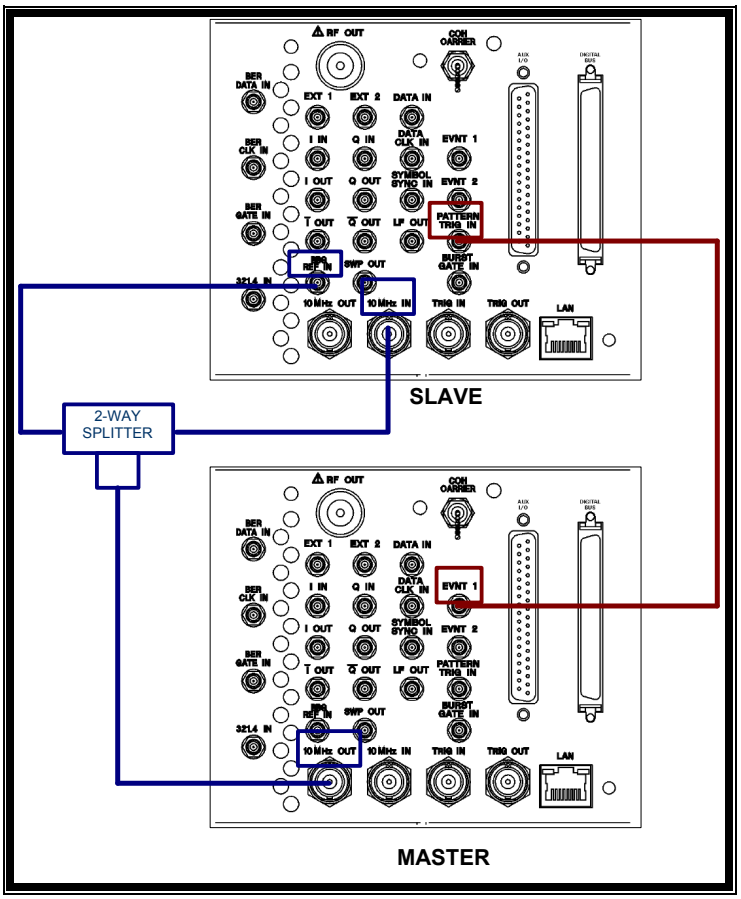


**Figure 6-5: Back panel interconnections between the two signal generators enabling MIMO configuration.**

- From now on, all the settings will be done by using the instrument front panel keys. The first instruction is to set the ARB (ARBitrary waveform generator) OFF:
  - *[KEY SEQUENCE: MODE / DUAL ARB / ARB OFF]*

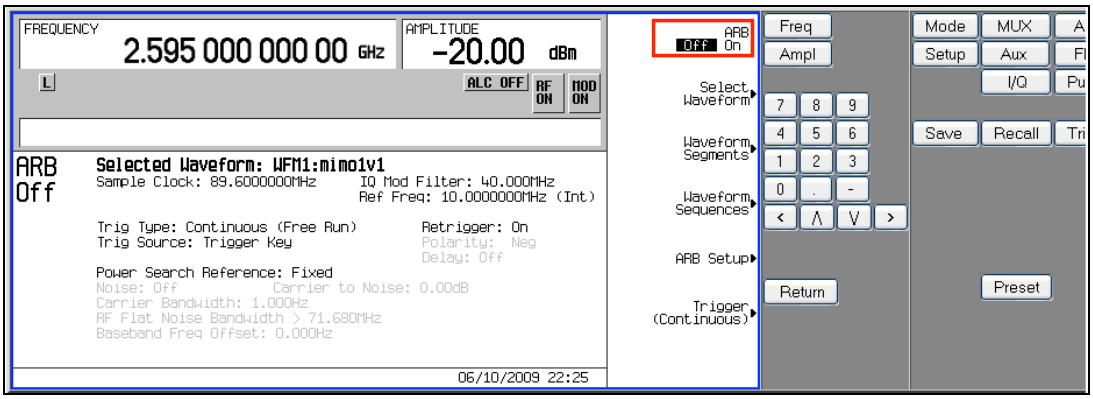


**Figure 6-6: Front panel Arbitrary Waveform Generator deactivation of MASTER and SLAVE signal generators.**

- Settings for the MASTER signal generator:

1) A Marker must be set in order to send an activation signal to the SLAVE signal generator (through the Back Panel EVENT1 and PATT TRIG IN connection):
   a. *[KEY SEQUENCE: MODE / DUAL ARB / ARB SETUP / MARKER UTILITIES/SET MARKERS].*
   b. *[Select Marker 1 & Push Set Marker on the First Point]*

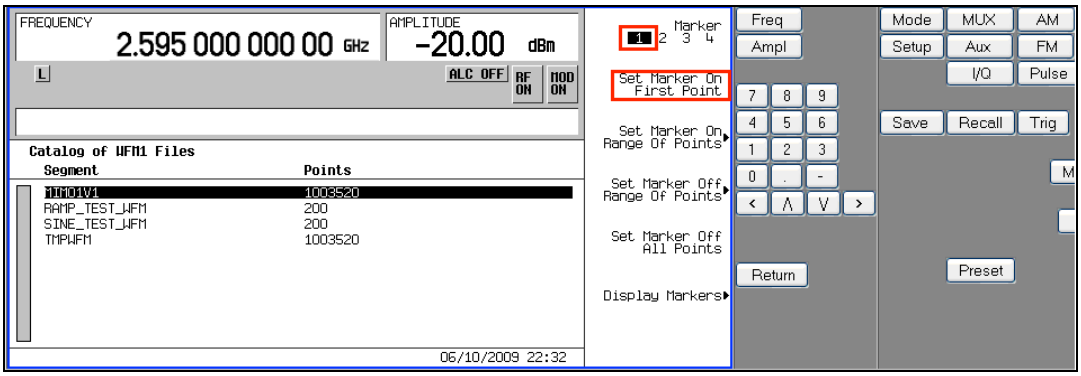


**Figure 6-7: Front panel settings to synchronize the two transmitted channels: MASTER signal generator (1/4).**

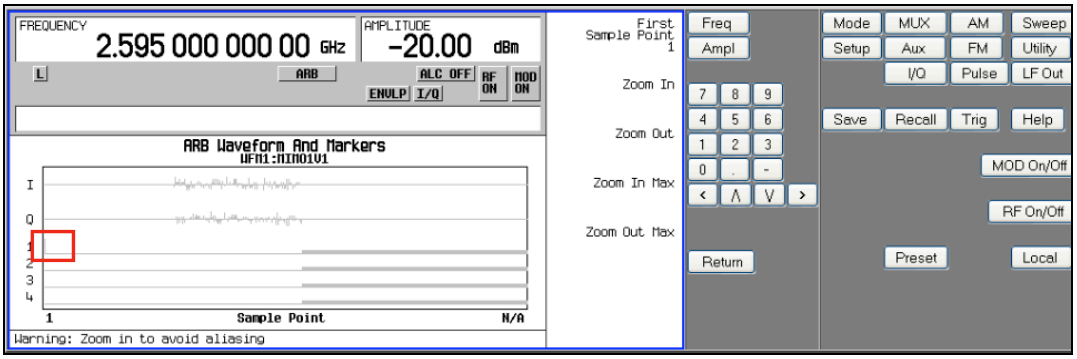


**Figure 6-8: Front panel settings to synchronize the two transmitted channels: MASTER signal generator (2/4).**

2) The MASTER signal generator trigger must be set continuous.
   a. *[KEY SEQUENCE: MODE / DUAL ARB / TRIGGER (CONTINUOUS)]*

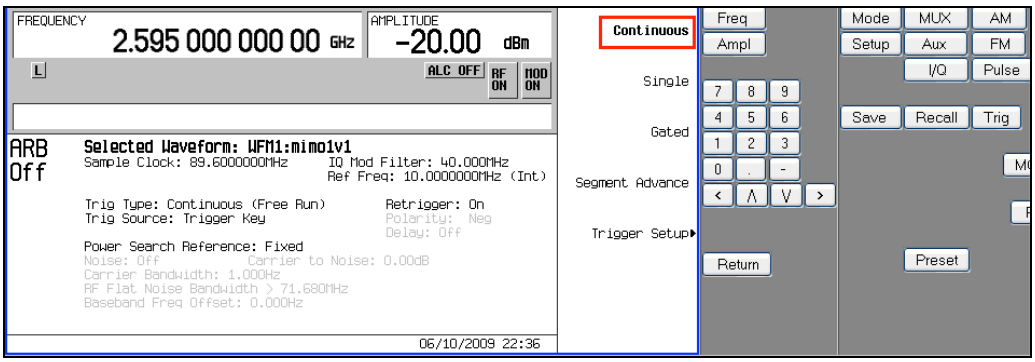


**Figure 6-9: Front panel settings to synchronize the two transmitted channels: MASTER signal generator (3/4).**

3) The trigger setup menu must be set to Free Run:

a. *[KEY SEQUENCE: MODE / DUAL ARB / TRIGGER (CONTINUOUS)/ TRIGGER SETUP / CONTINUOUS MODE / FREE RUN]*


**Figure 6-10: Front panel settings to synchronize the two transmitted channels: MASTER signal generator (4/4).**

- Settings for the SLAVE signal generator:

1) If the SLAVE signal generator trigger is set continuous (proceeding as specified for the MASTER signal generator) if the MASTER ARB generator were turned off (the signal at the output of the SLAVE generator would continue the cycle) and then were turned on again, the synchronization would be lost. In order to avoid that, the trigger must be set “single” (the signal at the output of the SLAVE generator will be blanked when the MASTER generator is “off” and will be synchronized when the generator is turned “on”).

2) The trigger source menu must be set as follows:
   a. *[KEY SEQUENCE: MODE / DUAL ARB / TRIGGER (CONTINUOUS)/ TRIGGER SETUP…]*

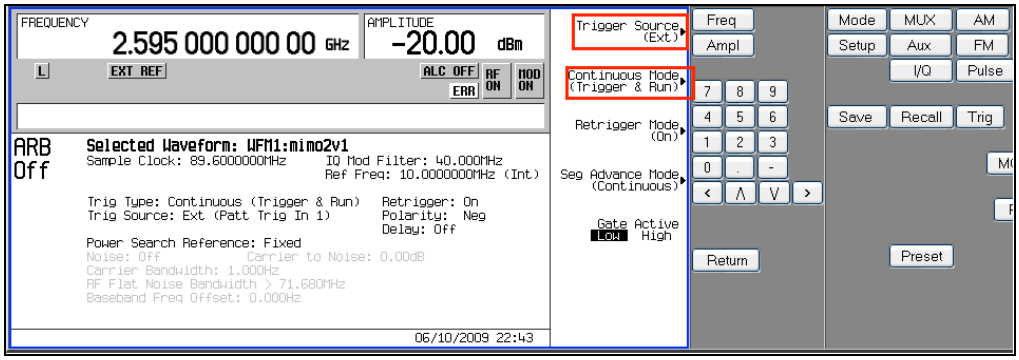


**Figure 6-11: Front panel settings to synchronize the two transmitted channels: SLAVE signal generator (1/2).**

b. Trigger source: Set to External and select the Back Panel PATT TRIG IN: *[…TRIGGER SOURCE / EXT] + […TRIGGER SOURCE / EXT SOURCE/PATT TRIG IN 1]*

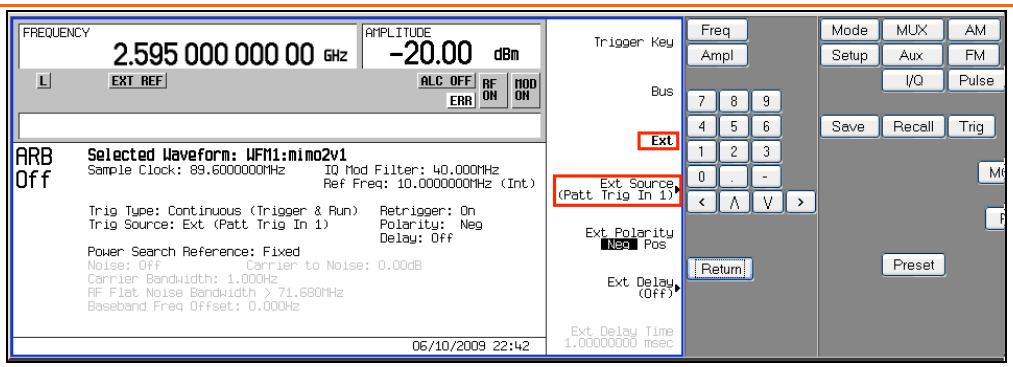


**Figure 6-12: Front panel settings to synchronize the two transmitted channels: SLAVE signal generator (2/2).**

*c.* Continuous Mode: Set to Trigger & Run: *[… CONTINUOUS MODE / TRIGGER & RUN]*

- MIMO transmitter verification:

1) Connect the outputs of the signal generators to the input ports of an Oscilloscope. As the ARB is OFF only the carrier signals are displayed (by reducing the time scale appropriately after activating the two measurement channels, e.g. 5ns).
2) Set the SLAVE signal generator ARB function ON. The signal should not be displayed yet (the signal generator is waiting for the trigger activation).
3) Set the MASTER signal generator ARB function ON. Now both the MASTER and SLAVE signal should be displayed and almost synchronized.

- Note about the delay of the SLAVE signal generation in the first setup round:

The trigger and sampling clocks should be synchronized. Without the acquisition of Option HEC, the trigger resolution is 10 ns (and thus this is the minimum synchronization time error), which is also the trigger clock rate. If the two ESGs are not fed with the same clock, the two trigger clocks will be independent and drift within one clock cycle or 10 ns. Additionally, the use of a marker in the MASTER signal generator to trigger the activation of the SLAVE signal generator introduces some delay.
In the SLAVE signal generator a function can be used to add delay to the external trigger activation:

*[KEY SEQUENCE: MODE / DUAL ARB / TRIGGER (CONTINUOUS)/ TRIGGER SETUP/TRIGGER SETUP / EXT DELAY [select time or samples and the quantity]*

After setting the Ext Delay to its minimum (10ns or 0 samples) it can be seen in the oscilloscope that the time offset between the two signals is around 1.1µs. Thus, additional delay is required to the SLAVE signal to calibrate the system. Provided that the delay will be added to the SLAVE signal generator, almost a full frame time length must be set in the trigger setup external delay (the same data frame is repeated in a cyclic fashion). The first tests visualizing the two signals at the oscilloscope have shown that an extra delay of 11.1988900 ms (a full frame signal and silence period plus an extra value for calibration) is required to be applied in the SLAVE signal generator. Nevertheless, it would be a good and safer practice to calibrate the system every time that the testing scenario could change.

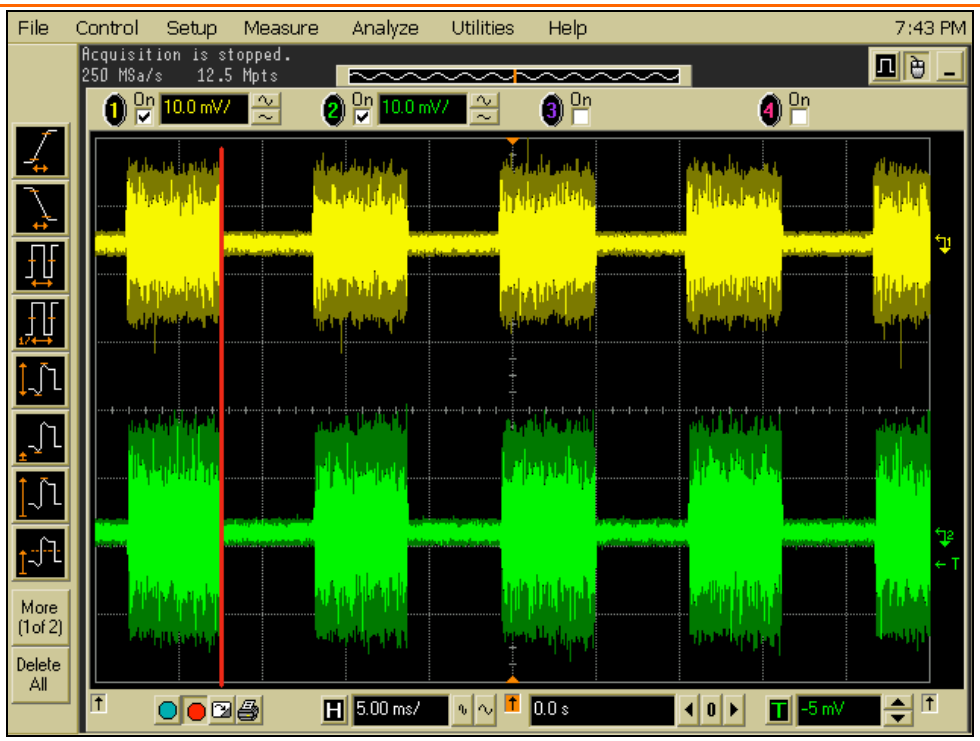


**Figure 6-13: Oscilloscope capture of the MIMO transmitted channels after synchronization of the ESG generators.**

- **Spectrum verification**:

- Select “Control/Download and Play” to load the signal into the generator. Connect the cable at the output of the signal generator at the input of the Spectrum Analyzer (tuned at 2595MHz) and verify that you have the right signal (OFDM signal centered at the selected frequency with good SNR) as it is displayed in Figure 6-14:

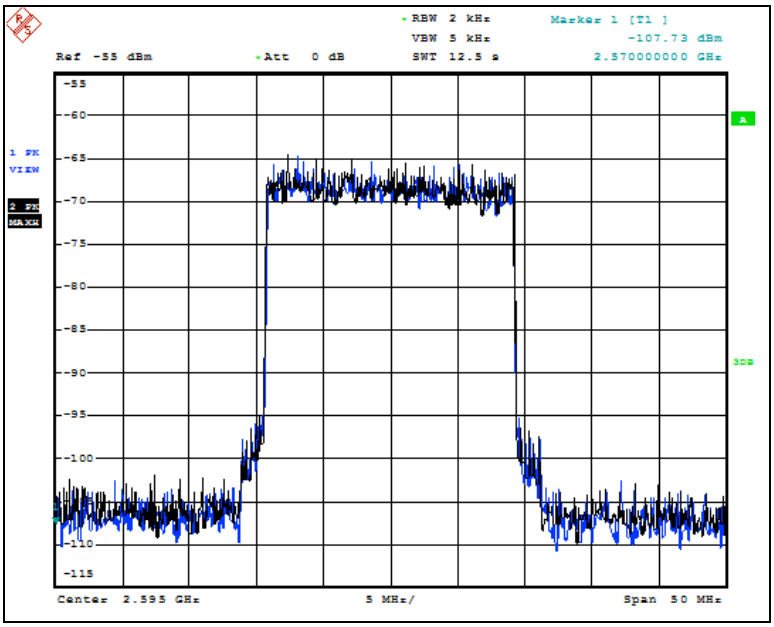


**Figure 6-14: Signal spectrum analyzer capture of the two transmitted signals.**

- In case that the user wanted to add noise or do testing with different TX SNR ratios, the following ESG Vector Signal Generator Front Panel buttons have to be used: [*"Local (beside the green RESET button)+Mode+Dual Arb+Arb Setup+Real-Time Noise Setup"]* and configure the values [*on/off, C/N ratio, noise BW, noise BW factor…* e.g. *on/35/20MHz/1*].

Note: Don't connect the cable at the output of the signal generator to the input of the RF downconverters or the channel emulator if they have not been powered and properly configured (to avoid damaging the equipments). Always bear in mind the instruments dynamic ranges and the maximum input power level ratings.

### *6.3.2 Channel Emulation*

- The channel emulator is provided with a proprietary application SW that eases significantly the setup of simulations. The principal components located in the main user interface that will be used are the Channel Model Editor ("Channel Modeling" Menu), the Simulation Editor ("Channel Modeling" Menu) and the Simulation Control ("Simulation Control" Menu). In this section the main features of the channel emulator software and hardware will be described. A set of screenshots will show the typical settings for a 2x2 MIMO setup using a standard channel model. A lecture of the maximum power ratings and the rest of electrical specifications is mandatory in order to avoid damaging the equipment and have the optimum signal quality.

- The Channel Model Editor defines the statistical radio channel specific parameters that characterize the CIR. It creates a simplified statistical channel model for a situation where the mobile station is moving away from the base station at a constant speed, by creating and editing TAP files and setting parameters like the operation center frequency, the mobile speed and the channel emulator resource usage. The application can be instanced from both the "Channel Modeling" Menu and the Simulation Editor.

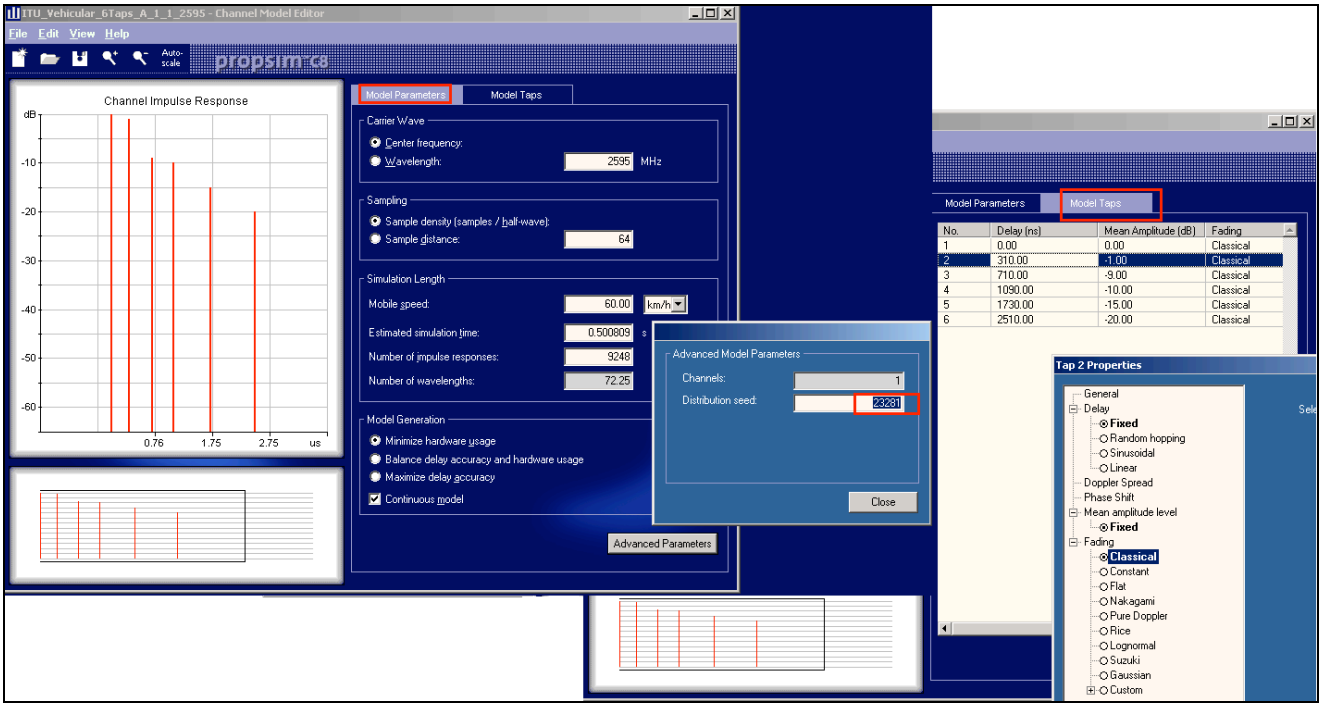


**Figure 6-15: Channel Model Editor two main windows.**

- For a 2x2 Mobile WiMAX setup, four channel model files will be created (ch11, ch12, ch21, ch22) using different Distribution Seeds (in “Advanced Model Parameters”) to have uncorrelated multipath fading channels. For the current case, the TAP tables introduced will be compliant with the International Telecommunication Union (ITU) Vehicular Profile A model with a mobile speed of 60km/h. Note that for each of the ITU channel models the Doppler spectrum is Classical and amplitude distributions on each of the paths are Rayleigh.

- The Simulation Editor is used to easily create and edit the simulation block layout (define the connections between inputs, channels models used and outputs). When the layout is ready, the Simulation Editor generates (“Generate Model Button”) hardware control files (.sim file extension) that can be loaded into the emulator. The tool offers predefined layouts/templates for correlating channels or MIMO channels among other options. It is important to remember that any change of the channel models, the old .sim files have to be deleted and replaced by new ones (otherwise the new ones will not be created). All the parameters that have to be set in this application will be described by using a set of Simulation Control screenshots in the following pages.

- The Simulator Control is used to load and emulate simulations (pregenerated .smu files linked to .sim simulation data files) that have been created by using the “Channel Modeling” herein mentioned tools. It can be used to control all the HW emulation operations, view and reset the settings of simulations and the hardware connectors, change the simulation parameters and control the playback of the channel emulation (e.g. play/stop/step/bypass/goto). As said before, the use of certain channel models for MIMO channels may exceed the available resources on the local emulator. In these cases, the user is prompted for another emulator to be used in a slave configuration connected to the main emulator. The user may notice this situation when a window with the appearance of Figure 6-16 is displayed on the screen (left picture when there is an available slave channel emulator, right picture, when it does not detect any slave channel emulator). A solution for this problem could be to regenerate the simulation model once again after changing the channel model parameters by selecting the “Minimize hardware usage” or “Balance delay accuracy and hardware usage” options for the Model Generation. The drawback will be that accuracy is lost.

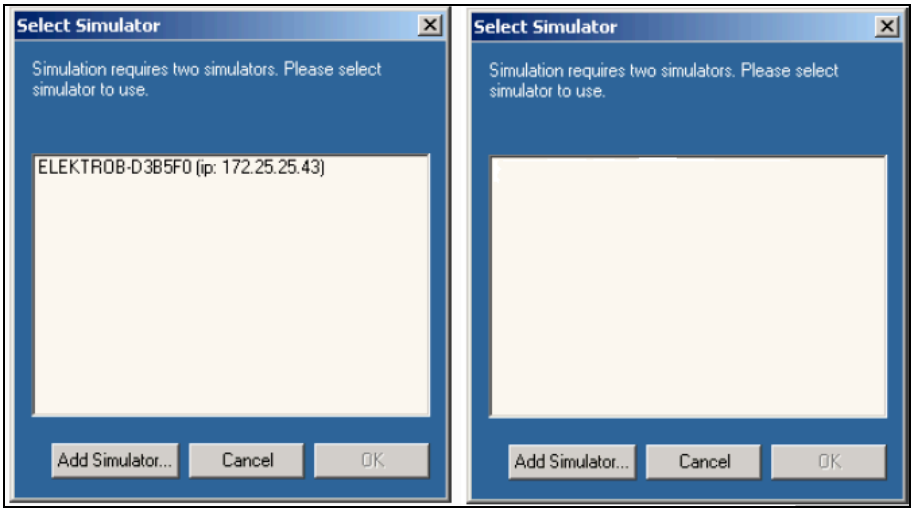


**Figure 6-22: Windows appearing when the channel emulator available resources are exceeded.**

- Before cabling the setup and run the channel emulator simulation after the simulation pregenerated .smu files has been loaded into the Simulator Control, it is recommended that the user will verify the connections created to avoid surprises with the input and output signal routing (see Figure 6-17):
-

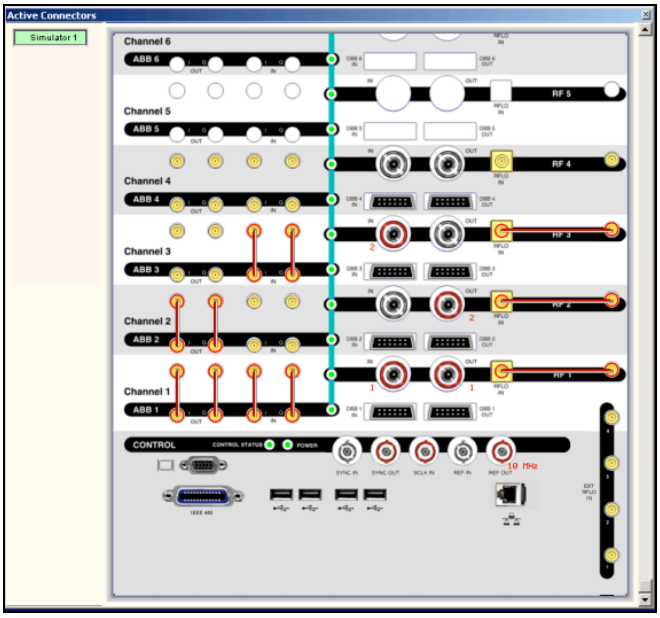


**Figure 6-17: Active connectors layout for the MIMO 2x2 Mobile WiMAX setup (connections marked in red).**

Marked in red, it shows graphically which connectors and jumpers have to be used for the current simulation.

- **Notes on parameters, settings, and considerations:**
- RF1 and RF2 “Input Settings / Settings” setup:
  - Crest factor: The Crest Factor (CF) is equal to the peak amplitude of a waveform divided by the root mean square (RMS) value. The channel emulator makes a downconversion of the RF signal to IF (300MHz) where an analog I/Q demodulator provides the I and Q components at the input of the channel emulator ADC converters. In order to maximize the SNR and avoid quantization errors the signal level is normally adjusted by the receiver in order to reach the ADC full-scale levels. The CF or Peak-to-average Power Ratio (PAPR) could saturate the ADC or provoke signal cut-offs and thus deteriorate the signal quality. For this reason, the CF is taken as a safe margin in dB with respect the desired power level. For instance, if we had a sinusoid we would employ a CF of 3 dB. For a mobile WiMAX signal the CF would be around 10-12dB during 0.1% of the time when having AWGN. In this case, even considering that we have a mobile WiMAX signal at the input of the value set for the CF is 3 dB to maximize the SNR (considering that the 1% that the signal will have a peak of 12 dB is not critical to damage the equipment or reduce the signal quality).
  - Average input level: This value is the estimated average power level at the input of the channel emulator (signal generator output power level after subtracting the cable losses). The value introduced is important since the input attenuation/gain of the downconversion chain will be fixed to match the optimum ADC signal power levels. If the value introduced is lower than the real input power level, the gain in the downconversion chain will be higher and could provoke cut-off warnings. The minimum average input power level is (-24dBm-CF) and the maximum (6dBm-CF).

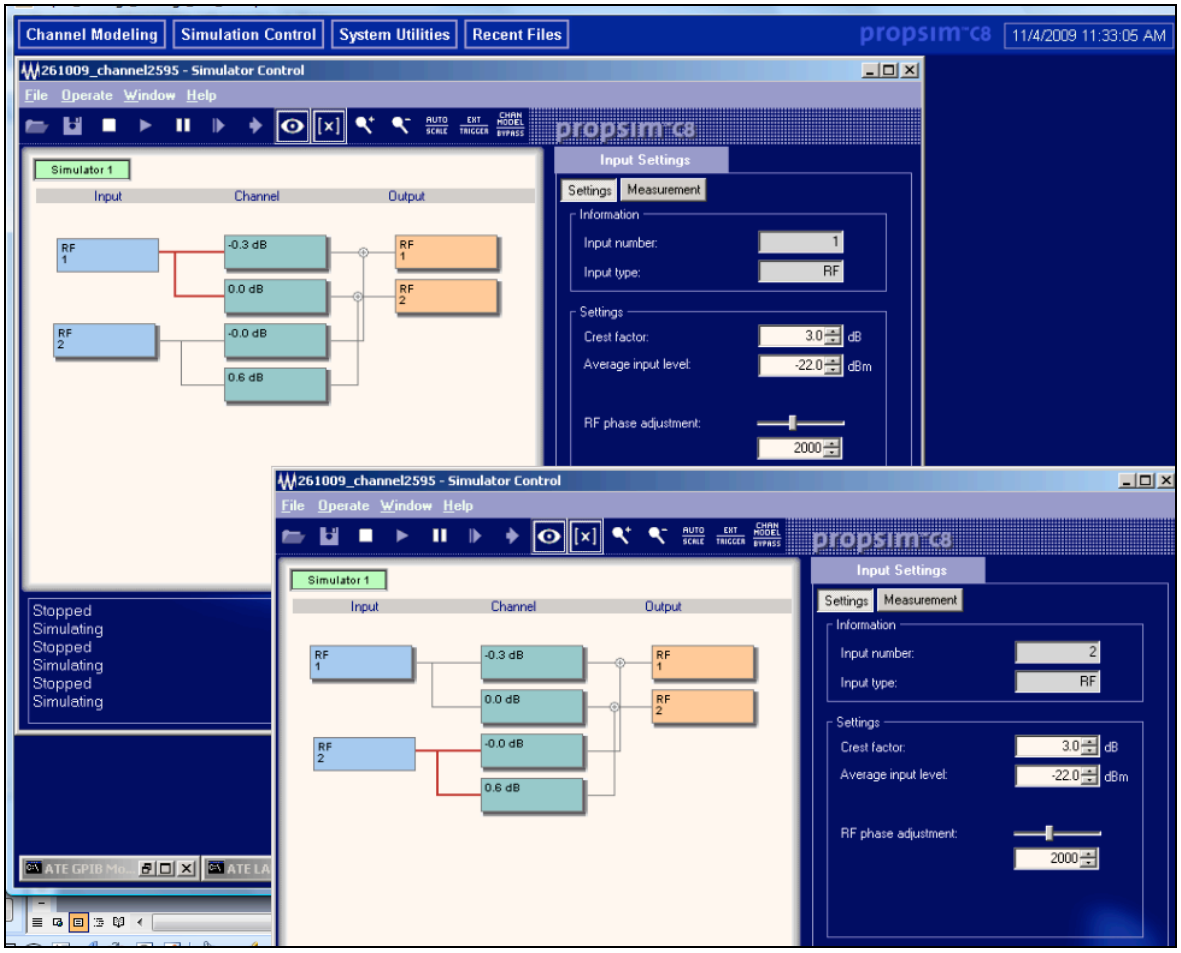


**Figure 6-18: Channel Emulator 2x2 MIMO setup: RF1 and RF2 Input Settings / Settings window.**

- RF1 and RF2 “Input Settings / Measurement” setup:
  - These settings can enable burst power measurement, where time-divided signal’s effective power (duty period) is measured in order to determine the input power level of EB Propsim C8.

  - The measurement result of each RF input can be used to verify if the connections are the correct ones (e.g. a significant difference between the two measurement results in our MIMO setup with similar TX power levels would imply, for instance, that the cables have not been properly routed to the channel emulator input connectors).

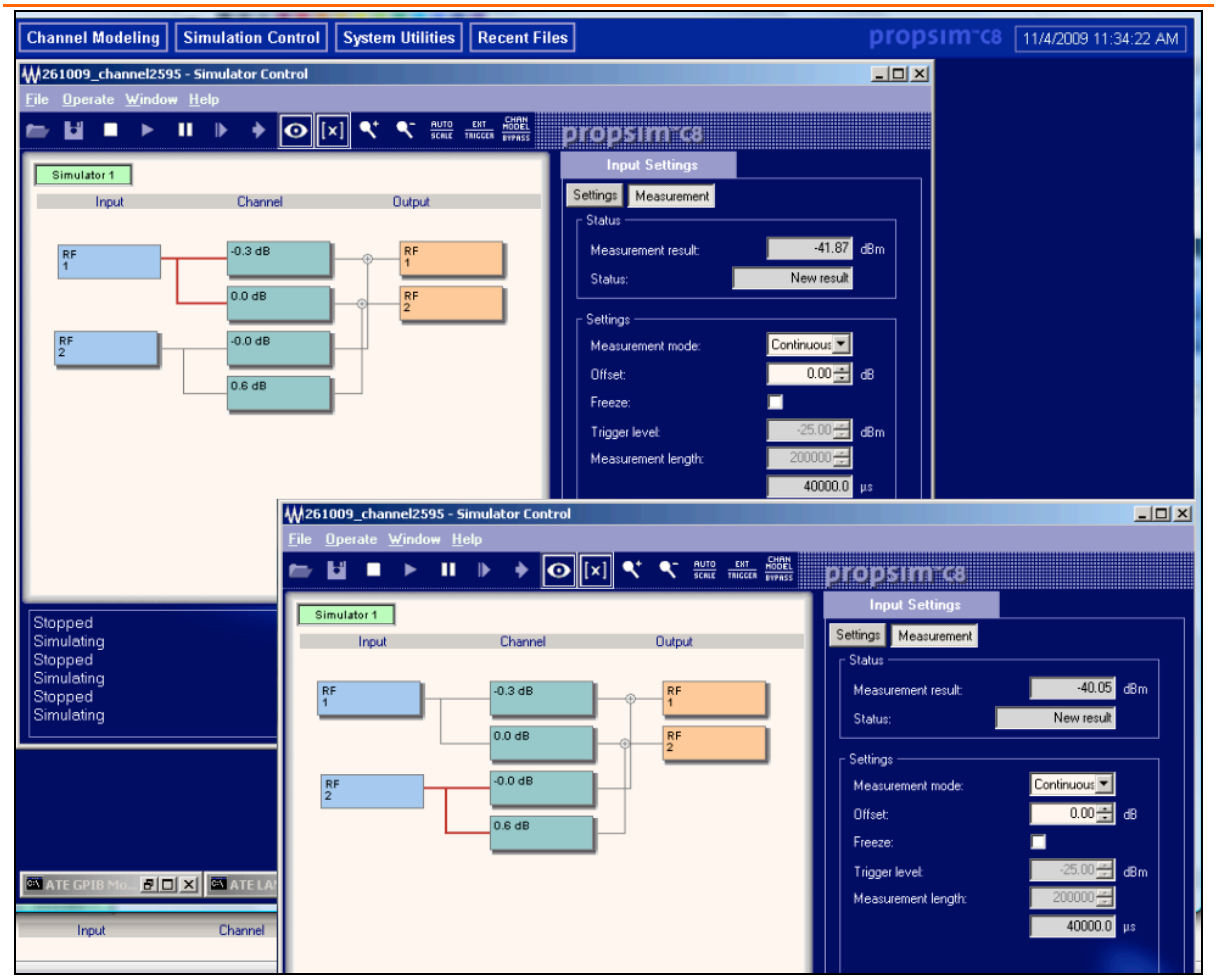


**Figure 6-19: Channel Emulator 2x2 MIMO setup: RF1 and RF2 Input Settings / Measurement window.**

- "Simulation Settings" setup:
  - As it can be seen in Figure 6-20, the selected center frequency is not matching the signal generators TX frequency (2620 MHz vs 2595 MHz). The reason to shift the channel emulator center frequency is to avoid DC-offset and IQ modulation imperfections (see Figure 6-21) which could critically impair the receiver demodulation. Additional RF filtering stages have been specifically designed to remove the remaining spurious signals, LO leakage or any intermodulation product existing near the frequencies of interest herein illustrated.
  - Figure 6-22 shows that some attention must be paid in order to avoid an excessive shifting of the center frequency of the channel emulator with respect the transmitters operating frequency because the channel emulator bandwidth (center frequency ± 35 MHz) could start filtering the upper or lower side of the 20 MHz bandwidth signal. This is the reason why instead of using a channel emulator center frequency of 2625 MHz when having an input signal of 2595 MHz, a center frequency of 2620 MHz has been used (see also Figure 6-26).
  - The rule to be followed would be:
    - (Fcenter-(Finput-BW/2)) < 35 MHz if Fcenter > Finput and
    - Finput+BW/2-Fcenter < 35 MHz if Fcenter < Finput

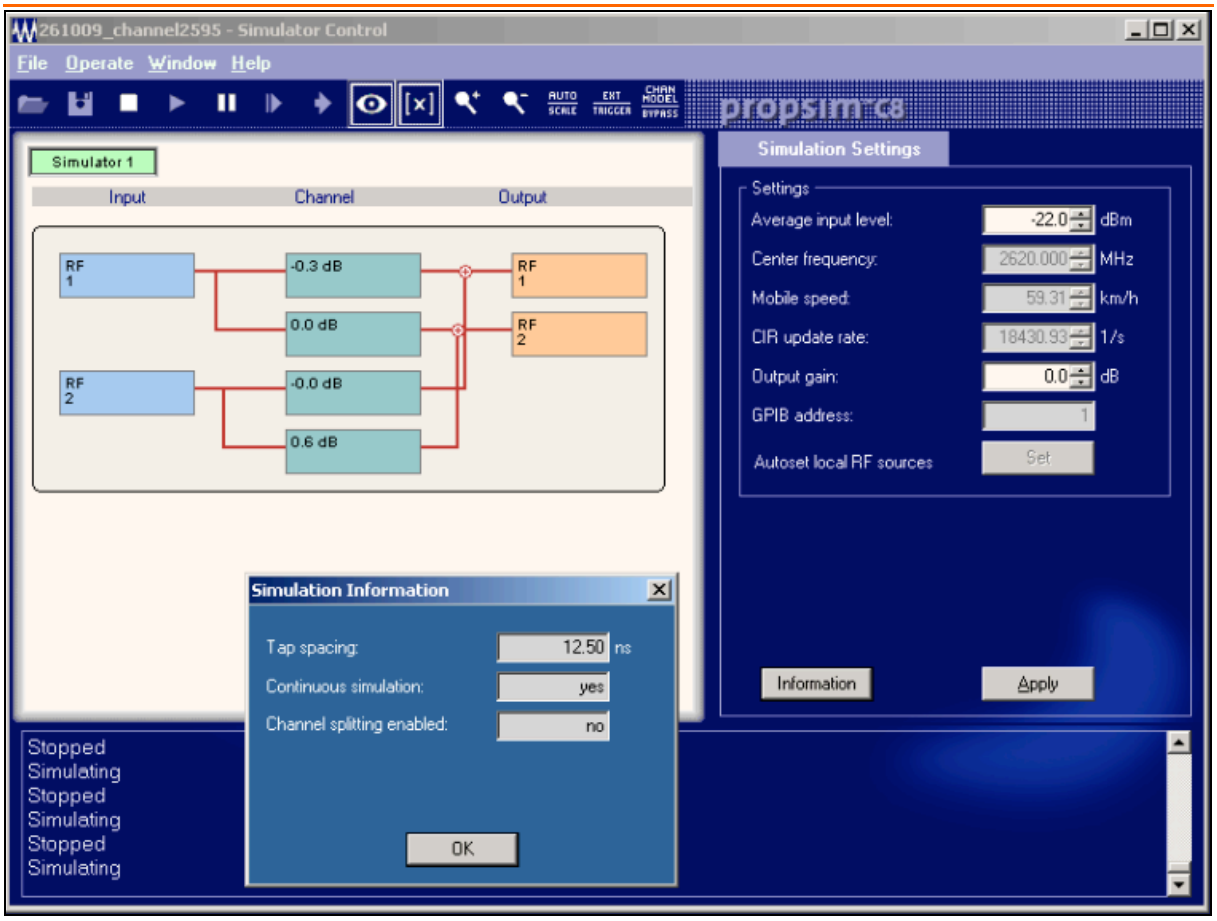


**Figure 6-20:23 Channel Emulator MIMO setup: Simulation Settings window.**

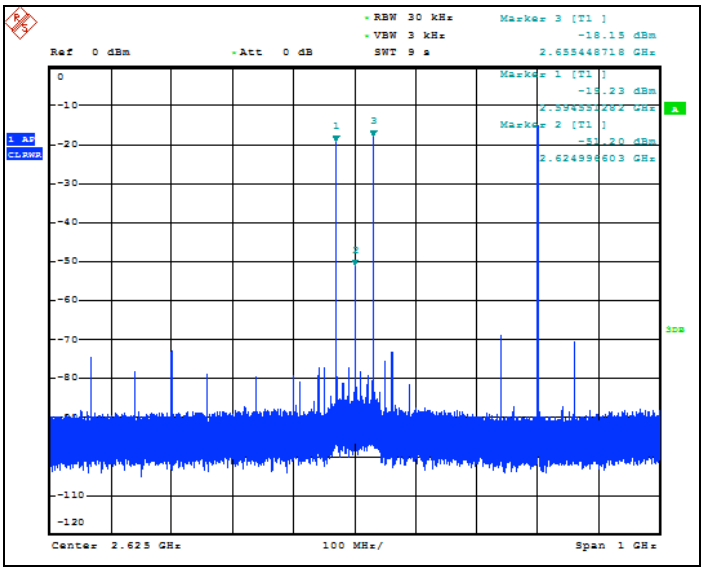


**Figure 6-21: Channel emulator spurious response of an RF signal at 2595 MHz and a center frequency of 2625 MHz.**

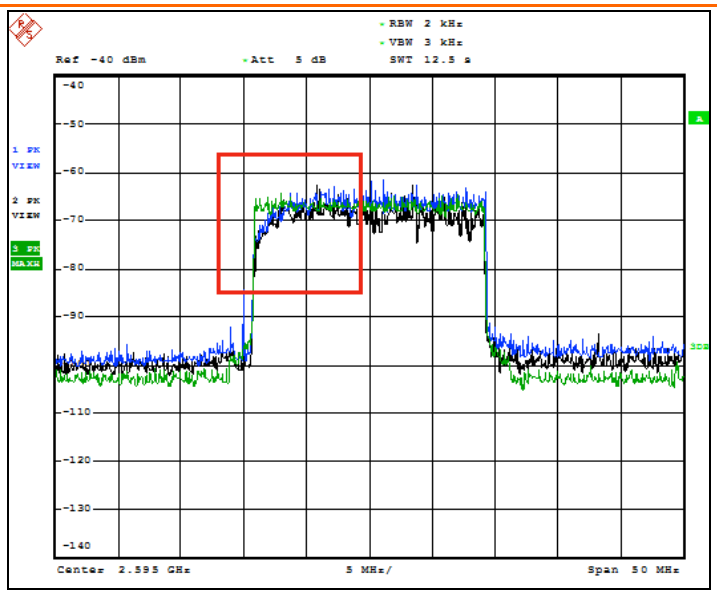


**Figure 6-22: Comparison of RF1 and RF2 outputs spectrum (black and blue) at the output of the channel emulator with the TX signal when the channel emulator is not used (green).**

Note: The input signals of 2595 MHz will not be affected by any CFO since the combination of the processes of downconversion and upconversion (and the architecture spectral inversions) compensate the deviation.

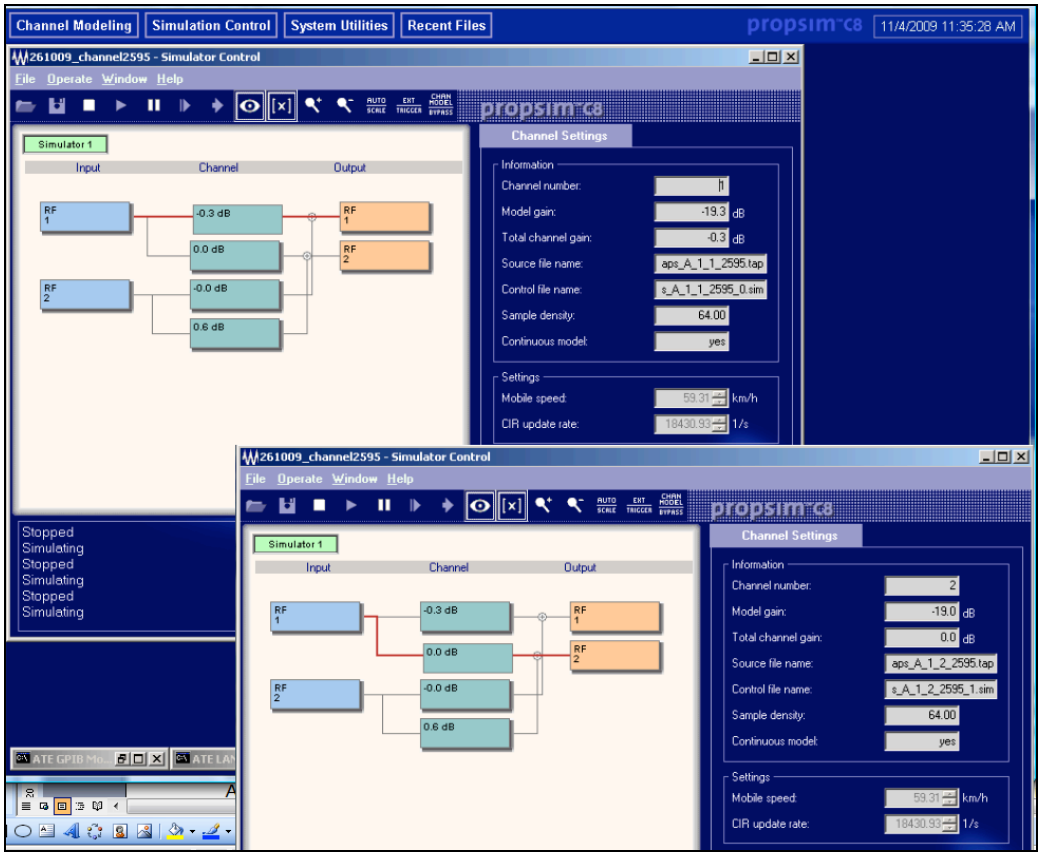


**Figure 6-23: Channel Emulator 2x2 MIMO setup: Channel Settings window for CH11 and CH12.**

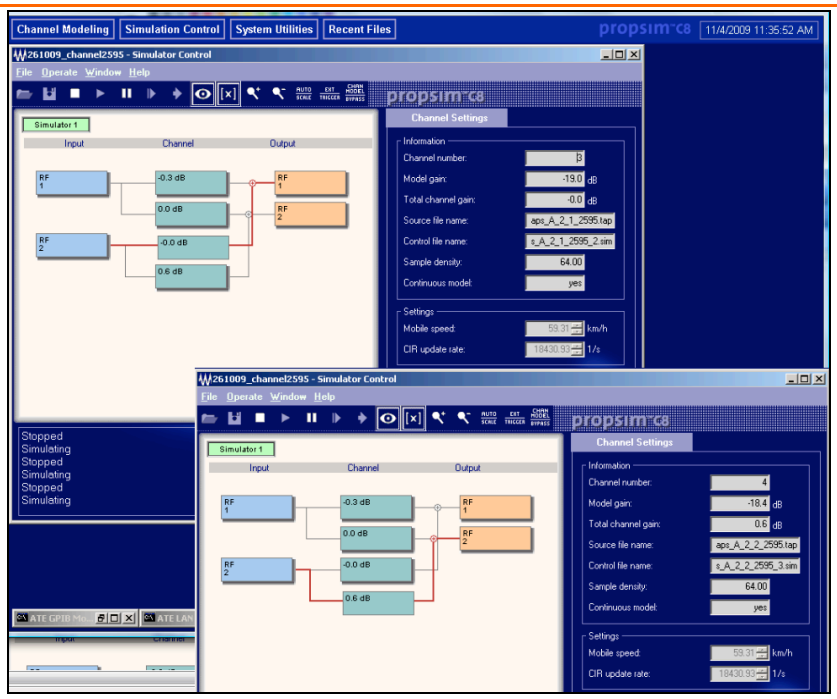


**Figure 6-24: Channel Emulator 2x2 MIMO setup: Channel Settings window for CH21 and CH22.**

- "Channel Settings" setup:
  - T_ch=G_in+G_ch+G_out, that is the Total channel gain (which also corresponds to the value displayed in the "green boxes") is the summation of the Input gain (the amplification or losses to adapt the input signal to the ADC required levels), the channel model gain (losses) and the Output gain set for the upconversion stages (see Figure 6-25).
  - The Model gain or is related to the channel model used plus intrinsic 10 dB losses.

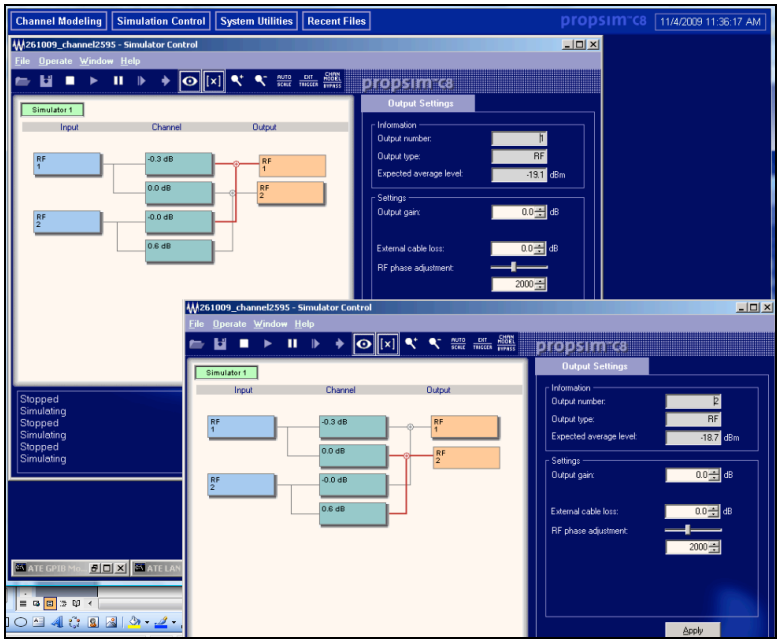


**Figure 6-25:24 Channel Emulator 2x2 MIMO setup: RF1 and RF2 Output Settings window.**

- "Output Settings" setup:
  - The Expected average level is the summation of the Average input power level and the Total channel gain. In MIMO setups the contribution of all the branches must be considered.
  - The output gain ranges from -45 dB to 9 dB.

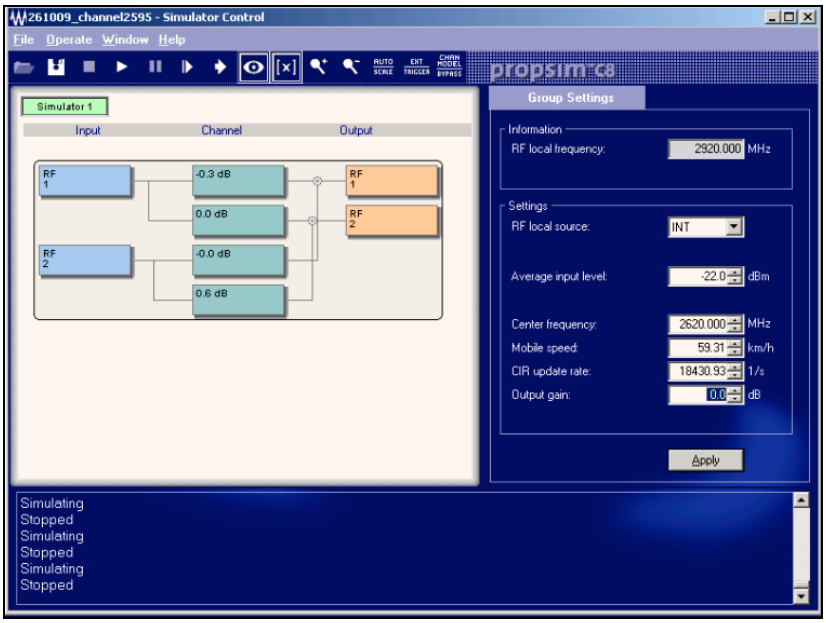


**Figure 6-26: Channel Emulator 2x2 MIMO setup: Group Settings window.**

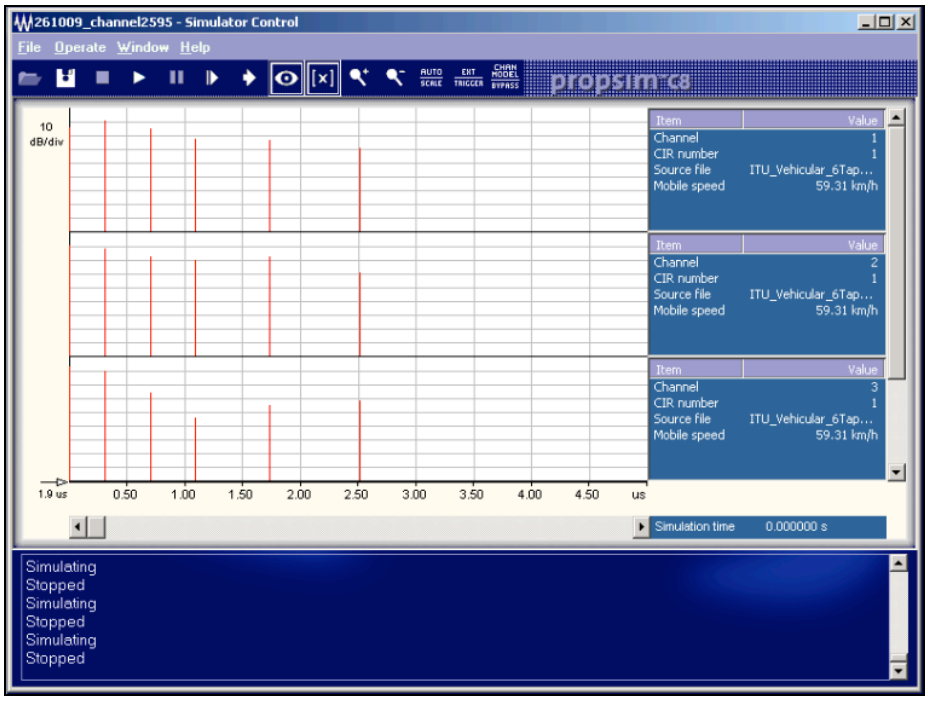


**Figure 6-27: Channel Emulator 2x2 MIMO setup: CIR visualization for the four channels.**

From Figure 6-28, it could seem that there is a very high noise level at the output of the channel emulator, but after proper visualization, it can be seen that the noisy source being

displayed is the strong local oscillator signal at the output that is coupled to the signal (and will thus be filtered by the RF downconverters).

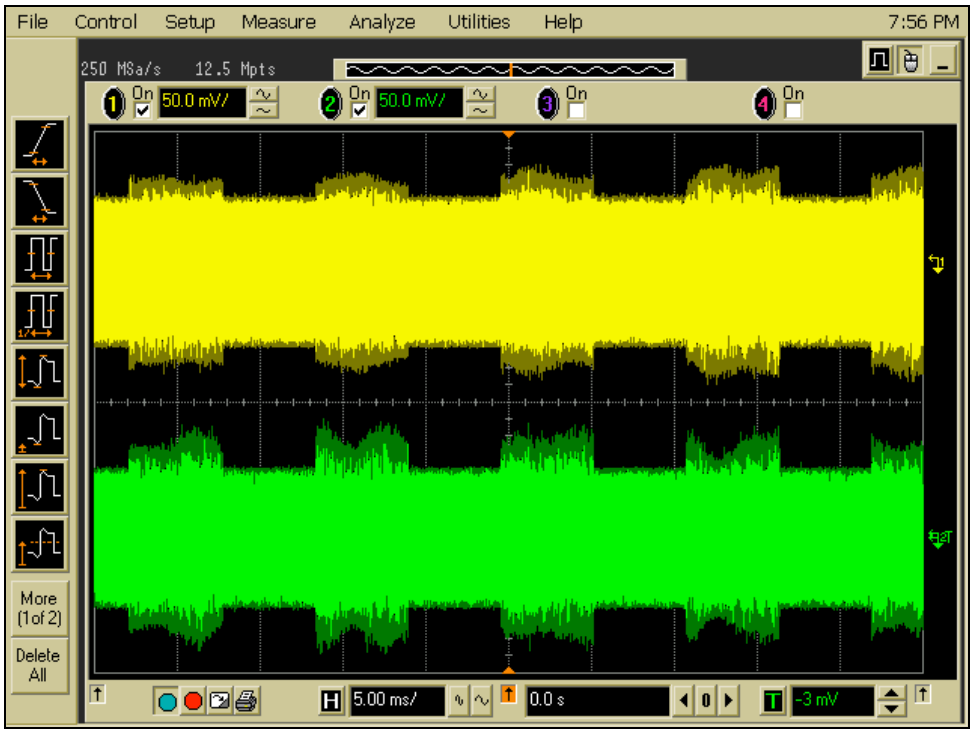


**Figure 6-28: Oscilloscope visualization of RF1 and RF2 channel emulator outputs.**

### *6.3.3 Signal Conditioning and Acquisition*

- **RF Downconverters Test Setup:**

1) Before powering up the chassis and boards, connect the RS232 to LEMO connectors (see the red trace mark for positioning) as follows :
    a. Connect the cable labelled P2-TO SYN to the SER/TG receptacle in the synthesizer board (the one on the left).
    b. Connect the cable labelled P3-TO TUNER to the SER/TG receptacle of the first tuner on the left (just at the right of the synthesizer).
2) Click the “Inspector” Desktop icon at GEDOMIS® PC1 to open the control application.
3) Power up the chassis and boards. Verify that everything is OK in the “Unit Status” and “Unit Info” Menus. Go to the “CW” Menu. In order to load the last configuration saved click on “File/Read/ and select CW”. Then click in “update” to load the RF configuration into the boards.
4) Connect the cables at the output of the channel emulator plus 10dB attenuators into the RF1 input of the first and third tuners (the second and fourth boards in the chassis, starting the count from the LO synthesizer on the left). Connect the cables at the IF OUT output ports of the two downconverter channels to the SAW Filter prototype board, and the output of the filter board to the input of the Spectrum Analyzer (tuned at 156.8MHz) and verify that you have the right signal (see Figure 6-30). In this setup, the SMD filter is used (the flatter one). After that, just connect the two IF channels to the MMCX connectors of the Lyrtech ADC boards.

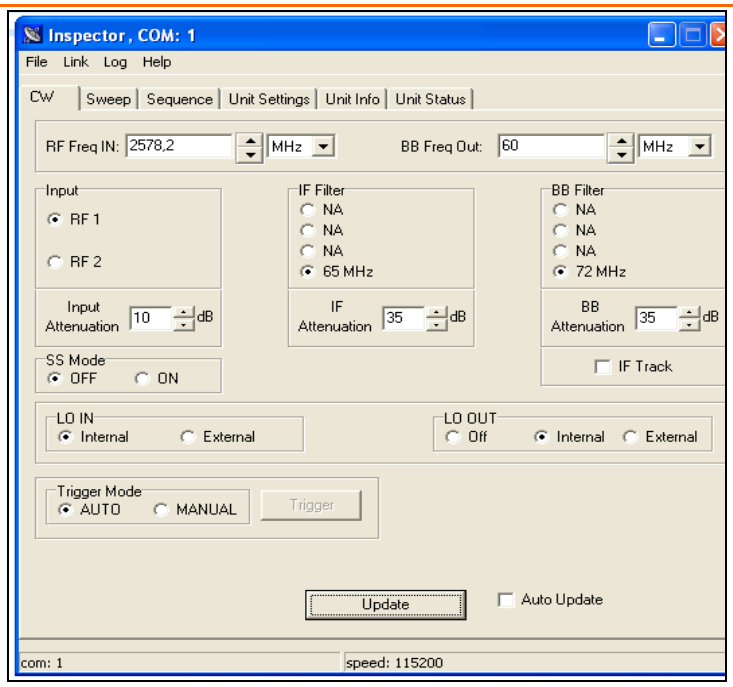


**Figure 6-29: Inspector.exe RF downconverters control application.**

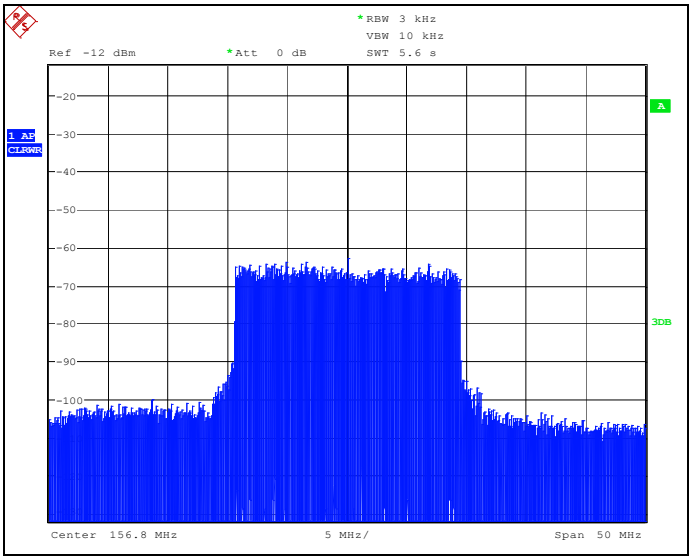


**Figure 6-30: Spectrum analyzer plot of the IF signal at the output of the RF Downconverters + SAW SMD filter.**

Notes:

- The RF Downconverters translate any RF INPUT signal from 20 MHz to 3000 MHz to fixed 140 MHz IF OUTPUT (65 MHz BW) or to a variable 3 MHz to 75 MHz BB output.
- When the BB OUTPUT is not being used the LO3 cables shared between boards must be removed to avoid massive spurious at IF OUTPUT.
- If the IF OUTPUT frequency must be set at 156.8 MHz we will modify the input frequency of the Inspector application to avoid having the output signal centered at 140 MHz (i.e. RF Freq. in = 2578,2 MHz instead of 2595 MHz).
- The activation of “SS Mode ON” implies slightly higher receiver sensitivity (about 1-1.5 dB of NF improvement) and around 12-14 dB gain increment.

- The input attenuation controller is calibrated until 30 dB of attenuation. All the following steps are uncalibrated and a combination of input attenuation control and IF attenuation control must be done to set the desired values.
- The prototyped SAW filter board includes two SMD and DIP SAW filters. The SMD filters have lower losses but higher bandwidth and the DIP filters have higher losses but the bandwidth fits better the 20 MHz signal bandwidth at 156.8 MHz. These filters help to filter out the undesired spurious signals introduced by the channel emulator and some noise.

The time signal at the output of the filters after the downconverters can be seen in Figure 6-31. If we compare this figure with Figure 6-28, we can see that the channel emulator local oscillator signal has been totally filtered out during the silence periods.

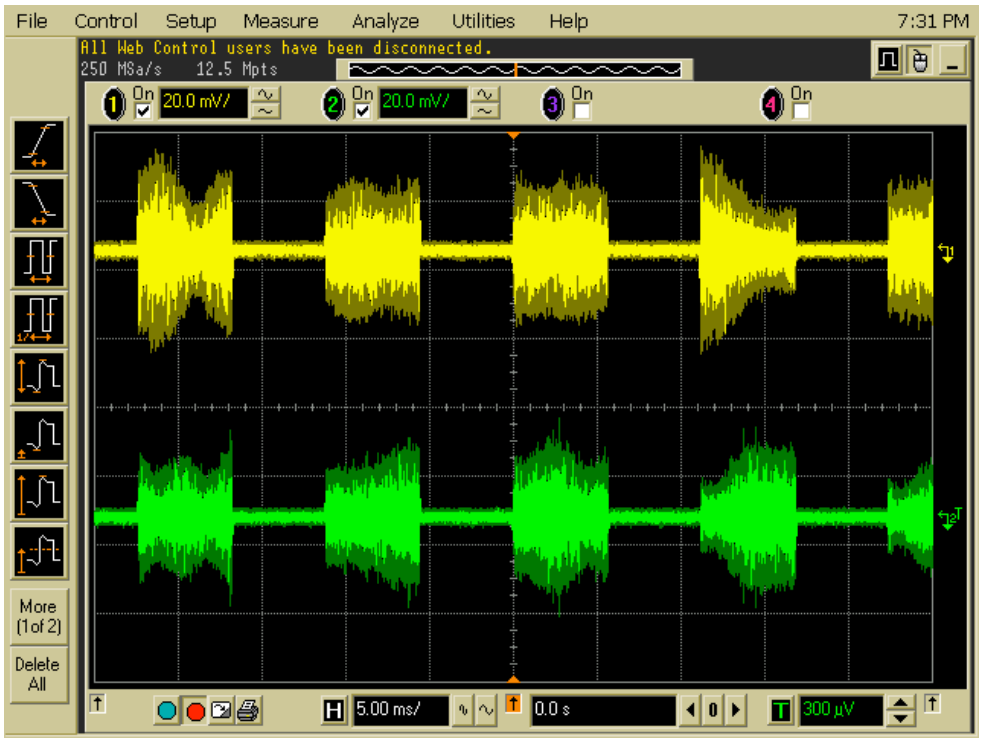


**Figure 6-31: Spectrum analyzer plot of the IF signal at the output of the RF Downconverters + SAW SMD filter.**

Additional data to be taken into account:

- Lyrtech VHS-ADC SPECS (Input power full scale levels that must be accounted)
  - G=0, 4 dBm, 1000mVpp
  - G=10 (step10)->gain of 19.5dB -> -5dBm.
  - G=15, -18 dBm, 80mVpp
  - Observation: 10-12 dB PAPR -> -6 dBm (315mV) / -28 dBm (25mV) for G=0/G=15 respectively.

  - VGA Noise Figure = 7.5 + 0.8N , APROX, N=attSTEP
  - VGA Gmax=33, Gmin=10.5, Gstep=1.5 (dB), Poutclipping=21 dBm -> Pin=-12 @ Gmax

- POWER budget (aprox. in this configuration):
  - Power delivered signal generator: -20 dBm = Power at the output of the channel emulator.

- Power at the input of RF downconverters: -20dBm-10dB(atten)-0.4dB(cable)= -30.4dBm.
- Power at the output of RF downconverters (input atten=10dB & IF atten=35dB imply gain of about 27.3 dB): -30.4dBm + 27.3dB= -4.1 dBm.
- Power at the output of cable + FILTER prototype (Note SMD_filt_losses=14.5dB, DIP_filt_losses=24 dB): -4.1 dBm-0.4dB(cable)-14.5=-19dBm (at the input of the ADC board). This is close to the full scale level of -18dBm, when Gadc=15dB (initial state when the demonstrator is using automatic AGC) if we don't account for the PAPR (that would require even less ADC input power to avoid saturation, e.g. 10 dB typ.).

In order to avoid saturation/clipping in the ADC board (e.g. higher signal power, less input attenuation in the RF downconverters….) this -19 dBm input power cannot be increased more than 7-10 dB (only if you required more power).

- **ADC Sampling frequency generator (Holzworth Microwave Source) Test Setup:**

1) Click on the HolzSource1.3.jar Desktop icon to open the application.
2) Push "Locate Device" and select the Source Model in the "Attached Devices" Menu.
3) Set the Frequency (89.6MHz) and the Power (5 dBm). Use the up/down cursor control keys in order to set the values.
4) Click on the "Power" button.

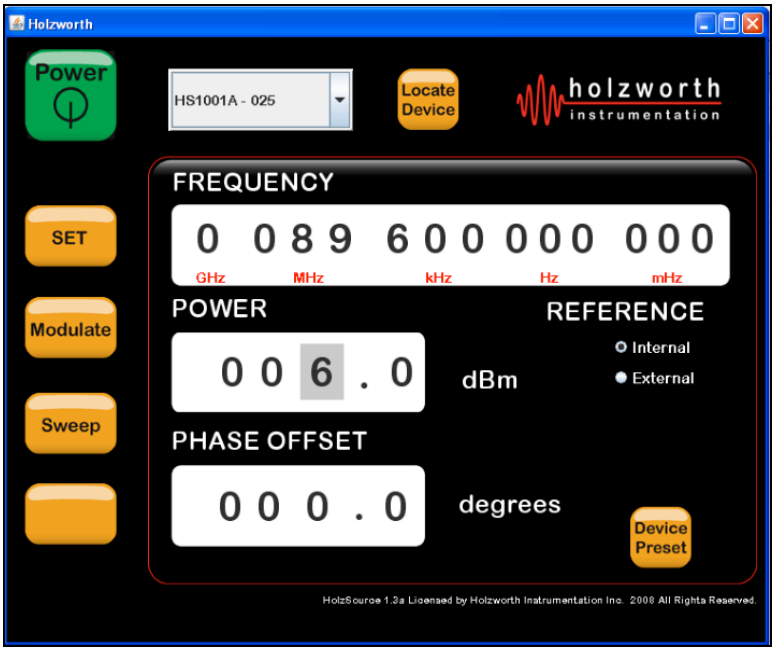


**Figure 6-32: HolzSource1.3.jar java application for control of the RF synthesizer generating the ADC boards sampling frequency.**

End of section note: The exhaustive review of signal generation with Signal Studio for 802.16OFDMA, and MIMO signal demodulation and qualitative system debugging with properly licensed VSA has been left for a separate document.

### *6.3.4 Configuring the ADP Platform as a MIMO Mobile WiMAX Receiver*

The MIMO WiMAX receiver uses both VHS-ADC and SMQUAD boards, since the design could not fit in a single FPGA device. The part of the MIMO that is hosted in VHS-ADC board was implemented using the BSDK software support package and the part hosted in the

SMQUAD board was implemented using the MBDK software support package (for more details about the BSDK and MBDK packages see Appendix 6.4). The respective steps to realize both board-configurations are given next:

- After switching on the ADP platform and waiting the Windows OS to load, the user should launch Lyrtech's SMCCE engine which is necessary for configuring certain steps (i.e. Start->Programs->Lyrtech->Host SDK->cPCI Platforms->SMCCE). This is a console program that configures the default firmware options for the DSPs and FPGAs and setting up the connection for remote access of the platform. This is required especially for using certain features of the SMQUAD board (e.g. when one of the DSPs is used to deliver control operations for a certain application example).
- Like in the previous example the user should initiate the VHS control utility (i.e. from the Windows task bar you select Start->Programs->Lyrtech->Host SDK->cPCI Platforms->VHS Control Utility). The GUI is used this time to configure the VHS-ADC board with a part of the MIMO system. The user should assign a bitstream file for configuring the FPGA device and consequently press the "PROGRAM FPGA" button to programming it. The bitstream for the MIMO configuration (i.e. from the AGC block up to synchronization block) is located in the desktop folder: Desktop\BSDK_bitstreams\ and then in the subfolder named: 281009_MIMO_VHSADC_AGC_to_SYNC_SDRAM_data_capture
- The clock source is external and when we apply the external clock source at the desired frequency (i.e. 89.6 MHz) the indication "DCMs" turns from "unlocked" to "locked".
- As long as the option "RUN" is kept unchecked, the system remains in a reset stage.
- At the "Channel Controls" tab of the VHS control utility we check the option "System Generator controls the gain", to allow the implemented Automatic Gain Control component of the 2x2 MIMO mobile WiMAX receiver to operate.
- As seen in the front panel of the Lyrtech platform the VHS-ADC is having a data transmission interface (i.e. RapidChannel) connecting the board through a blue flat-ribbon cable with the respective RapidChannel receiver component of the SMQUAD board (e.g. essentially the Rapidchannel receiver component belongs to the DRC daughtercard that is mounted on the SMQUAD board).
- The configuration of the SMQUAD board is quite different. First we open a Matlab window changing the working directory to: C:\Lyrtech\ADP\matlab\r2007a\VHS-V4\demos\Rx_2x2_MIMO_SMQUAD_files. We open the Simulink/System-Generator model "cttc-example.mdl" and then the respective sub-model corresponding to the "SignalMaster_Quad" block; finally we double click to the "DSP_1" submodel. In the windows that pops-up (i.e. "cttc_dsp") we can assign the bitstream file that will configure the FPGA device of the SMQUAD board (i.e. smquadc64x_fpga1_virtex4_ff1148_ioring.bit) by double clicking the "set bitstream" block (figure 4).
- Next, in the same window (Figure 6-33), we click the icon connect to target and after a while pops-out a window called "Lyrtech development platform detection". We select the second option of the available ones which corresponds to the IP address 127.0.0.1 and click the button "Connect to Lyrtech development platform" (Figure 6-34). By doing this the FPGA device 0 at processing bank 1 is configured with the pre-assigned bitstream and the DSP microprocessor 0 of the processing bank 1 with the executable file "cttc_dsp.out". After programming the two devices we select from the menu "Simulation" of the window named "cttc_dsp" (Figure 6.33) the option "disconnect from target".
- To debug/validate the functionality of system in real-time we may use two different instances of the Chipscope Pro Analyzer software. The two Chipscope Pro Analyzer instances require two JTAG cables since the Chipscope cores are placed in different FPGA devices of the Lyrtech boards. For simultaneous debugging the software has to be installed in two different PCs or mutually exchange the cables between the VHS-ADC board (when debugging this part of the design) and the SMQUAD board (when validating

the rest of the system). Thus, two different Chipscope Pro Analyzer projects exist, in the following directories: VHS-ADC -> (i.e. 211009_MIMO_AGC_to_SYNC.cpj)
Desktop\BSDK_bitstreams\281009_MIMO_VHSADC_AGC_to_SYNC_SDRAM_data_capture
and SMQUAD -> (i.e. smquad.cpj)
Desktop\BSDK_bitstreams\191009_MIMO_VHSADC_sync_SMQUAD_the_rest_chipscope_update

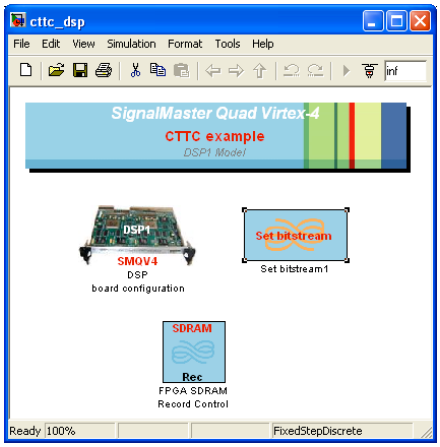


**Figure 6-33: DSP and FPGA configuration model.**

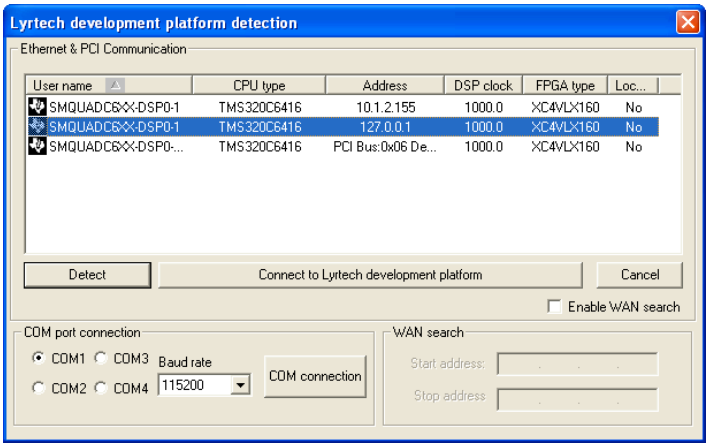


**Figure 6-34: The Lyrtech platform detection utility.**

The second Chipscope Pro Analyzer project is the one that displays the QPSK constellation of the MIMO system configuration.

- The user should press the button in the left top corner of the Chipscope Pro Analyzer, which on hover-on reveals the text “Open Cable/Search JTAG chain”. Assuming that the right signal is applied in the second and forth channels of the VHS-ADC board and the DCMs are locked (indicated in the VHS configuration utility GUI), then the system is ready and configured waiting data-delivery to start the baseband signal processing.
- Make sure that in the “Trigger Setup” window of the Chipscope Pro Analyzer, under the “function” column, the “>=” option is selected. Then the user should press the play button, which is waiting for a predefined trigger event to be satisfied to start capturing data. In our case this event is the logic-assertion of the “data valid out” port of the space-time decoding (STC) component of the receiver.
- When the user checks the “RUN” option of the VHS control utility, the FPGA of the VHS-ADC board populated with the WiMAX receiver start operating and the first QPSK constellation should appear on the respective window of the Chipscope Pro Analyzer (i.e. Bus Plot).

### *6.3.5 Data Capturing and Post Processing*

In order to enable data capturing certain modifications have to be made in the top-entity of the user’s design. The desired signals have to be mapped to those outputs of the top-level VHDL file of the firmware that are communicating with the SDRAM controller. For the VHS-ADC board an example of the component that needs to be instantiated is given next. It is very important to assign the clock that corresponds to the signals that have to be captured (e.g., the ADC sampling clock in this case) and not include signals that reside in different clock domains because this will render the FPGA data acquisition core useless. In the code-example that follows the "in_range_valid_Rx0"and "in_range_valid_Rx1" signals are the ones that are adjusted by the AGC block after the ADC stage. The remaining of the FPGA data acquisition input ports (e.g. the use is having 16 input port of 16 bit each one) have to be grounded as it is seen in the code that follows.

```
--
-- FPGA Acquisition
--

-- Extend sign for 16 bit data
acq1_d_sig <= in_range_valid_Rx0(13) & in_range_valid_Rx0(13) & in_range_valid_Rx0;
acq2_d_sig <= in_range_valid_Rx1(13) & in_range_valid_Rx1(13) & in_range_valid_Rx1;

acq_valid_sig <= '1';

u_fpga_acquisition: fpga_acquisition
  port map (
    clk => acquisition_clock_sig,
    reset => reset,

    acq_clk => adac_clk,
    acq_valid => acq_valid_sig,
    acq1_d => acq1_d_sig,
    acq2_d => acq2_d_sig,
    acq3_d => GND16,
    acq4_d => GND16,
    acq5_d => GND16,
    acq6_d => GND16,
    acq7_d => GND16,
    acq8_d => GND16,
    acq9_d => GND16,
    acq10_d => GND16,
    acq11_d => GND16,
    acq12_d => GND16,
    acq13_d => GND16,
    acq14_d => GND16,
    acq15_d => GND16,
    acq16_d => GND16,

    ext_trig => adac_trig,
    ext_trig_rst => adac_trig_rst_sig,

    sdram_clk => sdram_clk,
    sdram_active_state => sdram_active_state,
    sdram_burst_read => sdram_burst_read,
    sdram_burst_write => sdram_burst_write,
    sdram_pre_burst_write => sdram_pre_burst_write,
    sdram_burst_terminate => sdram_burst_terminate,
    custom_sdram_write_req => custom_sdram_write_req_sig,
    custom_sdram_write_ack => custom_sdram_write_ack,
    custom_sdram_write_addr => custom_sdram_write_addr_sig,
    custom_sdram_write_burst => custom_sdram_write_burst_sig,
    custom_sdram_write_data => custom_sdram_write_data_sig,

    emif_ed_in => emif_ed_in,
    emif_aoe_n => emif_aoe_n,
    emif_are_n => emif_are_n,
    emif_awe_n => emif_awe_n,
    emif_ce_n => emif_ce_n,
    emif_be_n => emif_be_n,
    emif_ea => emif_ea,
    emif_ed_out => emif_ed_out_sig,
    emif_ed_en_n => open,
    emif_ardy => rec_ardy_sig
  );
```

An equivalent core is instantiated in the FPGA of the SMQUAD board facilitating by this the capturing of the post-STC data.

- **Post-ADC data capturing**

The key element to control the VHS-ADC board (i.e., program and run it, as well as perfrom the data capturing) is the VHS Control Utility GUI. This vendor-provided GUI is featuring several tabs, but in this document we'll focus in two of them:

- *General Controls* – from this tab, shown in Figure 6-35, we can program the FPGA device through the '*PROGRAM FPGA'* button (first we must select the *.bit* file containing the RTL-design that we wish to load; by using the '*Bitstream file for FPGA*' file selector), select the clock source with the '*Clock Source*' dialog box and control the execution of the system through the '*RUN*' checkbox (i.e., in our case when the checkbox is unchecked the system's reset signal is asserted, otherwise the system is executing normally). Evidently, in the case that we are currently describing, the VHS-ADC board must be selected in the '*VHS-ADC/DAC Board Selection*' dialog (although the same exact procedure is valid for the VHS-DAC board as well).

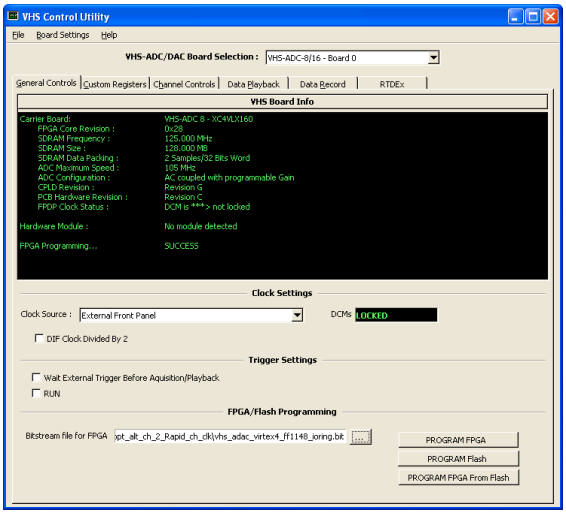


**Figure 6-35: 'General Controls' tab in the VHS Control Utility GUI.**

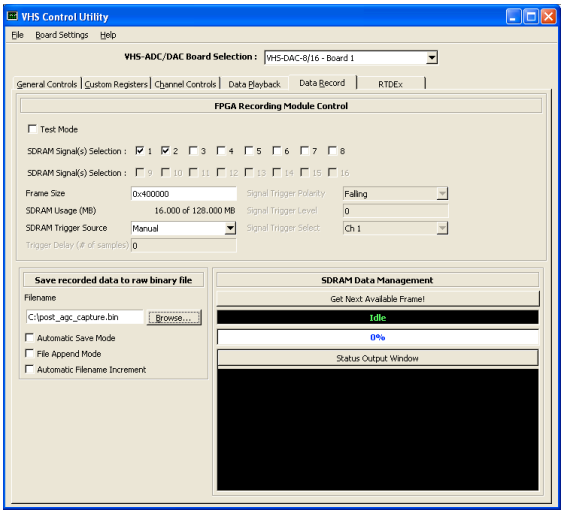


**Figure 6-36: 'Data Record' tab in the VHS Control Utility GUI.**

- *Data Record* – from this tab, shown in Figure 6-36, we can control de real-time data capturing after the ADC block (evidently, the system must be executing to do so, i.e., '*RUN*' checkbox must be checked). The following steps are to be followed:
  - Selection of the number of RAM channels to be captured, through the '*SDRAM Signal(s) Selection*' checkboxes; in the instantiation of the interfacing of the RAM memories (used to store the captured data, before writing it to a file in the hard-disk) with our logic (origin of the real-time data to be captured), we have available 8 16-bit ports that will allow to capture 8x16bits at each clock cycle. In the 2x2 MIMO receiver case, for the post-ADC data capturing, we are using 2 channels (i.e., two 14-bit ADC real outputs; which are enlarged to 16-bits through sign extension).
  - Length of the data capturing (i.e., number of (mega)bytes that will be written to the hard-disk file), by setting the value in the '*Frame Size*' dialog box. The length is expressed as the number of samples (in hexadecimal format) to be captured (taking into account the number of channels involved as well). For the MIMO receiver, which is expecting to receive frames – composed by 48 OFDM-symbols and a preamble (each one composed by 2048+512 samples) – which last 5 ms, being separated by 5ms-silence periods, we do advise to capture 0x400000 samples; which equals to 5 complete frames (plus its inter-frame silences) more or less (i.e., 16 MB file).

- A name (and a path) must be provided for the file that will be created, by using the '*Filename*' file selector. Note that the output file will have the *.bin* extension (i.e., binary file-formatting).
- When the data-capturing trigger is set to manual (i.e., the user decides when to capture data; '*SDRAM Trigger Source*' set to '*Manual*'), it can be initiated by pushing the '*Get Next Available Frame!*' button. This will create a file in the indicated location containing the post-ADC captured signal.

- **Post-Space Time Decoding data capturing**

The data capturing in the SMQUAD-4 board requires a more complex process than in the VHS-ADC case. To start with, because of the firmware provided with the boards, the specific GUI to be used in the real-time data capturing is requiring the programming of the FPGA through the Simulink/System Generator approach (i.e., the RTL-design for the baseband of the receiver is instantiated as a black box, which is connected to some firmware blocks provided by the vendor; one of them is related to the data-capturing). The Simulink/System Generator environment is also programming the DSPs, which in our case will only be used for controlling the data-capturing. The first required step, in this case, is to launch the ADP's SMCCE engine, depicted in Figure 6-37, which is a console program that configures the default firmware options for the DSPs and FPGAs, and is taking care of setting up the connection for remote access of the platform. This is required especially for using certain features of the SMQUAD board (e.g. when one of the DSPs is used to deliver control operations for a certain application, such as data-capturing).
In Figure 6-38, it can be observed an abstract vision of the Simulink/System Generator model, that is being used for the MIMO receiver's configuration: the '*DSP board configuration*' element is taking care of loading the required C code to the selected DSP, the '*Set bitstream1*' element is assigning a concrete *.bit* file to the selected FPGA and the '*FPGA SDRAM Record Control*' will allow the configuration of certain data-capturing parameters, as it will be described later. The DSP and FPGA selection will be performed through the ADP detection utility, as described in 6.3.4 (Figure 6-34).

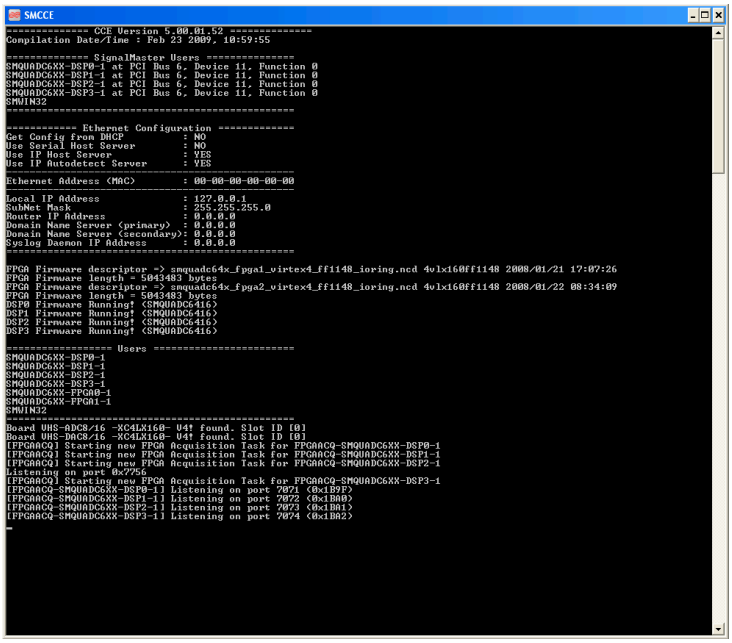


**Figure 6-37: Lyrtech's SMCCE engine.**

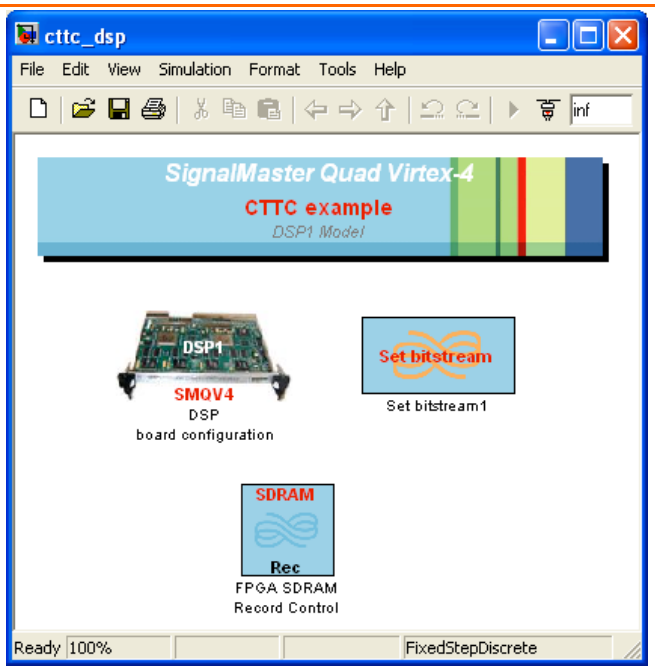


**Figure 6-38: basic Simulink/System Generator model used for the 2x2 MIMO receiver's configuration.**

For data-capturing, our main interest is set on the '*FPGA SDRAM Record Control*' element, whose parameter-setting GUI can be observed in Figure 6-39. From all the parameters that the use can define, we will use the following:

- *Recording Source* – from this dialog box we select the origin of the data to be captured (i.e., written in a file in the hard-disk). In our case we will select '*FPGA SDRAM Record*'.
- *Number of Channels* – in this dialog box, as in the VHS-ADC case, we do describe the number of 16-bit RAM ports that will be involved in the data-capturing. For the 2x2 MIMO receiver case, the Space Time Decoding block is providing 4 32-bit outputs each clock cycle (i.e., real and imaginary part for two QPSK streams, as OFDM symbols are processed by pairs), which is forcing the use of 8 16-bit channels (i.e., each 32-bit word is divided in two parts, which must be taken into account when retrieving the captured data).
- *Frame Size* – again, the size (in (mega)bytes of the file to be written) is described as the number of samples to be captured (this time through an integer value). For the post-Space Time Decoding data-capturing we do advise to capture 1024x1024 samples; which equals to the complete constellation-set for 5 complete frames more or less (i.e., 16 MB file).
- *Trigger Recording* – this checkbox will actually trigger the data-capturing (whenever the '*Trigger Source*' dialog box is set to '*Manual*', allowing the user to decide when to capture data). This (annoying) design decision made by the vendor is complicating data-capturing, since two different GUIs are involved at the same time, as we will describe in the following.

Once the basic parameters of the data to be capture are configured, as described above, the '*Lyrtech FPGA SDRAM Record and Playback Transfer Utility*', depicted in Figure 6-40, must be used to provide the configuration of some extra parameters related to the file that will be created with the capturing of data and to (partially) trigger the data-capturing itself, as described in the following:

- The '*Filename*' file selector will provide the means to indicate the path and the name of the file that is to be created as result of the real-time data capturing.

- The '*Lyrtech platform selection…*' button will launch the Lyrtech development platform detection utility to select (again) the DSP controlling the data capturing operation.
- We do advise to uncheck the '*Automatic Save Mode*' checkbox to have full control on how the data is written to the destiny file(s), avoiding by this way the undesired overwrite of meaningful captured data.
- Finally, the '*Get Next Available Frame*' button will (partially) trigger the data-capturing when pushed (i.e., the user will see that once the button is pushed nothing really happens unless the '*Trigger Recording*' checkbox is checked on the '*FPGA SDRAM Record Control*' GUI: this double manual-triggering must be performed each single time that data is to be captured).

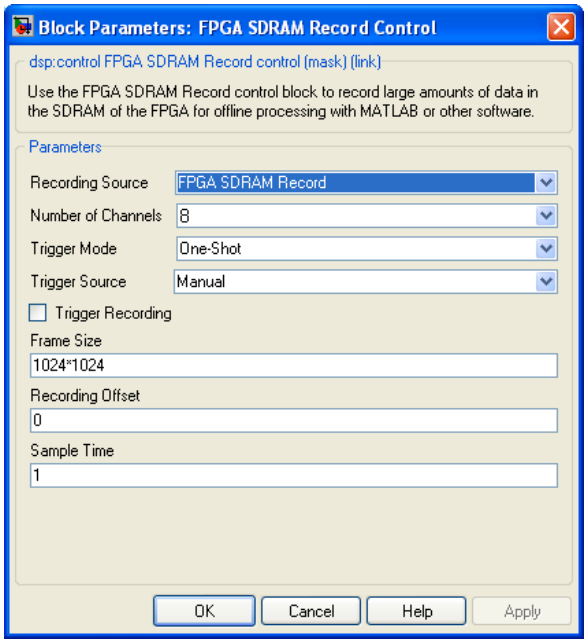


**Figure 6-39: parameter-setting interface for the 'FPGA SDRAM Record Control'.**

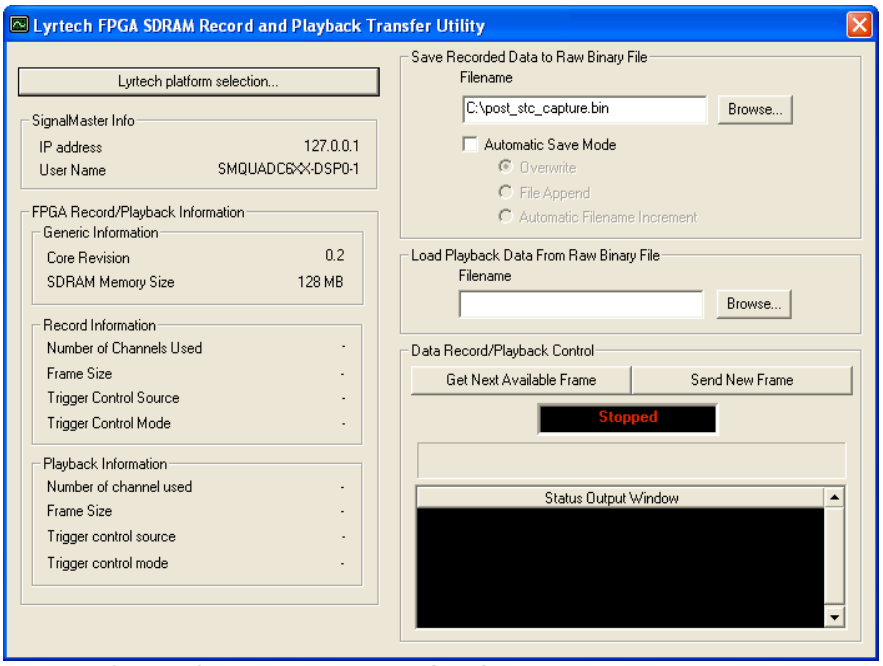


**Figure 6-40: interface of the 'Lyrtech FPGA SDRAM Record and Playback Transfer Utility'.**

- **Captured-data post-processing**

Once the captured-data is available in one (or several) binary-formatted file(s), the next step is to load it in Matlab where the actual post-processing can be easily implemented.
To interpret the captured-data, and consequently be able to load it in Matlab, two main options can be used: a translation to CSV format (comma separated values; widely spread – e.g., Matlab, Microsoft Excel), when the captured data-words are 16-bit long, by means of a software utility provided by the vendor, or the use of a custom parser (written in Java code) that will perform a translation to a customized (*.out*) file-format, using ASCII encoding, where each 16-bit(32-bit) value is written in a single line (e.g., [16-bit value] 0110111100001100). The outputs of this parser can be alternatively used for a posterior hardware captured-data/VHDL co-simulation, which, unfortunately, is out of the scope of this document.
In the CSV case the file can be directly loaded in Matlab through the '*File -> Import Data…*' menu (or alternatively with the '*load*' command in the main console or in a *.M* script), while when the custom parser is used, the *.out* files must be loaded by means of the I/O functions provided in the Matlab's API. A short example for the latter follows (excerpt of Matlab code to be used in a *.M* script):

```
%Reading from the post-Space Time Decoding captured-data file (i.e., 32-bit words)
fileIn=fopen('post_stc_data.out','r');
VHDLResult=fscanf(fileIn,'%s');
fclose(fileIn);

%Any required offset may be introduced here (e.g., we must skip the first 10 words)
t=10*32+1;
%The fixed-point formatting of the captured data is described here (e.g., 28 bits for the fractional part and 4 for %  the integer plus sign extension -> this allows for the representation of -7.9… to 7.9…)
q=quantizer([32 28]);

%We will read the complete constellations for 4 consecutive OFDM symbols (as each pair of OFDM symbols is %  jointly-processed the Space Time Decoding provides 4 32-bit words at each clock cycle – each QPSK sym-%  bol is composed of a real and an imaginary value, and two QPSK symbols are retrieved at a time – and a  %  complete OFDM symbol is having 1440 QPSK values). Thus, we are reading two pairs of OFDM symbols.
STDec_out_Symb0=[];
STDec_out_Symb1=[];
for m=1:1440*2;
    %First we'll read the real part (I) of the value for the first OFDM symbol
    realVHDLtmp=VHDLResult(t:t+31);
    tmpI=bin2num(q,realVHDLtmp);
    t=t+32 %There are 32 data digits and some blank spaces which must be skipped

    %Then we'll read the imaginary part (Q) of the value for the first OFDM symbol
    imagVHDLtmp=VHDLResult(t:t+31);
    tmpQ=bin2num(q,imagVHDLtmp);
    t=t+32; %There are 32 data digits and some blank spaces which must be skipped

    STDec_out_Symb0(m)=tmpI+j*tmpQ;

    %Then we'll read the real part (I) of the value for the second OFDM symbol
    realVHDLtmp=VHDLResult(t:t+31);
    tmpI=bin2num(q,realVHDLtmp);
    t=t+32 %There are 32 data digits and some blank spaces which must be skipped

    %Finally we'll read the imaginary part (Q) of the value for the second OFDM symbol
    imagVHDLtmp=VHDLResult(t:t+31);
    tmpQ=bin2num(q,imagVHDLtmp);
    t=t+32; %There are 32 data digits and some blank spaces which must be skipped

    STDec_out_Symb1(m)=tmpI+j*tmpQ;
  end
```

- **Post-processing the data captured in the Post-ADC stage**

As previously indicated, because the post-ADC values are 14-bit long (extended to 16-bit through sign-extension), we can use the utility provided by the vendor to translate the binary-formatted captured-data file to a CSV-formatted one. The tool, named *DataToCsv(.exe)*, unfortunately is only available for the Microsoft Windows OS (as the major part of the firmware provided by the vendor). As it can be observed in Figure 6-41, this command-line executable requires the user to define a list of parameters in order to perform the format translation, as described:

- *source* – here, the path and name of the (*.bin*) file containing the captured data must be specified.
- *destination* – here, the path and name of the (*.csv*) file that will be created as result of the translation must be detailed.
- *number of channel* – here, the number of channels (i.e., 16-bit words) written at each clock cycle during the data-capturing must be specified (i.e., this parameter must coincide with the number of channels selected in the '*Data Record*' tab in the VHS Control Utility, as described in section 2.3). This value will be 2 in our case.
- *-s / -u* – the first must be selected in the case of signed values (which is our case), and the second is to be selected otherwise.
- *fixed point* – the bit where the fractional part starts must be indicated (as long as the data at the outputs of the ADCs is not in overrange, this is not important, as the value-range of the signal can be later modified in Matlab – i.e., moving the point is equivalent to a division or a multiplication by a power of 2, but it's only a matter of quantization as no data, and thus precision, is lost).
- *-16 / -32* – this indicates if the length of the captured words is of 16 bits or of 32 bits. Our experience has shown that the -32 option is not working properly.

```
=======================================================
   Data record converter to CSV version 1.0.0.1
   (c) Lyrtech 2007
=======================================================
 This program convert binary data to CSV.
=======================================================

Convert binary to CSV
DataToCsv source destination [number of channel] [-s|-u]
                             [fixed point] [-16|-32]

    source                  Specify the binary source
    destination             Specify the csv destination
    number of channel       Number of channel in the binary file
    -s                      The binary is signed
    -u                      The binary is unsigned
    fixed point             Number of bit where the fixed point
                            is located
    -16                     The binary is 16 bits length (default)
    -32                     The binary is 32 bits length
```

**Figure 6-41: 'DataToCsv' command-line utility.**

Taking all the above into account, the following command must be launched in order to convert a capture file, for the post-ADC data captured in the real-time 2x2 MIMO mobile WiMAX receiver:

*DataToCsv post_adc_captured_data.bin post_adc_captured_data.csv 2 -s 12 -16*

To facilitate this process an automation environment (written in Java code) has been written, based on a predefined naming convention for the post-ADC captured-data files (which takes

into account the characteristics of the test, such as the channel model used, the presence or absence of mobility, the number of repetitions performed and the given predefined-scenario utilised – in terms of RF-equipment configuration, targeting better or more-impaired received SNR conditions). This custom program, named '*GEDOMIS_execute_DataToCsv*' is relying on the following API functions provided by Java:

- *Runtime.getRuntime().exec()* which allows the execution of external commands (i.e., the DataToCsv.exe utility provided by the vendor), passing all the required parameter-values in the call.
- *Process.getInputStream()* and *Process.getErrorStream()* which are monitoring the executed command's verbosing (e.g., an error message or some output text is displayed).
- *Process.exitValue()* and *Process.destroy()* to control if the program has exited with or without errors or to force it to end its execution after some time (in our case, the latter has been required – 5 minutes, more or less, are required for the conversion plus some safety margin).

With this custom Java program, long sets of captured data can be properly converted to CSV-format without any effort (i.e., no intervention of the user is required). Then, as mentioned above, the data can be easily loaded in Matlab where the post-processing itself can be easily implemented. As an example, two *.M* scripts have been developed: one is automatically calculating the SNR for all the captures (following the same naming convention as in the *.BIN* files), while another allows the captured frames to be feed to the Matlab model of the 2x2 mobile WiMAX receiver to verify its correct behavioural functioning or to calculate the "ideal" achievable baseband performance and compare it to the one observed in the testbed.

- **Post-processing the data captured in the Post-Space Time Decoding stage**

As previously indicated, because the post-Space Time Decoding captured values are 32-bit long, unfortunately, the utility provided by the vendor to translate the binary-formatted captured-data file to a CSV-formatted one doesn't work properly. Therefore, a custom translating program (written in Java) has been developed, which is based on the following API functions:

- *FileInputStream.read()* which allows to read one byte (i.e., 8 bits) at a time from the *.BIN* file. The read byte is stored as an integer value.
- *Integer.toHexString()* which converts each read byte to an hexadecimal value (e.g., 10 is represented as 0x0A). Here we must take care that when there are four 0s in the left (most important bits), the hexadecimal value returned will need a left-0 to be manually inserted (e.g., instead of 0x0A the returned value would be 0xA). The hexadecimal value is stored as a string (i.e., ASCII coding).
- *Integer.toBinaryString(Integer.decode("0x"+returned_hex_value.substring(i,j))* which converts each one of the digits in the previously generated hexadecimal value (e.g., *returned_hex_value(0,1)* for the first one) to its binary representation. Again, some left-0s must be manually inserted so 4 bits are finally produced each time. The binary value is stored as a string (i.e., ASCII coding).
- *BufferedWriter.write()* which allows to write the ASCII-representation of the retrieved binary values to a file in the hard disk, to be later used as an input to Matlab (or to a VHDL) simulation.

At this point it is worth noting that a (somehow) strange design decision has been detected during the implementation of the parsing code: when the selected DSP on the SMQUAD-4 board is writing the captured data to the SDRAM to be latter retrieved, the lower bits of the 16-bit RAM-channel (i.e., *7 downto 0*) are written first, being followed by the higher bits (i.e., *15*

*downto 8*). Thus, we have to correct its order when reading in order to correctly retrieve the 16-bit-value which represents each one of the halves of the 32-bit-word representing the Space Time Decoding outputs.

To facilitate the post-processing, this custom parsing utility is designed to be part of the previously mentioned automation environment. Therefore, it is also based on a predefined naming convention for the post-Space Time Decoding captured-data files (which takes into account the characteristics of the test, such as the channel model used, the presence or absence of mobility, the number of repetitions performed and the given predefined-scenario utilised – in terms of RF-equipment configuration, targeting better or more-impaired received SNR conditions). Again, then, trough this custom Java program long sets of captured data can be properly converted to to a customized (*.out*) file-format, using ASCII encoding, where each 16-bit(32-bit) value is written in a single line, without any effort (i.e., no intervention of the user is required). Then, as mentioned above, the data can be easily loaded in Matlab where the post-processing itself can be easily implemented. As an example, an *.M* script has been developed to automatically calculate the EVM and BER performance metrics for all the captures (following the same naming convention as in the *.BIN* files).

### *6.3.6 Performance Summary of the Testbed RF Equipment*

WiMAX presents very demanding requirements on RF dynamic range and fidelity. In order to take control over possible signal impairments high-end instrumentation has been used to generate the RF signals, emulate the channel conditions and enable the signal reception.

The Agilent E4438C signal generators include baseband generators that can be synchronized for multiple transmit antenna setups, enabling I/Q gain and phase imbalances control (and including a self-calibration routine) and the testing under different C/N conditions (i.e. AWGN waveform generator). The only impairment of the transmitter to be considered is that there is no null DC carrier in the generated OFDM signal due to the leakage of the local oscillator feeding the IQ modulator of the instrument as it can be seen in Figure 6-42.

| CFO related | SFO related | Phase Noise | IQ impairments, DC offsets |
|---|---|---|---|
| Internal reference oscillator:<br>-Aging:<±0.1ppm/year,<±0.005ppm/day after 45 days.<br>-Temperature:<±0.05ppm<br>- Line voltage (+5%to-10%margin): <±0.002ppm.<br><br>Age: 2.5 years-> Worst case of ±0.1057ppm @ 2.6GHz = 275Hz (max.) | Baseband generator (option 602):<br>- Sample rate: 1KHz-100MHz, 0.001Hz resolution.<br>- Accuracy: Same as timebase $+2^{-42}$ (in non-integer apps).<br>- 10MHz reference input ±10ppm standard timebase.<br><br>Note: The input reference deviation can be characterized and compensated if required. | RF Spectral purity:<br>-SSB Phase Noise @ 20KHz:<br>2GHz: <-124dBc/Hz<br>3GHz: <-121dBc/Hz<br>(Option UNJ improves spectral purity)<br><br>2.6GHz-> around -122.5dBc/Hz<br><br>BB Spectral purity (baseband generator):<br>-Phase noise: <-127dBc/Hz @ 20 KHz. | Baseband generator(option 602):<br>-I/Q amplitude imbalance not specified.<br>-I/Q phase imbalance not specified.<br>(Internal calibration routine)<br>-DC offsets, DC carrier power not specified. |
| Other considerations | | | |
| - Linearity: *RF)* Harmonics <-30dBc, NonHarmonics<-68dBc, No Subharmonics (option UNJ). Other non-linearities do not appear below the maximum output power of the signal generator (about 13-15 dBm). The Crest Factor of the signal being generated must be accounted to avoid non-linearities when operating close to the maximum output power level. *BB generator)* Harmonic distortion <-65dBm, IM performance <-74dB.<br>- AWGN: 89 bit pseudo-random generation, repetition period $3*10^9$ years.<br>- Triggers: External delay resolution: 10ns (valid for MIMO signals synchronization).<br>- Baseband generator: 16-bit resolution. | | | |

**Table 6-11: Agilent E4438C ESG vector signal analyzers specifications.**

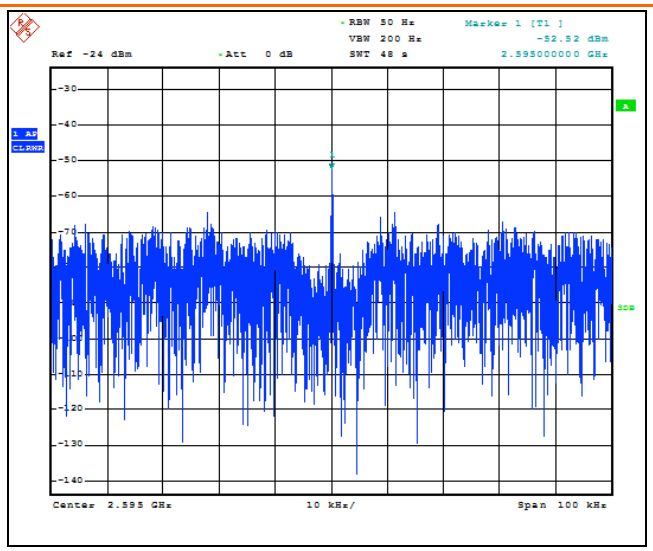


**Figure 6-42:25 Spectrum analyzer plot of the transmitted mobile WiMAX signals with LO leakage.**

The EB Propsim C8 is used to emulate real-world situations in a lab environment by adding complex and time-varying effects of multipath and Doppler shifts in the digital domain. This implies that the RF signal entering the emulator has to be downconverted and upconverted and the channel emulator has to feature noise floor, dynamic range and EVM with sufficient margin to avoid distorting the signal, and enough bits at the A/D and D/A converters to handle the signal level fluctuations (determined by the Crest Factor of the signal which is around 12 dB in our WiMAX OFDM system) and the dynamic range at the output. The architecture of the instrument compensates Carrier Frequency Offsets (CFO) produced in the downconversion and upconversion stages. Nevertheless the presence of high level leaking IF and LO (affected by the upconversion CFO) signals produce high power in-band mixing products near the central frequency of the transmitted signal as seen in Figure 6-43. In order to overcome this severe impairment and filter it out, the channel emulator central frequency can be shifted to separate these spurious from the 20 MHz OFDM signal (all within the 70 MHz RF bandwidth of the instrument).

| CFO | SFO | Phase Noise | IQ impairments, DC offsets |
|---|---|---|---|
| - Frequency resolution: 1KHz.<br>- Frequency accuracy: ±0.1 kHz @ fc±10MHz.<br>- Any local oscillator frequency offset is compensated by the channel emulator architecture (downconversion spectrum inversion). | Digital Baseband:<br>- 80MHz sampling clock (external sampling clock can be provided). | RF Spectral purity:<br>-SSB Phase Noise @ 20KHz: <105 dBc/Hz<br>Internal oscillator:<br>-SSB Phase Noise @ 1KHz: <-70 dBc/Hz, @ 100KHz <-104dBc/Hz. | -I/Q amplitude imbalance: <0.1 dB in 1..5 MHz range.<br>-I/Q phase imbalance: <1° in 1..5MHz range.<br>-Leaking carrier at RF fo <-35dBc, <100mV DC offset at analog baseband.<br>- In addition, the high level leaking IF and RFLO implies that there will be a strong intermodulation product falling in the middle of the band RF=RFLO-IF. |

Other considerations

- Linearity: *RF)* Image rejection of downconverters >-33dBc in 1..5MHz offset range, Baseband harmonics at RF<-35dBc (<-50dBc in the analog baseband), Leaking IF (fif=300MHz)<-10dBm, Leaking RFLO<+5dBm, Other in-band spurious signals (RBW=10KHz) <-55 dBm in fo±BW/2 (<-70 dBm in the analog baseband between DC and BW/2), Other out-of-band spurious signals (1MHz RBW)<-10dBm each. Spurious Free Dynamic Range (SFDR=power ratio between max. Output power signal and highest spurious)>33 dB in 1..5MHz. Spurious outputs inside the emulator band (internal oscillator): < -60dBc excluding ± 100kHz from carrier (*NOTE: DO TESTING USING ESG AS LOCAL OSCILLATOR*).
- Noise: Output noise floor at 1MHz offset (fo+1MHz) <-122dBm/Hz (<-135dBm/Hz at analog baseband), Output noise floor at 1MHz offset (fo+1MHz) <-140dBm/Hz at output gain setting -20 dB.
- EVM (for WCDMA): <2% rms.
- AWGN: Option not included in the instrument.
- A/D and D/A converters: 12-bit and 14-bit resolution respectively.
- In-channel Group delay variation: <5ns < 5 ns in fo ± 10 MHz.
- Delay variation between channels: <1ns @ 2 GHz.
- Path to path delay error (between paths per channel): <±6.25ns (Hardware usage optimization mode), <±1ns (Balanced delay and hardware optimization), < ± 0.5 ns (Delay accuracy optimization).
- Average phase error between channels, daily calibration and typical lab environment: ± 5° @ 2 GHz.

**Table 6-12: Elektrobit EB Propsim C8 channel emulator specifications.**

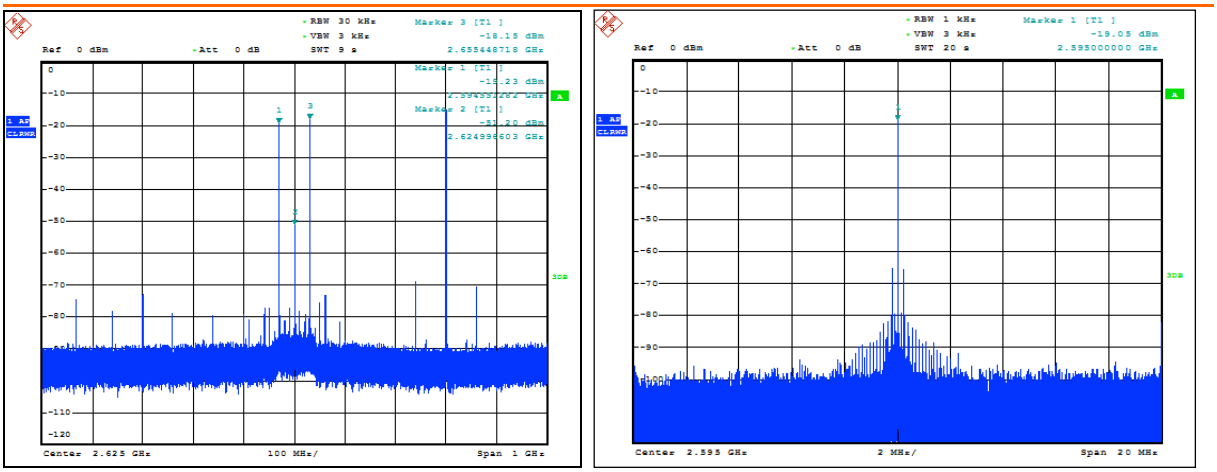


**Figure 6-43: Spectrum analyzer plot showing spurious signals and intermodulation products at the output of the channel emulator.**

Finally, the receiver is composed by MCS Echotek Series RF 3000T broadband multi-channel downconverters featuring high spectral purity, dynamic range and wide bandwidth (65MHz IF bandwidth). For the current setup, two channels are used in phase-coherent operation with the addition of a prototyped IF SAW filter (better matching the signal bandwidth) to reduce the noise and the spurious (introduced by the channel emulator) at the input of the A/D converters.

| CFO | SFO | Phase Noise | IQ impairments, DC offsets |
|---|---|---|---|
| -Tuning resolution: 1Hz.<br>-Internal reference accuracy: ±½ ppm max, 0°C to 50°C operating. | N/A | RF Spectral purity:<br>-SSB Phase Noise (typ.) @ 100Hz offset: <-95 dBc/Hz, @ 1kHz<-105dBc/Hz, @10kHz<-115dBc/Hz, @100kHz<-120dBc/Hz. | N/A |
| Other considerations | | | |
| - Linearity: Input-third order intercept point: 5dBm typ. Output-third order intercept point: 35dBm ( 40 dB gain setting). Theoretical input compression point (IP3-10dB) is below -5dBm. Considering a signal with CF=12, Pin_max would be set below -17dBm (40 dB gain setting) to avoid non-linearities. Internally generated spurious: Not greater than -90dBm.<br>- Image rejection: 100 dB.<br>- Noise Figure: >8dB (min. SSMODE ON). | | | |

**Table 6-13: MCS Echotek Series 3000T tuners specifications.**

All the herein described impairments must be taken into account: Both the SFO and the CFO must be minimized since the baseband developed receiver has not unlimited CFO correction (e.g. ±10KHz range) and we want to avoid phase rotation in the data constellation of received symbols and increased levels of inter-carrier interference (ICI). The spectral purity or the phase noise impairment disperses the constellation points and thus increases the EVM or RCE (dB) constellation errors (and thus reducing the Bit Error Rate or BER). The DC offsets may impair the custom developed synchronization strategies since when the CFO is corrected the DC component turns into a sinusoid with a certain level that can alter the frame detection. The I/Q imbalances can provoke constellation rotation, the spurious state spreading (circular), receiver saturation or noise performance degradation (i.e. due to reciprocal mixing with LO signals).

## 6.4 Appendix: Using GEDOMIS® to Develop the PHY-layer of Real-time Systems

The ADP features two different software support packages, namely the board support development kit (BSDK) and the model-based development kit (MBDK). The BSDK option allows the users to integrate custom VHDL code by using as templates various examples offered for the different boards. The BSDK examples are implemented in Xilinx ISE 9.2 and the user-code can be simulated prior to silicon-testing. The MBDK software package implies a high-level model approach of designing a system by using pre-compiled intellectual property (IP) cores and other add-on simulation tools. The MBDK is actually the only way that the user can have behavioural simulations of a custom VHDL code with the several board-level VHDL components that "surround" the user logic (i.e. FPGA I/O ring). Apparently, the FPGA I/O rings components vary in each ADP board; for this reason the MBDK has different versions targeting the different ADP boards as seen in Figures 6-44 and 6-45.

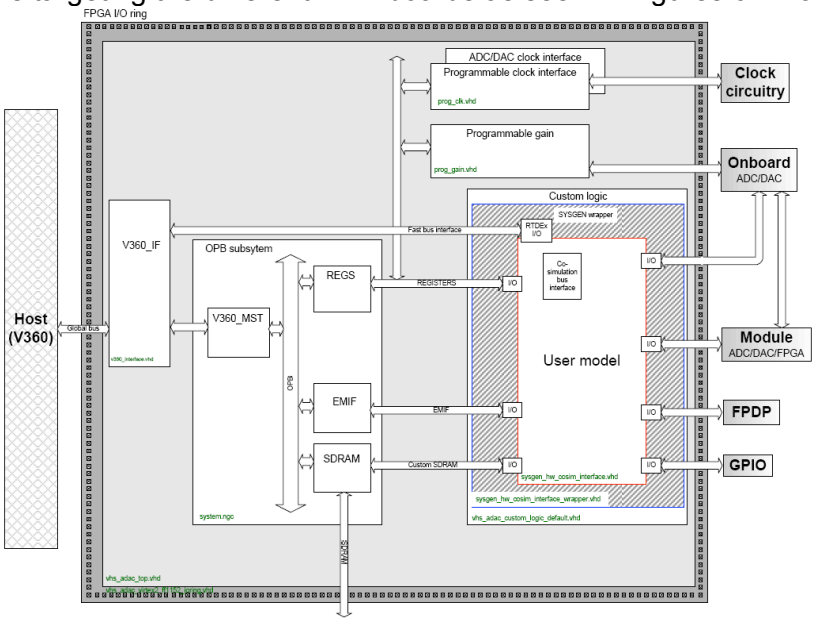


**Figure 6-44: The FPGA I/O ring for the Lyrtech VHS-ADC board.**

The MBDK option is making use of Simulink and Xilinx System Generator for a model-based approach of code integration. The ADP offers System Generator specialized libraries for each board that emulate the functionality of various I/O connectivity options for the FPGAs and DSPs, as well as other Simulink simulation-utilities (Figure 6-46). The supported versions of the underlying software are the Matlab 2007a and the Xilinx System Generator 9.2. The later is running exclusively under the 32-bit version of Windows XP. Table 6-14 indicates an incompatibility of MBDK and the XC4VLX160 devices of the ADP. In the following we give details of an unconventional way to tackle this problem.

| Virtex-4 LX Memory Recommendations in GB | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Windows | | | | Linux | | | |
| | 32-Bit | | 64-Bit | | 32-Bit | | 64-Bit | |
| | Typical | Peak | Typical | Peak | Typical | Peak | Typical | Peak |
| XC4VLX15 | .4 | .5 | .6 | .7 | .4 | .5 | .6 | .8 |
| XC4VLX25 | .5 | .7 | .8 | 1.1 | .5 | .7 | .9 | 1.2 |
| XC4VLX40 | .7 | 1.1 | 1.1 | 1.6 | .7 | 1.1 | 1.2 | 1.8 |
| XC4VLX60 | 1.0 | 1.5 | 1.5 | 2.3 | 1.0 | 1.5 | 1.7 | 2.5 |
| XC4VLX80 | 1.3 | 2.0 | 1.9 | 2.9 | 1.3 | 2.0 | 2.1 | 3.2 |
| XC4VLX100 | 1.7 | 2.6(2) | 2.5 | 3.9 | 1.7 | 2.6 | 2.8 | 4.3 |
| XC4VLX160 | N/A(1) | N/A(1) | 3.4 | 5.2 | N/A(1) | N/A(1) | 3.8 | 5.8 |
| XC4VLX200 | N/A(1) | N/A(1) | 4.4 | 6.8 | N/A(1) | N/A(1) | 4.9 | 7.5 |

(1) 32-bit machines are not suitable for these devices.

**Table 6-14: Memory constraints of the PC running the ISE software.**

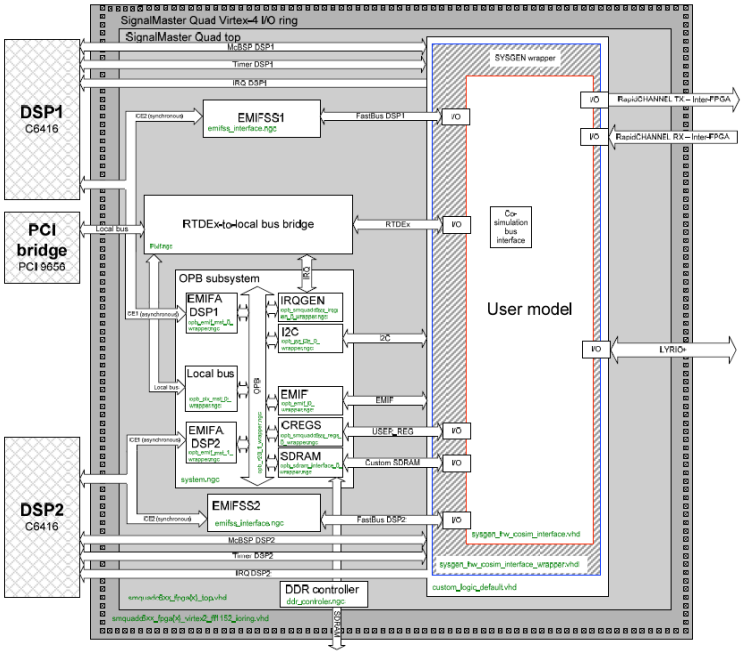


**Figure 6-45: The FPGA I/O ring for the Lyrtech SMQUAD board.**

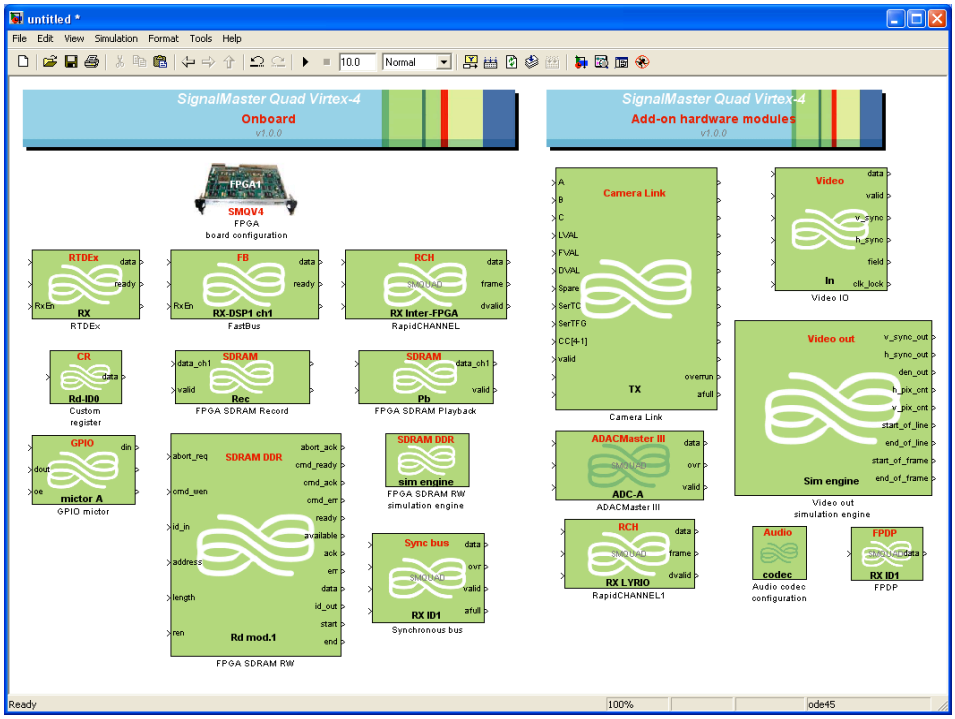


**Figure 6-46: The MBDK FPGA blocks of the SMQUAD-4 board.**

- **Using the MBDK for custom code integration**

As already shown the ADP MBDK package is essentially a set of libraries that utilize Simulink blocks and Xilinx System Generator blocks to represent the I/O connectivity options for each FPGA in each target board. The MBDK user is also having available the System Generator blocks for Simulink (Figure 6-47) as well as Simulink libraries to design a custom system. An experienced HDL designer can apply a limited use of this software solution for rapid prototyping of simple systems. In all cases there are various design-constraints that

users should be aware of, before starting implementing complex designs in model-based approach. A short compilation of them is given hereafter:

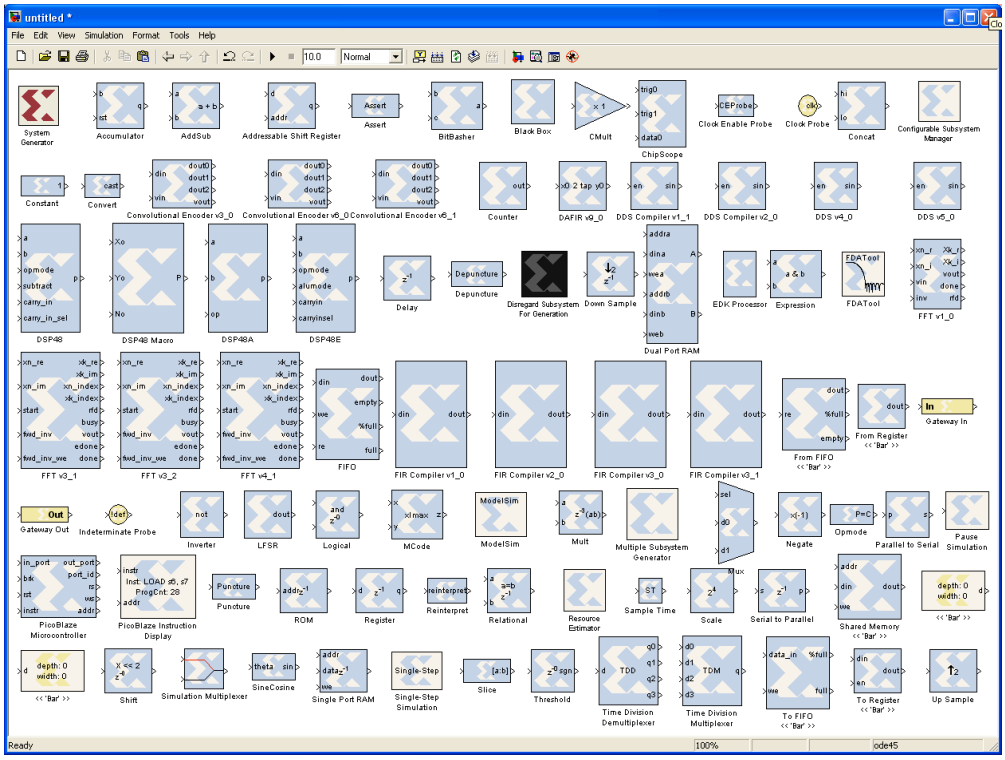


**Figure 6-47: Overview of the Xilinx System Generator blocks.**

- The model-based implementations provide non optimal FPGA design implementation results (i.e. in terms of the maximum achieved system clock).
- The Xflow toolchain is essentially a script that calls the basic command-line design-compilation options (i.e. xst, ngbuild, map, par, bitgen). However, it is not flexible enough leading the developers to more traditional ways of compiling their design (i.e. command-line utilities).
- The only way to integrate pre-verified custom VHDL-code with the MBDK design flow is to use the "black-box" block of Xilinx System Generator. The black-box is complying with the general design approach of System Generator which uses a single clock and clock-enable signals to implement multi-rate systems. This simply means that a digital clock manager (DCM) component cannot be used.
- To our best knowledge and experience, hierarchical precompiled VHDL designs featuring multiple clock domains are almost impossible to be integrated using a model-based Matlab-to-VHDL design flow. The proposed design technique of clock and clock-enable, available as the default (and unique) design technique for implementing multi-rate designs cannot support large precompiled synchronous designs with hierarchal structure; although you may apply a combination of clock and clock-enable in the top-level file of the hierarchy, this will not be propagated to the lower logic-levels of hierarchy as far as synchronous digital circuitry is concerned. This could only be achieved with a major redesign of the synchronous logic elements to account for the clock-enable signal (e.g. use the clock enable signal in every VHDL process). Such redesign is undesirable especially in projects that involve deep hierarchy and numerous VHDL files.
- Redesigning pre-verified VHDL code to account for the clock clock-enable design feature, may compromise the known performance, since it is highly likely that the use of System Generator's clock-enable signals will slow down the system clock (i.e. clock-enable signal is synthesized as a gated-clock resulting in an overall underrated performance) or as we

have experienced in other cases, the design will not be able to meet timing constraints (i.e. clock enable perceived as a gated clock).

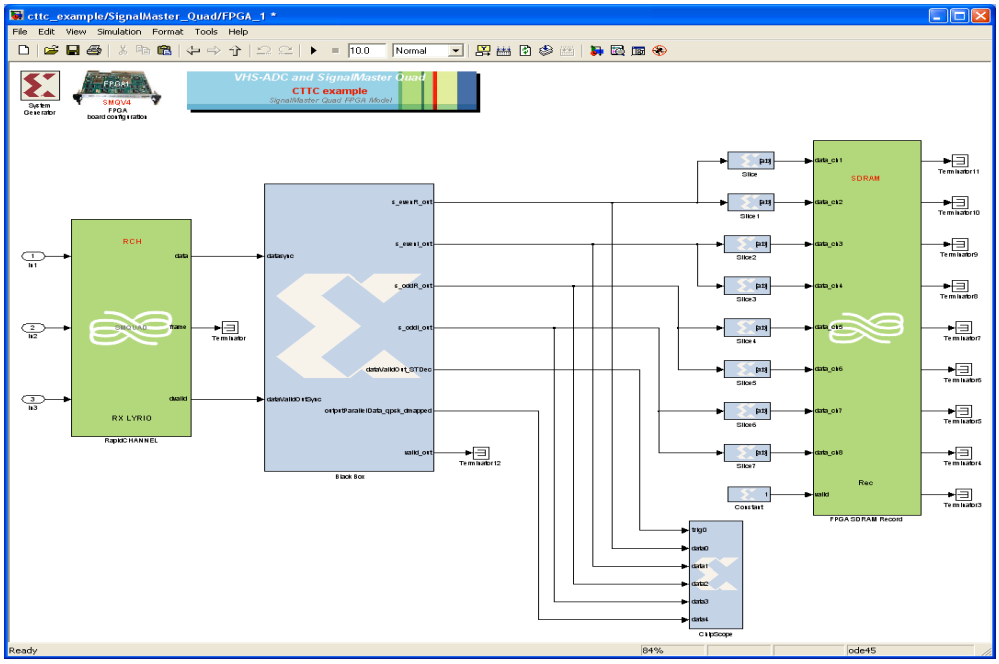


**Figure 6-48: Custom VHDL-code integration using black box and Lyrtech's MBDK components.**

A Simulink model utilizing a System Generator black box is shown in Figure 6-48. When a black-box is added in a Simulink model, a window pops up requesting the assignation of a VHDL file, which from a classic VHDL designer point of view is the top-level VHDL file of the whole custom-code. When this is done a Matlab file is generated having the same name as the VHDL file and describes the I/O port widths and names, the clock rates for each port and the VHDL file that corresponds to this black box. Apparently, the Matlab file has to be edited or updated to reflect all the VHDL files that are included in the hierarchical VHDL design, with the correct order of the file compilation.. An indicative Matlab-code extract that demonstrates this concept is given next (e.g. this code is from the Matlab configuration file generated as part of the black-box creation shown in Figure 6-48):

```
  this_block.addFile('Rx_2x2_MIMO_SMQUAD_top.vhd');
  this_block.addFile('cpRemoval.vhd');
  this_block.addFile('fft.vhd');
    this_block.addFile('xilinx_fft_2048_pipl_unscl_trnc_6phram_v32.xco');
    this_block.addFile('xilinx_fft_2048_pipl_unscl_trnc_6phram_v32.ngc');
  this_block.addFile('cyclicShiftPostFFTAndCtrlSignalsGen2x2MIMO.vhd');
  this_block.addFile('pusc2x2MIMODesubchannelization28bAgilent.vhd');
    this_block.addFile('puscNullCarrierAndDcRemoval28b.vhd');
    this_block.addFile('puscDeweighting28b.vhd');
    this_block.addFile('Div1428b.vhd');
    this_block.addFile('pusc2x2MIMOPilotOrDataDecision28b.vhd');
  this_block.addFile('channelEstimation32b2x2MIMO_vehA.vhd');
    this_block.addFile('chanEstMemCtrl28b2x2MIMO.vhd');
    this_block.addFile('pilotMem28b2x2MIMO.vhd');
    this_block.addFile('dataMem28b2x2MIMO.vhd');
    this_block.addFile('coefficientsCalculation32b2x2MIMO_vehA.vhd');
    this_block.addFile('ffShiftRegister_10positions_77bwide.vhd');
        this_block.addFile('xilinx_ffShiftReg10_77b.xco');
        this_block.addFile('xilinx_ffShiftReg10_77b.ngc');
  this_block.addFile('STDec2x2MIMO_vehA.vhd');
    this_block.addFile('div_32bremainder.vhd');
    this_block.addFile('xilinx_pipelined_divider_32b32b_sign_32bfract_1clk.xco');
```

```
    this_block.addFile('xilinx_pipelined_divider_32b32b_sign_32bfract_1clk.ngc');
    this_block.addFile('ffShiftRegister_68positions_24bwide.vhd');
        this_block.addFile('xilinx_ffShiftReg68_24b.xco');
        this_block.addFile('xilinx_ffShiftReg68_24b.ngc');
  this_block.addFile('puscDeclustering2x2MIMO.vhd');
  this_block.addFile('memController2x2MIMO.vhd');
  this_block.addFile('puscPermutationFormulaRead2x2MIMO.vhd');
  this_block.addFile('memReceiver32b2x2MIMO.vhd');
  this_block.addFile('PUSC_zone_reading.vhd');
  this_block.addFile('qpskDmap32b2x2MIMOAgilent.vhd');
```

- **A design trick to overpass the implementation constraints of MBDK**

As it has been already mentioned before, both the VHS-ADC and SMQUAD boards feature a Virtex-4 LX160 device which cannot be targeted for designs that exceed 40% slices utilization. During the FPGA compilation process and more specifically during the mapping process, the required physical memory of designs with FPGA slice utilization more than 40%, exceeds the maximum physical memory allocated by the Windows XP (version 32 bit) to the mapping process. Generally the Windows 32-bit operating system (OS) can support up to 4 GB of physical memory (a part of it is reserved by the OS and other application running by default as background processes). Increasing the Virtual Memory of the system is simply not an option since the mapping process is requiring physical memory. The Xilinx System Generator version supported by ADP and used from the MBDK, is only running under Windows XP 32-bit. Therefore the Xflow script used by Simulink to invoke the System Generator and the ISE software (e.g. in command line) is failing during the mapping process. For the case of the 2x2 MIMO mobile WiMAX receiver presented in Appendix 6.3 we had to use two Virtex-4 LX160 devices (FPGA1: 81% slices, 93% RAMB16s, 100% DSP48 and FPGA2: 49% slices, 71% RAMB16s, 57% DSP48). The only viable and tested solution found to this problem, other than using numerous FPGA devices with device-utilization less than 40%, is an unconventional way to continue the compilation process that fails when it runs out of memory. A step-by-step description of this way is given next:

- Open the respective MBDK Simulink system-model which resides in a PC with Windows 32-bit (i.e. the suitable one to host the compatible version of Xilinx System generator and Lyrtech MBDK).
- Double-click in the system generator token and initiate the compilation of the design by pressing the “generate” button (Figure 6-49).
- The xflow script is invoking in command-line every FPGA compilation process (i.e. in the following order: xst, ngbuild, map, par and bitgen). The synthesis process will run without any problems and the same applies for the translation process. However during the mapping the system runs out of memory and thus the FPGA compilation fails.
- Assuming that we are having a PC with Windows XP 64-bit, more than 6GB of RAM memory (e.g. it is advisable an 8GB physical memory configuration) and the respective version of the ISE software for this OS (i.e. version 9.2), we may copy and paste the whole Lyrtech folder from the 32-bit PC to the 64-bit PC (i.e. C:\Lyrtech).
- Once the copy of the Lyrtech folder finishes we may invoke from command line (e.g. the path is \design-directory\ netlist_smquad\xflow) the same processes that have failed (see the code-box that follows).

```
@REM # Command line for ngdbuild
ngdbuild -p xc4vlx160-10ff1148 -nt timestamp "C:\Lyrtech\ADP\matlab\r2007a\VHS-
V4\demos\Rx_2x2_MIMO_SMQUAD_files\netlist_smquad\xflow/smquadc64x_fpga1_virtex4_ff1148_ioring.ngc"
smquadc64x_fpga1_virtex4_ff1148_ioring.ngd
@REM # Command line for map
map -ignore_keep_hierarchy -pr b -cm balanced -timing -ol high -xe n -o
smquadc64x_fpga1_virtex4_ff1148_ioring_map.ncd smquadc64x_fpga1_virtex4_ff1148_ioring.ngd
smquadc64x_fpga1_virtex4_ff1148_ioring.pcf
@REM # Command line for par
par -w -ol high smquadc64x_fpga1_virtex4_ff1148_ioring_map.ncd smquadc64x_fpga1_virtex4_ff1148_ioring.ncd
smquadc64x_fpga1_virtex4_ff1148_ioring.pcf
```

- If everything flows as expected the compilation will be successfully completed.
- The dense device utilization usually results in a volatile implementation, since the place and routing process only manages to meet timing constraints in an arbitrary way. This limitation is posed by ISE software technology or even by physical device constraints. The only solutions are to apply more stringent timing constraints and separate the design in 3 FPGA devices.

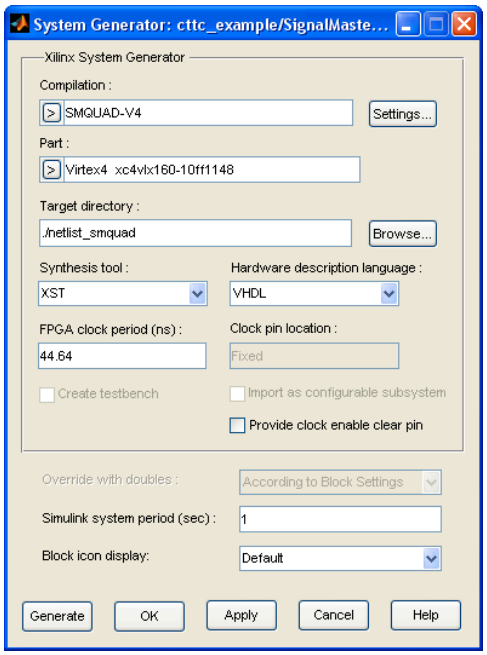


**Figure 6-49: The system generator token.**

- **Using the BSDK for custom code integration**

The BSDK custom VHDL code integration package is a more reliable way to implement complex designs targeting the ADP. The users have to study the given VHDL application-examples, understand how the VHDL board-firmware is implemented and try to fit their custom VHDL code in one of them, modifying the I/O interconnection option and registers according to their design requirements. The main known issues of BSDK are the following:

- The user cannot simulate the custom VHDL code with the on-board custom-registers and interconnection interfaces due to the absence of the respective simulation testbenches.
- The documentation is missing some essential information.
- The BSDK requires a long learning curve.
- The only available way to make functional verification of the system after integrating custom VHDL code with Lyrtech's VHDL firmware is the onboard real-time debugging by using Xilinx ChipScope Pro software tool.
- The use of Chipscope implies an overhead of memory and slices utilization that has to be accounted during design-time. Chipscope also has a limited data-capturing capacity a constraint that makes functional verification of the BSDK-based design a hard task.
- Multiple clock domain implementations of user custom VHDL code have very stringent timing requirements. Every signal that crosses a clock domain has to pass through a specialized FIFO that is meant to synchronize the communications of different clock zones (i.e., these FIFOs use a different clock to drive the read and drive processes, along with some control logic, thus ensuring the reliability of the communication between the two parties on different clock domains). The processes written by the user in charge of controlling these FIFOs must be carefully writing in order to avoid timing problems.

Comments and suggestions for the improvement of this document are most welcome and should be sent to:

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