3.1 Publishable summary

This Support Action - the FP7 project **S-PULSE** - has been established in order to prepare Superconductor Electronics (SE) technologies for the technology generation beyond the CMOS scaling limits. In the field of logic operations, Rapid Single Flux Quantum (RSFQ) circuits are the technology with the lowest risk. The advantages of these electronics are a very low on-chip power consumption in combination with data and signal processing rates that are an order of magnitude higher that those of semiconductor technology. All essential circuit elements of SE have been developed and demonstrated, but so far not implemented in industrial applications. The unprecedented potential of SE for the requirements of the future information and communication society can only be exploited if the economical impact of superconducting technologies in Europe is strengthened. S-PULSE supports joint efforts of European academic and industrial groups in the superconducting technologies field. This Support Action strengthens the vital link between research and development on the one hand and industry on the other hand. It unites industrial expectations, visionary extrapolation, and the current status of technology. It improves the image of SE and aims to push SE technologies out of their niche as a successful but alien technique. It advances the exchange of knowledge and ideas, takes charge of education, and wins public interest. These goals will be achieved by knowledge dissemination with particular attention to inspire industrial interest, to assess application fields for SE, and to prepare a European Roadmap for SE. The project will maintain regular contacts with representative partners from industry and thereby encourage a possible implementation of an industrially guided European Technology Platform (ETP) at the end of the project.

WP1: Strategic work towards the industrial visibility of SE

The WP1 is the kernel of the Support Action includes strategic work for monitoring and assessment of SE and the preparation of a European Roadmap on SE, both for the aim to enable a feasibility study of a European Superconductive Electronics Centre (ESEC).

Following the assessment of international RSFQ activities (D1.1.1) we proceed to observe the activities of the major countries for RSFQ Japan and US (**D1.1.2**).

The report **D1.2.2** outlines the technological requirements of a European foundry for fabrication of superconductor electronics devices. A foundry should consist of three divisions: design, fabrication and testing. For a reproducible fabrication and a significant yield, the processes have to be ISO-9001 certified, as is the case for the FLUXONICS foundry. A second report (**D1.2.3**) provides an analysis of requirements for the ESEC. The recent installation of FLUXONICS Foundry for the first time provides for a high-level and open-access technological basis for the production of integrated superconductive electronics. As a consequence, long term stability of this highly trained technological basis for superconductive electronics is essential to maintain Europe competitiveness with U.S.A and Japan. The increasing of complexity to VLSI requires resources and has to be embedded into a long-term shrink-path strategy which can be implemented by an ESEC as proposed here.

The final first version of European roadmap on SE (**D1.3.1**) has been sent to the EC S-PULSE project officer on May 15th, 2009. The second version of the SE roadmap has been initiated with a meeting on September 24th, 2009 subsequent the EUROFLUX 2009 conference. A time table has been elaborated for the delivery of the final version D1.3.2.

WP2: Seminars, workshops, training summer schools and conferences

The aim of WP2 is to strengthen the European SE community and disseminate the knowledge about the potential of SE electronics in Europe. The workshop (**D2.2.2**) about *Applied SE in Metrology* was held at the PTB in Braunschweig, Germany. The first *Workshop on Experimental Aspects of SE* (**D2.3.3**) dealing with experimental considerations associated to Superconducting Electronics has

taken place in Chambéry (Savoie, France). The *6th FLUXONICS RSFQ Design Workshop* (**D2.3.4**) was held in Ilmenau, Germany. The *S-PULSE International RSFQ Technology Workshop* (**D2.3.5**) took place in Jena, Germany. The major event for this work package was the conference *EUROFLUX 2009* (**D2.1.2**) about SE systems in Avignon, France. During these five events, the participants from both European and non- European countries were able to broaden their knowledge on SE while attending the presentations and involving in lively discussions.

WP3: International visibility and dissemination of European SE

Two newsletters (of 4 pages in April 2009 and 8 pages in October 2009) have been created and send by regular mail to nearly 300 recipients. Moreover, all the newsletters are now posted in pdf format on S-PULSE website and can be freely downloaded.

Left: Cover page of newsletter n°2 – Right: Cover page of newsletter n°3

In order to test the full procedure regarding the FLUXONICS Foundry, a **virtual** run has been prepared, with user interface, end-user specification, technical specifications, time schedule and estimated cost (**D3.2.1** to **D3.2.4**). As a result, **D3.2.5** provides the procedure to access the FLUXONICS Foundry: it is associated to a new page *"Foundry Access"* in the menu of S-PULSE website.

WP4: Fundamental aspects of Josephson-junction technologies with nanometer dimensions

The name of the Working Package WP 4 of the European S-PULSE project is "Study the ultimate technology dimensions". This study includes technical work as well as theoretical analyses.

The deliverable **D4.1.1** consists of two parts. The first part of this technical work is based on the experimental data resulting in the development of a fabrication process for SQUIDs with sub-micrometer-sized Josephson junctions. To adapt this new technology to the more complex RSFQ logic circuits, four development steps have been suggested within the European FLUXONICS Foundry. All four steps of process development are time and material consuming. It is outlined how the improvement of a new RSFQ logic technology can be based on a DC SQUID process with sub-micrometer-sized Josephson junctions. This plan can be realized only by additional funding for the FLUXONICS Foundry. The second part of **D4.1.1** is to support the project partners by performing a RSFQ run in the frame of the FLUXONICS Foundry. The circuits were fabricated as wafer run

4SO-2010. All parameters are within the allowed tolerances. The chips have been sent to the project partners Univ. Savoie, TU Ilmenau, and Univ. Stellenbosch.
The report **D4.1.2** describes the role and influence of test arrays and test circuits for validation of technological processes and their improvements and optimisation. It additionally gives some benchmarks for technological process steps. The report is focused on a superconductor electronics fabrication technology for large series arrays of Josephson junctions, which are used for example for RSFQ circuits and Josephson voltage standards. Josephson voltage standards contain up to several 10,000 or even a few 100,000 junctions and RSFQ electronics aim for 1,000,000 junctions. Only a few institutions have available the thin-film equipment for fabrication of these complex circuits. The yield for fabrication of devices presently corresponding to R&D requirements will significantly be increased by the improvements of fabrication processes. FLUXONICS Foundry should make use of the promising starting position to reach these ambitious aims.
The deliverable **D4.2.1** discusses the ultimate dimensions of circuit elements for practical applications. The ultimate clock speed of single Josephson and circuits containing few JJs can be as high as the gap frequency, exceeding 700 GHz for Nb based circuits. For more complex circuits based on Nb technology, a clock speed of ~100 GHz can be expected. Since the speed of RSFQ circuits is proportional to $j_C^{1/2}$, junctions with j_C in the range of 10 kA/cm^2 can potentially attain the projected clock speed. Additionally, miniaturization of the active junctions is a necessary requirement to attain practical large scale integration levels. In the past years, a high level of complexity has been achieved in the design of superconducting electronic circuits. However, increasing circuit complexity has necessitated a revaluation of several fundamental and fabrication related issues for high current density operation of the sub-micron sized junctions.
A new circuit fabrication technology for superconducting electronics circuits is discussed in deliverable **D4.2.2**. This report descripts process benchmarks and design rules for the new Nb/Au/YBCO junctions. For many applications, Nb based fabrication technologies are a natural choice due to their ability to construct complex circuits containing large numbers of junctions with a high degree of reproducibility. However some alternative materials do provide capabilities not available with the basic Nb based process and the fabrication of Josephson devices can also provide a deeper understanding of superconductivity itself. The unconventional electronic state of YBCO enables one to construct devices with a built in π phase shift which allows one to construct novel and gives rise to ways of designing circuits. In particular, in collaboration between the University of Twente and University of Ilmenau, loops which spontaneously generate flux were incorporated in a toggle flip flop as memory storage elements. The first collaboration was a study of the fabrication process for Nb/Au/YBCO junctions using RHEED and the second was the development of a technique for investigate the current-phase relationships.

WP5: Project Management
The project web page (www.s-pulse.eu) was used as communication platform to distribute documents between the project partners. Especially for the preparation of the European Roadmap of Superconductor Electronics (D1.3.1 and D1.3.2) this was a very helpful tool.
The first Review meeting on March 13th 2009 in Frankfurt Airport Centre has been organized by the coordinator. The reviewer gave some important comments and suggestions to improve the project work. His main remark was that involvement of industry is still missing. As reaction to this hint a special meeting concerning industry involvement took place in Frankfurt on June 4th, 2009.
Subsequently to the symposium EUROFLUX 2009 in Avignon (D2.1.2) the second General Assembly of the S-PULSE project took place. There was stated that all activities are as scheduled in the project plan.
Further, WP5 includes the preparation of the second review report on the status of the project (**D5.3**; this report). The project management has been resulted in a successful second project period.