Publishable summary

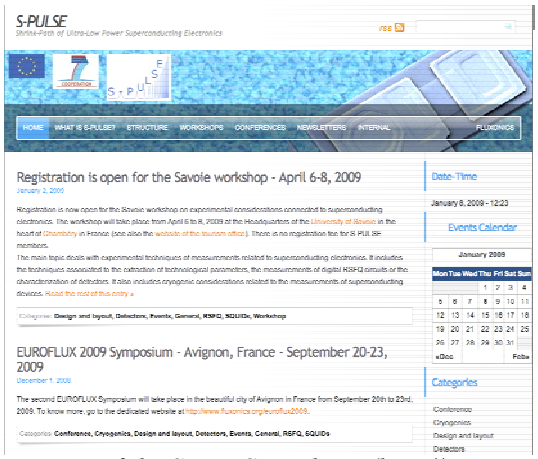
This Support Action - the FP7 project **S-PULSE -** has been established in order to prepare Superconductor Electronics (SE) technologies for the technology generation beyond the CMOS scaling limits. In the field of logic operations, Rapid Single Flux Quantum (RSFQ) circuits are the technology with the lowest risk. The advantages of superconductive digital electronics (SDE) are a very low on-chip power consumption in combination with data and signal processing rates that are an order of magnitude higher that those of semiconductor technology. All essential circuit elements of SE have been developed and demonstrated, but so far not implemented in industrial applications. The unprecedented potential of SE for the requirements of the future information and communication society can only be exploited if the economical impact of superconducting technologies in Europe is strengthened. S-PULSE supports joint efforts of European academic and industrial groups in the superconducting technologies field. This Support Action strengthens the vital link between research and development on the one hand and industry on the other hand. It unites industrial expectations, visionary extrapolation, and the current status of technology. It improves the image of SE and aims to push SE technologies out of their niche as a successful but alien technique. It advances the exchange of knowledge and ideas, takes charge of education, and wins public interest. These goals will be achieved by knowledge dissemination with particular attention to inspire industrial interest, to assess application fields for SE, and to prepare a European Roadmap for SE. The project will maintain regular contacts with representative partners from industry and thereby encourage a possible implementation of an industrially guided European Technology Platform (ETP) at the end of the project.
The S-PULSE project consists of five work packages:

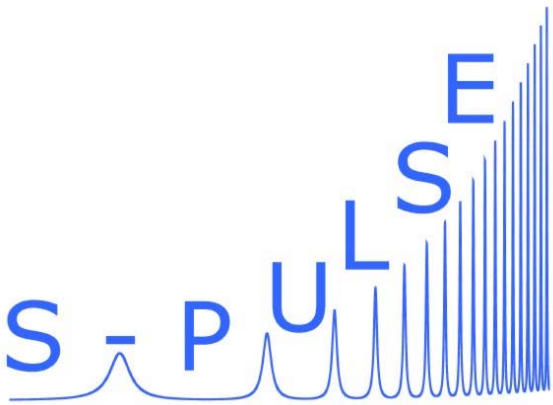
- WP1: Strategic work towards the industrial visibility of SE
- WP2: Seminars, workshops, training summer schools and conferences
- WP3: International visibility and dissemination of European SE
- WP4: Fundamental aspects of Josephson-junction technologies with nanometer dimensions
- WP5: Project Management

WP1: Strategic work towards the industrial visibility of SE
Prior to the creation of a European roadmap for SE, which is an integral part of the S-PULSE Support Action, the beginning of the road must be established. We begin this task by an assessment of international RSFQ activities (deliverable **D1.1.1**). The recent progress attained by Japanese groups in fabrication technology and circuit design for superconducting electronics is very impressive. Cryo-cooled systems with a high-speed I/O interface and a multi-chip module carrier, a wide-band hybrid ADC system, and the CORE1 microprocessor demonstrate the capability to solve technical issues. The availability of the worldwide most advanced foundry process for digital superconducting electronics, the mature level of a digital cell library and the automatic integrated circuit design based on hardware description languages open the way to quantum electronics engineering in the near future. A second report (deliverable **D1.2.1**) was about the SE potentials in telecommunication and scientific satellites, target mission description and associated specifications.
Based on the current 'SCENET roadmap for superconductor digital electronics' (published 2006), a **European roadmap for SE** will be prepared. The information content will be comparable to the 'International Technology Roadmap for Semiconductors' (ITRS) and will show our vision on future developments of SE. Special emphasis will be put on the further 'shrink path' towards nanoscale dimensions of the circuitry. The information will be assembled in cooperation with all relevant research laboratories and industries in Europe. At the **two roadmap meetings** in 2008, the document structure, the responsibilities of the sections, and a first timeline of the roadmap were established. Also, the first text components, tables and pictures were discussed. To obtain a more general view, European experts that are not participating in S-PULSE were invited as well.

WP2: Seminars, workshops, training summer schools and conferences
Before the start of the S-PULSE Support Action, the cooperations in SE were conducted mostly on a national or bilateral level. With S-PULSE, we are now able to strengthen the SE community on a European level. To achieve this purpose, in the WP2 a series of seminars, workshops, and conferences are to be organized. During the first project period the following events took place. The *Twente Microcooling Workshop* (**D2.2.1**) about micro-cooling and scaling laws was held at the University of Twente, The Netherlands on April 7th and 8th with 25 participants from industry and SE community. The *First Karlsruhe Detector Workshop* (**D2.2.3**) about radiation detectors at the quantum limit took place in Karlsruhe, Germany from May 5th to 7th with 35 participants. The *5th FLUXONICS RSFQ Design Workshop* (**D2.3.1**) was held from June 29th to July 2nd in Ilmenau, Germany with 25 participants. The *First S-PULSE Jena Technology training Workshop* (**D2.3.2**) took place in Jena, Germany with 27 participants. The major event for this work package was the conference *EUROFLUX 2008* (**D2.1.1**) about SE circuits in Naples, Italy from September 29th to October 1st with 70 participants. During these five events, the participants from both European and non-European countries were able to broaden their knowledge on SE while attending the presentations and involving in lively discussions.

WP3: International visibility and dissemination of European SE
To enhance the visibility by the public and to facilitate the communication between project partners, a website dedicated to European SE has been set up (http://www.s-pulse.eu). This website is a basic platform for the coordination of all project management tasks (see **D5.1.3**). Apart from freely accessible contents, the website contains internal restricted pages plus a server to upload and manage S-PULSE documents. A first newsletter (see **D3.1.1**) has been distributed throughout the Support Action, an S-PULSE logo has been created (see **D5.1.5**), and an S-PULSE calendar has been assembled.





Left: Homepage of the S-PULSE website (http://www.s-pulse.eu) - Right:S-PULSE logo, showing a train of quantized-area pulses whose height increases with time, to express the expected increase of speed and performance of superconducting electronics.

Several decisions have been made that affect the cooperation and conversation with other European and international bodies concerned with superconductors (see **D3.3.1**). Among these actions is an agreement that the board of the European Society for Applied Superconductivity (ESAS) must in the future include more candidates of the Superconducting Electronics community. To further strengthen the influence and visibility of the Superconducting Electronics community, the European Conference on Applied Superconductivity (EUCAS) in 2011 will be organized together with the International Superconductor Electronics Conference (ISEC). To embed European Superconducting Electronics in the international community, a workshop with partners from the US was organized in the summer of 2008 in Brussels.

Front pages of the first S-PULSE newsletter and of the S-PULSE 2009 calendar

Four project partners have been appointed to be responsible for e-learning activities in the field of SE. A first abstract for a future e-learning project has been prepared and is to be submitted to FP7 (deliverable **D3.4.1**). Related actions will be pursued in 2009.

WP4: Fundamental aspects of Josephson-junction technologies with nanometer dimensions

The $Nb/Al_2O_3/Nb$ junction technology, which requires cooling to around 4 K, is suitable for the fabrication of SFQ/RSFQ circuits with a complexity of up to several thousand gates per chip. High-T_c technology, permitting the operation at 30 to 40 K, may be used only for SFQ circuits with junction counts below about 50, such as for example samplers.

The WP4.1 is a study with preparatory technical support. This feasibility study of niobium-based RSFQ technology with reduced line width of the Josephson junctions is under development. The current European technology is limited by a minimum line width and an overlap of 2.5 micrometer.To achieve reduced specifications with a minimum line width of 0.8 micrometer and an overlap of one micrometer, the lithographic process has been transferred from a mask aligner (direct printing) to a wafer-stepper (reduction of the features on the photo-mask by a factor of five). This advanced process has so far been implemented for the SQUID process, which is less complex than the highly integrated RSFQ process and therefore better suited for the early stages of this study. The optimization for low parameter spread and high yield is in progress. Based on the results, RSFQ test circuits will be designed together with the Ilmenau University of Technology. The knowledge gained from these RSFQ circuits will allow studying the potential use of sub-micrometer Nb/Al junction technology for superconducting electronics.

The WP4.2 investigates the ultimate physical dimensions of SE circuit elements. This work is in progress under the lead of the University of Cambridge.

WP4.3 is a study about possibilities for efficient cryo-packaging for SE in cryo-coolers with rated shielding capabilities. SE circuits are usually cooled with liquid helium for laboratory experiments. However, reliable SE circuit operation inside a mechanical cryo-cooler is a prerequisite for widespread industrial acceptance of superconductor electronics. A cryo-package that allows reliable, repeatable mounting of such SE circuits in a cryo-cooler while providing sufficient magnetic and noise shielding, good thermal contact to the cold finger, and stabilisation against thermal oscillations is an integral part of such a system. This study includes preparatory technical support. The investigated RSFQ circuits have been fabricated at IPHT Jena. The study was about the cryo-package for the operation of these RSFQ circuits in cryo-coolers. The results have been summarized as a report (**D4.3.1**).

WP5: Project Management

The project was introduced to the SE community by an announcement on IEEE (**D5.1.1**) and by an article (**D5.1.2**) on a public superconductor platform. The organisational structure of the project has been defined at a first general assembly in Frankfurt (Germany) on January 24, 2008. Following this kickoff meeting, the consortial agreement was negotiated. Communication with the Consortium members is realized through several channels. A web domain has been reserved and a web page (**D5.1.3**) has been set up (www.s-pulse.eu) as part of WP3. The web site comprises of an external part for the information of the general public as well as an internal part where documents like the grant agreement, the consortial agreement, and the protocols of all meetings are archived. A project presentation as powerpoint file is available on the server so that any project member may disseminate its contents freely (**D 5.1.5**). Further, WP5 includes the preparation of the Review report on the status of the project (**D 5.2**; this report). The project management has been resulted in a successful first project period.

Conclusion

The Support Action S-PULSE has been active in its first 12 months in the areas of the assessment of international RSFQ activities and the cooperation with other European and international bodies concerned with superconductors. The national activities in the field of Superconducting Electronics prior to the Support Action have been integrated on a European level by means of seminars, workshops, and a conference. To increase the visibility of the Support Action and Superconducting Electronics, a website has been established, a newsletter and a calendar have been prepared, and discussions about an e-learning project have started. The envisaged European roadmap for SE is under preparation. Technical support concerning the fabrication of circuits with reduced line width and the operation of RSFQ logic in cryo-coolers is in progress. The project management concludes that a successful first project period has been accomplished.