7th RTD Framework Program

REALITY

Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

Contract No 216537

Deliverable D8.5

Dissemination and Use Plan

(second issue, at the end of project)

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The REALITY Consortium consists of:

Interuniversity Microelectronics Centre (IMEC vzw)	Prime Contractor	Belgium
STMicroelectronics S.R.L. (STM)	Contractor	Italy
Universita Di Bologna (UNIBO)	Contractor	Italy
Katholieke Universiteit Leuven (KUL)	Contractor	Belgium
ARM Limited (ARM)	Contractor	United Kingdom
University Of Glasgow (UoG)	Contractor	United Kingdom

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1. Disclaimer

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2. Acknowledgements

The author acknowledges contributions by all work-package leaders of the REALITY consortium.

3. Document revision history

Date	Version	Editor/Contributor	*Comments*
30/09/2010	V0.1	Miguel Miranda	First draft
6/10/2010	V1.0	Miguel Miranda	Final version

4. Preface

The scope and objectives of the REALITY project are:

- Development of design techniques, methodologies and methods for real-time guaranteed, energy-efficient, robust and adaptive SoCs, including both digital and analogue macro-blocks

The Technical Challenges are :

- To deal with increased static variability and static fault rates of devices and interconnects.
- To overcome increased time-dependent dynamic variability and dynamic fault rates.
- To build reliable systems out of unreliable technology while maintaining design productivity.
- To deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.

Focus Areas of this project are :

- “Analysis techniques” for exploring the design space, and analysis of the system in terms of performance, power and reliability of manufactured instances across a wide spectrum of operating conditions.

- “Solution techniques” which are design time and/or runtime techniques to mitigate impact of reliability issues of integrated circuits, at component, circuit, architecture and system (application software) design.

The REALITY project has started its activities in January 2008 and is planned to be completed after 30 months. It is led by Dr. Miguel Miranda of IMEC. Five contractors (STM, ARM, KUL, UoG, UNIBO) participate in the project. The total budget is 2.899 k€.

5. Abstract

The goal of this document is to provide the details regarding the deliverable “D8.5 Dissemination and Use Plan (DUP)” for the REALITY Project (IST-216537) at the end of last reporting period.

The DUP aims at describing the planned strategy for the internal and external dissemination of the project’s objectives and also at stating a preliminary approach to the market analysis and exploitation of the REALITY project’s results and outputs.

The DUP is conceived in conjunction with all the Consortium partners in order to give way to the most effective strategy and to obtain the highest return in terms of mass-knowledge on the project’s topics and of economic gain. This deliverable in particular, addresses specific dissemination actions and proposes an approach to the future exploitation of the REALITY project results and outputs.

This document is issued in the third year (M32) close to the project end date and it summarizes the dissemination and use strategy. It also provides a more in depth analysis of the valorisation and use case scenarios.

After an introduction to the general aims of the dissemination and preliminary exploitation planning, D8.5 is subdivided into two main sections. The first chapter offers a detailed description of the dissemination activities performed and planned for promoting and spreading the REALITY results among and to the international academic and industrial organizations. The second chapter provides an overview of the exploitation possibilities from the viewpoint of our industrial parents.

Within the REALITY consortium all partners contribute to a large extend equally to the dissemination of the project results.

IPR, Access rights and licensing have been made explicit and described in an elaborate way in the Consortium Agreement which was signed by all consortium partners.

6. Introduction

The REALITY project has started its activities in January 2008 and has completed after 32 months. It is led by Dr. Miguel Miranda of IMEC. The Project Coordinator is also Dr. Miguel Miranda from IMEC. Five contractors (STM, ARM, KUL, UoG, UNIBO) participate in the project. The total budget is 2.899 k€.

This FP7 funded project is the base for collaboration between major industrial players in this field, research institutes and academic partners: ST, ARM, University of Glasgow, University of Bologna, KU Leuven and IMEC.

The selected target test vehicles for REALITY project comes from the two industrial partners: ST and ARM.

The “REALITY” project activity provides solutions for coping with variability and reliability issues that occur when scaling to and beyond the 32 nm technology node. A system-level solution is provided by focusing on two main axes: Analysis Techniques and Solution Techniques.

7. Dissemination Activities

7.1. Dissemination Strategy

The dissemination ensures the spreading of the project's outcome among other industrial and academic organizations so that the methodologies and tools developed can be used in these sectors.

This objective has been achieved by using multiple different strategies.

In general terms, the dissemination of the REALITY project adopted the following principles:

- Dissemination of project results to the international research and design community, which is a crucial aspect for the effective exploitation of the project results in the community and outside the consortium. This objective has been achieved through tge many scientific publications, participation to conferences, and the maintenance of the project website.

- The organizations of training actions/workshops has complemented and strengthen the dissemination. The mobilization of resources of REALITY (most of which invested in R&D activities) coupled with the expertise of the partners involved, have guaranteed that innovative technologies in the area of reliability and variability have been created during the execution of the project.

- The dissemination of project results by the consortium partners as well as by the broader community of designers vary depending on the specific technological results obtained in REALITY and the specific business segments addressed by the partners. Dissemination opportunities have been created though by advertising to the right audience and communities.

7.2. Internal Project communication / dissemination

7.2.1. **Internal website and wiki**

At the start of the REALITY project, IMEC has created and hosts an internet website (www.fp7-reality.eu) which is up and running since April 2008. The goal of this site has been to share research results among the general public and enhance the visibility of the research activity. A wiki (http://www-micrel.deis.unibo.it/~reality/wiki/index.php/Main_Page) has been setup by the University of Bologna. The primary goal of the wiki is to stimulate the effective communication within the project consortium. It is also intended as a way to limit the circulation of files and paper as much as possible.

The REALITY consortium registered and acquired the right to use an ".eu" domain name for the project website : www.fp7-reality.eu

During the course of the project, the REALITY website contents will be progressively enriched in order to provide an up-to-date view of the research progress.

Access to the wiki is password protected and meant for keeping internal project data like:

- action trackers
- confidential presentation material
- risk management plan and updates
- document templates
- deliverables (non public), and related draft work documents
- scientific reports, in case they are for restricted use
- communication lists

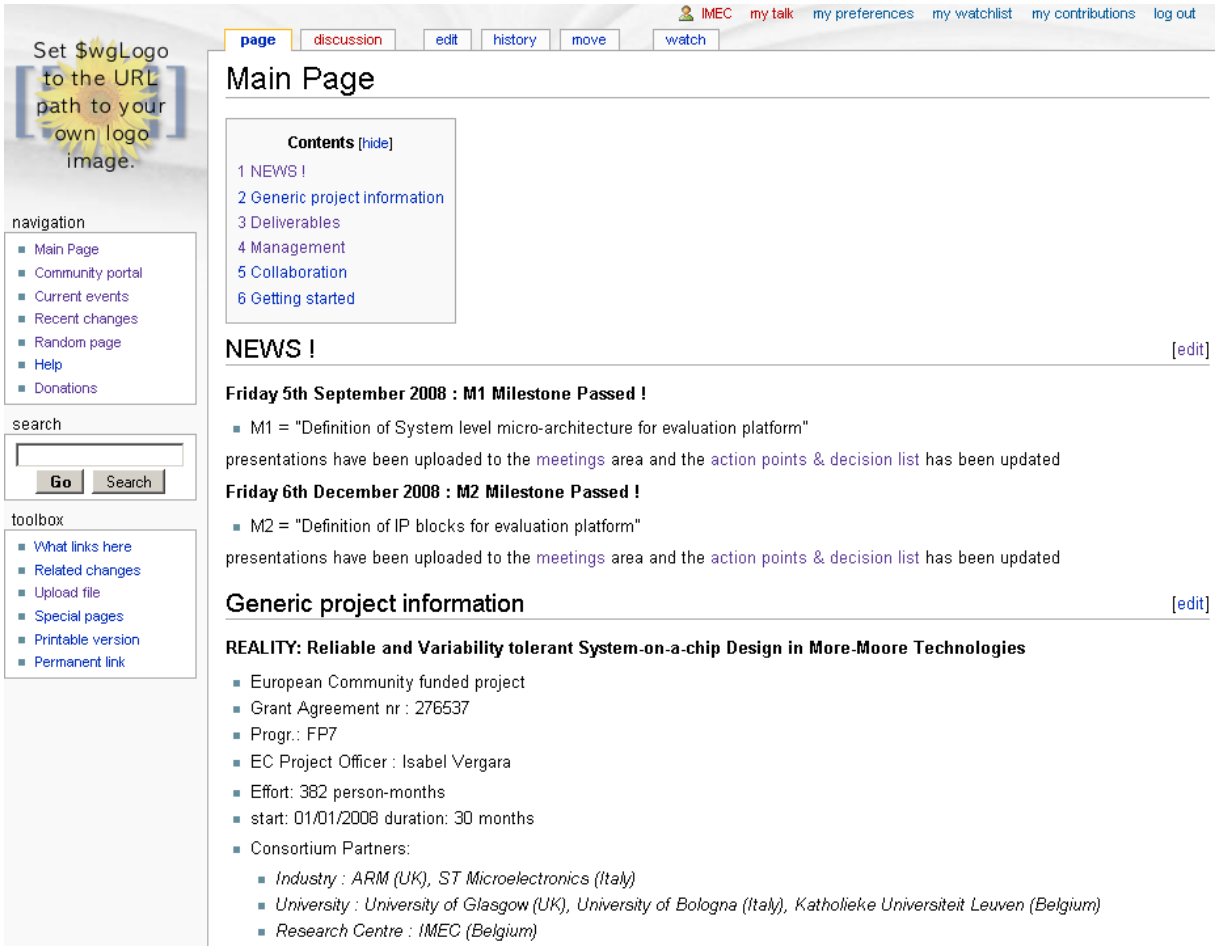

Figure 1: Screenshot of the wiki page for internal communication purposes

The contents and objectives of the public website can be found below.

7.2.2. **Project meetings**

Face to face project meetings with having all consortium partners to join, have been held each six months approximately. A fixed item on the meeting agenda has been a brief status review by each of the individual consortium partners on their realized and planned dissemination activities. Also the inventory and outlook for new scientific publications in the past and next half year was shared. Finally, tactics and approach towards dissemination of the potential project results to industrial companies outside the consortium were discussed. In this way a close monitoring of the joint dissemination activities were realized as well as the possibility to anticipate to the definition and fine-tuning of near term actions.

Besides the regular consortium meetings, another path that the consortium followed was the internal scientific dissemination. This action aimed at exploiting the REALITY results towards the academic consortium partners in order to advance relevant research in the

corresponding laboratories of these academic partners and to support their teaching activity through enrichment of the relevant courses or the introduction of new ones.

7.2.3. **Communication list**

An integral part of the project management has been team organization and communication. The REALITY project team has setup a simple but effective communication list which features all the team member names, their role in the project or function, and their coordinates.

This communication list has been updated and reviewed on a regular base, typically each month.

The use of this list obviously enables proper communication among the consortium and to the relevant stakeholders. More importantly it makes sure no valuable information gets lost, stakeholders are informed about project events and the persons responsible for dissemination are clearly identified.

The communication list is available to all the partners via the project wiki page.

7.3. External communication / dissemination

7.3.1. **Public Web site**

The www.fp7-reality.eu website contains also a Public area that is the official homepage of the project and that serves as a public repository for all project related information.

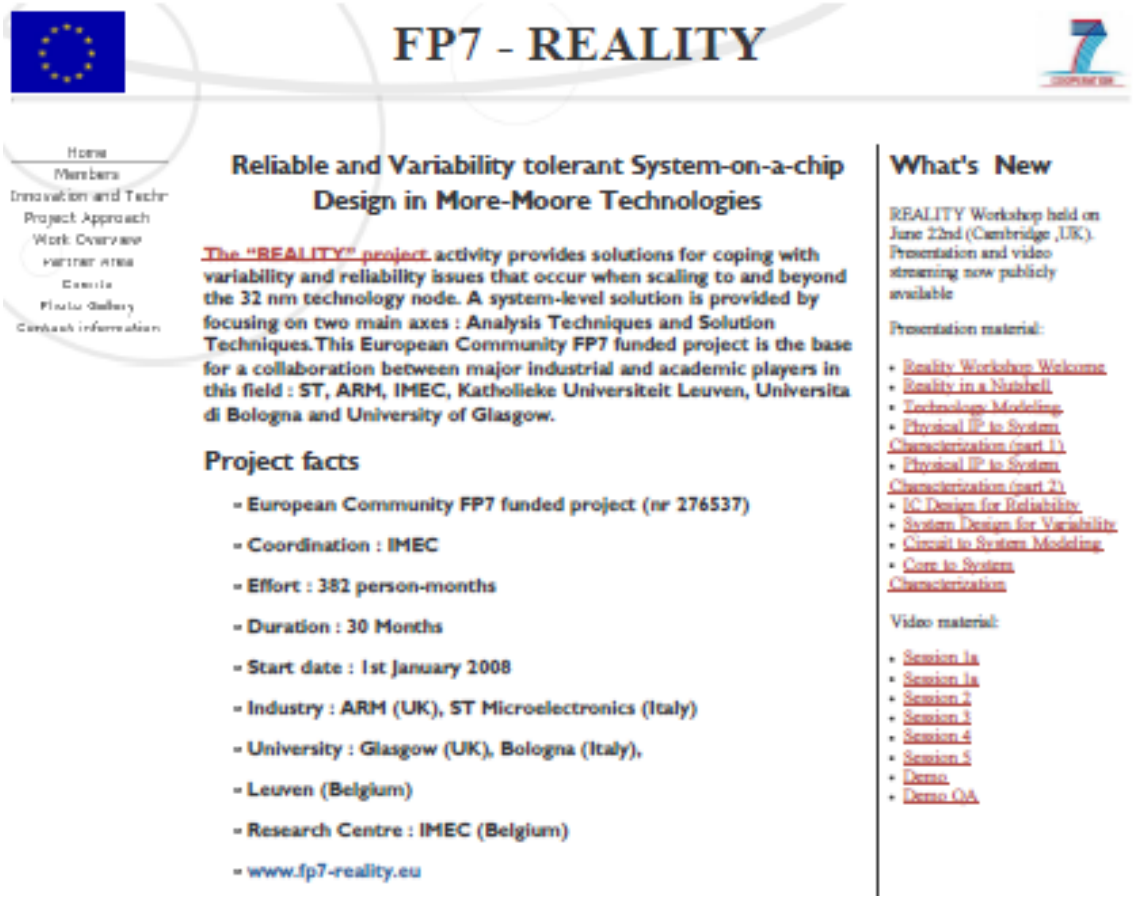

Figure 2 : Recent screenshot of the REALITY web homepage

The web site gives interested users access to a number of public pages providing a description of the project objectives, news, announcement of upcoming events, links to exhibitions where the REALITY project will be represented, contact information and reports or specifications.

Figure 2 provides a recent screenshot of the REALITY web site. In the public area (upper corner at the right hand side) it is clearly visible the announcement of the REALITY workshop held during June 2010 was participants could get access to the latest results of the project. In the same area we make accessible the material presented at the workshop to the public.

The www.fp7-reality.eu website contains a statistical monitoring function which allows the host to analyse the website traffic. In the course of the project it will help the project team to gain a better view of the interested audience and fine-tune the available information and contents of the website.

Relevant information which is monitored :

- traffic tracking
- amount of page views
- visitors and their geographical location (country of origin)
- the way visitors came to the site
- comparison of traffic per month and intensity

7.3.1.1. Statistical information

This statistical information can be accessed at all times via the following link: http://webstats.motigo.com/stats?AETKZALB7G6GmCZQTm2KB0i8F7cQ

Access statistics of the web site are as follows: The statistics demonstrating the total accesses of the REALITY website have been marked since the 22nd of April 2008, and especially after the first ten days of the website's settlement and functionality. The statistics are based on ***Motigo Webstats*** (http://webstats.motigo.com). The Motigo Webstats engine is employed to let the external visitors of the Website have access on the visits and the access rates of the website and has been chosen, because, it does not require that the visitor has any username and password in order to demonstrate the web statistics.

In this report, the statistics of the REALITY website accesses are obtained from ***Motigo Webstats*** engine and they are demonstrated below, in the following figures. The reporting period relates to January 1st 2009 till August 30th 2010. Records previous to June 2008 have been provided in the first issue of this report (deliverable D8.3).

7.3.1.2. Extra statistical information

In the two following figures, the screenshots of Motigo Web pages for the REALITY website are shown, for the duration of the reporting period. These figures are given to demonstrate the format of these Web tracking engines and the way of showing the information about the web accesses of a certain website.

Country of origin

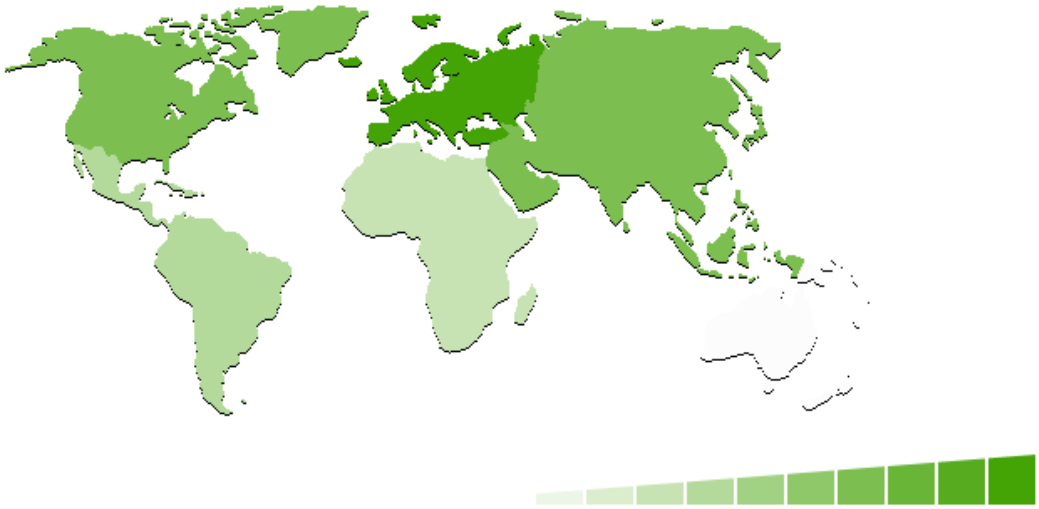

Figure 3: Overview of worldwide website traffic

Figure 4: Table pie of website traffic per continents

1.	Belgium	142	32.3 %
2.	United Kingdom	93	21.2 %
3.	France	31	7.1 %
4.	Italy	31	7.1 %
5.	United States	28	6.4 %
6.	Germany	16	3.6 %
7.	Spain	13	3.0 %
8.	Netherlands, The	12	2.7 %
9.	India	11	2.5 %
10.	Greece	6	1.4 %
11.	Japan	5	1.1 %
12.	Cyprus	5	1.1 %
13.	Singapore	5	1.1 %
14.	Slovakia	4	0.9 %
15.	Korea	4	0.9 %
16.	Sweden	3	0.7 %
17.	Brazil	2	0.5 %
18.	Switzerland	2	0.5 %
19.	Romania	2	0.5 %
20.	Mexico	2	0.5 %
21.	Canada	1	0.2 %
22.	Croatia (Hrvatska)	1	0.2 %
23.	Liechtenstein	1	0.2 %
24.	Puerto Rico	1	0.2 %
25.	Ireland	1	0.2 %
	The rest	17	3.9 %
	Total	**439**	**100.0 %**

Table 1: Overview of traffic in specific countries worldwide

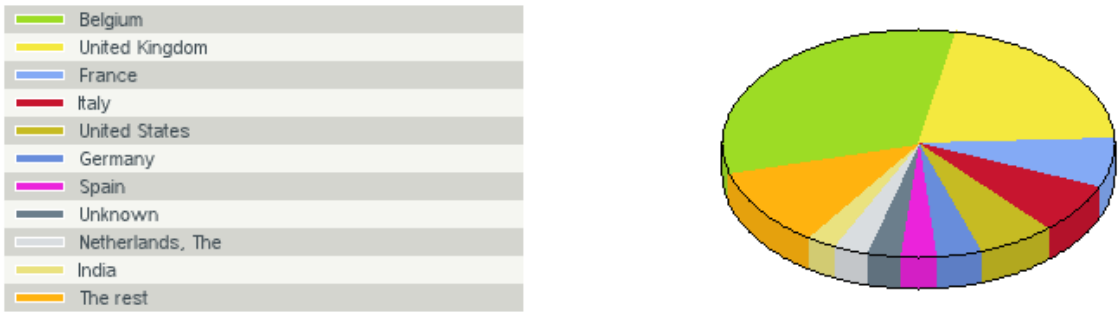

Figure 5: Table pie of website traffic worldwide

The statistics information given in this paragraph includes the most prevalent metrics, which could let someone have a clear enough picture of the total visit rate during the years 2009 and 2010. The Web tracking engine installed on the website derives several other metrics and features.

On request, this information can be delivered to the REALITY Consortium partners via the common communication channels (via email, wiki or website)

7.3.2. **Promotion at exhibitions and conferences**

During the first reporting period a multitude of occasions were exploited with the aim to make the start of the REALITY project public and to explain the target objectives to the general public. These actions are a part of a broader dissemination strategy.
The path which was rolled out by the consortium is a mix of dedicated promotion activities combined with key note lectures and presentations at renowned conferences.
The result is clear: the presence of the REALITY project team was observed by a broad audience both general public and specialists. This yields a number of contacts showing interest in the REALITY research topic. On top of this, the start of the REALITY project has been picked up by the press resulting in a variety of press articles.

Exhibitions and conferences fulfil a complementary role as a fast medium for diffusion of results. All the REALITY consortium partners have definitely continued during the reporting period joining exhibitions and with technical presentation as much as possible in order to show the benefits of the developed methodologies and tools with presence at key European Conferences such as DATE.

The Design, Automation, and Test in Europe (DATE) conference is one of the worlds premier conferences dedicated to electronic and embedded systems. It was held at the Acropolis Centre in Nice, France during 20-24 April 2009 and at the International Congress Centre in Dresden, Germany during 8-12 March 2010.

DATE is sponsored by the European Design and Automation Association, the EDA Consortium, the IEEE Computer Society : (TTTC), (CEDA), ECSI, RAS and ACM SIGDA.

7.3.3. **Organization of training - workshops**

The organization of training - workshop actions complements and strengthens the dissemination. The mobilization of resources of REALITY (most of which will be invested in R&D activities) coupled with the expertise of the partners involved, guarantees that innovative technologies in the area of the REALITY project will be created during the execution of the project.

7.3.3.1. DATE 2010 Workshop: The Fruits of Variability Research in Europe

With respect to the REALITY FP7 project, a workshop was organized at DATE conference 2010. The conference is sponsored by an impressive list of industrial companies and was an excellent opportunity to disseminate results from the REALITY project to the public and in specific to the representatives of the industrial companies active in this domain.

Overview of this workshop

This workshop is prompted by the confluence of a recent upsurge in academic interest in the area (for instance, after a special session flagging variability at the 2007 VLSI Technology Symposium, the coverage of variability and associated reliability jumped from a single session in 2008, to three sessions in 2009), significant political backing (Dr Georg Kelm, EU Head of Sector Information Society and Media, is quoted as saying “this is an area of great success for Europe where national and EU funding complement each other”), and because of the presence of a number of EU and UK consortia involved in grants in the area, either starting or presently producing results:

2007-10 The UK EPSRC (gow.epsrc.ac.uk/ViewGrant.aspx?GrantRef=EP/E003125/1) design for variability project (Glasgow, Manchester, Southampton, York, Edinburgh Universities)
2008-10 REALITY FP7 STREP (www.fp7-reality.eu) on the impact of variability on design (IMEC, KU Leuven, Bologna, ARM, ST)
2009-11 EU ENIAC MOdeling and DEsign of Reliable, process variation-aware nanoelectronic devices, circuits and systems (29 EU partners)

Specifically the Workshop covered recent significant results from EU projects and pointed to future research directions. I featured a keynote talk from one of the recognised experts in the field from Asia, and then sessions on: the measurement, simulation and modelling of device variability in today's and end-of-roadmap devices; progress in simulation tools to analyse the effects of device variability on circuit and systems level manufacturability, design, reliability and circuit performance; techniques for creating variability-resilient solutions in circuit and systems design. Also a Poster session, running during coffee and lunch breaks, that gave attendees a focal point for sharing new developments in the field, and future aspects of variability and reliability research and knowledge transfer were discussed in a concluding think-tank session.

Figure 6 shows a snapshot of the DATE 2010 web site announcing its workshop on "The Fruits of variability Research in Europe".

Figure 7 shows the program of the workshop featuring five out of nine speakers who are active team members of the REALITY project, covering different topics of our project: from statistical variability and reliability aware device modelling to system level variability aware design and analysis.

Figure 6 Snapshot of the DATE 2010 web site announcing its workshop on "The Fruits of variability Research in Europe"

Workshop structure:

Session 1 – Perspective	
09:00	Keynote: Toshiro Hiramoto (University of Tokyo) *Variability research: accomplishments and future directions – a Japanese perspective*
10:00	Asen Asenov (Glasgow University) *Device variability and reliability: towards the end of the roadmap.*
10:30	Coffee & Poster Session
Session 2 – Simulation strategies and tools	
11:00	Scott Roy (Glasgow University) *Statistical compact model strategies: efficiently bridging the gap between devices and circuits.*
11:30	Miguel Miranda (IMEC) *Hierarchical, variability aware circuit and system simulation.*
12:00	Lunch
Session 3 – Solutions	
13:00	Andy Tyrrell (University of York) *Evolutionary algorithms as an aid to synthesis in the presence of variability.*
13:30	Georges Gielen (Katholieke Universiteit Leuven) *Variability and degradation resilient analogue and digital circuit design: techniques and solutions*
14:00	Luca Benini (DEIS Università di Bologna) *System-level variability countermeasures in many-core computing - a vertically integrated view*
14:30	Coffee & Poster Session
Session 4 – The Future	
15:00	Steve Furber (Manchester University) *SpiNNaker: a large scale SoC design as a test vehicle for variability modelling*
15:30	Enrico Macii (Politecnico di Torino) *MODERN, a European flagship project in variability and it's impact on design –overview and goals*
16:00	Panel Discussion *Variability research: Our place in the world? Where next?*
17:00	Conclusions

Figure 7 Description of the program of the 2010 DATE workshop on "The Fruits of Variability Research in Europe" featuring five out of nine speakers who are active team members of the REALITY project, covering different topics of our project.

A complete overview of this workshop can be found at http://www.date-conference.com/date10/conference/date10-workshop-W2

7.3.4. **Promotional Flyer and Bulletin**

A brochure (leaflet) was compiled during the first reporting period containing the key information about the REALITY project: funding, start-end date, consortium partners, objectives, methodologies, benefits and target achievements.
The brochure has been printed and distributed in the different events in which the consortium partners have participated. During the first reporting period the REALITY flyers were distributed at DATE '08 (March 2008, Munich - Germany). During the second and third reporting periods flyers were distributed during the subsequent organizations of such event at Nice in 2009 and Dresden in 2010. In 2010 flyers were also distributed during the

The below figure shows a selected page from the brochure as an example.

Figure 8 : The REALITY Brochure

7.3.5. **Press Releases**

The start of the REALITY project has been noticed and picked-up by the press. Multiple contacts led to several articles. A the end of the project a second press release was lunched reporting the main outcome of the project and this has been widely picked-up by the specialized press. A total number of 19 press release clips echoing the end of project REALITY press release have been identified by October 1st 2010, distributed along the three main continents: Europe, America and Asia. With the large majority of them in them concentrated in the US. This reflects the tremendous impact that the project results of REALITY has had in the electronic industry.

- One example of such a press announcement can be found http://www.eetasia.com/ART_8800621262_480200_NT_af62c44b.HTM

DATE	MEDIUM	TITLE	K	PLACE
21/09/2010	EETimes Europe	REALITY European project concludes after 2.5 years		Belgium
23/09/2010	Industrial Sourcing News	Project maps ARM core variability at 32-nm		Belgium
24/09/2010	EETimes India	IMEC-led project characterizes ARM926 core		India
21/09/2010	Bits & Chips Online	Europees consortium rondt project Soc-variabiliteit af		The Netherlan
21/09/2010	Electronic Specifier	European project solves variability issues of designing in deep submicron IC technology		UK
21/09/2010	New Electronics	Project finds way to avoid variability in 32nm cmos designs		UK
21/09/2010	EETimes News & Analyses	Project maps ARM core variability at 32-nm		US
21/09/2010	Chip design Magazine	REALITY Consortium Solves Deep Submicron Variability		US
21/09/2010	EDA Café	European project solves variability issues of designing in deep submicron IC technology		US
21/09/2010	Newswire Today	European Project Solves Variability Issues of Designing in Deep Submicron IC Technology		US
21/09/2010	Global SMT & Packaging	European project solves variability issues of designing in deep submicron IC technology		US
21/09/2010	Semiconductor Packaging News	Project solves variability issues of designing in deep submicron IC technology		US
21/09/2010	Nanotechnology Now	European project solves variability issues of designing in deep submicron IC technology		US
21/09/2010	IC Market Place	Project maps ARM core variability at 32-nm		US
22/09/2010	Electro IQ (Solid State Technology	IC design project concludes on self-adaptive system on chip: Discoveries summarized		US
24/09/2010	Nanotech Wire	European project solves variability issues of designing in deep submicron IC technology		US
21/09/2010	PR ZOOM	European Project Solves Variability Issues of Designing in Deep Submicron IC Technology		US
21/09/2010	Nanowerk	European project solves variability issues of designing in deep submicron IC technology		US
22/09/2010	EETimes Asia	"Reality" project characterizes ARM926 for inherent variability at 32nm		Asia

7.3.6. **Cross reference promotion**

- **Cross reference promotion within the REALITY consortium**

In order to increase the visibility on the ongoing project research work as well as to increase the traffic to the REALITY website, consortium partners have setup a link from their own website to the project website. In addition to these references, links from other project websites where the REALITY consortium partners participate in have been made to the REALITY URL (e.g. http://www.nanocmos.ac.uk/essderc/). Where ever possible the REALITY project URL is mentioned in publications, reports and conference presentations.

A search at Google yields :

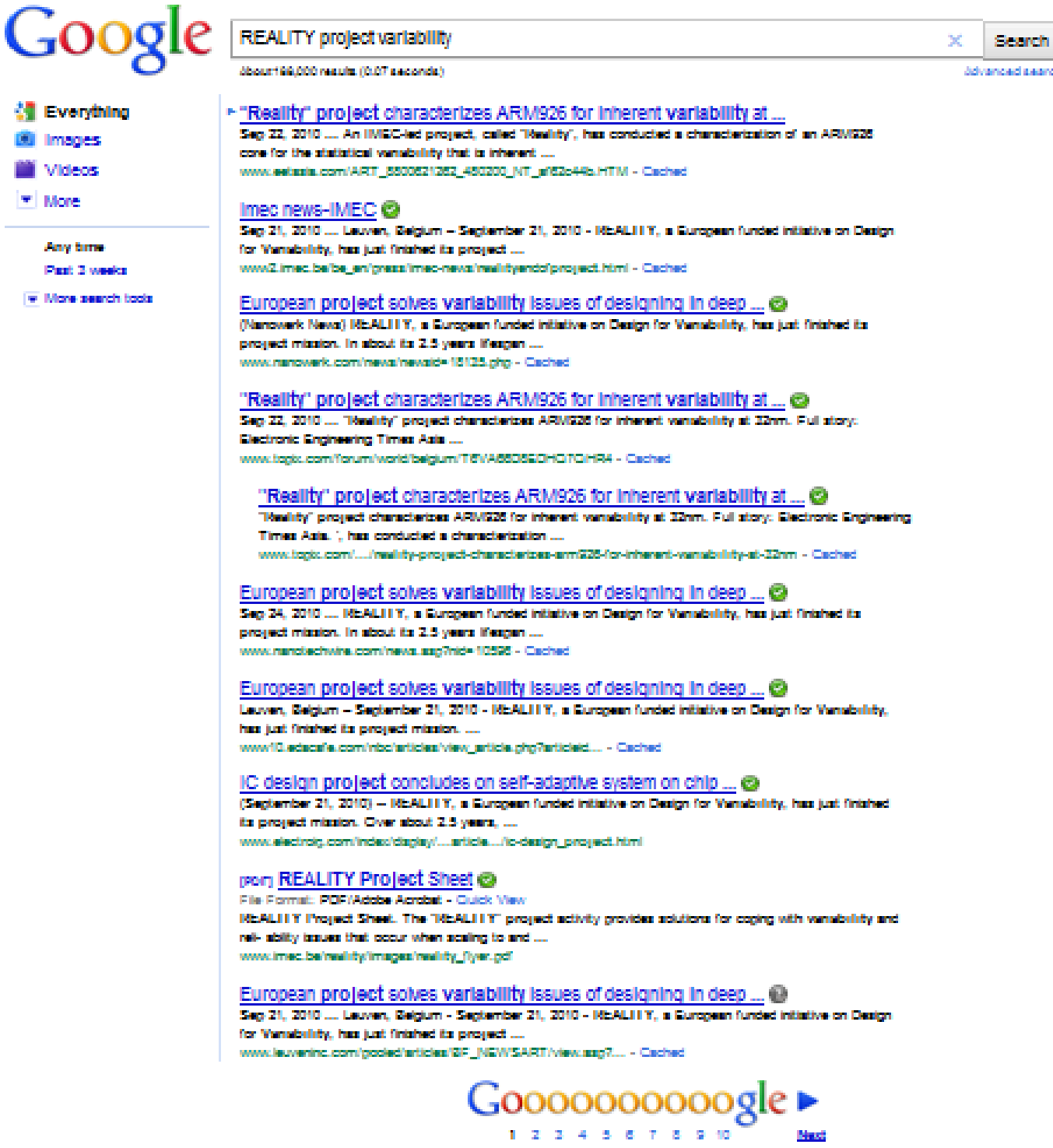

Figure 9 : Cross reference promotion inside & outside the REALITY consortium

The acronym REALITY is a common English word. To maximize the search results, the term "variability project" has to be added. The use of non-existing words as acronym would raise the number of relevant search results. This is an interesting fact for future European projects.

- **Cross reference promotion outside the REALITY consortium**

Clear signs of interest for the REALITY research progress have been shown by other project teams (this was very clear during the setup of new projects in this area, e.g. ENIAC initiatives). The REALITY consortium actively pursues to keep a good relation with these other project teams as it may be a potential channel for dissemination and future exploitation. Running activities in this area will be elaborated further in the next reporting periods.

7.4. Scientific dissemination

One of the main vehicles for diffusion of research results is, obviously, to publish in outstanding journals and conferences in the field of interest, appropriate presentations and publications will be encouraged to ensure wide visibility of the project results.

The partners promised to publish papers in conferences and journals of the related field. This promise has been kept. In addition several team members have been invited for keynote speeches and presentations on the topics covered by REALITY. The following summarizes the publications obtained

7.4.1. **Publications in conferences**

Conferences fulfil a complementary role as a fast medium for diffusion of results. A list of the most relevant conferences in the fields of interest for the project includes: DATE, ESSDERC/ESSCIRC, IEDM and IEEE International Symposium on Quality Electronics Design. All these conferences are targeted by all partners in order to show the benefits of the developed methodologies and tools.

- C. Forzan and D. Pandini, “Statistical Static Timing Analysis: A Survey,” Integration, the VLSI Journal, vol. 42, pp. 409-435, Jun. 2009.
- D. Pandini, “Statistical Static Timing Analysis: A New Approach to Deal with Increased Process Variability in Advanced Nanometer Technologies,”
- Intl. Conf. on CMOS Variability (ICCV), May 2009.
- Paul Zuber, Petr Dobrovolny, Vladimir Matvejev, Philippe Roussel and Miguel Miranda, "Using Exponent Monte Carlo for Quick Parametric Yield Prediction of CMOS Circuits under Process Fluctuations", 19th International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS), Springer, 2009
- Miranda Corbalan, M.; Dierickx, B.; Zuber, P.; Dobrovolny, P.; Kutscherauer, F.; Roussel, P. and Poliakov, P., Variability aware modeling of SoCs: from device variations to manufactured system yield, International Symp. On Quality Electronic Design, San Jose, USA, 2009.
- Zuber, P.; Miranda Corbalan, M. and Dobrovolny, P., “Statistical Memory Analysis for SRAM Design”, 2nd IEEE Design for Reliability and Variability Workshop, Austin, TX, USA, 2009
- Francesco Paterna, Luca Benini, Andrea Acquaviva, Francesco Papariello, Giuseppe Desoli, Mauro Olivieri: Adaptive idleness distribution for non-uniform aging tolerance in MultiProcessor Systems-on-Chip. DATE 2009: 906-909
- Francesco Paterna, Luca Benini, Andrea Acquaviva, Francesco Papariello, Giuseppe Desoli: Variability-tolerant workload allocation for MPSoC energy minimization under real-time constraints. ESTImedia 2009: 134-142
- Root Causes and Impact of Random Variability in Advanced Technologies - Yves Laplanche - ARM Global Engineering Conference - 5-8 May 2009 - Loughborough - UK
- Analyze of Temporal and Random Variability of a 45nm SOI SRAM Cell - Y. Laplanche - International SOI Conference - 5-8 October 2009 - Crowne Plaza Hotel, Foster City, California, USA

- E.Maricau and G.Gielen, "Efficient Reliability Simulation of Analog ICs Including Variability and Time-varying Stress", DATE proceeding 2009.
- E.Maricau and G.Gielen, "A Methodology for Measuring Transistor Ageing Effects Towards Accurate Reliability Simulation", IOLTS proceedings 2009.
- G. Paci, D. Bertozzi, L. Benini, Effectiveness of adaptive supply voltage and body bias as post-silicon variability compensation techniques for full-swing and low-swing on-chip communication channels, in Design, Automation & Test in Europe Conference & Exhibition, DATE 2009.
- Sathanur, A. Pullini, L. Benini, G. De Micheli, E. Macii, Physically clustered Forward Body Biasing for variability compensation in nano-meter CMOS design, in Design, Automation & Test in Europe, DATE 2009.
- Asenov, Variability Headaches in Sub-32 nm CMOS, ECS Trans. Vol. 25, p. 131 (2009)
- B. Cheng, S. Roy, A.R. Brown, C. Millar, A. Asenov, Evaluation of statistical variability in 32 and 22nm technology generation LSTP MOSFETs, Solid-State Electronics, Volume 53, Issue 7, pp.767-772 (2009)
- M. F. Bukhori, A. R. Brown, S. Roy and A. Asenov, Simulation of Statistical Aspects of Reliability in Nano CMOS Transistors, IEEE Trans. Reliability (Accepted)
- E. Maricau and G. Gielen, "Variability-aware reliability simulation of mixed-signal ICs with quasi-linear complexity", DATE, pp.1530-1591, 2010.
- E. Maricau and G. Gielen, "Efficient variability-aware NBTI and hot carrier circuit reliability analysis", IEEE Transactions on Computer Aided Design, vol.29, no.12, 2010.
- A. R. Brown, V. Huard and A. Asenov, “Statistical simulation of progressive NBTI degradation in a 45nm technology pMOSFET”, IEEE Trans. on Electron Devices, Vol.57, No.9 pp.2320-2323 (2010)
- A. R. Brown, N. M. Idris, J. R. Watling and A. Asenov, “Impact of Metal Gate Granularity on Threshold Voltage Variability: A Full-Scale 3D Statistical Simulation Study”, IEEE Electron Device Letters, (in press)
- F. Paterna, A. Acquaviva, A. Caprara, F. Papariello, G. Desoli, L. Benini, “Variability-tolerant run-time workload allocation for MPSoC energy minimization under real-time constraints”, ACM Conf. Computing Frontiers, pp. 109-110 (2010)
- Francesco Paterna, Andrea Acquaviva, Alberto Caprara, Francesco Papariello, Giuseppe Desoli, Luca Benini: Variability-tolerant run-time workload allocation for MPSoC energy minimization under real-time constraints. Conf. Computing Frontiers 2010: 109-110
- Selma Laabidi, Advanced Variability Analysis from devices to systems ARM Global Engineering Conference - 4th-7th May 2010 - Loughborough – UK

7.4.2. **Workshops, seminars, tutorials and Keynotes**

Regarding section 7.3.3, academic project members have made efforts to advance the research in the area in the laboratories of the academic partners (as promised) and beyond. Toward this end, the partners have actively held tutorials and presented keynotes. The following is a list of keynotes and tutorials for the first reporting period:

- Concerning invited presentations, Miguel Miranda, project coordinator gave an overview of the project status of REALITY on his talk: ***Design for Variability Efforts in Europe – REALITY project*** at the 2nd NMI International Conference on CMOS Variability: ICCV 2009, Wednesday, 13th May 2009 in London-UK (http://www.nmi.org.uk/conference/index.html)
- A. Asenov, Statistical variability and reliability in next generation CMOS technologies and the ITRS response. 2nd NMI International Conference on CMOS Variability: ICCV 2009, Wednesday, 13th May 2009 in London-UK (http://www.nmi.org.uk/conference/index.html)
- A. Asenov, Statistical variability: a roadblock to future scaling (How the statistical variability is shaping the ITRS) Proc. INSIGHT 2009, pp 309-316 (2009) Invited
- A. R. Brown, "TCAD simulation of statistical variability" at Workshop on Simulation and Characterization of Statistical CMOS Variability and Reliability, Bologna (September 2010)
- A. Asenov, Modelling and Simulation of Transistor and Circuit Variability and Reliability, IEEE CICC, San Jose (September 2010).
- A. Asenov, Interaction between TCAD, compact models and circuit simulation to support statistical and robust design " at Workshop on Simulation and Characterization of Statistical CMOS Variability and Reliability, Bologna, (September 2010)
- A. Asenov, Advanced Monte Carlo Techniques in the Simulation of CMOS Devices and Circuits, 7th Int. Conf. Numerical Methods and Algorithms, Borovetz, Bulgaria (August 2010)
- A. Asenov, SINANO Summer School, Bertionoro, Italy (July 2010)
- A. Asenov, Statistical variability in conventional and modern CMOS devices 1, UPC, Barcelona (July 2010)
- A. Asenov, Statistical reliability in conventional and modern CMOS devices 2, UPC, Barcelona (July 2010)
- A. Asenov, Statistical Variability and Corresponding Compact Model Strategies, COMON Compact Model Training Course, Taragona (June 2010)
- A. Asenov, Statistical variability and reliability, TSMC (April 2010)
- A. Asenov, Variability Prediction via TCAD Tools, VLSI-DAT Workshop, Taiwan (April 2010)
- A. Asenov, Modelling and simulation of statistical variability in nanometer CMOS technology, AACD'10, Graz (March 2010)
- A. Asenov, Forever CMOS, UKDF, Manchester (March 2010).
- A. Asenov, Statistical variability and reliability: Physical device simulation, statistical compact model strategy, statistical circuit simulation, GLOBALFOUNDRIES, Dresden (March 2010).
- A. Asenov, Modelling perspective of future n-channel high-mobility transistors, ULIS, Glasgow (March 2010)
- A. Asenov, Device variability and reliability: towards the end of the roadmap, DATE, Dresden (March 2010)
- Davide Pandini, Statistical Static Timing Analysis: A New Approach to Deal with Increased Process Variability in ***Europe – REALITY project*** at theAdvanced

Nanometer Technologies, 2nd NMI International Conference on CMOS Variability: ICCV 2009, Wednesday, 12th-13th May 2009 in , London-UK (http://www.nmi.org.uk/conference/index.html) (invited)

- D. Pandini, "Variability in Advanced Nanometer Technologies: Challenges and Solutions," (Keynote Speech) PATMOS, Sep. 2009.
- D. Pandini, "Computing and Design for Silicon Manufacturing," *HIPEAC Cluster Meeting*, Jan. 2009.
- D. Pandini, "Statistical Static Timing Analysis: A New Approach to Deal with Increased Process Variability in Advanced Nanometer Technologies," *Intl. Conf. on CMOS Variability (ICCV)*, May 2009.
- D. Pandini, "Variability in Advanced Nanometer Technologies: Challenges and Solutions," (Keynote Speech) *PATMOS*, Sep. 2009.
- D. Pandini, "Variability in Advanced Nanometer Technologies: Challenges and Solutions," (Keynote Speech) *VARI*, May 2010.
- D. Pandini, "Variability in Advanced Nanometer Technologies: Challenges and Solutions," *SINANO*, Jul. 2010.
- G. Gielen, Elie Maricau, Pieter De Wit, Design for Reliability of Analog Circuits in Nanometer CMOS Technology, Reliability and Design Conf., Stuttgart, 2009 (invited)

7.4.3. **Education**

Again relating to training activities R&D team members have actively been involved in courses related to the topic of the project. The following courses were held by the partners:

IMEC:

- P.Zuber, P.Dobrovolny, M.Miranda IDESA lecture on Statistical SRAM Analysis, May 3rd 2010, IMEC

8. Final Use Plan (exploitation strategy)

The objective of defining the exploitation strategy is to identify the results from the project that can be used or exploited by partners. Therefore, an initial analysis has been assessed on the exploitable results. Based on these results, possible exploitation strategies have been defined. Both the academic and industrial partners have been instrumental in using the methodologies and tools developed during the project course.
On the one hand, the academic partners have been interested in the results of the project because they can use them in a near future to continue some of their active research lines.
On the other hand, the project results have been crucial to asses and improve the design flows and production processes of the industrial partners, since the specific technical area of the project belongs to some of the leading edge business cases of these companies. Finally, the exploitation phase aims to develop and market new design techniques and methods for future SoC's and to use these results in the design flow of the industrial companies resulting in real-time guaranteed, energy-efficient, robust and self-adaptive SoC's.

8.1. Use by industrial partners in proprietary products

The use of the REALITY project results in products will be useful for the major industrial partners in this project: ARM and ST

The participation of STMicroelectronics and ARM to this project was motivated by both the strong impact of the research activities and topics addressed, which are critical for a leading company like ST and a leader in microprocessor Intellectual Property like ARM, and by the outstanding competence and scientific reputation of the participating scientific partners.

The major impact from REALITY has been to develop such tools that on the one hand will link process technology and design and on the other hand will address process issues by offering design solutions.

8.1.1. **ST Microelectronics**

STMicroelectronics has extensive collaborations and links with many CAD and EDA vendors aimed at fostering and improving the design flows deployed within the company to address increasingly more demanding constraints of sub-nanometer design nodes and very large volumes products. Trough these links ST can stimulate the R&D of those tools and design flow providers to focus on the relevant problems and address new methodologies and technologies such as the ones developed within the REALITY consortium.
In order to disseminate the knowledge of the benefits of the REALITY methodologies and techniques, STM will organize internal audits and workshops inviting product architects and designer as well as partners of the REALITY consortium.

Moreover, the design flows and methodologies for statistical timing analysis and variability impact evaluation will be included into the top-down design flow currently used at ST. In particular, the statistical timing analysis tool used in REALITY will be deployed to perform sensitivity-based optimization to reduce the pessimistic design margins that significantly reduce the potential benefits and advantages introduced by technology scaling. The automatic internal standard cell library characterization tool will be extended with the techniques for statistical characterization developed and validated in REALITY, to include the impact of process variations in the characterization of industrial libraries.
Finally, exploiting the variability data and statistical device compact models developed in REALITY, a path ranking based on statistical timing analysis will be generated during sign-off to provide a better correlation with at-speed testing and to improve the parametric yield using the statistical optimization methods defined in REALITY.

In concrete ST has been especially interest on Statistical analysis solutions for random within-die (WID) variations available which today are quite complex for an effective industrial exploitation. In REALITY we demonstrated that Statistical Static Timing Analysis (SSTA) is a good estimator of random WID variations, but in general, it lacks ease of deployment in an industrial environment, and requires a lot of efforts to characterize the statistical libraries, as it was demonstrated by means of the work carried out in WP2. Moreover, it is also true that chip designers in an industrial environment, who have to satisfy tough turn-around-time requirements, and have to meet strict time-to-market windows dictated by an increasingly fierce competition, do not want to change the traditional sign-off methodology for timing verification based on Deterministic Static Timing Analysis (DSTA). Therefore, it is necessary to develop a rapidly deployable solution based on existing and reliable commercial CAD tools and on an industrial digital design flow, which also uses industrial models to reduce the impact of random intra-die variations at the cell level. Moreover, it is necessary to define the basic set of process parameters to effectively characterize the standard cell libraries, thus drastically reducing the library statistical characterization runtime These two critical issues were addressed in REALITY at ST, and practical methodologies and design flows based on the research activities carried out in REALITY work packages were developed and are currently exploited at ST.
From a system design perspective, the technologies developed by REALITY can be key to achieve the goal of meeting the worst case constraints associated to both performance and reliability of complex products; such as the ones designed for advanced consumer multimedia chips. Consider for example the cost associated to worst case design margins in complex multimillion cells designs; the variability analysis flows provides by REALITY for both memories and cores allow relaxing of constraints while at the same time the deployment of SW/HW countermeasures can significantly reduce the energy consumption level while guaranteeing or improving the expected quality of service in many cases; as illustrated by the test cases in the previous section of this report.
Another key aspect from a system architecture standpoint is the ability to predict QoS, Power and to some extent yield for aged conditions and the overall system effects of aging for a specific application or product.

Statistical Characterization of Standard Cell Libraries

Local random mismatch is a potential bottleneck to increase design working frequency. Mismatch requires extra margins for skew and pulse width, thus impacting achievable performance. Using larger cell size to reduce mismatch conflicts with tight area and power constraints. In REALITY at ST, we have developed a local random mismatch-aware Static Timing Analysis (STA) technique that can provide a bridge between traditional DSTA and SSTA, in the frame of the Hybrid Statistical Timing Analysis (HSTA) flow concept.

The traditional approach of handling variations in DSTA is to use percentage margins. However, the contribution of mismatch to delay variations (in %) decreases with increasing path length as it was demonstrated in the activities carried out in WP2. Moreover, there is a shift in average value of mismatch impact caused by non-linear delay relationship in subthreshold region that can increase pessimism when using simple margins.
At ST we characterized the impact of mismatch at cell level and used it to predict the mismatch impact on paths for digital clock networks within 10% error margin that in absolute terms is within few picoseconds. This mismatch characterization activity was focused on including the mismatch impact in clock-tree network design. The approach can be implemented in current timing analysis tools using inputs from DSTA.

The standard approach to handle mismatch would be through cell margins in corner conditions (derating factors). However, it was demonstrated in WP2 that traditional margins can be either pessimistic or risky. Application Specific Integrated Circuit (ASIC) designs today are working at GHz frequencies and even 10's of picoseconds are important. Using simple margins may cause a significant waste of achievable performance.

In REALITY, we developed an approach to calculate the impact of mismatch on clock-tree parameters, and we used this approach to derive advanced margins for DSTA. The developed technique builds on mainstream DSTA; hence, it is easily implementable in current design flows. Using DSTA inputs, the computation time using scripts will add minimal overheads. The characterization is robust against small process changes that can affect statistical characterization based on process parameter variations.

Statistical timing characterization typically requires foundry information and needs multiple days of computation time on server farms (see the results presented in WP2). However, the proposed method is based on spice models using very small test circuits and thus the required cells can be fully characterized within few hours without requiring any additional foundry information. We also extended the approach to skew and pulse width that typically are the limiting factors in presence of local random mismatch. The novelty of this approach is to compromise on error margins to enable fast implementation time and minimal overheads. The error margins are within acceptable limits. We obtained a good level of accuracy through mismatch aware STA to calculate the impact of mismatch on different parameters in a clock path. The approach was validated using Monte Carlo simulations on different configurations, and it can be easily implemented in current design flows with small overheads.

Hybrid (corner/statistical) Statistical Timing Analysis Flow for Digital Blocks

The *hybrid statistical timing analysis* (HSTA) f*low* based on commercial DSTA tools and a new technique to consider the impact of random WID variations (i.e., device mismatch) was developed in REALIY at ST.. By means of this approach it is possible to analyze the local random variations without using the traditional design margins (based on derating factors) that we demonstrated with the previous work in WP2 to be pessimistic and risky at the same time. The hybrid flow allows reducing the design margins and removing some pessimism, without changing the standard digital sign-off flow and methodology. To enable this hybrid flow, new techniques to characterize statistical libraries including the contribution of local device mismatch were defined and developed. Furthermore, new characterization techniques based on innovative algorithms were developed and exploited, in order to avoid running a full Monte Carlo analysis, which is extremely time-consuming as it was demonstrated by the work carried out in WP2.

The HSTA flow is outlined in Figure 10

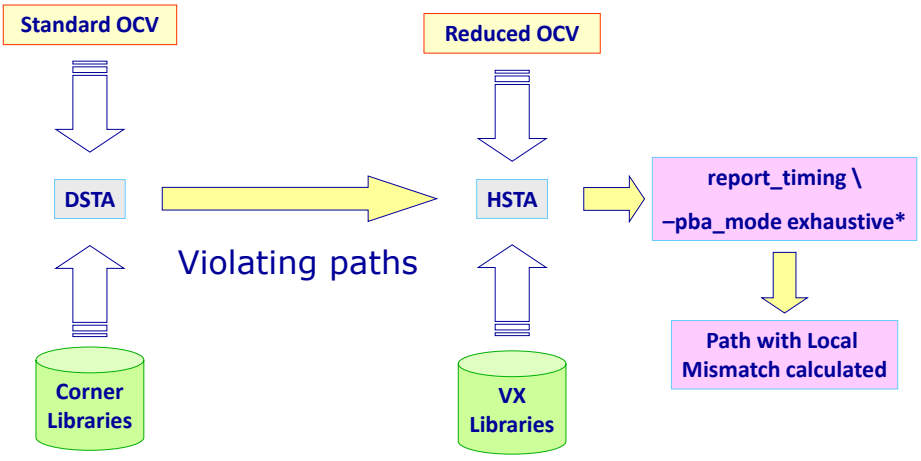

Figure 10: Hybrid statistical timing analysis flow

A traditional DSTA based on corners is carried out using the tools currently available in the digital sign-off flow. After DSTA, we considered the critical paths violating the timing constraints and also we considered those paths that were “potentially” critical, i.e., whose timing slack was very small and subject to the detrimental impact of unknown process variability. During this analysis, on-chip variations (OCV) were taken into account by means of derating factors (which can be overly pessimistic).
After selecting the critical/violating paths, on one side we reduced the OCV margins (based on process variability data) and we also carried out a path-based SSTA (i.e., HSTA) based on the statistical libraries we characterized in WP2. Following this approach it was possible to single out the paths which were most critical, to carefully analyze them considering the random WID variations, and to optimize those paths by removing the timing violations without taking unnecessary margins. This approach was used to evaluate the impact of random mismatch variations on digital designs in CMOS045LP (45nm low-power) technology.
The HSTA flow developed and exercised in REALITY will be used at ST to consider the impact of process variations during timing verification. The results obtained so far are quite encouraging, both in terms of reduced pessimism and reduced turn-around-time.

REALITY: not only technical achievements

During the project, the partners had the remarkable opportunity to work in close cooperation, to exchange ideas, to discuss about novel design techniques, and to develop new methodologies which are currently exploited by the design teams. Therefore, we believe this project was a unique opportunity to perform advanced and innovative research activities that otherwise would have been quite problematic within a typical industrial environment, and the proper blend of world-class academic theoretical background and industrial expertise allowed achieving outstanding results within the timeframe of the project, thus providing the European industry a significant competitive advantage. Hence, we consider REALITY a highly successful project and we would pursue further research activities and cooperation with all the partners.

8.1.2. **ARM**

The impact at the system level of random variations observed on the transistors of the most advanced technologies is quite difficult to analyse. Acquiring a good knowledge on variability issues through the whole development flow and developing an accurate methodology to percolate the variability information from the device level up to the SoC is fundamental to develop the next generation processors. As a consequence the dissemination of the knowledge acquired during the project has been one of the main challenges for the ARM team.

The exploitation of the outcome of the project has happened in three different ways:

1. Transversal team work organisation

To address the specific transversal needs of the project ARM has build up a project team with engineers coming from different horizons:

- Device
- Physical IP
- System design

A strong synergy between these three fields is becoming mandatory to understand the challenges we will face at each step of development of the next generation nodes. Within the project the team is developing characterisation methods as well as innovative design solutions to address the random variation issues in the designs. The ability to produce useful solutions will validate the transversal team organisation.
The team will survive the project and take advantage of this specific organisation to address new challenges we will face in the future technologies.

2. Internal knowledge spreading

The project is the place of a strong cooperation between ARM engineers and well known European researchers. The links drawn are essential for ARM to build a strong knowledge in variability phenomenon, characterization methods and remedial solutions.
Workshops and tutorials have been organised at ARM enabling fruitful exchanges between partners and in house engineers. These events were profitable for both parties:

- ARM has got through these discussions a deeper understanding of the troubles they will face in the future technologies. This is especially done with the cooperation with University of Glasgow and IMEC who develop a good synergy to forecast the random effect on advanced devices.
- We provide our partners with a better understanding of the industry constraints we are facing both in the Physical IP field and in the System level development era. This is outstanding information to lead the frontend researches toward investigations closer to the applications.

This cooperation between universities, research institutes and ARM gives us a strategic understanding of the issues and allow to better target our research efforts by knowing the industrial constraints as well as the fundamental physics issues we will face.

Beyond the knowledge exchange organized with our partners, the engineers involved in the project have build an strong internal know how for ARM. They have been participating to quarterly meetings with their peers inside ARM to internal research teams with information on the result of the project and discuss the interesting way to lead their technical work.
To train the development engineers, internal conferences involving engineers from all divisions of the company have been organised within ARM. Technical presentations in these events were also proposed.

Finally the knowledge built during the project led the basis of broader publication in conferences or tutorials in order for us to advertise towards our potential customers on our strategic understanding of the issue.

3. Production phase of tools and methodologies developed during the project

ARM was interested by the Variability Aware Methodology developed during the project. As a consequence a demonstration of the methodology on an ARM926 processor was proposed and achieved. The method will therefore be exploited within ARM. The ultimate demonstration of the methodology could be an application on more advanced processors to address the most power demanding applications.
The demonstration of the methodology has been a crucial phase which has really opened the door to exploit the method more widely inside the company if we feel it may provide us with a strategic differentiator toward our competitors.

ARM engineers have also developed internal tools to analyse accurately the variability impacts at the physical IP level as well as at the system level. The tools developed are not supposed to compete with any EDA vendor tool but aims at providing the most accurate information on variability for punctual analysis. One the one hand the information of these tools has been exploited either to provide accurate information on some specific designs. On the other hand this tool has been quite useful to validate the accuracy of the commercially available characterization tools since the statistical analysis is supposed to provide a more exact description of the design electrical behaviours then classic methodologies.
At the end of the project, the R&D team has provided the development engineers with prototypes. They have had the capability to test the concepts on their own designs and analyse how the tools can be integrate in their production flow

The tools and methodologies investigated within have allowed analysing the impact of the statistical variations. The wanted impact of these tools has been to allow engineers to analyse the robustness of their design, simple or complex, in a reasonable timeframe towards the effects of random variability. As a side effect, the project has provided us with the necessary information to develop more robust systems and efficient resilient systems.
What is more, the accurate analysis of random variability has also paved the way to a better understanding of systematic variability. The comparison between the different effects on the new technologies gives a good understanding where to put our development efforts.

From the 65nm node technology developers and designers have started to be confronted to the variability issues due to local and global effects. In concrete ARM designers have started investigations in variability characterization very early but the lack of technology information was a real limitation for a company focused on design. The main issues on our designs have showed up at the 45nm node. A real need for strong cooperation with experts in this field was identified. Early access to the information on future technology nodes is mandatory for a company developing Physical IP.

Variability Characterization:

The first idea we can develop when facing a new issue is to try to model it accurately. This is what we have started doing in the REALITY project. At the transistor level there has been a strong development work to assess accurate variability information. The second step is to analyze the variability impact on simple design.

At the time the project started we could see a strong momentum from the EDA companies to put in place variability aware flows. New tool features and new library format appeared: CCS-VA, S-ECSM. Designers needed to understand the interest of these tools. For this we needed to produce the right liberty data incorporating the correct variability information. We also needed to use the tools and evaluate the results. This is what we carried out on simple standard cells. We also developed a validation flow to verify the output of the flows. This was a really strategic work since were able to identify accuracy issues on these new tools and challenge the EDA vendors on their own expertise.
A full characterization of a system could be carried out using the VAM flow. This tool is based on Monte Carlo simulations. It is really demanding in term of library characterization since to achieve a good accuracy a large number of runs is required. Each run is one library characterization. The results of the tool are really valuable since it is the only tool to our knowledge providing a real correlation between power, leakage and speed of the system.
Even though tools were developed for standard cells characterizations no EDA flow addressed the issue of variability characterization of SRAM array was. It is important to notice that the first area where the variability issues could be clearly identified is the SRAM array functionality. Due to the high number of SRAM cells a memory array acts like a net catching the extreme variability information. Indeed a memory array is limited in term of functionality as well as in term of performance by the worst case cell in the array. This is why a great interest has been raised on SRAM array characterization. In our case the investigations have taken two different forms. First we needed to understand the limits of functionality of designs. This has been answered by investigations on the memory margining. Strong mathematical models have been used to develop accurate statistical descriptions to account for the variability issues.
Secondly we wanted to understand the impact of the SRAM variability on a full system. The memory VAM methodology gave us interesting clues on this issue. The methodology based on MC runs as well first provides interesting information of the stand alone memory variability. In addition with the help of the full system VAM we could directly understand how the system behavior is impacted by our memory design.

Importance of variability aware design

On advanced technologies one of the major issues is coming from the exponential leakage. 32nm technologies have already demonstrated very high leakage level and the first figures coming from papers showing latest technology development is very alarming. We might face in the near future a problem when the chip cannot be fully active at the same time otherwise it will simply melt (Android processor shines light on dark silicon - Rick Merritt – EETimes). New techniques will have to cope with these issues.
An ultra-low power SRAM designs do not seem fully suitable for general purpose solutions today, however it paves to way to the low power design that will be needed in “dark silicon” systems as described in the previous article. It is also fully adequate for ultra-low power systems as the one seen on medical devices which is a growing market.
Low voltage and ultra-low voltage designs are also identified as a potential solution for future developments. When reducing the voltage supply a great gain in leakage power will be witnessed but we will hit the variability wall as well. Design techniques to cope with the increasing variability we will face at the 22nm node and below will be mandatory. The design techniques proposed by the partners in this field make these options possible.

Beyond the technical discussions

The interest of the project goes far beyond the technical conclusions we have drawn during the 2.5 years of the project. The partners had the opportunities to exchange ideas, start cooperation and understand each others’ objectives and issues. It has been a great opportunity to create a network we all would like to keep alive during further exchanges.

8.2. Use by academic partners to advance relevant research

8.2.1. **University Of Glasgow**

The capability has been developed to simulate statistical reliability in nanoCMOS devices. Validation in respect of experiment has increased confidence in using particular sources of variability to explain experimental variability measurements in real devices.

8.2.2. **KULeuven**

Exploitation is through the dissemination effort described below. The software results could be exploited through KUL's spinoff company later on, but it is too early at the moment.

8.3. Use by Research Institution IMEC

- The Main Exploitation Target is 2-fold :

  1. *Inclusion of results in its IP portfolio (IIAP)*

Main Exploitation Target : inclusion of results in its IP portfolio (IIAP) and more specifically in the Apollo research program, which is the successor of the M4 research program.

IMEC is one of the few research institutes in the world, with proven experience on bringing together top-tier industry partners for cooperation into a shared research program. IMEC has been very successful in deploying this model of shared research.

IMEC vzw's business strategy is based upon its 'IP Portfolio'. The exploitable results from the REALITY project will be included in this portfolio and will be exploited through:

- IMEC vzw's Industrial Affiliation Program (IIAP)' partnerships;
- Bilateral contracts with national and international industry and universities, and;
- Technology transfers and licensing of proven technology to industry and spin-off companies.

Each industrial partner joins the IIAP research program on a bilateral basis, with clearly defined technical scope and deliverables, allowing the partner to tune the bilateral project to some of its industrial needs. An industrial resident can be delegated to IMEC by the partner to join IMEC's research teams, typically for one year.

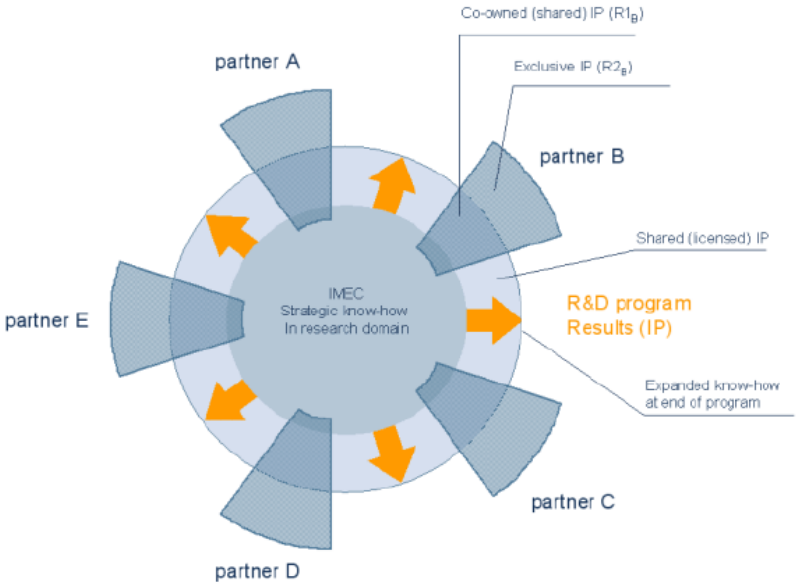

Figure 11 REALITY results can be licensed through the IIAP business model

- Type R1: The more generic or methodological type of project results, based on IMEC's strategic know-how (background information, R0) are co-owned by both IMEC and the industrial partner, without any accounting to each other;

- Type R2: Company-specific results or confidential information are the exclusive ownership of the industrial partner;
- Type R0: Results owned exclusively by IMEC are available for licensing, providing full user rights for the industrial partner. This type of IP relates to more fundamental, generic technologies;

In addition, the industrial partner gets access to IMEC's background information in the research domain specific to the IIAP, and the R0 and R1 results of the other industrial partners in the same IIAP.

Benefits:

- The industrial partner gets access to strategic IMEC background information at an early stage;
- The industrial partner gets access to other R0 and R1 (shared) results from other partners in the same IIAP;
- The industrial researcher (resident) is taken up into the IMEC mixed research team to execute the IIAP program. This intensifies the process of technology transfer and shortens the learning curve;
- The program induces a flexible interaction between the research team at IMEC (including the industrial researcher) and the industrial headquarters;
- Each IIAP contract is conducted on a bilateral basis, allowing for tuning and confidential information (exclusive R2) as described in the bilateral agreement;
- Each IIAP contract is standard as well as the corresponding prices.

Leverage effects:

Joining an IIAP program induces:

- A pricing leverage, through the cost-sharing principle of R0 and R1 results;

- An information leverage, as each industrial partner gets access to much more information (project info, IMEC's background information, R0 and R1 of other program partners) than its financial commitment;
- A cross-fertilization leverage, through the sharing of R0 and R1 results and through a good combination by IMEC of leading-edge partners, also coming from complementary fields (e.g. foundries, equipment or materials suppliers) but interested in the same research topic;
- A time-to-market leverage, as the industrial partner gets a competitive advantage in both strategic results and rapid time-to-market.

IMEC has a proven transfer record in the running APOLLO initiative (long term research program) in the domain of nomadic embedded system (Samsung, CoWare, Mentor Graphics, Arteris, …). This type of program is aimed to drive strategic cooperation between IMEC and the industry on the field of nomadic embedded systems. Hereto, IMEC has made a strong investment, bringing together the needed critical research mass of almost 150 researchers in this field. Based on this work, IMEC is also building up more extended networking and cooperation relationships with other European universities, which can contribute on complementary know-how creation. As a result, IMEC positions itself as centre-point in the chain for providing leading know-how and research to the industry. By the tight interaction with IMEC's partners, they are optimally prepared to exploit the know-how into leading solutions in their specific markets. It is anticipated that the results of REALITY will be instrumental to build the next generation solutions targeted by the long-term roadmap of its Apollo research program initiative. Research performed in REALITY has also created new opportunities for extending IMEC research cooperation with leading academic and industrial partners.

9. List of Abbreviations

REALITY	Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies
CAD	computer aided design
DLC	
DMT	discrete multi-tone
DSP	digital signal processing
TAD	Technology aware design
IP	Intellectual Property
FFT	fast Fourier transform
HW	hardware
IC	integrated circuit
QoS	quality of service
SoC	system on chip
SOHO	small office/home environment
SW	software

