7th RTD Framework Program

REALITY

Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

Contract No 216537

Deliverable D7.4

Periodic activity report

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The REALITY Consortium consists of:

Interuniversity Microelectronics Centre (IMEC vzw)	Prime Contractor	Belgium
STMicroelectronics S.R.L. (STM)	Contractor	Italy
Universita Di Bologna (UNIBO)	Contractor	Italy
Katholieke Universiteit Leuven (KUL)	Contractor	Belgium
ARM Limited (ARM)	Contractor	United Kingdom
University Of Glasgow (UoG)	Contractor	United Kingdom

1. Disclaimer

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2. Acknowledgements

3. Document revision history

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19/02/2008	V1.1	Yves Laplanche, Tom Tassignon	Final Version

4. Preface

The scope and objectives of the REALITY project are :

- Development of design techniques, methodologies and methods for real-time guaranteed, energy-efficient, robust and adaptive SoCs, including both digital and analogue macro-blocks“

The Technical Challenges are :

- To deal with increased static variability and static fault rates of devices and interconnects.
- To overcome increased time-dependent dynamic variability and dynamic fault rates.
- To build reliable systems out of unreliable technology while maintaining design productivity.
- To deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.

Focus Areas of this project are :

- “Analysis techniques” for exploring the design space, and analysis of the system in terms of performance, power and reliability of manufactured instances across a wide spectrum of operating conditions.

- “Solution techniques” which are design time and/or runtime techniques to mitigate impact of reliability issues of integrated circuits, at component, circuit, architecture and system (application software) design.

The REALITY project has started its activities in January 2008 and is planned to be completed after 30 months. It is led by Mr. Miguel Miranda of IMEC. The Project Coordinator is Mr Tom Tassignon. Five contractors (STM, ARM, KUL, UoG, UNIBO) participate in the project. The total budget is 2.899 k€.

5. Abstract

This report is deliverable 7.4: “Periodic activity report”. The reporting period is from M1 until M12.

6. List of Abbreviations

REALITY	Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies
CAD	computer aided design
DMT	discrete multi-tone
DSP	digital signal processing
FFT	fast Fourier transform
HW	hardware
IC	integrated circuit
QoS	quality of service
SoC	system on chip
SOHO	small office/home environment
SW	software

7. List of Tables

Table 1 : typical REALITY Risk management list (version of 9-12-2008) 45
Table 2: Update of the DoW 47
Table 3: overview of project meetings 50
Table 4: List of deliverables submitted to the EC.. 50

8. List of Figures

Figure 1: Calibration of the Glasgow simulator against TCAD simulation of the ST 45nm devices17
Figure 2: I_D-V_G curves for a statistical ensemble of 200 n- and p-channel devices. V_D=0.05V 18
Figure 3: Electrostatic potential in the n-channel and p-channel devices with sources of variability included. 17
Figure 4 Comparison between full gate-level analysis and SoC-level analysis for joint PDFs: (a) dynamic energy and longest path delay; (b) leakage power and longest path delay 20
Figure 5: Schematic representation of the reliability simulation methodology. 22
Figure 6: (a) Traditional solution (left); and (b) Proposed solution: readbuffer and extended GBL (right). 25
Figure 7: (a) Without readbuffer (left); and (b) With readbuffer (right) 26
Figure 8 : Distributions of the delay from WL activation to 150mV swing on GBLH for the two setups in Figure 7 as obtained by performing 20K Monte Carlo runs. Gaussian distributions have been fitted to both full datasets. All curves are displayed both on a linear and a logarithmic scale. 26
Figure 9: Setup for SA tuning (N=16 ; word length=32). 27
Figure 10: Effective offset of a tuned sense amplifier. 28
Figure 11: A block diagram showing FBB implementation methodology 29
Figure 12: MPEG-2 Decoder : Scheme for parallel implementations in T6.5.1 37
Figure 13: REALITY project team and coordination 42
Figure 14: REALITY Risk management methodology 44

9. Table of contents

1. DISCLAIMER 2
2. ACKNOWLEDGEMENTS 2
3. DOCUMENT REVISION HISTORY 2
4. PREFACE 3
5. ABSTRACT 4
6. LIST OF ABBREVIATIONS 5
7. LIST OF TABLES 6
8. LIST OF FIGURES 6
9. TABLE OF CONTENTS 7
10. DECLARATION BY THE SCIENTIFIC REPRESENTATIVE OF THE PROJECT COORDINATOR[1] 10
11. PUBLISHABLE SUMMARY: "RELIABLE AND VARIABILITY TOLERANT SYSTEM-ON-A-CHIP DESIGN IN MORE-MOORE TECHNOLOGIES" 11
12. PROJECT OBJECTIVES FOR THE PERIOD 1, PROJECT M0 UNTIL M12 16
13. WORK PROGRESS AND ACHIEVEMENTS DURING THE PERIOD 17
 13.1. WP1: DEVICE VARIABILITY AND RELIABILITY MODELS (WP LEADER: UOG) 17
 13.2. WP2: SYSTEM AND CIRCUIT CHARACTERIZATION AND SENSITIVITY ANALYSIS (WP LEADER: IMEC) 19
 13.3. WP3: MIXED MODE COUNTERMEASURES (WP LEADER: KUL) 21
 13.4. WP4: SYSTEM LEVEL COUNTERMEASURES (WP LEADER: UNIBO) 30
 13.5. WP5: DESIGN FLOW, INTEGRATION, PROOF OF CONCEPT (WP LEADER: ARM) 32
 13.6. WP6: VALIDATION AND ASSESSMENT OF RESULTS (WP LEADER: ST) 34
14. DELIVERABLES AND MILESTONES TABLES 39
15. PROJECT MANAGEMENT 42
 15.1. CONSORTIUM MANAGEMENT TASKS AND ACHIEVEMENTS; 42
 15.2. PROBLEMS WHICH HAVE OCCURRED AND HOW THEY WERE SOLVED OR ENVISAGED SOLUTIONS : 43
  15.2.1. Applied approach within REALITY : 43
  15.2.2. REALITY Top Risks to date: 45
  15.2.3. Changes: 46
 15.3. LIST OF PROJECT MEETINGS, DATES AND VENUES IN YEAR 1 : 48
 15.4. PROJECT PLANNING AND STATUS : 50
 15.5. IMPACT OF POSSIBLE DEVIATIONS FROM THE PLANNED MILESTONES AND DELIVERABLES 50
 15.6. DEVELOPMENT OF THE PROJECT WEBSITE : 51
 15.7. USE OF FOREGROUND AND DISSEMINATION ACTIVITIES DURING THIS PERIOD : 51
 15.8. COORDINATION ACTIVITIES COMMENT – KEY MESSAGE : 51

16. EXPLANATION OF THE USE OF THE RESOURCES 52
16.1. ST MICROELECTRONICS 52
16.2. IMEC 52
16.3. UNIVERSITY OF GLASGOW 52
16.4. KATHOLIEKE UNIVERSITEIT LEUVEN 53
16.5. UNIVERSITY OF BOLOGNA 53
16.6. ARM 54
17. FINANCIAL STATEMENTS – FORM C AND SUMMARY FINANCIAL REPORT 54
18. CERTIFICATES 54

PROJECT PERIODIC REPORT

Grant Agreement number: 216537

Project acronym: REALITY

Project title: “Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies”

Funding Scheme: Collaborative project (STREP)

Date of latest version of Annex I against which the assessment will be made:

Periodic report: 1st X 2nd □ 3rd □ 4th □

Period covered: from 01/01/2008 to 31/12/2008

Name, title and organisation of the scientific representative of the project's coordinator:

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Project website address: http://www.fp7-reality.eu/

10. Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project has fully achieved its objectives and technical goals for the period;
- The public website is up to date, if applicable.
- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 15 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: Miguel Miranda Corbalan

Date: 23/02/2009

Signature of scientific representative of the Coordinator

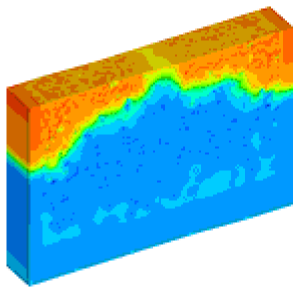
11. Publishable summary: “Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies”

Project Facts:

- FP7 Project : European Community funded
- Coordination : IMEC
- Website : www.fp7-reality.eu
- Duration : 30 Months
- Effort : 382 person-months
- Industry : ARM (UK), ST Microelectronics (Italy)
- Start date : 1st January 2008
- University : Glasgow (UK), Bologna (Italy), Leuven (Belgium)
- Research Centre : IMEC (Belgium)

Scope:

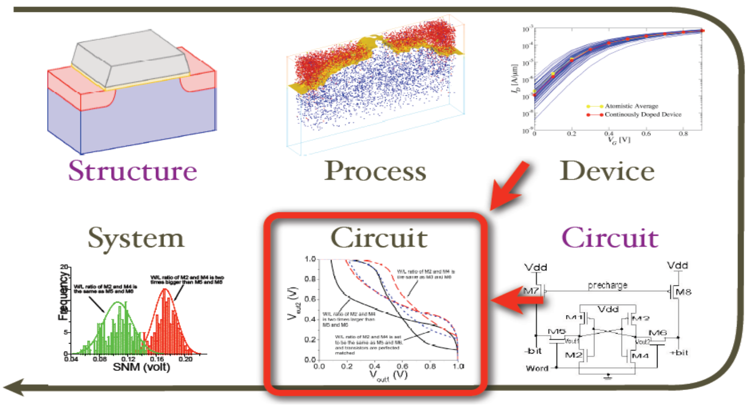
- Scaling beyond the 32 nm technology
- Tackle the increased variability and changing performance of devices from device unto system level.



Random discrete dopants in a 35 nm MOSFET from the present 90 nm technology node.

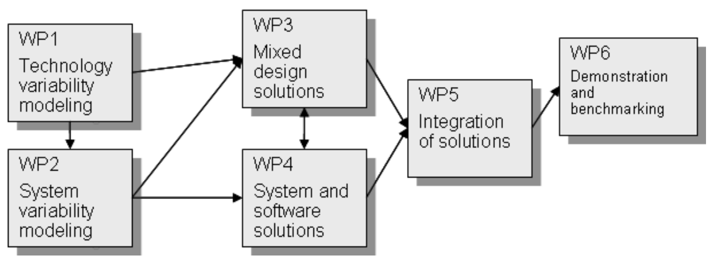
Challenges:

- Increased static variability and static fault rates of devices and interconnects.
- Increased time-dependent dynamic variability and dynamic fault rates.
- Build reliable systems out of unreliable technology while maintaining design productivity.
- Deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.



Proposed solution:

- System analysis of performance, power, yield and reliability of manufactured instances across a wide spectrum of operating conditions.
- Generally applicable solution techniques to mitigate the impact of reliability issues of integrated circuits, at component, circuit, and architecture and system design.



WP1: Device variability and Reliability Models (WP leader: UoG)

Since the start of the project the work on this work package has been on the physical modelling of variability at the 45nm technology node including the generation of statistical compact models. The work is based on the 45nm low-power technology devices provided by the project partners at STMicroelectronics. The modelling is performed by the University of Glasgow using their advanced 3D quantum-corrected drift-diffusion simulator which can account for the different sources of variability that will exist at this technology node. STM provided TCAD files of their device structures from which the doping profiles were extracted in a suitable form for input to the Glasgow simulator. The simulator has been successfully calibrated against the I-V data provided by STM.

The main sources of variability for this technology are random discrete dopants, line edge roughness and poly-silicon granularity. Statistical samples of 200 device characteristic, including these appropriate sources of variability, have been simulated for both the n- and p-channel devices.

A baseline compact model has been extracted from simulations of the calibrated device structure with continuous doping. From the simulation data including variability, statistical compact models are produced by taking the baseline model and, for each of the 'atomistic' devices, re-extracting seven parameters which can account for the variation in the characteristics. This allows propagation of the variability information up the 'food-chain' to the circuit and system design stages.

IMEC has provided data on the temporal degradation of devices related to formation of defect states. An analysis of the reliability of devices due to different levels of degradation has been performed. This shows that an increasing density of trap states results not only in the expected increase in the average threshold voltage, but also in a spreading in the distribution of threshold voltages meaning greater variability.

This work meets the requirements of deliverable D1.1 which is due at T0+12.

WP2: System and circuit characterization and sensitivity analysis (WP leader: IMEC)

In this work package we have worked in three main fronts: (a) the design of a first version of a 32nm CMOS library which is a key enabler not only for the work developed here but also in other work packages (e.g., WP3, WP4 and WP5); (b) the definition of a methodology and flow to percolate impact of process variations from the device compact model level (see WP1) to the SoC integration level; (c) the first design of an information format to enable exchange of process variation information along the different electronic levels of abstraction in digital circuits.

In this first year we (STM, IMEC, ARM and UoG) have designed a process variability analysis framework that brings commercial and academic tools into a holistic analysis/simulation flow. Commercial EDA products for process variability analysis such as Statistical Static Timing Analysis (SSTA) have been be reused in combination with Monte-Carlo based simulation techniques there were statistical analysis techniques are missing. This comprises novel techniques to bring correlated statistical timing and power and/or energy metrics from the level of the IP block to the SoC integration level (IMEC).

For power and energy estimation a given Register Transfer Level benchmark is used to properly characterize the system. The level below system architecture differentiates between IP components built using standard cell logic and macro-blocks (e.g. memories) that exist as transistor net-lists or layouts from which the netlist can either be extracted or generated via specific compilers (e.g., memory compilers). For standard cell logic existing commercial offerings for statistical timing analysis are used. In case of IP macro-blocks, however, timing and energy are usually characterized using transistor-level simulations and given the increasing complexity of the typical macro-blocks in SoC design, there are no commercial solutions available. Therefore new developments for Monte-Carlo based SRAM macro-blocks statistical analysis were also carried out on 45nm technologies. An in house (ARM) comprehensive solution to evaluate how the statistical variation impacts the yield is under development. First Yield forecasts have been done on the READ cycle.

The aim of this work has been to understand the impact of the variations on our designs and evaluate the needs of new development methods. In contrast, standard cell logic follows the classical characterization both for timing and power and each library component is later characterized with statistical techniques, such as Statistical Static Timing Analysis (STM) and/or Monte Carlo (IMEC, UoG) to capture the impact of variability on timing (and eventually power/energy).

The final step has been the merging of the statistical properties of the various library cells into a common format representation of statistical energy and timing. Statistics at the level of cell library needs still to be propagated up for post-synthesis analysis of standard-cell based designs. After both the macro-blocks and the standard cell based design have been statistically characterized, their statistical properties can be integrated into a unified representation at the system. When energy must also be considered, the correlations between timing and energy consumption can be propagated through the different levels of abstraction.

Particularly important in this WP has been starting to look to various standardization efforts for the interfaces to transfer this information through different levels of abstraction (IMEC). Variability propagation from process technology to analog simulations can be done in a number of ways and no standard is emerging yet in the industry. Similar considerations apply for the interface between standard cell calibration and digital simulation. Existing SSTA solutions use proprietary standards for the cell library characterized for variability.

The expected final result of the work package is a set of techniques supporting the overall analysis method and flow developed during this first year of the project. These techniques or a subset of them potentially combined with other techniques already available in the form of commercial tools or combination of them will be used to demonstrate the feasibility of applying such flow to a test vehicle of industrial relevance. Such effort is expected to take place during 2009.

WP3: Mixed mode countermeasures (WP leader: KUL)
During the first year in this work package (task 3.1) accurate models have been developed for the simulation of degradation effects for analog circuits. Focus has been on NBTI and HC (hot carrier) degradation. Also, techniques have been developed to simulate the resulting degradation of analog circuits. The aim is to be able to accurately and efficiently analyse and detect reliability problems in analog circuits processed in nanometer CMOS processes. Modeling for analog circuits poses more challenges since the models have to be developed for a continuous range of voltages (rather than just 0/1) and device sizes. The impact of the increasing variability in nanometer technologies on this degradation has also been investigated. An initial version of a variability-aware reliability simulation methodology optimized for the simulation of analog circuits in nanometer technologies has been developed. The methodology has been demonstrated on some very common circuits, and will be improved and extended in the next year. Also a start has been made on applying the knobs&monitors principle to make analog circuits degradation-resilient.

The work performed by UNIBO in this first period focused on Task 3.3 about Development of architectural solutions for variability management of data path and controllers". The aim of these techniques is to automatically identifying static and dynamic variations, recalibrate the operation mode to adapt to these variations and finally to provide monitoring information to the system level.

WP4: System level countermeasures (WP leader: UNIBO)
The work performed in this first period by UNIBO focused mainly on Task 4.1 concerning the development of software infrastructure for the implementation of policies do be designed in Task 4.2. This work lead to the Deliverable 4.1 on M9. In the last 3 months the work concerning Task 4.2 has begun for the next Deliverable 4.2 due on M18.

Main activities related to Task 4.1 in this period concerned:

1. Learn how to use the simulator of the target multicore platform made available by ST and contribute to its refinement so that it can implement the requirements needed to evaluate the software policies and run the benchmarks for validation (i.e. support of interrupts, timers, frequency scaling);
2. Development of interprocessor message passing and synchronization library;
3. Development of task migration support (work done by the subcontractor);
4. Porting of an embedded operating system (FreeRTOS) to the target platform (work done by the subcontractor);
5. Development of workload models and a simple policy to test the functionalities of the infrastructure.

Initial activities related to Task 4.2 concerned:

1. Interaction with IMEC to define the variability information made available in WP2 their system level view;
2. Understanding of system level impact of variability effects;

3. Definition of policy scenarios;
4. Identification of metrics for the evaluation of policy effectiveness;
5. Implementation of preliminary policies for compensation of variability effects at the software level;
6. Interaction with ST to define the benchmarks for policy evaluation;

Additional activities:

1. Definition of a back-of-the-envelope model for rapid computation of power and energy consumption of the target platform for a nominal and degraded system. The model includes also aging effects;
2. Definition of a strategy for integration of the back-of-the-envelope model in the target simulation platform.

WP5: Design flow, integration, proof of concept (WP leader: ARM)
This Work Package coordinates and carries out the evaluation of the different project components. It is the place where the components of the project come together and will involve developing methodologies and test platforms to enable the evaluation to take place. It is responsible for assessing the severity of the un-compensated situation, and quantifying the improvements that result from the application of techniques identified in other Work Packages. It is also responsible for identifying the techniques that prove to be unsuccessful (and why), as well as to point to other techniques that might be worth investigation (beyond this project). Task 5.1 and task 5.2 were therefore dedicated to the identification of the circuit level components and maco-blocks to be used for the evaluation and assessment of the output of WP 2, 3 and 4. These are the elementary items to be integrated and then evaluated in order to analyze the statistical variability issues.
Task 5.3 was dedicated to the definition of system microarchitecture platforms on which will be evaluated the output of WP3 and WP4. The selected platforms will enable the evaluation of the characterization flow as well as to demonstrate the effectiveness of the countermeasures. The deliverable 5.1 concluded this work and gives an exhaustive description of the chosen strategies.
These three first tasks aimed at clearly defining the scope of the integration work to feed the other work packages. The output of the other work packages, including characterization methods, design flows or design solutions will all be evaluated within the defined scope. The choice of the different components was done to give a good picture of the industry application the projects is addressing.
During this period task 5.4 was dedicated to the initial deployment of a statistical aware characterization flow within an “industrial” design flow. The goal of the task is to prove the feasibility of the integration of a variability aware characterization tool in a library development flow. Demonstrations of the tools had to be performed on real products. The next step is to assess and compare the additional costs and information such a methodology will provide.
The tasks 5.5.1 and 5.5.2 aimed at starting the necessary code development to integrate the different elements produced in the other work packages in the demonstration platforms.

WP6: Validation and assessment of results (WP leader: ST)
This work package is the place were most of the results, methodologies, flows, IPs developed and/or leveraged in the other workpackages come together for a proper industrial criterion driven assessment of pros vs. cons, basically validating the project’s goal of “build reliable system with unreliable components”.
An important aspect of this work aims at the identification of a suitable set of applications and requirements, and feed them into the guidelines and requirements for the other work packages, especially WP5.
The WP tasks are designed to validate and assess the project results through the benchmarking of individual IP blocks along with the identification and porting of a set of industrially relevant applications (digital video and audio encoding, standard system performance benchmarks, etc.). The general focus is the leverage of IPs and applications along with their integration and mapping onto the integrated application platform developed with contributions from WP3,4,5. The output of the workpackage is the evaluation both in terms of NRE, final product cost, and in general advantages over the uncompensated case, of the benefit stemming from the methodologies, techniques and components developed by the project.
The tasks covered included the projection of the application requirements onto the test platforms templates as defined by WP5 and their integration with the feedback/control mechanism as defined by WP3/4; an activity to define a suitable validation plan for the various components, incorporating outputs of modelling from WP1, and providing feedback to tasks of WP2/3/4. Suitable figures of merit and estimation of objective functions, for example in terms of tolerance to variation of critical process parameters, as well as modelling of individual circuits, is to be derived from WP1/2/3 and validated in platforms validation models as defined by the work package.
The initial focus of the WP execution has been the study and analyses of suitable industrial applications and scenarios, the identification of metrics for components, methodologies and platform, and the initial gathering of inputs towards the definition of a validation plan. This included the definition of scenarios to drive the subsequent phases and tasks of the final assessments. Additionally some preliminary work has been done to plan for the porting of the selected application into the REALITY simulation platform defined in WP5.

12. Project Objectives for the period 1, Project M0 until M12

The reporting Period 1 covers the project time-schedule M0 until M12, i.e. starting from 1st January 2008 until 31st December 2008.

Description of the performance / research indicators

WP	After year 1	After year 2	At end of project
WP1 Device variability	Physical modeling and understanding of the variability at 45/32 nm technology nodes (TN). First statistical compact models.	Compact models that accurately capture the variability and the reliability issues at 32 nm TN.	Models fine tuned. Feedback from device measurements incorporated.
WP2 Analysis	Preliminary version of a RDR std. cell library [32nm]. Flow definition and framework set up for variability characterization. Correlated variability energy timing flow definition and set up.	Variability characterization of a [32nm] RDR std cell library. Exploitation of the variability aware modeling flow on the driver application vehicle, including a solution for IP blocks and memories.	Methodology fine tuned. Feedback from benchmarking acknowledged.
WP3 Mixed design	Description of the variability and reliability analysis methods at circuit level	Demonstration of the developed method on SRAM and analog circuits	Validation of the developed method
WP4 Algorithm	Software techniques for flexible data and workload allocation for migration (the base flexible RTSM support)	Control algorithms for system level reliability and variability management (exploiting of the base RTSM support)	Porting, optimization and tuning for the target evaluation platform of: (a) the flexible RTSM, (b) the control algorithms
WP5 Integration	Definition of characterization blocks, macrocells, and system level architecture	Validation and application of methods to macrocells and integration into system	Final system integration, validation feeding into WP6 benchmarking
WP6 Benchmarking	Identification of relevant industrial applications and associated requirements and evaluation metrics	Definition of the validation plan Benchmarking of block level IPs	Benchmarking of system level platform Evaluation of results and impact according to validation plan criteria

13. Work progress and achievements during the period

13.1. WP1: Device variability and Reliability Models (WP leader: UoG)

Work progress in task 1.1, 1.2 and 1.3

The aim of WP1 is the physical modelling and understanding of the variability at 45/32 nm technology nodes including the generation of statistical compact models. The statistical variability stems from the discreteness of charge and matter and the statistics of small numbers. The major sources of statistical variability include random discrete dopants (RDD), poly-silicon granularity (PSG), line edge roughness (LER), oxide and body thickness fluctuations (OTF/BTF) and the high-κ gate stack morphology (GSM). Realistic reliability measurements and accurate estimates of statistical variability are only available for mature technologies. In this work package (WP1) we use 3D statistical numerical simulations of large statistical samples of microscopically different devices in order to estimate statistical variability. We provide reliable quantitative data on which the design technologies and solutions in WP2-WP6 will be based. The simulations are carried out with the University of Glasgow (UoG) 3D physical statistical device simulator which incorporates RDD, PSG, LER, OTF, BTF and GSM as sources of statistical variability. The simulator can also estimate the gate leakage variability associated with the above statistical variability sources.

STM have provided TCAD process simulation data of the doping profiles of their 45nm LP technology, along with I_D-V_G characteristic of their TCAD device simulations calibrated to experimental data. The first step in the work here is to introduce the provided device structures into the UoG 'atomistic' device simulator. The profiles of each dopant species are mapped onto the simulation mesh used by the simulator, and saved as doping files to be read in upon execution of the simulator. The second step is to run the simulator to produce I_D-V_G characteristics at low and high drain voltage and calibrate the simulations to match the TCAD simulation results provided by STM. This is done by adjusting parameters in the mobility models (such as the saturation velocity). The results of this calibration are shown in Figure 1 for the n- and p-channel devices. Good agreement is achieved in both cases.

Once the simulator has been calibrated to match the provided data, the different sources of variability which are important for this particular bulk MOSFET technology can be introduced. For the n-channel device we include random discrete dopants (RDD), line edge roughness (LER) and Fermi-level pinning at poly-silicon grain boundaries (PSG). For the p-channel device we include RDD and LER. The absence of donor-type interface states at the grain boundaries of p-type poly-silicon means that Fermi-level pinning along these boundaries will not be a source of variability in p-channel devices. Figure 3 shows the electrostatic potential in the n- and p-channel devices with these sources of variability included. The surface potential is shown above each device demonstrating the source-to-drain barrier due to the doping being modulated by the different sources of variability. In particular, the sharp potentials due to RDD are clear with the attractive potential wells in the source/drain and the repulsive barrier spikes in the channel. The reason for the variation in device characteristics is clear from this picture as the potential in each device will be affected differently depending on the particular configuration of the RDD, LER and PSG.

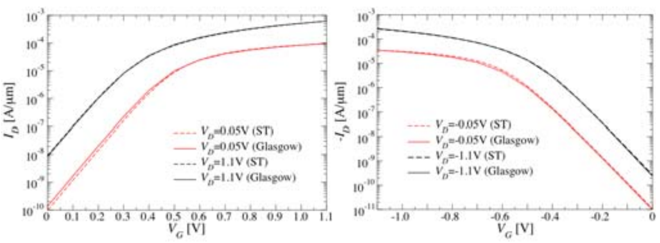


Figure 1: Calibration of the Glasgow simulator against TCAD simulation of the ST 45nm devices

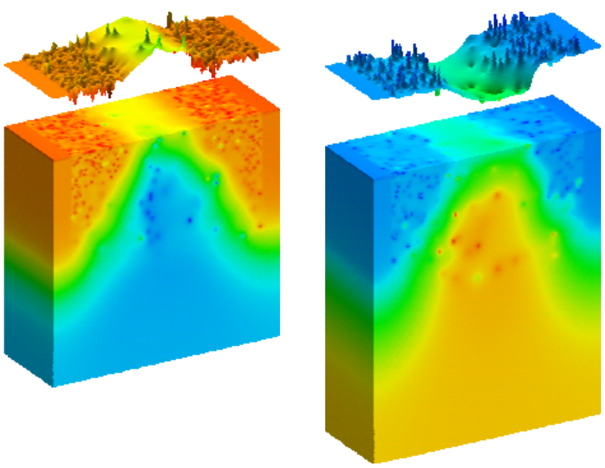


Figure 3: Electrostatic potential in the n-

channel and p-channel devices with sources of variability included.

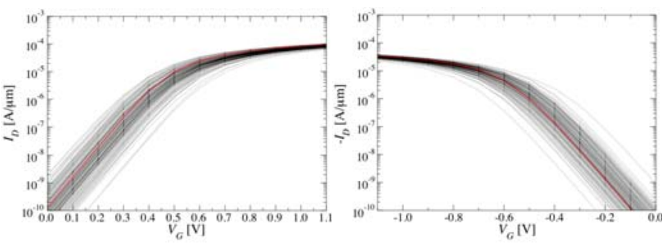


Figure 2: I_D-V_G curves for a statistical ensemble of 200 n- and p-channel devices. V_D=0.05V

Investigation of variability requires the simulation of a statistical ensemble of microscopically different devices – different random distribution of discrete dopants; different line edge roughness pattern along the gate edge; different pattern of poly-silicon grains, etc. For this work we simulated 200 different devices based on each of the nominal n- and p-channel devices. I_D-V_G characteristics are produced at low and high drain voltages. Figure 2 shows the curves for the n- and p-channel devices at V_D=0.05V. Each set of 200 I-V curves requires approximately 3-5 CPU-years of simulation time depending on the drain bias, highlighting the computational expense of the task, and demonstrating the need for large computer clusters in order to perform such work.

Compact models are the interface between technology and design. The approach adopted here for this interface is to generate a different compact model card for each of the 200 different devices. Then, during the statistical circuit simulation stage a Monte Carlo approach is used, whereby for each transistor in the circuit, one compact model card is selected at random from the ensemble and used to characterise that particular transistor.

Extraction of statistical compact models first requires the extraction of compact models for the continuously doped n- and p-channel devices. During this first stage, a combination of local optimisation and group extraction strategy is employed to extract the complete set of BSIM4 parameter using the Synopsys tool Aurora. This is based on the simulation of a set of transistors with *continuous doping concentration* and different channel lengths, focusing on those critical to long channel behaviour, the threshold voltage in the short channel regime, and drain current response in the presence of high fields. The parameters extracted from the first stage are divided into two groups: those which have been found to be relatively independent of statistical variation that are then fixed during the next stage, and those sensitive to the statistical variation which will be re-extracted for each 'atomistically' different device at the second stage. For each of the 200 devices in the statistical sample a compact model can be generated by re-extracting 7 parameters which can account for the variability, while the remaining parameters are kept from the initial extracted model. The rms errors in the extracted statistical compact models were found to be below 5% for the n-channel devices and below 7% for the p-channel devices.

Most device reliability problems are associated with generation of fixed charges or the trapping of electrons and/or holes in defect states in the gate stack during circuit operation. IMEC have provided data on expected trap sheet densities for different levels of degradation allowing UoG to run statistical simulations to investigate the impact of stress on device performance at different points in the lifetime of the devices. This allows propagation of reliability information along the design 'food chain' – combining pure TCAD-like simulations and reliability measurements as reliability modelling. Simulations at three different levels of degradation have shown a systematic increase in average threshold voltage with increasing trap density, and also an increase in the spread of the threshold voltage distribution meaning increased variability.

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*15*	*15*
IMEC	*3.6*	*3.6*
UNIBO	*0*	*0*
ST	*2*	*1.95*
KUL	*0*	*0*
ARM	*0*	*0*

TOTAL	*20.6*	*20.55*

13.2. WP2: System and circuit characterization and sensitivity analysis (WP leader: IMEC)

Work progress in task 2.1, 2.2, 2.3, 2.4 and 2.5

The increasing impact of process variations on design performance, particularly of the within-die (WID) random variations is becoming more and more critical in advanced nanometer technologies, at 65nm and below, as it was demonstrated by silicon characterization and variability analysis performed on specific test structures and during at-speed testing on several fabricated products. Statistical static timing analysis (SSTA) is a promising technique to deal with process variability on large multi-million gate System-on-Chip (SoC) designs, to decrease the pessimistic design margins based on worst-case PVT corners that are progressively reducing the benefits of technology scaling especially at 32nm and below, to improve the performances, and to increase the parametric yield.

Several problems have been addressed, firstly the process parameter selection for statistical characterization. Ideally, all the process parameters present in the transistor compact model directly impacting the library cell timing quantities should be used, but with an unaffordable characterization time and file size. We have developed in Task 2.1 a practical yet accurate characterization technique, where only a subset of these parameters are considered, still using the corner values for the other parameters. Secondly, also in Task 2.1 a methodology and flow for an efficient and accurate statistical characterization of industrial standard cell libraries have been exploited to characterize a complete set of cell libraries in the relevant Power Supply/Temperature corners in 65nm and 45nm CMOS low-power technology. The cell libraries are available and ready for exploitation, and can be used for the statistical timing analysis of digital blocks. Thirdly, in Task 2.3 analysis and simulation techniques for statistical timing analysis of digital logic blocks, taking as input data the circuit gate-level netlist, and the statistical standard cell libraries characterized. In this case, the target digital block was ILP, a mobile processor for imaging applications designed by the Imaging Division of STMicroelectronics, of about 370K nets with the fastest clock running at about 322MHz, designed in 65nm CMOS low-power technology. It is worth pointing out that ILP is an advanced design included into a real product.

The results obtained on ILP demonstrated that by using SSTA it is possible to remove some pessimism with respect to the corner-based analysis (which is the current sign-off methodology). This result is even more interesting since it was obtained considering only the lot-to-lot global variations instead of the WID random variations and it clearly demonstrate the process variations impact on performances even at 65nm. By considering the process random variations and their correlations it will be possible to potentially achieve a more significant pessimism removal. A very relevant result obtained with SSTA was that a few timing paths had the 3σ slack value smaller than their corresponding worst-case corner value. In this case, we may have potential timing violations that were not identified by traditional STA, thus causing timing failures during at-speed testing.

Regarding the statistical characterization of macro-blocks, their statistical characterization is more complicated than digital standard cell libraries therefore we have considered in Task 2.2 the use of the third party tool Extreme DA's ROAD. It creates a quadratic response surface model (RSM), and second-order polynomials are generated. The number of required simulations is known in advance and depends on the number of free variables, fixed corners, and accuracy, but not on the number of performances (cost functions or constraints). However, in case of strong performance non-linearity against a design variable it is possible to tighten the range of perturbation of the parameter. However, if the non-linearity depends on process parameters this is not possible and the model is not reliable. Hence, other solutions will be explored for the statistical characterization of macro-blocks, to assess the real gain we can achieve vs. the effort required to deploy this technique. Therefore new developments for Monte-Carlo based SRAM macro-blocks statistical analysis were also carried out on 45nm technologies. A comprehensive solution to evaluate how the statistical variation impacts the yield is under development. First Yield forecasts have been done on the READ cycle. The aim of this work has been to understand the impact of the variations on the designs and evaluate the needs of new development methods.

A SoC comprises high-level components such as processors, memories, accelerators, etc. The large majority of SoCs contains well defined register boundaries between any of these high-level components. This is not only needed for easy plug&play IP-level and architectural trade-offs but also to alleviate timing closure during the physical design phase. Even when the SoC is optimized across block boundaries during synthesis, these registers remain still in the synthesized netlist.

We have therefore formalized the SoC critical path delay to be the maximum of any the critical path of the combinational logic islands between registers, and this irrespective of their interconnection pattern: parallel, serial, tree-like etc. This assumption made in Task 2.4 is also applicable to each of the multiple voltage islands of a complex SoC even when each is operating each at different frequencies. The slack available in timing for each of the islands refer to the difference between their statistical longest path delay and the cycle-time of the frequency associated.

We have applied the variability analysis flow mentioned to a wireless protocol processor and characterized at the gate level. We have proceed for the whole processor at once (all 120 Kgates), and for each of its five pipeline stages one at a time. The purpose is to compare the statistics obtained when simulating the whole processor against the ones obtained by characterizing each of the stages and then using the product-convolution to obtain the full processor statistics. For this we have used the joint statistics between longest path delay and dynamic energy and leakage power respectively. Figure 3 displays the results obtained. Worth to mention that the five stages of the processor have been simulated considering the actual load and driving conditions of each stage as present in the complete processor netlist.

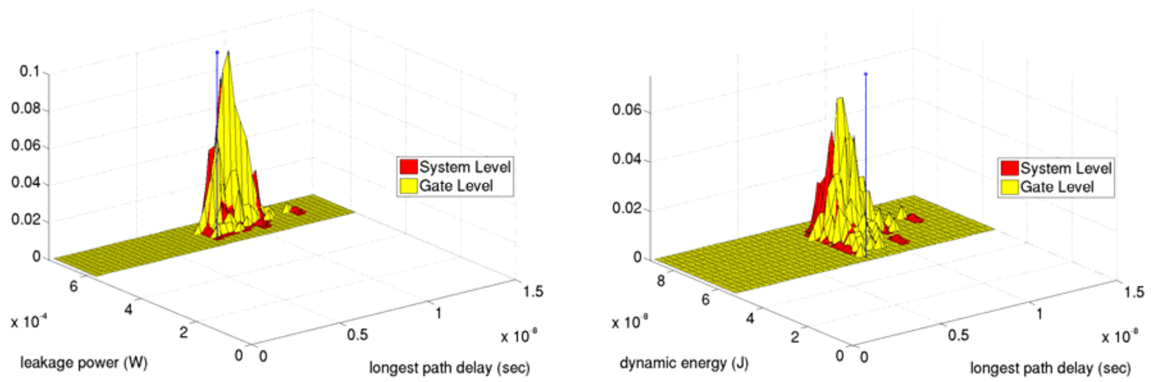


Figure 4 Comparison between full gate-level analysis and SoC-level analysis for joint PDFs: (a) dynamic energy and longest path delay; (b) leakage power and longest path delay

In this WP we also have started in Task 2.5 to look to various standardization efforts for the interfaces to transfer this information through different levels of abstraction. Variability propagation from process technology to analog simulations can be done in a number of ways and no standard is emerging yet in the industry. Similar considerations apply for the interface between standard cell calibration and digital simulation. Existing SSTA solutions use proprietary standards for the cell library characterized for variability.

Following with the unavailability during 2008 of the 32nm PDK, the statistical characterization and analysis activity has been focused on 65nm and 45nm CMOS low-power technologies. It is worth pointing out that these technologies are the most advanced ones currently available for production. Hence, the methodologies, tools, and flows evaluated and developed in 2008 in WP2 will also be relevant and exploited for 32nm CMOS low-power technology. The limited negative impact of the late availability of the 32nm PDK could be promptly recovered in 2009, taking advantage of the work carried out in 2008.

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*1.5*	*1.5*
IMEC	*10.8*	*10.8*
UNIBO	*0*	*0*
ST	*13*	*10*
KUL	*0*	*0*
ARM	*8*	*8*

TOTAL	*33.3*	*30.3*

13.3. WP3: Mixed mode countermeasures (WP leader: KUL)

Task 3.1 : Development of a formal method to analyze the effect of device level variability at the circuit level

Objectives task 3.1
In order to develop design-time and run-time solutions at circuit level, there is a need for analysis methods that link the physical phenomena (variability, time-dependent degradation) to the performance of these circuits. This requires the availability of good models that characterize the effect of degradation of device performance as a function of the applied stress levels, the device sizes and time. Such simple models are being developed in task 3.1 for hot-carrier injection and NBTI, based on physical analysis and measurement results. By means of these models, the reliability effects can then be propagated up to the performance of the circuit. This allows identifying weak spots in the circuit design. Some of these effects can be addressed to large extent at design time. Circuits will be modified at design time based on the analysis results to make them more robust to these phenomena. This is the subject of Task 3.2. Other effects, like the time-varying degradation, can only be solved at run time. The run-time methodology that we will follow in Task 3.2 consists of monitoring or measuring the effects on chip after fabrication, and then correcting the circuit through knobs (e.g. changing the supply or bias) or by changing the circuits through reconfiguration and/or recalibration. Advantage will be taken here of the abundant availability of small and cheap digital circuitry in the systems for signal processing, calibration, etc. The analysis method developed in this task allows identifying in the targeted circuits where monitors are needed and what the effects of the remedies (knobs, reconfiguration…) are. Furthermore, in this task formal analysis methods are created to perform the required analysis as described above. These methods will be incorporated in prototype tools if appropriate.

Work progress in task 3.1
a) Reliability Simulation Methodologies for Analog ICs

An analog circuit typically consists of tens to a few hundred transistors but is never as large as a common digital circuit. Digital circuits mostly switch between a single high and a single low signal level, which significantly simplifies the problem when trying to predict the circuit lifetime. In analog circuits all four nodes on every transistor can be subjected to any arbitrary voltage. Furthermore, most transistor degradation effects depend exponentially on the stress voltages. When trying to predict the degradation of an analog circuit, it is therefore very important to take into account the exact waveform on every node of the circuit. To calculate the exact signal waveform on every node of the circuit, a transient simulation must be performed. We are, however, interested in the behavior of a circuit over a time-span of a few years. Since the period of a typical analog signal varies from nanoseconds to milliseconds, performing a transient simulation on a circuit over a timeframe of a few months or even years is therefore not feasible at all.
Figure 5 gives a schematic representation of the developed basic reliability simulation method used in this work. The input to the simulator is a fresh (i.e. unstressed) netlist. To ensure a good accuracy, a transient simulation over some limited time is performed on the input netlist. The stress pattern on every transistor node is extracted and passed on to a degradation model to calculate the degradation of every transistor. The degradation model extrapolates the impact of the applied stress waveform to the desired circuit operation time. Finally, a degraded version of the netlist is created as an output of the simulator. A designer can use this degraded output netlist to study the impact of degradation on the circuit specifications.

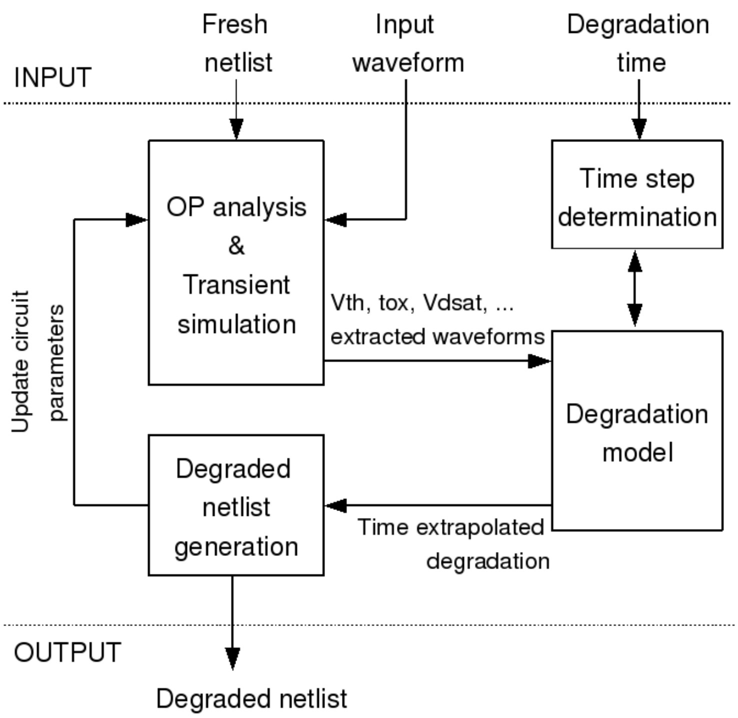


Figure 5: Schematic representation of the reliability simulation methodology.

To further increase the simulation accuracy, an iterative simulation method is adopted. The entire reliability simulation over degradation time Td is performed in smaller timesteps. These timesteps are automatically determined based on the variation of the observed circuit specifications. An error parameter determines the maximum procentual deviation of every system specification per timestep.

b) Modeling of Die-Level Degradation Effects for Analog Circuit Simulation

Hot Carriers (HC) and Negative Bias Temperature Instability (NBTI) are considered to be the most important phenomena for analog circuits. Both phenomena affect different transistor parameters (e.g. the threshold voltage and the output conductance). The time-dependent behavior of VTH can, for both HC and NBTI, be described as a power-law function of time:

$$V_{TH} = V_{TH0} + At^n$$
$$A = f\left(V_{DS}, V_{GS}, V_{TH0}, T, W, L, \ldots\right)$$

where VTH0 is the initial threshold voltage (for an unstressed device) and n is a degradation parameter related to the type of degradation effect (about 0.5 for HC and 0.18 for NBTI). A is a function of geometrical (e.g. L), environmental (e.g. temperature T) and process-related (e.g. VTH0) transistor parameters. Although we consider both degradation effects to be deterministic on there own (they are controlled by a deterministic diffusion process, degradation dispersion occurs due to statistical variations of process-related and geometrical transistor parameters:

$$\sigma^2\left(\Delta V_{TH}\right) = \left[1 + \frac{dA}{dV_{TH0}} t^n\right]^2 \sigma^2\left(\Delta V_{TH0}\right) + t^n \sigma^2\left(\Delta A\right)$$

The equation indicates how different, statistical transistor parameters induce dispersiveness in the degradation of different, identically designed, transistors.
Both NBTI and HC increase exponentially with the stress voltage. Therefore, the effect of time-varying stress signals must be included in the model to assure a sufficiently accurate degradation calculation. Also, prior degradation already present in the transistor must be taken into account. A general degradation model, valid for both NTBI and HC can be written as:

$$V_{TH}(t) = \left[\left(V_{TH}^{'}\right)^{1/n} + \left(C \exp\left(\frac{\beta V_{GS}}{\alpha} \right) \right)^{1/n} \left(t - t'\right) \right]^{n}$$

where V'_{TH} represents the degradation present at time t' and □ is a process dependent parameter, to be determined through measurements. □ is a parameter including the effect of time-varying stress signals with an average value V_{GS}. C is a parameter that is a function of other transistor parameters (e.g. V_{DS}, T, L, ...) and is different for either degradation phenomenon..

c) Degradation resilient circuits
Because of variability and degradation effects, is has become very difficult to guarantee the performance of high-end integrated circuits at design time. Traditional design methodologies (e.g. overdesign) to cope with this uncertainty, add an unacceptable power and area penalty to a design. This severely limits the low-power or high-performance operation of these systems.

The solution to this problem consists of the use of the Knobs & Monitors principle. Using this concept, the operation of a system is continuously monitored using on-chip monitor circuits. If needed, countermeasures to compensate for the changed performance can be taken by changing the settings of the knobs: since the (sub)systems are reconfigurable, their performance can be changed at runtime. The optimal configuration of the system, based on the inputs from the monitors and current specifications needed, will be determined by the on-chip controller. The knobs&monitors principle is currently being applied to an example circuit, a high-voltage line driver, in order to demonstrate the feasibility of the approach.

A high voltage output driver can be found e.g. at the output of an xDSL modem and is used to deliver a high output power in a (resistive) load at maximum efficiency. This efficiency is determined by the on-resistance of the transistors at the output of the driver. In order to achieve a high efficiency, high voltages are required at the output of this stage. These voltages cause degradation (HCI and NBTI) is the transistors at the output of the driver. This results in an increase of their on-resistance, yielding a decrease in efficiency of the resulting system. Hence the knobs&monitors principle can be used to keep up the power efficiency of the line driver, even in the presence of degradation.

Task 3.2 : Design of variability/reliability resilient memory IP blocks

Objectives task 3.2
In this task variability/reliability resilient IP blocks will be designed. Both design time and run-time techniques will be investigated and applied. Design techniques imply that the effects of variability and reliability are mitigated by the structure of the circuit itself. The run time techniques that we will apply are based on “monitors and knobs”. The effect of variability/reliability on delay-energy-robustness will be monitored. The result of this monitoring will then be used to adapt circuit properties e.g. the power supply voltage or back gate bias to compensate for eventual degradation. The coupling of the monitors can either be done at circuit level or at higher (system) level abstractions. Local compensation at circuit level is easier to implement but only takes the IP block under consideration into account. System-level compensation requires more advanced strategies but can find a system wide optimum.
The focus will be on memory circuits, which can largely be considered as analog circuits. The requirements for the memory blocks that will be studied will be derived based on system and architectural properties provided by the industrial partners. Statistical characterization of the delivered memory circuits will be performed to assess the metrics of this one in the context of the system architectural properties provided by the industrial partner.
During the design of the memory IP blocks the techniques developed in task 3.1 as well as more classical design methods will be applied. This will allow to asses the effectiveness of the newly developed design strategies.

Work progress in task 3.2

Design-time techniques

Several new circuit techniques are been investigated to improve the resilience of SRAM memories to uncorrelated intra-die variations. Up till now, the target memory specifications that have been considered are relatively small memories (16Kbit-1Mbit), with relatively short word length (16bit-64bit), operating at reasonable operation speeds (single-cycle, runtime configurable from e.g. 250MHz to 800MHz) while targeting minimal total energy consumption. All analyses up to now have been performed using commercial 90nm fab data and traditional mismatch models. Time-dependent effects have not yet been incorporated into the analyses. Both design-time and run-time techniques are being investigated.

The following design-time techniques to mitigate the impact of variations have been investigated :

- Dynamic cell stability has been improved with a write-back-after-read scheme to further relax cell requirements.
- Selective voltage scaling was adopted. Because the memory cells and word line hardly contribute to the dynamic energy consumption of a memory (2% to 5% of total energy consumption), the energy cost of increasing the associated supply during memory operation is small. However, the increased voltage greatly improves the operational margins for the cell.
- The impact of variations on the improved bit line structure was analysed. For identical memory cells, this bit line structure reduces the standard deviation of the bit-line delay from 14.4% to 9%, a 40% reduction.

Figure 6(a) shows the traditional implementation of hierarchical bit lines when combined with subdivided word lines. A pass transistor connects the local bit line (LBL) with the global bit line (GBL). The cell needs to develop a signal on the large GBL capacitance, which makes the cell read current a critical factor in the total memory access delay. At the column level, sense amplifiers amplify the voltage difference on the bit lines to a full level signal. In traditional designs, this amplification at the column level is required to limit the impact of Iread,cell on the memory speed. After this amplification, the data still needs to be transmitted to the memory output.

In the improved bit line structure with buffered LBL, the readbuffer can easily deliver more current. This allows the global bit lines to be extended to the memory output, as shown in Figure 6(b). A major advantage of this architecture is the fact that only one set of sense amplifiers is needed for the entire memory, rather than one set per column. This allows the use of more advanced sense amplifiers. This architecture also provides a performance improvement over the more traditional setup from Figure 6(a) and it enables the use of dynamic read stability.

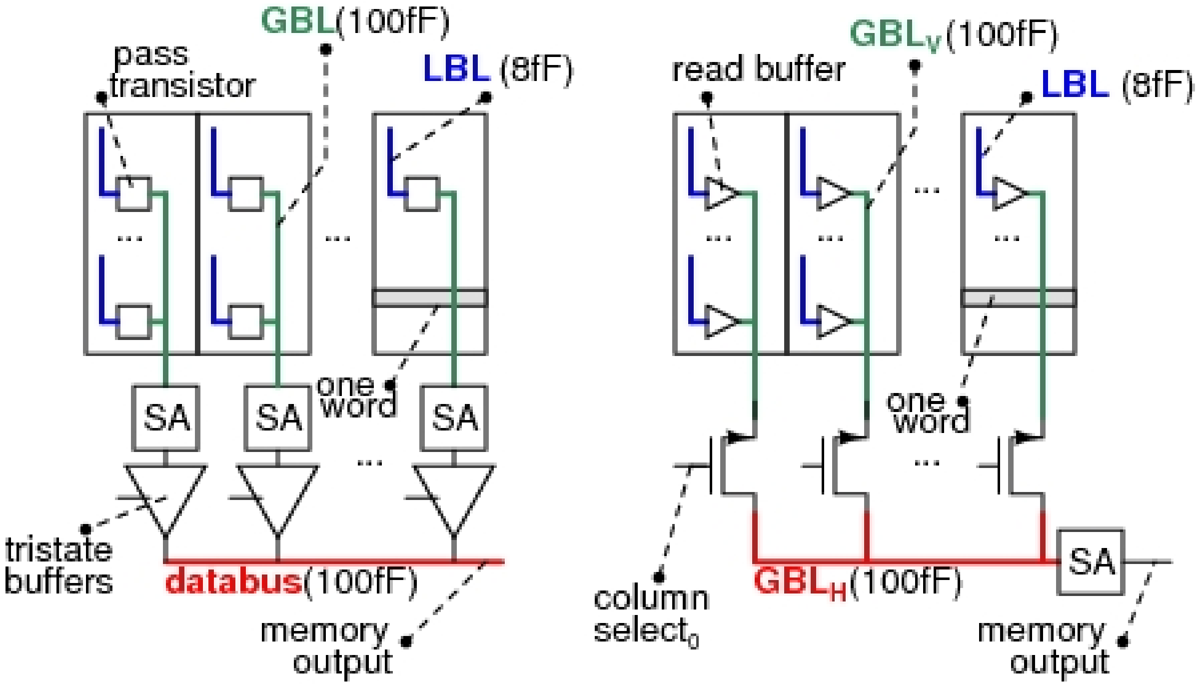


Figure 6: (a) Traditional solution (left); and (b) Proposed solution: readbuffer and extended GBL (right).

The insertion of a readbuffer between LBL and GBL greatly reduces the impact of the cell read current Iread,cell on the memory speed. This becomes especially beneficial in technology nodes with large intra-die variations. In these technology nodes, the cell read current varies widely because cell transistors must be kept as small as possible to preserve area. Another problem for Iread,cell occurs with low-power designs: to limit the amount of standby leakage, the cells must be implemented using high threshold transistors. This greatly reduces cell read current, and further aggravates the issue of variations. The readbuffer current suffers less from these intra-die variations for two reasons. The readbuffer does not have to use HVT transistors, and because the size of the readbuffer transistors has less impact on the memory area, they can be made somewhat larger.

Figure 7 shows the two simulation setups for which the performance under intra-die variations will be compared in the next paragraph. In the setup without readbuffer, a pass transistor connects LBL and GBL, and their precharge voltage must be equal. Due to cell stability requirements, the precharge voltage of the LBL cannot be close to 0V. A precharge voltage around vdd/2 would result in a problematic switch resistance because both NMOS and PMOS have only a small overdrive voltage at this source voltage. In this exercise, we use a 1V precharge voltage. In the setup with readbuffer, the precharge voltage on GBL can be selected independently from that of the LBL. In this setup, GBL is precharged to 0.2V. In both setups, it is assumed that the SAs require an input swing of 150mV to perform reliable sensing, so delay is measured from WL activation to 150mV swing on GBLH.

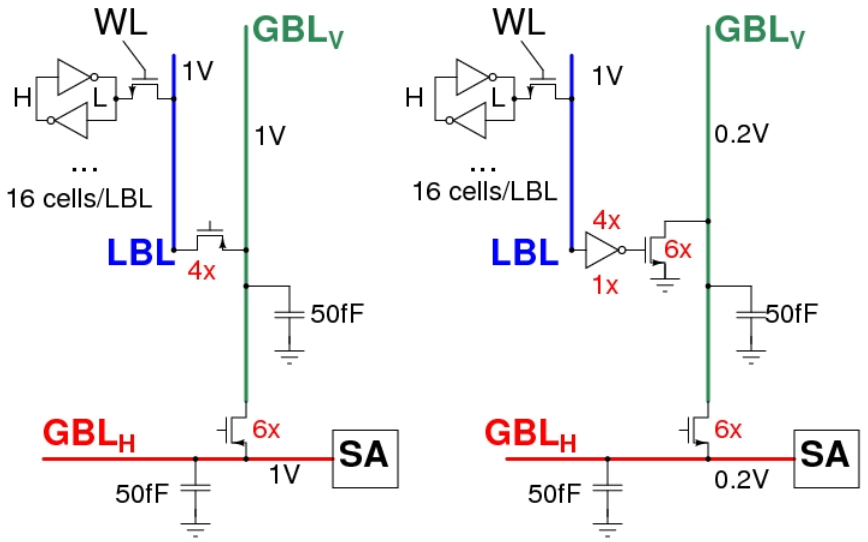


Figure 7: (a) Without readbuffer (left); and (b) With readbuffer (right)

20000 Monte Carlo (MC) runs were performed to obtain a good impression of the impact of intra-die variations. Figure 3-8 shows the resulting cumulative distribution of the delay for both setups. The nominal delay for the setup without readbuffer is 600ps, for the setup with readbuffer, it is only 400ps, so the readbuffer provides a significant speedup. The ratio of the 99.9% percentile to the mean value can be considered as a crude estimate for the sensitivity to intra-die variatons. For the setup with readbuffer, this ratio is delay99.9% delay50% = 126.5%, while it is 143.3% for the setup without readbuffer. The setup with readbuffer obviously suffers less from intra-die variations. Figure 8 also shows the normal distributions that have been fitted to both full datasets. Notice that the tail of the distribution is not well predicted by such a normal distribution. Also notice that safe operation requires a much higher percentile, e.g. 1 failure in 109 rather than 1 failure in 103, so the overhead due to intra-die variations will be twice as big as those numbers suggest (about 6 sigma rather than about 3 sigma).

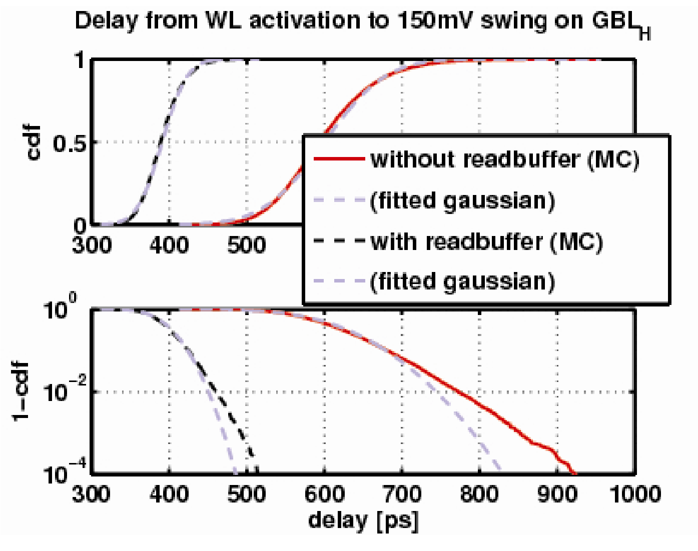


Figure 8 : Distributions of the delay from WL activation to 150mV swing on GBLH for the two setups in Figure 7 as obtained by performing 20K Monte Carlo runs. Gaussian distributions have been fitted to both full datasets. All curves are displayed both on a linear and a logarithmic scale.

Run-time techniques

Two run-time design techniques have been implemented: calibrated timing and sense amplifier tuning.

a) Calibrated timing

Calibration of the asynchronous timing circuitry allows to reduce the timing margins without introducing design risks. Traditional SRAM timing solutions do not cope well with delay changes under different supply voltages, such as used in dynamic voltage and frequency scaling. Calibrated timing allows to use optimal timing and voltage settings in each performance mode, adjusted to the
actual state of the die. The knobs for calibrated timing have been implemented. The monitor would consist of dedicated calibration accesses with ever more aggressive timing settings until failure is observed. Voltage regulation and the control algorithm have not been designed, as this is better handled at the system level.

b) Sense amplifier tuning

Sense amplifier (SA) tuning has been introduced as a better calibration method for SAs. This concept greatly reduces the energy that is needed to sense very small signal swings on the global bit lines. Figure 9 shows a setup of SA tuning with 16 reference voltage levels for tuning (4 calibration bits). These tuned SAs can sense a 40mV single-ended global bit line swing while consuming only 18fJ/bit, while traditional SAs without calibration require at least 7x more energy for the same input signal.

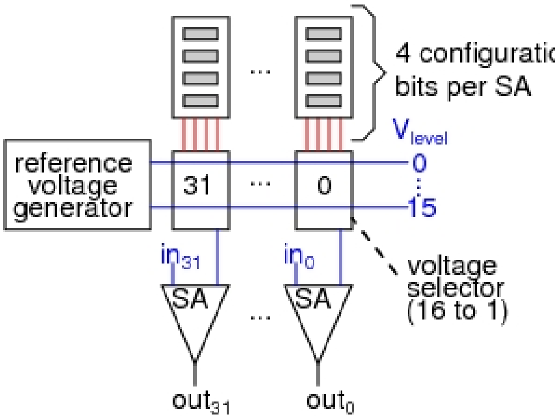


Figure 9: Setup for SA tuning (N=16 ; word length=32).

Figure 10 illustrates how such a scheme changes the effective offset distribution of the SA after tuning. The probability density function (PDF) at the bottom is the offset distribution for a normal SA. If a failure rate of 10−9 is acceptable, the SAs with native offset beyond 6.1 sigma can be discarded. Now we introduce tuning with two voltage levels (N=2). If a fabricated SA has a negative native offset, the offset is shifted by +Delta V . If the fabricated SA has a positive native offset, the offset is shifted by −Delta V , with Delta V = 3.05 sigma. The distribution after tuning with N = 2 is the sum of the two partial PDFs displayed in the figure. The effective offset range after tuning is only half of the native offset range. The same approach can be used with larger values of N.

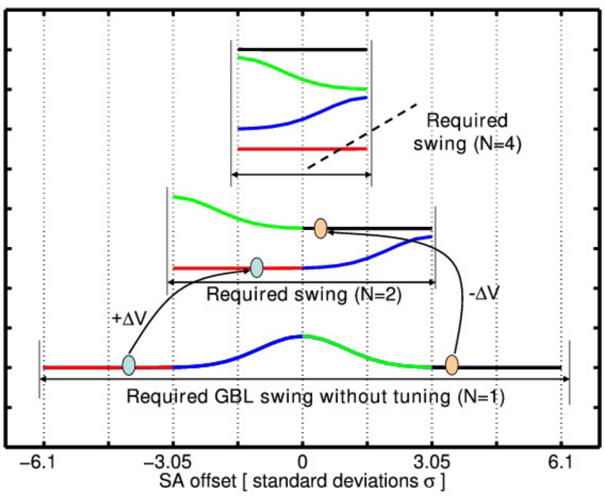


Figure 10: Effective offset of a tuned sense amplifier.

Tuning outperforms the previously proposed SA redundancy because it scales better to a higher number of calibration bits per SA, and because it reduces the effective SA offset after calibration more per calibration bit. The reference voltages can be generated on chip with a simple resistive divider if an appropriate SA is used, one that does not draw current from its inputs.

c) Automated test benches

Finally, dedicated automated test benches have been developed to analyse the impact of variations on the two most critical memory building blocks: SRAM cells and sense amplifiers. At this moment, a combination of linear response surface modelling (parameter sweeps) and monte carlo simulations is used.

Task 3.3 Development of architectural solutions for variability management of data path and controllers

Objectives task 3.3
The objective of this task is the development of architectural techniques for: (i) automatically identifying static and dynamic variations with limited performance/energy overhead; (ii) locally, and at run time modify/recalibrate the operation mode of the datapath and controller components in order to adapt to variations (iii) provide monitoring information and expose adaptation control inputs to the system level controller in order to enable optimized chip-wide run-time variability management.
For this purpose , the datapath and controller will be enhanced to implement the objectives of the task, using functionally redundant circuits with two purposes: (a) monitor and detect variations and provide information about variations to higher-level system controllers, (b) react to variations by modifying the operation of the circuit (e.g. reducing operation frequency or extending completion time) either autonomously or under control inputs provided by the system controller. The enhanced components will be modelled and simulated to explore the trade-off between monitoring and tuning versus latency/bandwidth/energy penalties.
The outputs of this task are:

- Methodology for enhancing datapath and controllers for increased variability tolerance
- Definition of error monitors and control knobs and their interface with the system controller
- Trade off exploration of costs/benefits of the proposed solutions

Work progress in task 3.3
This year the activity of UNIBO focused on the development of architectural countermeasures for datapath and controller variability tolerance (Task 3.3). To this purpose, UNIBO explored two approaches, namely Adaptive Voltage Supply (AVS) and Adaptive Body Biasing (ABB) and investigated in depth the cost/benefits of both. We developed two innovative AVS and ABB techniques. We identified the ABB technique as the most suitable solution for the integration in the target demonstrator developed in WP5. This techniques has been called “Physically Clustered Forward Body Biasing”. Variability characterisation information provided by WP2 for the reference target architecture of this project will be exploited to tune the proposed technique.

Concerning AVS, we designed a placement driven VI generation, which aims at the minimum modification of performance pre-optimized placements through the grouping of physically adjacent cells into the same voltage island. Moreover, we precisely quantified the level shifter overhead and its impact on total system power and area for an industrial 65nm technology library. Nonetheless, we proved the viability of the voltage island approach to deal with process variations by assessing the power savings with respect to chip-wide supply voltage adaptation.

The main drawback of this technique is the area overhead of level shifters. Even though all advanced technology libraries include level shifter cells to support signals across voltage islands, these cells have an area, timing and power cost. Level shifters are an affordable cost in coarse-grained core-by-core voltage island clustering. Our fine-grained approach does support re-synthesis with insertion of level shifters, but we found that preservation of the original cell placement becomes impossible. Iterative re-synthesis allowed us to converge to a clustered solution meeting the design constraints, but in our experiments significant designer intervention and effort was required to achieve final convergence on all design constraints.

Our characterization experiments performed on the VEX processor show that the contribution of level-shifters to total power is limited to at most 5% of total processor power. Indeed, the considered technology libraries are optimized for low power and for this reason leakage power is not a major concern. However, as mentioned before, the main drawback of AVS is the area overhead. Our experiments indeed show that the impact of level-shifter insertion on logic chip area is around 30%.

Our first objective in REALITY is to privilege post-silicon tuning techniques that can be applied with minimal designer intervention within the synthesis flow. For this reason, we explored ABB as an alternative solution for the final integration in WP5.

In our methodology, to compensate the slowdown, we need to sense the timing of the circuit block to find if it is necessary to apply FBB and how much voltage is required to compensate the circuit slowdown. Process variation induced timing failures are static in nature and require only one-time compensation in contrast to temperature and circuit aging induced timing failures which are dynamic in nature. In order to track timing failures caused by dynamic effects, one has to periodically sense the circuit timing and then trigger a control circuitry which then generates optimal body bias voltage to be applied to the design under consideration.

Our ABB methodology is compatible with various timing sensing approaches. However, we believe that in aggressively scaled technologies it may be difficult to ensure strong timing correlation between critical path replicas and the actual critical paths in the circuit, hence we assume that timing-monitoring (also called crystal ball) flip-flops are used for timing sensing.

In general ABB (FBB and RBB) techniques have very low implementation area overhead which makes them preferred choice for post-silicon tuning. Here we assume we have a 50mV resolution from the body bias generator. So we have 11 different vbs values at our disposal, for NMOS starting from 0 to 0.5V in steps of 50mV and for PMOS starting from 0.95 to 0.45 in steps of 50mV. Figure 11 shows a block diagram summarizing our tuning methodology. As shown in the figure, there are 4 circuit blocks in a design each having a Tci (*i* indicating the block number) which indicates a timing violation in the block. The central body bias generator generates appropriate body bias voltages (in the figure, number of vbs=2) to compensate the slowdown in the block.

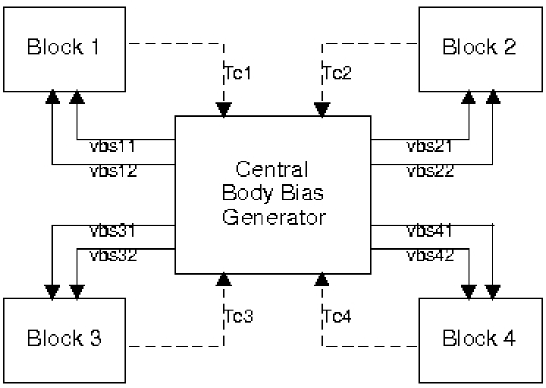


Figure 11: A block diagram showing FBB implementation methodology

We designed two algorithms for optimal body bias allocation, the first one is an exact solution where we cast the problem into an ILP to find the optimal clusters with their respective body bias voltages. In the second algorithm, we propose a two pass linear time heuristic to solve the same problem. In both the cases, the body bias clustering problem can be defined as follows.

Given a placed design with a set of rows, partition the design into C clusters (each with a sub-set of rows), each with its own body bias voltage such that the overall timing is met while minimizing the leakage power.

We implemented also a linear run-time heuristic, to solve the FBB clustering and allocation problem. It is a two-pass greedy algorithm based on timing sensitivity of the rows in the design.

More details about both techniques and their implementation can be found in D3.3.

Work progress in task 3.4
In preparation to the task of modelling interconnects be enhanced to implement the objectives of the task, using functionally redundant circuits with two purposes: (a) monitor and detect variations and provide information about variations to higher-level system controllers, (b) react to variations by modifying the operation of the circuit, ST has analyzed the advantages and drawbacks of various schemes aimed at inserting monitoring features into ST's proprietary interconnects technologies (STBus and STNoC). In order to enable the study of the architectural enhancements an initial high level model for a generic interconnect to be plugged into the REALITY simulation platform (part of WP5/6) has been defined, this will be further enhanced with the simulation of the countermeasures that UNIBO will produce in the rest of this task execution.

Use of resources

Partner	Planned effort (MM)	Actual effort (MM)
UOG	*0*	*0*
IMEC	*0*	*0*
UNIBO	*11*	*11*
ST	*1*	*1*
KUL	*16.6*	*16.6*
ARM	*0*	*0*
TOTAL	*28.6*	*28.6*

13.4. WP4: System level countermeasures (WP leader: UNIBO)

Main activities in this WP4 concerns the development of software techniques for hiding the effects of variability on the system. In order to carry on this work, the following information have been determined in the early stage of the project. First of all, the architecture of the platform have been defined as part of WP5. The consortium decided to focus on a multi-core platform for embedded multimedia applications. A simulation model was made available to UNIBO on M3 of the project and since then UNIBO started the development of the software infrastructure needed to develop the software level countermeasures. The infrastructure is composed by a library and a runtime engine for supporting: i) multiprocessor communication and synchronization based on message passing support and semaphores; ii) task migration. This infrastructure has been implemented directly on the target validation platform for REALITY project.

Work progress in Task 4.1 and Task 4.2
The software organization of our system is composed by support functions for task loading, data communication and synchronization, statistic collection. All the cores load the same program, following a SPMD (Single Program Multiple Data) approach, where each core executes a different portion of the program depending on its identifier. The accelerator code contains all the possible tasks to be executed. The program executed by each core contains a main loop from which all the function are called, depending on a schedule decided by the master core. In the final version of the support software we will consider also the implementation of local schedulers. Currently, dynamic loading of tasks is not supported. As such, to execute a certain task, cores have to jump to the related code portion, which is identified by a pointer. To control the execution on the accelerators, the master core changes the pointer depending on which task the accelerator has to run. Shared memory is used to exchange data among cores. Currently, semaphores are also allocated in shared memory.

Message passing and synchronization. Concerning synchronization, since the target platform currently does not provide hardware semaphore support, they have been implemented in software using the Peterson's algorithm.

As regards message passing, we ported the MPQUEUE library developed by University of Bologna for an ARM7-based simulation platform (MPARM). The choice of this library for REALITY project has been dictated by its extreme flexibility and customizability. For instance, semaphores can be allocated either in shared memory or in core private memories and support interrupt based notification mechanisms. The library provides 1-N, N-1 and N-N communication paradigms, where synchronization between producers and consumers is achieved thanks to the software semaphores above mentioned.

Task allocation. In the current implementation, only static loading is supported on the slave cores. I.e., the code to be executed by slave cores is loaded in their private memories before simulation starts. The master indicates also the shared memory location where the slave can retrieve the data to be elaborated.

Task migration. To enable a fully dynamic task allocation, a task migration strategy has been implemented. The design of a task migration strategy for embedded systems is a critical issue because it cost depends on the efficiency of the memory transfers performed to move the context of a task from a processor to another one. Main requirements are: i) predictable and negligible overhead; ii) controllability and flexibility so that the programmer can optimize the migration mechanisms to the underlying architecture.

In order to improve predictability and ease context transfer, we implemented a checkpoint based strategy where the migration is allowed only on migration points defined at compile time. This eases predictability because of two main reasons. First, the possible migration instants are known in advance; ii) migration points can be placed by the programmer or by the compiler in such a way to minimize the amount of data to be moved. Moreover, in this implementation we do not have to move the function code, as it is replicated on all the cores. This further reduces migration costs, even if it increases memory occupation. This assumption will be eventually removed on the final implementation depending on the evaluation of migration costs in the final target platform. Migration points are implemented as function, made available to the programmer as a migration library.

To validate the support, UNIBO developed a preliminary software policy and a number of workload models close to the final benchmarks for validation that were not still available at that time. This work has been reported in D4.1 on M9, which is about software infrastructure development.

Currently, UNIBO is working to achieve the tasks included in the next deliverable D4.2, concerning the development of software policies for hiding variability effects. In order to design meaningful policies for the system targeted in this project, the following information has been collected during this first year of the project: i) what type of variability information will be available from the other work-packages; ii) what types of benchmarks and metrics will be used for policy evaluation and validation. This information allowed to perform a preliminary description of policy scenarios to be used for WP4 evaluation on WP6 and to defined the needed validation infrastructure to be developed in the target simulation system during WP5. This information has been included in deliverable D5.1 and D6.1.

Concerning the first point, UNIBO will exploit information provided by WP2. Based on that, two classes of policies can be developed. First, a class of policies will be devoted at hiding as much as possible the performance and energy impact of variability by playing with allocation and scheduling of tasks, core clock frequencies and voltages. This class of policies do not consider aging issues.

A second class of policies will be developed that take aging into account. In this case, the scenario for variability/reliability compensation will be based on a what-if analysis case. Thus, assuming the variability information model coming from WP2 being applied to each of the SoC components and later evaluating the feasible range for compensation assuming a correlated drift of such variability data in the performance axis as function of lifetime. Since this drift will depend on voltage and temperature conditions, a subset of relevant operating points (i.e. temperature and voltages) will be selected as corner cases for this analysis.

We started the development of the first class of policies during the last months of this year and we obtained preliminary performance and energy results in two configurations: single clock domain and multiple clock domains.

Work progress in Task 4.4

In the last two months of this year, UNIBO started the development of a back-of-the-envelope approach in order to perform policy evaluation for different voltage and temperature combinations.

This approach has been exposed and agreed on with IMEC and ST, UINBO and ST have also started the definition and design of an integrated simulation platform enhancement to perform fast estimation of variability trends of the system. Its accuracy will be validated against the reference flow resulting from WP2, and deployed in WP6

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*0*	*0*
IMEC	*0*	*0*
UNIBO	*30*	*30*
ST	*2.5*	*2*

KUL	*0*	*0*
ARM	*0*	*0*
TOTAL	*32.5*	*32*

13.5. WP5: Design flow, integration, proof of concept (WP leader: ARM)

The REALITY project is an opportunity for the industrial partners to broaden their understanding of the variability issues we will face in the next generation semiconductor manufacturing technologies. For designers two main topics are quite crucial in this era. On the one hand we are looking at design characterization methodologies and on the other hand we are evaluating counter measure solutions developed on the different work packages:
During this period an important effort has been spent to accurately define the scope of the evaluations to be carried out. Two main test vehicles are analyzed: an ARM926 processor and a xSTream processor.
We also started evaluating the statistical aware characterization tools in order to put in place a way to analyze the variability sources and their impacts on the design at the library level up to the system level. The analysis of commercial variability aware tools was done using as a basis in house available 45nm designs. The tested tools must now be evaluated on the 32nm technology. This paves the way to validation plans to be carried out in the future.
A substantial effort has been spent in the integration work of the outcomes of WP3 and WP4. The relevance of the counter measure solutions will hereby be assessed.

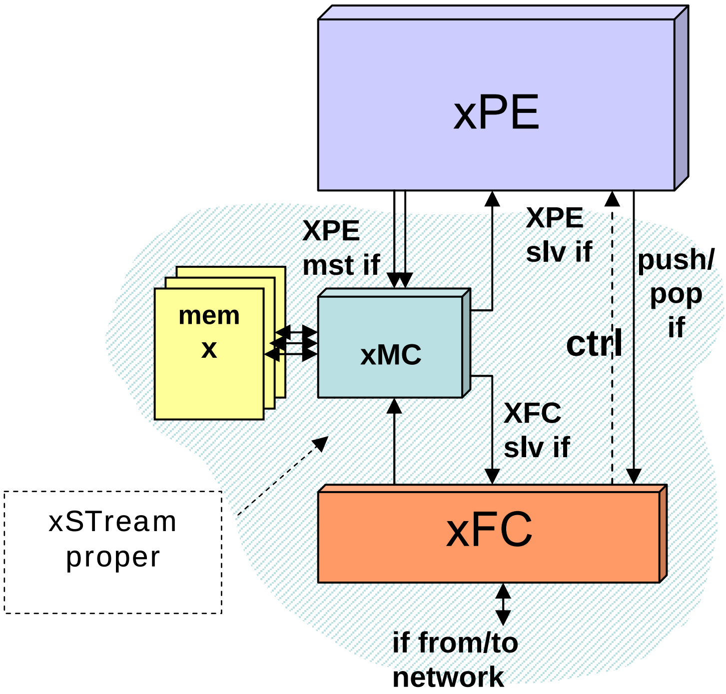
Work progress in Task 5.1:
The circuit level components to be used for the evaluation of WP 1, 2 ,3 ,4, 5 and 6 have been defined. A simplified library containing between 50 and 100 cells has been provided for the evaluation. The library allows a synthesis of system level designs defined in task 5.3.

Work progress in Task 5.2:
In the task 5.3 the partners defined two system platforms for the integration work. The specificity of these systems defined two different sets of macroblocks.
First to allow the synthesis of the ARM926 soft core a collection of SRAM architectures needs to be implemented and generated:

Name	Ports	Port Width	No. of entries
I$ DATA	1R/W	32	1024
I$ TAG	1R/W	22	128
I$ VALID	1R/W	24	32
D$ DATA *	1R/W	32	1024
D$ TAG	1R/W	22	256
D$ VALID	1R/W	24	32
D$ DIRTY	1R/W	8	128
MMU13	1R/W	30	32
MMU02	1R/W	26	32

Second ST has identified a suitable set of IP blocks that support the statistical characterization flow, the interfacing with the higher level controls and SW countermeasures for variability tolerance, some of the IP contributed to this end are:

- STNoC Router
- STNoC NI (Network Interface)
- xDMA a flexible DMA engine with native support for streaming programming models, open to future enhancements such as CC transactions, security, etc.
- xBridge: An added value optional component that support sophisticated interactions between the xSTream engine and the rest of the system
- xFC: An application level (in a ISO/OSI sense) block that implement a virtual queue/data-flow oriented communication semantic
- xPE: a streamlined, templated high performance, low power & area compute engine for massive distributed parallel fabrics



- Wrappers to support legacy, external IPs and/or HW based coarse/middle grained functions and accelerators

Simplified block diagram for a single node of the computing array: the xPE is the processing engine while the xMC is the local node memory Controller

Work progress in Task 5.3:
This task was dedicated to the definition of a system platform suiting able to allow the evaluation and validation of WP2, 3 and 4 within WP5 and WP6. The initial strategy proposed to the partners was to create a heterogeneous system incorporating an xSTream processor from ST as well as an ARM926 processor. This solution was replaced by two separate platforms because of the unavailability of a cycle accurate model for the ARM926 as well as the unnecessary complexity of the integration work.
The first system platform proposed is the ARM926 strand alone processor. This system is widely spread in the industry and therefore represents an industry standard. The ARM926EJ-S contains a 32-bit RISC processor (the ARM9EJ-S) and a supporting debug/trace and L1 memory sub-system. The L1 memory sub-system implements an MMU for physical to virtual address translation plus caches for instruction and data storage. External interfaces include those for the Embedded Trace Macrocell, external co-processors, Tightly Coupled SRAM Memories and AMBA AHB Bus interfaces.
The second platform is the multimedia system level microarchitecture template. The platform defined and deployed within the REALITY project for benchmarking of multiprocessor heterogeneous SoC is based on a subset of the STM's xSTream platform template, namely the IPs leveraged are: the programmable elements xPEs, the local nodes memory controllers xMC and a version of the interconnect that is either a full fledged network on chip bus (STNoC) or a more conventional splitted transaction bus (STBus), to cover for the host functionality a general purpose media engine from ST has been identified (ST231), that is going to be deployed for the control parts of the demonstration platform SW components, while the focus of the variability aware system level countermeasures is going to be on the distributed processing nodes.

Work progress in Task 5.4:
In the scope of this task commercial characterization tools have been integrated in a classical library development flow. The tools have been successfully installed and could characterize subsets of 45nm standard cells libraries. The evaluation of the tools on 32nm technologies has to be performed and the impact of the variability on the cells performances must now be analysed.
What is more, the aim to switch to a statistical modelling is to get a better description of the systems. A validation work has started to check the results of the tools compared to heavy but very accurate characterization methods.

Work progress in Task 5.5:

The necessary RTL developments to incorporate the output of WP3 and WP4 in the system platform have to be carried out in the scope of this task. The initial single platform strategy has induced some preliminary work within this task which has been stopped now waiting for a clear identification of the necessary RTL development to incorporate countermeasures.
To integrate some of ST's contributed IPs RTL work was required to adapt the platform interfaces to the REALITY system platform requirements. In addition to this the models of the IP were extended to accommodate the monitoring and recording of certain real-time metrics such as idle cycle counts, active time windows, etc. this in order to carry out the system level integration of the simulation platform with the models developed in T5.4 for the variability analysis. As an example the models for the programmable accelerators cores (xPEs) where enhanced with the capability of supporting a variable frequency operation, in light of the requirement of WP4 SW countermeasure scheduling policies.

Work progress in Task 5.6:
To accommodate timing constraints from progresses in WP3/4 this task's work has been started 2.5 months earlier than originally planned by ST's contributing a full fledge simulation environment capable of modeling the system level and IP blocks at different levels of abstractions; this platform needs various enhancements and extensions to accommodate the WP6 validation tasks and gathering of the required figures of merit to compare against the uncompensated case. The xSTreamISS environment provides composable models for: ST231 host processor, ST231-xPE processor (ST231 + streaming operations) and xPE accelerators, in addition to memory and bus models at different level of accuracy.
The model of the xPE accelerator has been perfected, so as the ST231-xPE processor in the first phase of the WP5 execution.
Concerning the xSTreamISS proper, the major implementations/modifications have been:

- Creation of the MMU device for the ST231 model, since it is required to run an operating system
- Creation of the timers devices for the ST231, ST231-xPE and xPE models
- Implementation of the multi-threading support for the xPE models
- Core models modified to support clock frequency modifications at runtime
- Implementation of a write buffer device
- Implementation of an interconnection model to make the gap between the C-based model and the SystemC based model smaller
- Started tuning of latencies
- Improvement of simulation performances
- Improvement of the user interface

For the systemC modeling platform:

- Finished/tested the STNoC integration, through an automatic checker device
- Started a simulation performance estimation and optimization

Use of resources

Partner	Planned effort (MM)	Actual effort (MM)
UOG	0	0
IMEC	9.12	9.12
UNIBO	1	1
ST	9	10
KUL	0	0
ARM	13.4	13.4
TOTAL	32.52	33.52

13.6. WP6: Validation and assessment of results (WP leader: ST)

Work progress and achievements during the period
During the first year of execution of WP6 activities, the work has progressed mainly for tasks T6.1, T6.2, T6.3 and T6.5.1, allocation of resources to task has been aligned to expected levels from the DoW.

In the context of WP6 validation tasks, the initial planning of WP5 platform definition and integration activities was based on the premises of only one industrial platform that integrated both the host IPs and blocks provided by ARM and the STs contributed IPs. This plan was later on changed because of an intervening lack of the continued availability of a suitable simulation environment capable of supporting an integrated modeling of all of the IPs required. As a consequence, the partners of REALITY have agreed to validate the technologies and methodologies developed with two separated flows for the multimedia (STM) and general purpose (ARM) platform components. For the multimedia scenarios, a suitably defined simulation platform based on the REALITY platform definition tasks of WP5 will be made available. Such simulation platform provides a set of parallel media acceleration engines from STM (called xPEs) and an STM proprietary host processor, ST231, supporting Linux and a suitable run-time environment for the accelerators.

Once this has been clarified, the WP tasks have progressed towards the second year stage of the WP execution mainly by the identification and definition of the application and their requirements, the identification of criteria and evaluation metrics for the components and methodologies and the initial phases of gathering the required data for the definition of the project validation plan.

Additionally, task T6.5.1 associated to application porting and mapping was started earlier than expected because of the need to provide an adequate early input to second year tasks.

Objectives in Task 6.1
Identification of industrially relevant demanding applications and associated requirements to provide inputs to WP1, 2, 3, 4 and 5. This task will ensure that key parameters and requirements are identified to ensure comprehensive coverage and evaluation of useful scenarios with a large potential industrial impact. (ST/ARM).

Work progress in Task 6.1
An accurate analysis of the industrial applications landscape has been performed by ARM and STM that identified a short list of candidate applications and associated requirements that will be used for the IP and system level validation tasks in the second year. The focus has been to identify industrially relevant media code to drive the benchmarking and validation process; and because of the timeframe and available resource constraints, the selection has been made on a reduced set of consolidated industrial applications that will be ported on the target platform. The selection process has lead to identification of an MPEG2 parallel decoder and an AC3 parallel audio decoder, as well as a standard set of general purpose performance benchmarks such as Dhrystone.

Highlight: A reference implementation of the application has been made available

Objective in Task 6.2
Identification of criteria and evaluation metrics for the components and methodologies in WP2, 3, 4,. This task will ensure that key metrics are identified that are required to both drive the design process and evaluate the results in WP6. (ARM/ST/UniBo/IMEC/KUL/UoG)

Work progress in Task 6.2
Work has been carried out to provide information on expected outcome from WP2 to feed variability and reliability models of platform components defined in WP5, for example what is been produced is a list of important parameters and metrics associated to the VAM flow and its deployment for the project validation tasks. Some of those parameters are the number of samples in the input space, the number of Monte Carlo iterations to be done in transformation box, etc. Additional criteria identified are the classification and containment of different sources of errors when the flow will be applied to the project developed IPs; this last topic it's especially meaningful given that the project can't provide a silicon demonstrator.

Objective in Task 6.3
Definition of a validation/verification plan according to the system level microarchitectures defined in WP5, based on WP3,4 deliverables, this involve a description of how the various blocks and circuits will be evaluated and according to what metrics and objective/qualitative functions (ARM,ST/IMEC/UniBo/IMEC/KUL/UoG).

Work progress in Task 6.3
The aim of this task is the definition of a validation plan for the integration and benchmarking activities of the project, incorporating outputs of modeling from WP1, and providing feedback to tasks of WP2/3/4.

Suitable figures of merit and estimation of objective functions, for example in terms of tolerance to variation of critical process parameters, as well as modeling of individual circuits, have been derived from WP1/2/3

and will be validated with the platform models as defined by WP5. As far as possible simulation based quantification will be the objective, but where this is not possible, qualitative conclusions will be offered or mixed models can be developed to integrate analytical and qualitative approximations into simulations as defined.
The objective of the validation plan is to clearly state as the various contributions come together and how the overall results will be evaluated and exactly what kind of metrics will be developed.

The validation plan should be structured along two main lines:

One defining how to evaluate and benchmark the block level IPs integrating components and design flows produced in WP2, WP3, and WP4, this might for example include ARM processors cores and programmable accelerators from ST retrofitted with such technologies with contribution from ARM ST, IMEC and UniBo. (T6.4)

A part of the plan has been defined aimed at analyzing how the statistical design flows can be integrated in the traditional flows. ARM expects to benchmark the VAM flow using information from IMEC, in addition to commercially available statistical characterization flow. The focus is on defining criteria for library and system levels.
On the final system, the impact on the IPs footprint must be assessed with and without countermeasures. It's expected that the solutions developed in WP3 will have a minimal timing/power impact. As a consequence, ARM proposed to analyze the impact using 3 different means:
1. Impact using the traditional characterization flow.
2. Impact using one statistical characterization flow to be defined with the partners
3. Impact using statistical flow but taking into account different scenarios. This should validate the counter measure efficiency. On these, timing, static power and dynamic power impacts will be measured.

The second part of the validation plan covers (T6.3) the definition of how the system level microarchitectures defined in WP5, based on WP3,4 deliverables should be benchmarked; this involves a description of how the various blocks and circuits will be evaluated when aggregated together in the prototype simulation platform in terms of:

- Metrics: Performance (variability impact compensation), Power consumption, Energy consumption and Reliability (aging tolerance)
- Software and Hardware Knobs, such as:
    - Task allocation on the different cores,
    - Task scheduling on the same core,
    - Task migration from a core to another one,
    - Global frequency scaling (single domain),
    - Independent frequency scaling (independent core level domains) , Idleness distribution (clock gating),
- Workloads: different kinds of task graphs, task communication patterns, streaming models, different metrics for execution time, throughput, and deadline miss rate, etc.
- Operating conditions: three values of power supply voltage: Vdd1, Vdd2, Vdd3 to be determined; two values of temperatures: Tmin and Tmax, to be determined.

Highlight: Initial definition of validation scenarios

Objectives in Task 6.5.1
Porting of application benchmarks selected in T6.1 for both the host ARM926 and the subsystem composed of STM's xPE accelerators to the system level simulation platform, this includes application mapping and partitioning onto the multiple platform IP blocks and integration with the SW runtime heuristics and countermeasures defined in WP4 (ST/UniBo)

Work progress in Task 6.5.1
This task was not originally part of the plan, but became apart it was needed during execution of WP4/5/6 tasks, work on this task has already started during last two months of the first year by ST.
The multimedia applications deployed need to be parallelized to fully demonstrate some of the added value in terms of variability tolerance and objective function improvements (e.g. yields, power consumption, performance),.

An initial planning on how this work will take place has been carried out, as well as identification of the required run-time support and APIs to be implemented and supported for WP4 tasks (e.g. threading API, run-time scheduler), and WP5 simulation platform enhancements (e.g. variable Voltage/frequency modeling, variability modeling, etc.)

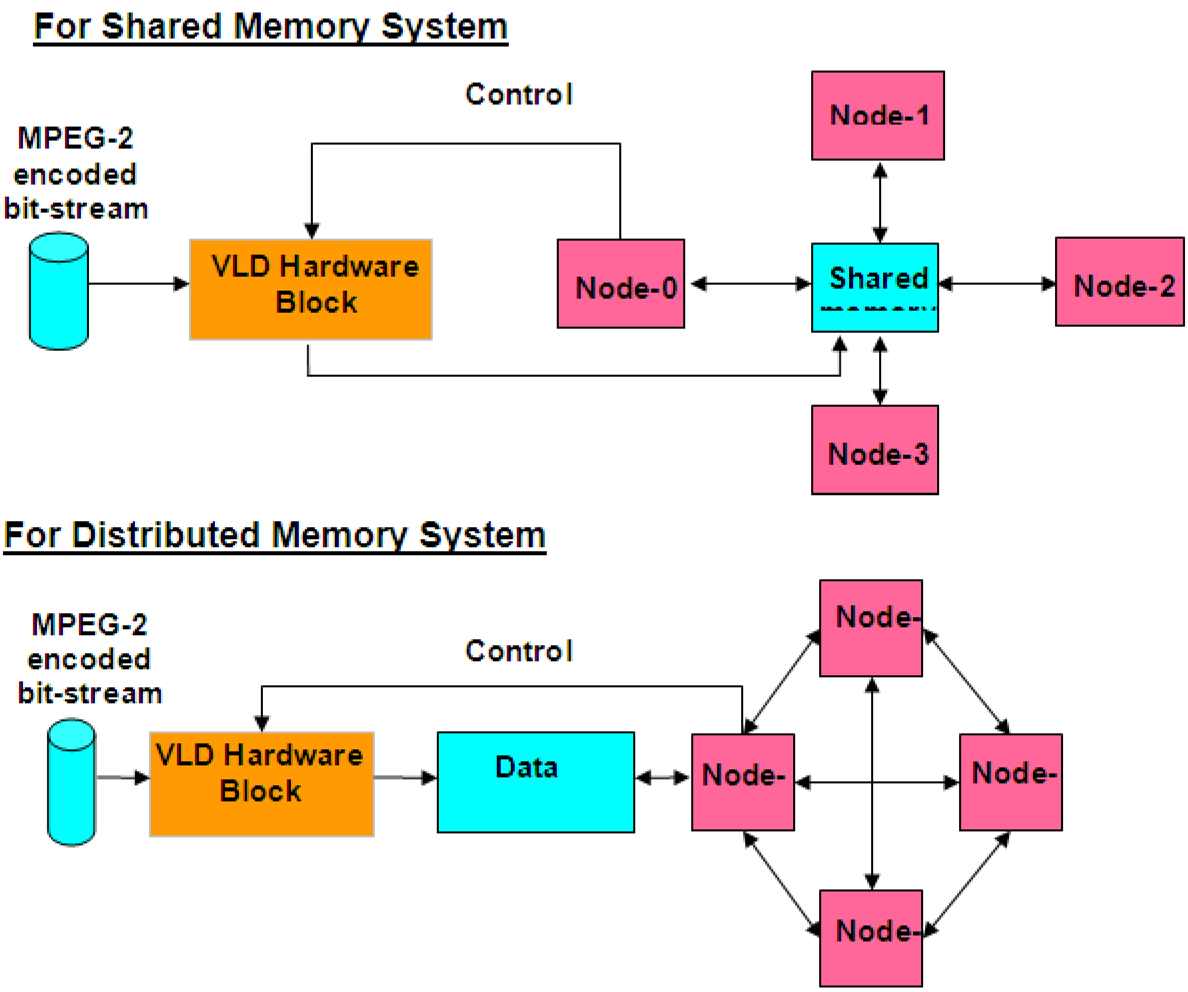


Figure 12: MPEG-2 Decoder : Scheme for parallel implementations in T6.5.1

Use of resources

Partner	*Planned effort (MM)*	*Actual effort (MM)*
UOG	*3*	*3*
IMEC	*2.4*	*2.4*
UNIBO	*1*	*1*
ST	*6*	*6.4*
KUL	*0*	*0*
ARM	*3*	*3*
TOTAL	*15.4*	*15.8*

WP7: Project management (WP leader: IMEC)

A description of the work in this work package can be found in section 15 on project management.

Partner	Planned effort (MM)	Actual effort (MM)
UOG	0	0
IMEC	4.8	4.8
UNIBO	0	0
ST	0.5	0.63
KUL	0	0
ARM	0.3	0.3
TOTAL	5.6	5.73

WP8: Exploitation and Dissemination (WP leader: IMEC/ARM)

A description of the work in this work package can be found in deliverable 8.3 which is the dissemination and use plan. This deliverable contains the work of all partners.

Partner	Planned effort (MM)	Actual effort (MM)
UOG	0	0
IMEC	1.56	1.56
UNIBO	1	1
ST	2	0.62
KUL	0	0
ARM	1.1	1.1
TOTAL	5.66	4.28

14. Deliverables and milestones tables

Deliverables

TABLE 1. DELIVERABLES									
Del. no.[1]	Deliverable name	WP no.	Lead beneficiary	Nature [2]	Dissemination level [3]	Delivery date from Annex I (proj month) [4]	Delivered Yes/No	Actual / Forecast delivery date	Comments
D1.1	Variability simulation and comparison for the 45 nm technology generation	WP1	UoG	R	PU	T0+12M	Yes		
D2.1.1	Creation of a scaled down library	WP2	IMEC	P	RE	T0+8M	Yes		First split of delivery D2.1: a preliminary cell library was developed to anticipate the 32nm data availability.
D2.2	Report on methodology for percolating	WP2	IMEC	R	PU	T0+12M	Yes		

[1] Deliverable numbers in order of delivery dates: D1 – Dn
[2] Please indicate the nature of the deliverable using one of the following codes:
R = Report, **P** = Prototype, **D** = Demonstrator, **O** = Other
[3] Please indicate the dissemination level using one of the following codes:
PU = Public
PP = Restricted to other programme participants (including the Commission Services)
RE = Restricted to a group specified by the consortium (including the Commission Services)
CO = Confidential, only for members of the consortium (including the Commission Services)
[4] Month in which the deliverables will be available. Month 1 marking the start date of the project, and all delivery dates being relative to this start date.

	variability sensitivity								
D3.1	Report describing the methods to assess device level variability at the circuit level	WP3	KUL	R	CO	T0+M12	Yes		
D3.3	Report: techniques for enhancing data path and controller variability tolerance	WP3	UNIBO	R	PU	T0+M12	Yes		
D4.1	Report: Software techniques for flexible data allocation	WP4	Unibo	R	PU	T0+M9	Yes		
D 5.1	Specification of the circuit, block level, and system level microarchitecture to be used as the evaluation platform for the project.	WP5	ARM	R	PP	(T0+8M)	Yes		Due to organisation of the project two systems will be analysed. A RTL level ARM926 processor which is a industry standard soft core and a xSTream processor which is a multicore system allowing software evaluation.
D 6.1	Description of application drivers and their requirements	WP6	ST	R	CO	T0+6M	Yes		
D7.1	Internal project website	WP7	IMEC	R	PU	T0+1M	Yes		Dedicated wiki has been setup for exchange of files.
D7.2	Risk management plan	WP7	IMEC	R	PU	T0+6M	Yes		
D7.3	Semi-annual project progress	WP7	IMEC	R	PU	T0+12M	Cancelled		This deliverable was cancelled in agreement with

	report								EC.
D8.1	Public part of the project web-site first issue	WP8	IMEC	D	PU	T0+1M	Yes		Project website is used for public dissemination.
D8.2	Press release at the start of the project	WP8	IMEC	R	PU	T0+3M	Yes		Press releases issued during Date '08

Milestones

TABLE 2. MILESTONES							
Milestone no.	Milestone name	Work package no	Lead beneficiary	Delivery date from Annex I	Achieved Yes/No	Actual / Forecast achievement date	Comments
M1	Definition of System level micro-architecture for evaluation platform	WP5,WP2	ARM	Month 6	Yes		Project board meeting in Glasgow.
M2	Definition of IP blocks for evaluation platform	WP3, WP4, WP5	ARM	Month 12	Yes		Project board meeting in Leuven.

15. Project management

15.1. Consortium management tasks and achievements;

The Project Coordination and related Management tasks are a vital part of the successful execution of the REALITY project. The applied management approach is fully embedded into the daily operations of the REALITY project. This section describes the achievements and organization in the REALITY project during the first reporting period. This way of working will be continued throughout the entire project timeline. The project coordination and management aims at providing the necessary infrastructure to support the complicated task of decision making and communication between the REALITY partners. The organizational structure of the REALITY project management is presented in the figure below:

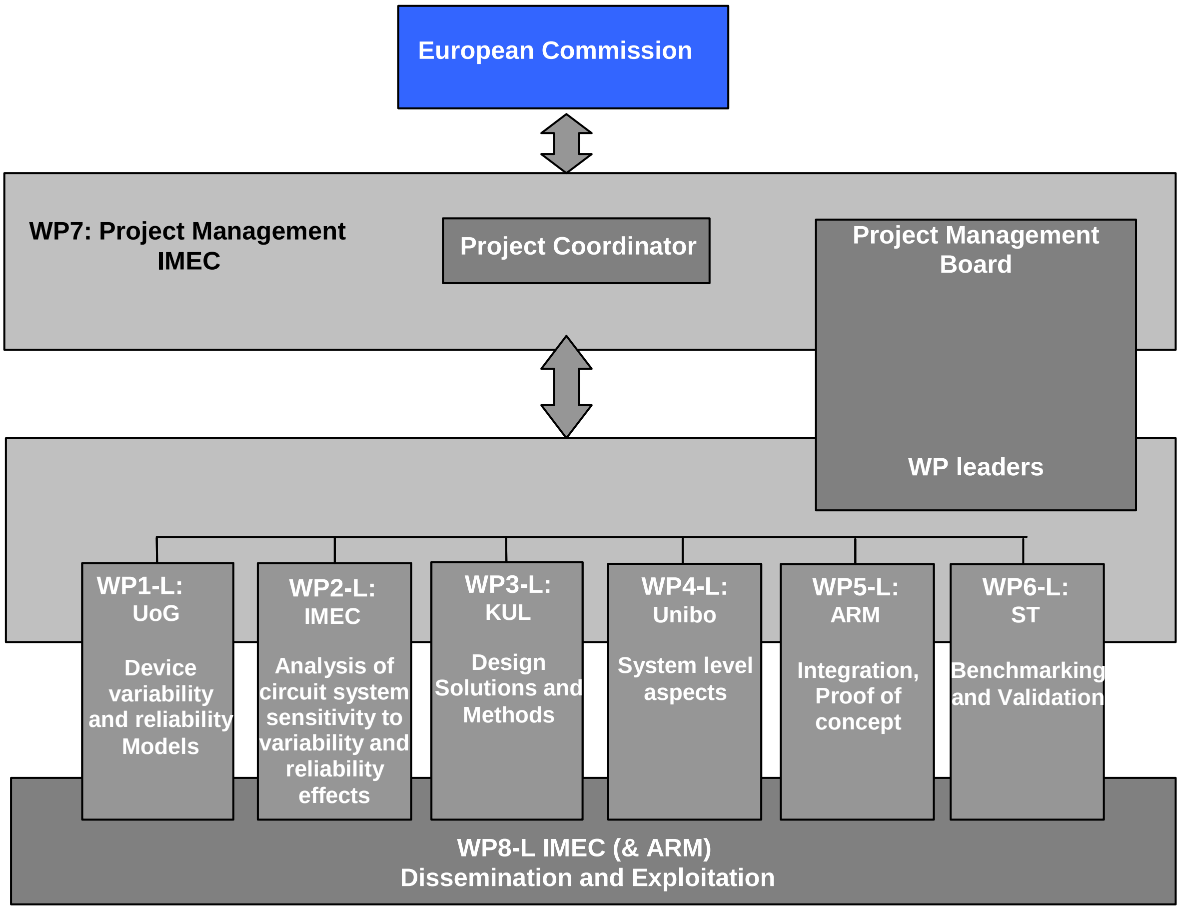


Figure 13: REALITY project team and coordination

IMEC acts as the project coordination of the **REALITY** project. IMEC oversees the day-to-day management and acts as the liaison between the project and the EC.

<u>A Snapshot of the main management tasks :</u>

- Keeping the global overview of the project.
- Communication list compilation and keeping it up-to-date.
- The technical management of the project, oversight and steering the scientific and technological development in the project.
- Keeping the actiontracker and follow-up the timely closure of actions.
- Keeping and follow-up of the Decisions list.
- Organizing the Risk Management.
- Monitoring deliverables and milestones, organizing the proper review of deliverables.
- Measuring the actual progress against technical objectives.

- Recommendations about major changes in the planned work.
- Chair the Project Management Board.
- Organization of the Project Management Board meetings and Project Technical meetings, including definition of the Agenda and key topics.
- Driving the dissemination and use (see deliverable report D8.3) activities
- Collection and submission of cost statements, overview of budget situation
- Promotional flyers and posters
- Organizing Contract negotiation for consortium agreement
- Update of the Description of Work, version v2.0

The Project Management Board is comprised of one member from each partner (WP leaders) and is chaired by the project coordinator. The input from the respective organization of each member regarding coordination, planning, monitoring and reporting will be disseminated in the board. Finally, the board is responsible for all the strategic decisions regarding the direction of the project. These responsibilities include:

- Strategic planning
- Managing assets complementary to innovation: budget, addition of new partner
- Contract negotiation for consortium agreement
- Set up of Non Disclosure Agreement (NDA)
- Contracts and licensing agreements resulting from the valorization initiatives
- Protection of intellectual property
- Technology transfer

For practical reasons, the project management board meetings and project team meetings – except the technical workshops – have been combined in the first reporting period.

The Work package leaders are responsible for the coordination and execution of the tasks and the deliverables within their respective work package. They have reported all technical results regarding the project (deliverables, publications, etc.) to the project coordinator.

15.2. Problems which have occurred and how they were solved or envisaged solutions :

15.2.1. Applied approach within REALITY :

The REALITY project consortium has started working on the risk management right from the beginning of the project. By using a dedicated risk management approach, the consortium believes that problems can be identified in an early stage and proper actions can be defined in advance such that these problems can be avoided or, in case risks materialize, the impact of problems can be reduced.

The risk management methodology as used within the REALITY project consists of 2 main parts : “risk assessment” and “risk management”. An overview is provided in figure 14.

The project related risks or potential problems can be research oriented, as well as organizational, schedule or resource (meaning operational, within the consortium) oriented.
Risks that are external to the project but which may have a direct impact are also considered. These latter are usually outside the control of the project coordinator or the projectteam.

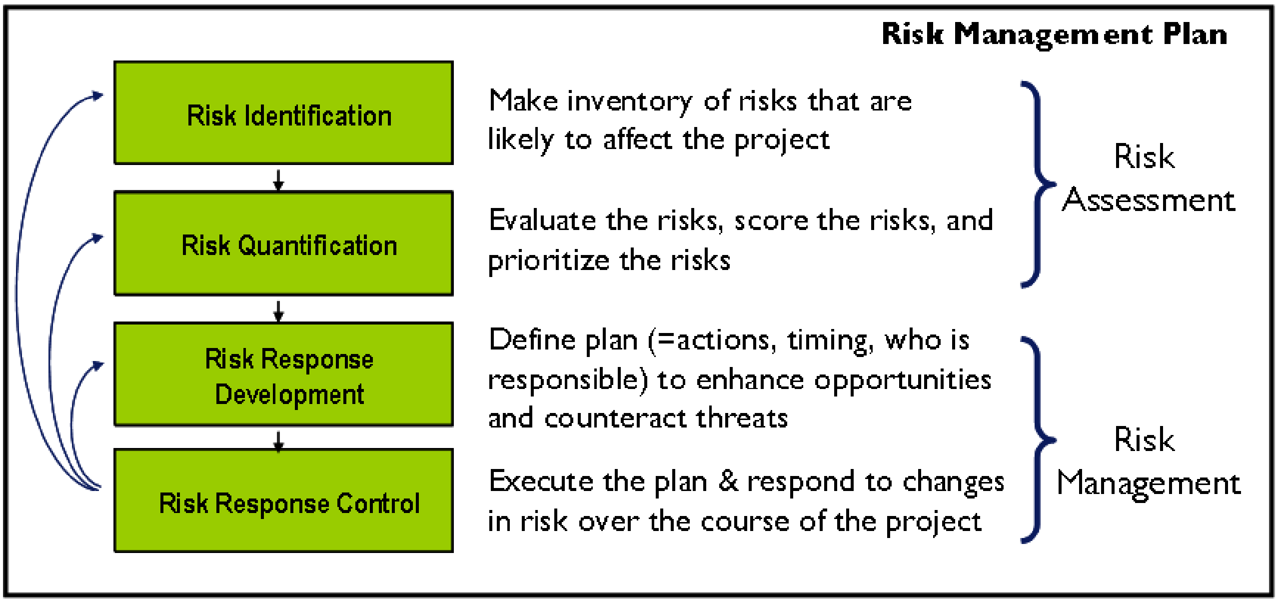


Figure 14: REALITY Risk management methodology

An Excel © template is used to facilitate the risk management process and to capture the results of each of the depicted steps in a transparent way. This template is managed and owned by the project coordinator and updates are under version control.
The consortium partners are able to provide their input and view, typically at each project board meeting or technical meeting, or via e-mail in between meetings. The template is updated periodically with the result of an evaluation that decides if the previously defined risks and actions are still applicable and if the assigned risk level is still appropriate. If managed well, the total risk value of the project reduces over time.
Details of the template used in the REALITY project will be shown below.

Risk Identification

The risk identification of the REALITY project has started at the conception of the initial project proposal (October 2006). At that moment a general inventory of potential risks was compiled by the consortium members. The purpose was to identify potential problems in an early stage that were likely to affect the project and to consider a strategy in case these risks would actually occur. This initial risk identification list did not contain a strategy for each of those risks, however it was more than suitable to gain an insight in the overall project risk and attention points.

The inventory was defined based upon brainstorming with a small team at the project proposal initial meeting, under guidance of the project coordinator. Based upon the expertise of each of the consortium partners in the research area of the REALITY project, their historical experience in similar projects and by interviewing a limited number of experts belonging to the respective organizations (e.g. science directors), a fairly accurate initial inventory was made.

It was decided by the consortium members, at the project kick-off meeting (January 2008), to compile a more detailed risk overview, including elaborate descriptions for cause and effect. This overview has been updated on a regular base by the project coordinator in the first reporting period.

REALITY RISK ASSESSMENT									
No.	Category	work package	Risk description	Cause	P	Probability 0-- Severity 0--5 Effect	S	Px S	P = Preventive C = A = Avoidance R = Reduction Actions
1	external	wp1	Availability of process data in 32nm cannot be guaranteed	#NAME?	1	difficulty in preparing the device variability modelling	1	1	[C] use preliminary data and TCAD simulation for 32nm
2	external	wp2	Statistical spice models including process parameter variations and their spatial correlations in 45nm and 32nm can not be guaranteed, given the uncertainty in the Crolles2 Alliance	Currently ST has an on-going project for 65nm, but there are no plans for next technologies	4	This might limit the effectiveness of SSTA	1	4	[C] spice models on 45nm from WP1 are ready, spice models on 32nm will be developed in WP1 when the process data in 32 nm is available from ST
5	technology	wp5	Longer than planned (extended) delivery time of low level building blocks	multiple causes, manpower or key personnel priorities, changing company strategy, IP confidentiality...	4	limited integration and evaluation time-scales	1	4	[P] Identify critical blocks and follow their development closely
	external	WP5	Availability of ARM926 softcore is not guaranteed	-Legal Problems IMEC-ARM concerning liability	3	This has a direct impact on the target platform	5	15	[C] ARM and IMEC will bring legal dptms into contact to solve the liability issue
3	technology	wp3	the developed methodologies and flows being may not be implementable	- low implementability in existing tools - computationally too expensive	1	impossible integration and evaluation at a system level. Only academic value	2	2	[P] Adapt the approach and rely upon own (KUL) sources.

Table 1 : typical REALITY Risk management list (version of 9-12-2008)

<u>Risk Assessment</u>

The risk assessment MS Excel template as used within the REALITY project consists of the following elements :

- **Risk description :** a concise description of the risk itself
- **Cause :** defining what makes this a risk and what triggers the problem. This can also include risk symptoms or indirect indicators of actual risk events.
- **Cluster :** area of the risk, like : technology, external, organizational, schedule
- **Probability P** : chance of the risk in case it occurs
- **Effect :** importance of the risk in affecting or impacting the project
- **Severity S :** describing the extend or impact in case the risk occurs
- **Product PxS :** used to prioritize the risks
- **Action strategy** : 4 categories are being used
- **Action description :** general description of the defined action

The categories used to define the action strategy are :

- **Preventive :** measures to avoid or reduce the effect or probability of the risk.
- **Reduction :** what to do to reduce the probability of the risk occurring and/or reducing the effect of the risk.
- **Avoidance :** what to do to stop the risk occurring.
- **Contingency :** what to do if the risk occurs, i.e. a planned reaction.

The initial list as shown in table 1 is also being used by the REALITY project team to indicate and prioritize which risk is seen as acceptable and for which risk further follow-up actions need to be defined.

Some risks require multiple actions and multiple owners and may change in time. To be practically and in order not to overload the risk assessment list, the REALITY project team decided to organize the follow-up in a dedicated action tracker list. This list contains assigned owners for a risk and detailed actions with due dates. The owner is the person responsible for execution and tracking of the risk related action, and it can only be one of those consortium partners which attend the meeting. Every month, during the regular conference call, this action-tracker should be reviewed and the status updated. The owner of the risk may change over the course of the project.

The project coordinator is owner of both the action tracker and risk assessment list. Appropriate version control is being maintained and documented by keeping track of changes in a revision history tab.

15.2.2. REALITY Top Risks to date:

There is a continuous evolution in problems occurring. Some major risks which were identified at the project kickoff have materialized and proper actions have made sure the impact was mitigated. Some other risks which were identified did not come true or the priority (severity or probability) was much lower than expected, and finally a few new risks popped up during the course of the first reporting period.

The top risks to date (project M12, December 2008) are:

- Availability of process data in 32nm cannot be guaranteed
- Availability of ARM926 softcore is not guaranteed
- the developed methodologies in WP3 and flows being may not be implementable

15.2.3. Changes:

Changes in the Description of work:

The description of work was updated with version 2, on January 19th 2009 reflecting the changes in the consortium and updates and clarification in the original D.O.W.; Table 2 below shows the overview of the justifications of the updates.

Partner	WP	Changes	Explanation if needed
KUL	WP3	Added to WP3 the analysis of the effect of reliability on analog circuits, methodology and solutions	The analog group of KUL (Georges Gielen) joined the project. “Reliability effects on analog circuits” has been added to the project.
		Timing change of deliverable D3.1	Minor update of timing of D3.1 (reported to the EC)
ST	WP2	Effort change in task 2.2 and task 2.4	Sum of the effort of task did not match with total effort. Therefore reduction of ST effort in T2.2 and T2.4 has been done
	WP5	Skip task T5.4 “Implementation flow investigation” and reallocated 4pm to task T5.5.2 (now T5.6)	Task 5.4 was reoriented towards the ARM926 processor. Therefore Task 5.4 will be done by ARM.
	WP6	Delivery date of Deliverable 6.2 in text is changed to T0+18M	This was an inconsistency with the previous DoW. D6.2 is related to Task 6.2 which ends at M18.
		Name change of WP6 to "validation and assessment of results“	Minor update
		T6.5 is split into two subtasks	To make explicit the activities of porting the application benchmarks and integrating them with the simulation platform and SW runtime provided by UniBo, this was not covered anywere else while the work has already started
UniBo	WP5	Clarification added related to the modeling effort (relating to T5.5.2 (now T5.6)). Effort from UniBO has been added.	Effort from UniBo was not clear in the first version of the DoW. Effort has been assigned to T5.6.
IMEC	WP2	No effort in task 2.2 (from 2MM to 0MM) & 2.3 (from 2MM to 0MM)	The overall effort in the WP did not match the effort breakdown per task and the focus was from the beginning on task 2.4 and task 2.5
		Decreased activity in task 2.5 (from 24MM to 14MM)	The overall effort in the WP did not match the effort breakdown per task.
		Split D2.1 into D2.1.1 and D2.1.2	The lack of the 32 nm design kit triggered the action to split the deliverable up into a preliminary (2.1.1) and a final library delivery (2.1.2)

	WP3	Added description on how WP3 work links to WP5	It was not clear how the work in WP3 links to WP5. This has been clarified by adding a description concerning the IMEC effort.
	WP4	Manpower from 10MM to 0MM	On Q1 IMEC decided to focus only on analysis activities, therefore cancelling the effort in WP4 + asked permission to WP4 leader to shift effort to WP5.
	WP5	Manpower WP5: from 2MM to 12MM	Increased effort coming from WP4. The increase in task 5.5.2 (now 5.6) reflects the tight collaboration between IMEC and ARM for demonstrating the analysis capabilities into the test vehicle.
	WP6	No effort in Task 6.5	This task is related to WP4 and because IMEC has no effort in this WP4 (shift of activities in Q1 of the project), no effort will be spend in this task. The effort is distributed over the other 2 tasks in this WP6.
ARM	WP2	Increased activity Task 2.1.2 (from 0MM to 3MM)	Manpower from WP5 was shifted to WP2 as consequence of the re-adaptation of the effort in WP5 concerning the split of the test vehicles. ARM invests here manpower in the statistical characterization of libraries.
		Increased activity in task 2.2 (from 6MM to 9MM)	Manpower from WP5 was shifted to WP2 as consequence of the re-adaptation of the effort in WP5 concerning the split of the test vehicles. SRAM statistical analysis has become more important after the beginning of the project and therefore the manpower has increased.
		Split D2.1 into D2.1.1 and D2.1.2	The lack of the 32 nm design kit triggered the action to split the deliverable up into a preliminary (2.1.1) and a final library delivery (2.1.2).
	WP5	Shift 6MM from WP5 (decrease activity in task 5.5.2 (now 5.6)) to WP2 (increase in task 2.1.2 and task 2.2)	Manpower from WP5 was shifted to WP2 as consequence of the re-adaptation of the effort in WP5 concerning the split of the test vehicles.
		Shift 6MM from WP5 (decrease activity in task 5.5.1 (now 5.5)) to perform task 5.4	Task 5.4 was reoriented towards the ARM926 processor. Therefore Task 5.4 will be done by ARM.

Table 2: Update of the DoW

Changes in the project plan
As identified in section 15.2.2, some risks have materialized. Therefore corrective actions have been planned, resulting in a change of the original work plan. All changes in the original work plan have been identified in table 2.

TOP RISK	Corrective action and implication on workplan
Availability of process data in 32nm cannot be guaranteed	During 2008 the project team has spent effort in making a 32nm dataset available to the consortium. Because the delay of this dataset originated on a external technology provider to STM, the work plan has changed. The following steps have been taken to reduce this risk: - Due dates of deliverables have been delayed. This has been reported to the EC. The due dates of these new deliverables will be respected. - Currently an NDA is circulating to make the 32nm dataset available to University of Glasgow and ARM. The NDA is setup between STM, University of Glasgow and ARM. STM has confirmed however that IMEC will not receive this information to avoid overruling conditions that the technology provider may have set-up upfront. This is expected to be finalized in M13, 2009.

	- The split of deliverable D2.1on the design of an standard cell library in two sub-deliverables. The first sub-deliverable provides an early version of such a library which is a design using a public domain 32nm device model and using linearly scaled dimensions and a second. A second one being the originally planned worked once the 32nm dataset becomes available.
Availability of ARM926 softcore is not guaranteed	During the project the project team has identified two test vehicles that will be used in the project. The ARM test vehicle contains the ARM926 core. The availability of the ARM926 softcore was identified as a top risk and therefore corrective action was taken during 2008. Even when the softcore can be made available the legal conditions to do so are too restrictive. The following steps have been taken to reduce this risk: - In 2009 a research island between ARM and IMEC will be setup to perform the planned work on the ARM926 soft-core complemented with stages of IMEC personnel at ARM. This will solve all current pending legal issues including the availability of the 32nm data set to IMEC by making the 32nm data set only available to the ARM engineer. - Split of the demonstration activities in two main vehicles: one focused above the RTL level using STM processors (hereafter called system level) and one below (hereafter called RT-level) using ARM processors. A back of the envelope model will be developed to connect the two vehicles.
The developed methodologies in WP3 and flows being may not be implementable	From the original work plan it was not clear how the developed methodologies in WP3 would be implemented in the project. The following steps have been taken to reduce this risk: - The original work plan has changed in order to use the developed memories in WP3 in the test vehicle. IMEC will analyse the memories in WP3 and benchmark them against ARM memories.

15.3. List of project meetings, dates and venues in year 1 :

The table 3 shows an overview of the meetings held in the first reporting period (project month M1 until M12). One room project meetings with having all consortium partners to join (work package leaders and scientific key members), are typically held each 6 months or more frequently when necessary. For efficiency reasons it was decided by the consortium partners to combine as much as possible the milestone meeting with the project management board meeting and the technical review. When necessary, separate and dedicated technical meetings were organized with specific topics. Conference calls were planned monthly during the first year of the project.

Meeting name	Meeting Purpose	Meeting Type	WP's	Date	Venue
Kickoff	• Tick-off the REALITY Project Start • Get a common understanding of the objectives and priorities • Outline the project	MILESTONE + PROJECT MANAGEMENT BOARD	WP1 until WP8	21, 22 & 23 January 2008	IMEC offices, Leuven Belgium

	organization, individual roles and responsibilities of team members • Align the work packages, milestones, timelines and (administrative) reporting • Assessment of all the risks, including definition of alternative actions • Clarify the expectations of all partners • Team building	+ TECHNICAL			
Monthly conference call	• Handle administrative issues • Keep track of deliverables and delivery dates • Follow up of the action tracker • Clarify technical contributions from partners • Any other business	Administrative + TECHNICAL	WP1 untill WP8	Monthly	Conference call
Partner Meeting 1 (Pm1)	• Measure and ensure a constant level of information sharing about the progress in all the Work Packages. • Get a common understanding of the technical status and priorities • Align the work packages, milestones, timelines and (administrative) reporting • Assessment of all the risks, including definition of alternative actions • Escalation path if necessary, • Update of the DoW • Clarify the expectations of all partners • Review and approval of the deliverable report • Team building	MILESTONE M1 PROJECT MANAGEMENT BOARD + TECHNICAL	WP1 until WP8	4 & 5 Septermber 2008	University of Glasgow, Glasgow, UK
Partner Meeting 2 (Pm2)	• Final Review and approval of the due deliverables • Review of the Dissemination and Use Plan. • Review of the planned objectives. • Get a common understanding of the technical status and priorities • Align the work packages, milestones, timelines and reporting. • Start preparing the 1st Annual Review by the EC. • Update of the DoW • Re-Assessment of all the risks, including definition of alternative actions. • Team building	MILESTONE M2 + PROJECT MANAGEMENT BOARD + TECHNICAL	WP1 until WP8	4 & 5 December 2008	IMEC, Leuven, Belgium

Table 3: overview of project meetings

15.4. Project planning and status :

The table 4 shows an overview of the committed deliverables in the first reporting period which were submitted to the EC. All of the scientific and dissemination deliverables were provided on time as planned. Some deliverables were postponed. This was also communicated towards the EC.

List of Deliverables submitted for review to the EC

Del. no.	Deliverable name	WP no.	Lead bene-ficiary	Nature	Dissemination level	Delivery date (proj. month)
D1.1	Variability simulation and comparison for the 45 nm technology generation	WP1	UoG	R	PU	T0+12M
D2.1.1	Creation of a scaled down library	WP2	IMEC	P	RE	T0+8M
D2.2	Report on methodology for percolating variability sensitivity	WP2	IMEC	R	PU	T0+12M
D3.1	Report describing the methods to assess device level variability at the circuit level	WP3	KUL	R	CO	T0+M12
D3.3	Report: techniques for enhancing data path and controller variability tolerance	WP3	UNIBO	R	PU	T0+M12
D4.1	Report: Software techniques for flexible data allocation	WP4	Unibo	R	PU	T0+M9
D 5.1	Specification of the circuit, block level, and system level microarchitecture to be used as the evaluation platform for the project.	WP5	ARM	R	PP	(T0+8M)
D 6.1	Description of application drivers and their requirements	WP6	ST	R	CO	T0+6M
D7.1	Internal project website	WP7	IMEC	R	PU	T0+1M
D7.2	Risk management plan	WP7	IMEC	R	PU	T0+6M
D7.3	Semi-annual project progress report	WP7	IMEC	R	PU	T0+12M
D8.1	Public part of the project web-site first issue	WP8	IMEC	D	PU	T0+1M
D8.2	Press release at the start of the project	WP8	IMEC	R	PU	T0+3M

Table 4: List of deliverables submitted to the EC

15.5. Impact of possible deviations from the planned milestones and deliverables

No major deviation exists in the planning of deliverables, nor the execution of the REALITY project compared to the original schedule. Whenever necessary, practical constraints have been taken into account in the precise definition of meetings and in providing deliverables.

15.6. Development of the Project website :

The www.fp7-reality.eu website is online since april 2008 and contains a Public area. It is the official homepage of the project and that serves as a public repository for all project related information. Consortium restricted information and project related documents (action trackers, deliverables, meeting slides…) are stored on a dedicated wiki page (http://www-micrel.deis.unibo.it/~reality/wiki/index.php/Main_Page).

The public web site gives interested users access to a number of public pages providing a description of the project objectives, news, announcement of upcoming events, links to exhibitions where the REALITY project will be represented, contact information and reports or specifications.

Further details on the website and its statistical monitoring information can be found in **deliverable report D8.3**

15.7. Use of foreground and dissemination activities during this period :

Within the REALITY consortium all partners contribute to a large extend equally to the dissemination of the project results. Extensive details on the dissemination approach and achievements can be found in deliverable report D8.3 which will be submitted to the EC in February 2009.

IPR, Access rights and licensing have been made explicit and described in an elaborate way in the Consortium Agreement which was signed by all consortium partners.

15.8. Coordination activities comment – key message :

The key message regarding the REALITY coordination activities can be summarized as follows :

- **Deliverables have been achieved on time as planned.**
- **Numerous Scientific Publications have been achieved.**
- **Information is being shared within the consortium, but individual partners have also become active in a bilateral context.**
- **True collaboration exists within the consortium, as well as outside the** REALITY **context.**
- **The** REALITY **research topic has and will remain to have industrial relevance.**
- **Furthermore, the** REALITY **research topic is at the core of the industrial partners activity.**

Based upon this observation, it can be concluded that the REALITY project is in a good shape to proceed with the planned activities for the 2nd period.

16. Explanation of the use of the resources

16.1. ST Microelectronics

Table : Personnel, subcontracting and other major cost items for Beneficiary "ST" for period 1			
STM	**Item description**	**Amount**	**Explanations**
	Personnel costs	340,343.00	1 Manager, 5 R&D eng, 4,564.06 hours total 0.63MM Management 14.6MM senior engineers 17.4 engineers
	Travels	909.00	Kick Off meeting in Leuven
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		341,252.00	

16.2. IMEC

Table : Personnel, subcontracting and other major cost items for Beneficiary "IMEC" for period 1			
IMEC	**Item description**	**Amount**	**Explanations**
	Personnel costs	260,655.57	RTD Personell costs of 17.4MM engineers and 13.8MM senior engineers. Management cost of 4.8MM.
	Consumables	2,648.00	registration fp7-reality.eu and contribution to ESSDERC
	Travels	4,131.69	Travel cost of invited paper at ESSDERC workshop on Variability, quarterly project board meeting, AMD project prospect, invitation for talk at European Technology Platform Nanoelectronics
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		267,435.86	

16.3. University of Glasgow

Table : Personnel, subcontracting and other major cost items for Beneficiary "UoG" for period 1			
UoG	**Item description**	**Amount**	**Explanations**
	Personnel costs	62,404.00	PDRA costs
	Travels	5,347.00	Project meetings and

			conferences
	Consumables	528.00	Modest computer consumables
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		68,279.00	

16.4. Katholieke Universiteit Leuven

Table : Personnel, subcontracting and other major cost items for Beneficiary "KUL" for period 1			
KUL	**Item description**	**Amount**	**Explanations**
	Personnel costs	77,704.16	16.6 Manmonths R&D
	Other costs	2,973.07	Small components
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		80,677.23	

16.5. University of Bologna

Table : Personnel, subcontracting and other major cost items for Beneficiary "UNIBO" for period 1			
UNIBO	**Item description**	**Amount**	**Explanations**
WP3/4/5/6	Personnel costs	93,564.53	Four grants for research are activated with four young graduated collaborators in order to carry out the activities foreseen for UNIBO in the REALITY project, corresponding to 36 person/month. Dr Andrea Acquaviva and Dr Giacomo Paci are involved in this project through two research collaboration contract to cooperate on all project related activities, their activities in this first year, correspond to 5 person/month. Prof. Luca Benini and Prof. Michela Milano are involved in the research activities foreseen within WP3 and 4 for a total of 3 person/month. Due to the unavailability of a senior researcher at the beginning of the project, the number of PM has been higher and at low cost than foreseen because the activities have been performed by junior researchers.
WP4	Subcontracting	23,810.00	According to the Annex I of the Grant Agreement a subcontract is activated with the University of Cagliari in order to carried out the following activities: - development of task migration support for the target architecture - development of OS support for the target architecture This amount correspond to the first tranche of payment.
WP3/4	Major cost item & Subsistence'	2,913.64	Reimbursements of travel and subsistence cost for their participation to the following events: • Kick Off meeting in Leuven; • Participation to DATE conference and workshop in Munchen; • First review meeting in Glasgow;

			• Participation to ESSDERC/ESSCIRC Workshop in Edinburgh; • Local coordination meeting in Bologna.
WP3/4/5/6	Major cost item Costs'	134.00	• These costs are incurred for the registration fee to DATE 2008 Conference in Munchen
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		120,369.17	

16.6. ARM

Table : Personnel, subcontracting and other major cost items for Beneficiary "ARM" for period 1			
ARM	**Item description**	**Amount**	**Explanations**
	Personnel costs	212,166.00	1 manager, 8 engineers working part time on the project: 25.8pm spent during the period
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		212,166.00	

17. Financial statements – Form C and Summary financial report

The form C has been uploaded to the NEF online webtool by all partners.

18. Certificates

