REALITY

Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

Contract No 216537

Deliverable D7.6

Annual project progress report (Year 2)

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The REALITY Consortium consists of:

Interuniversity Microelectronics Centre (IMEC vzw)	Prime Contractor	Belgium
STMicroelectronics S.R.L. (STM)	Contractor	Italy
Universita Di Bologna (UNIBO)	Contractor	Italy
Katholieke Universiteit Leuven (KUL)	Contractor	Belgium
ARM Limited (ARM)	Contractor	United Kingdom
University Of Glasgow (UoG)	Contractor	United Kingdom

1.   Disclaimer

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2.   Acknowledgements

3.   Document revision history

Date	Version	Editor/Contributor	*Comments*
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11/02/2010	V0.2	Andrea Acquaviva, Asen Asenov,, Luca Benini, Andrew Brown, Binjie Cheng, Wim Dehaene, Giuseppe Desoli, Georges Gielen, Virgile Javerliac, Yves Laplanche, Miguel Miranda, Davide Pandini, Scott Roy, Paul Zuber	Technical inputs from all partners for the different technical WPs (WP1, WP2, WP3, WP4, WP5, WP6, WP8). WP7 and financial sections still needs to be completed
25/02/2010	V0.3	Andrea Acquaviva, Asen Asenov,, Luca Benini, Andrew Brown, Binjie Cheng, Wim Dehaene, Giuseppe Desoli, Georges Gielen, Virgile Javerliac, Yves Laplanche, Miguel Miranda, Davide Pandini, Scott Roy, Paul Zuber	Includes all financial information in Sections 15 and 16 (NEF). WP7 still needs to be completed
4/03/2010	V1.0	Miguel Miranda	Full version including project management sections
22/3/2010	V1.1	Miguel Miranda	Update of Section 15 with the list of the people involved in the project and their function (those who claim for personnel costs).
24/3/2010	V1.2	Miguel Miranda	Corrected inconsistencies found in Tables 7, 8 and 10 (marked in yellow to highlight the changes made)

4.   Preface

The scope and objectives of the REALITY project are :

- Development of design techniques, methodologies and methods for real-time guaranteed, energy-efficient, robust and adaptive SoCs, including both digital and analogue macro-blocks"

The Technical Challenges are :

- To deal with increased static variability and static fault rates of devices and interconnects.
- To overcome increased time-dependent dynamic variability and dynamic fault rates.
- To build reliable systems out of unreliable technology while maintaining design productivity.
- To deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.

Focus Areas of this project are :

- "Analysis techniques" for exploring the design space, and analysis of the system in terms of performance, power and reliability of manufactured instances across a wide spectrum of operating conditions.

- "Solution techniques" which are design time and/or runtime techniques to mitigate impact of reliability issues of integrated circuits, at component, circuit, architecture and system (application software) design.

The REALITY project has started its activities in January 2008 and is planned to be completed after 30 months. It is led by Dr. Miguel Miranda of IMEC. The Project Coordinator is Dr. Miguel Miranda from IMEC. Five contractors (STM, ARM, KUL, UoG, UNIBO) participate in the project. The total budget is 2.899 k€

5. Abstract

This report is deliverable 7.6: "Annual project progress report". The reporting period is from M13 until M19. Hence it covers roughly the first semester of project execution after the first review meeting.

6.   List of Abbreviations

REALITY	Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies
CAD	computer aided design
DSP	digital signal processing
HW	Hardware
IC	integrated circuit
SoC	system on chip
SW	Software

7. List of Tables

8. List of Figures

9. Table of contents

PROJECT PERIODIC REPORT

Grant Agreement number: 216537

Project acronym: REALITY

Project title: "Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies"

Funding Scheme: Collaborative project (STREP)

Date of latest version of Annex I against which the assessment will be made:

Periodic report: 1st □ 2nd X 3rd □ 4th □

Period covered: from 01/01/2009 to 31/12/2009

Name, title and organisation of the scientific representative of the project's coordinator:

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10. Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;

- The project has fully achieved its objectives and technical goals for the period;

- The public website is up to date, if applicable.

- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project and if applicable with the certificate on financial statement.

- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 15 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: Miguel Miranda Corbalan

Date: 15/02/2010

Signature of scientific representative of the Coordinator

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11. **Publishable summary: "Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies"**

Project Facts:
- FP7 Project :   European Community funded
- Coordination :   IMEC
- Website :   www.fp7-reality.eu
- Duration :   30 Months
- Effort :   382 person-months
- Industry :   ARM (UK), ST Microelectronics (Italy)
- Start date :   1st January 2008
- University :   Glasgow (UK), Bologna (Italy), Leuven (Belgium)
- Research Centre :   IMEC (Belgium)

Scope:
- Scaling beyond the 32 nm technology
- Tackle the increased variability and changing performance of devices from device unto system level.
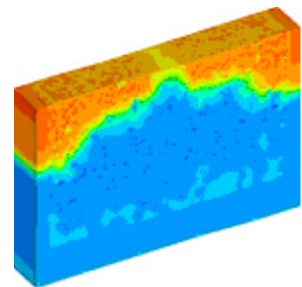
Random discrete dopants in a 35 nm MOSFET from the present 90 nm technology node.

Challenges:
- Increased static variability and static fault rates of devices and interconnects.
- Increased time-dependent dynamic variability and dynamic fault rates.
- Build reliable systems out of unreliable technology while maintaining design productivity.
- Deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.
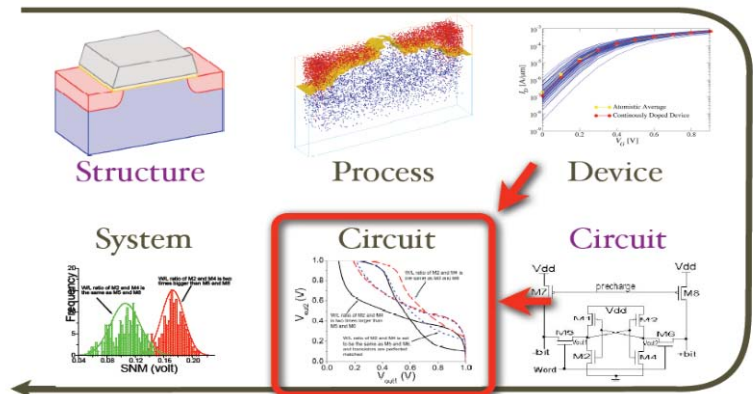
Proposed solution:
- System analysis of performance, power, yield and reliability of manufactured instances across a wide spectrum of operating conditions.
- Generally applicable solution techniques to mitigate the impact of reliability issues of integrated circuits, at component, circuit, and architecture and system design.

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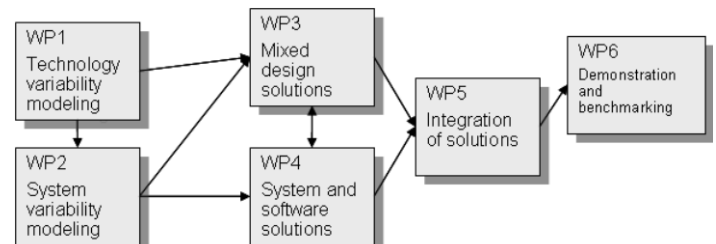
WP1: Device variability and Reliability Models (WP leader: UoG)

Task T1.1.1 (Validation and calibration against 45 nm technology generation devices) was completed and reported in 2008. This year's efforts have been focused on tasks T1.1.2 (started in 2009) and tasks T1.2.1, T1.2.2, T1.3.1, T1.3.2 and T1.3.3 already started in 2008.

T1.1.2   Simulation of variability in 32 nm technology generation devices.
An NDA was signed on 9/4/2009 to allow transfer of 32nm TCAD data from ST to UoG with the 4-way agreement being signed on 15/5/2009. The TCAD data was transferred to UoG on 28/04/2009. UoG has introduced the provided doping profiles into their simulator and calibrated the simulations against the provided I-V curves. UoG has performed simulations to investigate the variability in threshold voltage due to random discrete dopants and line edge roughness. A new source of variability (workfunction variation due to metal gate granularity) has also been included in the simulator for the first time. Full I_D-V_G characteristics for both n- and p-channel devices, at high and low drain voltage, have been simulated. Ensembles of 200 devices that differ due to random discrete dopants, line edge roughness and metal gate granularity have been used.

T1.2.1   Statistical simulation of the impact of fixed/trapped charges.
Simulation of the impact of fixed/trapped charges in 45nm devices was completed and reported in 2008. Further analysis of the simulation results was performed in early 2009 and the results have been submitted for publication in IEEE Transactions on Electron Devices. The equivalent work for 32nm devices will be performed at the start of 2010.

T1.2.2   Modelling of time dependent variation:
Simulation models for NBTI, HCD and SDB: this was completed and reported in 2008.
Variability aware method to incorporate reliability effects (NBTI, HCD and/or SBD) in transistor level netlists: This task goal is a modelling technique to include reliability effects in a variability aware transistor level model of any given circuit with the goal of simulating the combined impact of static variability and reliability. The inputs are the extracted variability injectors from 3.3 and the simulation models for reliability defined the previous year in 2.2

T1.3.1   Statistical compact model parameter sets.
45nm statistical compact models were delivered by UoG and reported in 2008. Due to differences in release number between the 32nm compact model supplied by STM and the TCAD simulation data to which the UoG simulator was calibrated, a different approach has been adopted for the 32nm devices. UoG have provided the I_D-V_G characteristics from T1.1.2 to IMEC who have extracted variability injectors that can be used in the provided STM compact models. This allows other partners to use compact models with variability without violating the NDA between STM and UoG on the supply of device information.

T1.3.2   Extraction of key statistical parameters.
More physically based compact models, such as PSP, will allow the extraction of key parameters which could have geometry dependent statistical distributions: UoG has developed a statistical extraction strategy for PSP.

T1.3.3   Extraction of variability injectors
Method and tool flow to extract Vt and beta variations from I-V curves (device DC transfer characteristics): Application of extraction flow to ST 45nm data was completed and reported in 2008. Application of extraction flow to ST 32nm data to extract Vt and beta variations from I-V curves provided by UoG (based on the low-level technological information received from ST) has been done in 2009 and variability injectors have been provided to project partners.

WP2: System and circuit characterization and sensitivity analysis (WP leader: IMEC)

Although it might be considered a straightforward task, statistical library characterization is a critical showstopper to the adoption of statistical analysis and optimization techniques in industrial digital flows. ARM has kept on developing with his EDA partner the characterization tool capable of generating a CCSA-VA liberty file with a high accuracy. A good correlation between analysed variability and Monte Carlo simulation was finally achieved. A 80 cell library has been characterized and will be evaluated on a system level design. In parallel, ST developed and validated a practical, yet accurate technique to reduce the mismatch characterization time during the reporting period. It is based on the simultaneous identification of the transistors impacting the cell performances, on the reduction of the characterization grid size, and on the identification of a restricted set of transistor parameters that largely impact on the device performances, since it would not be feasible to consider all the parameters present in typical transistor compact models.

While industry support exists for library characterization of standard cells, entirely new ways have to be gone for non-standard cells. ARM developed a push button tool for the designers to easily apply the read current characterization, based on spreadsheet tables and SPICE. In parallel, implications of Silicon-on-Insulator (SOI) technology on variability are investigated. KUL has prepared a memory for use in imec's MemoryVAM characterization tool.

On digital block level, ST introduced its new hybrid approach. A traditional DSTA based on corners is carried out using the tools currently available in the digital sign-off flow. After DSTA, ST considers the critical paths violating the timing constraints and also those paths that are "potentially" critical, i.e., whose timing slack are very small and subject to the detrimental impact of process variability. During this analysis, OCVs are taken into account by means of derating factors (which can be overly pessimistic as it was demonstrated during the previous WP2 activities). After selecting the critical/violating paths, on one side ST reduces the OCV margins (based on process variability data) and also carries out a path-based SSTA (HSTA) based on the statistical libraries described earlier. Following this approach it is possible to remove timing violations without taking unnecessary margins.

Imec has continued to implement and verify the technique to translate IP-level variability to System-level variability. The electronic Information Format (IF) that imec develops to exist parallel to the classical top-down and bottom-up design flow is continuously extended in order to cope with advanced information like block-level-sensitivity data.

WP3: Mixed mode countermeasures (WP leader: KUL)

The work of KUL between M13 and M24 has focused on task T3.2.

Task T3.2 has been divided into two sections: a first section extends the work done in T3.1 to include variability awareness to the reliability simulation of electronic circuits. In a second section, this knowledge is used to design a variability/reliability-resilient memory IP block.

A. Variability and degradation phenomena demand the use of novel design techniques, e.g. Knobs & Monitors, to guarantee optimal performance over a specified lifespan. A nominal reliability simulation methodology is used in combination with a variability-aware framework to maintain simulation accuracy while taking process variations into account. The methodology has been demonstrated effectively, but efficiency can still be improved in the coming months.
B. The design of a memory IP-block has been carried out as a case study to develop and validate variability-aware and low-power design methodologies for a state-of-the-art memory. To be able to cope with variability, statistical behavioural models are required. In this way the number of design loop iterations between the architectural and the circuit level can be reduced. The techniques that have been studied in this work are: (fully) divided word and bit lines, charge recycling, asymmetric sense amplifier redundancy, low swing techniques, etc. This work has temporarily been halted due to the lack of 32nm device models, which has caused serious delays and personeffort underspending. Part of this task has also been done collaboratively by IMEC, who set up the VAM environment and ran the statistical characterization flow on the KUL SRAM memory.

Since the work in this task has not yet been completed due to the delay and personeffort underspending as discussed above, KUL will continue and finalize this work by extension of Task T3.2 into June 2010. The completion of this work is also essential to support the activities in WP6. KUL will report this extended work in an updated version D3.2b of the Deliverable D3.2.

The work of UNIBO between M13 and M24 has focused on T3.4, and more specifically analyzing variability effects on on-chip communication and developing techniques for compensating for them and supporting run-time adaptation and variability management. The analysis has identified on-chip communication links (and more specifically Network-on-chip links) as critical components to be analyzed and protected by adequate countermeasures, based on Adaptive body bias (ABB) and adaptive supply voltage (ASV), which have been identified in T3.3 as effective methods for post-silicon tuning to reduce variability on generic combinational circuits or microprocessor circuit sub-blocks. The results have been reported in D3.3 (delivered on time at M12).

WP4: System level countermeasures (WP leader: UNIBO)

The work performed by UNIBO until M18 was focused on Task 4.1, 4.2, 4.3 and 4.4 (in collaboration with ST). The first two tasks (results are reported in D4.1 – delivered on time at M9) allowed to build the software infrastructure for the development of variability countermeasures developed in Task4.3 (results are reported in D4.2 – delivered on time at M18).

Main activities related to Task4.3 have been:

1. Definition of the problem of task allocation under variability effects to minimize energy under time constraints. We devised an Optimal solution with Integer Linear Programming. It is very slow and suitable for off-line validation. We then developed a sub-optimal solution based on Linear Programming and BinPacking, which is suitable for implementing task allocation at startup time. Finally, we developed an approximate solution based on a Look-up Table, which is much faster and allows online implementation.
2. Development of a theoretical solution and its implementation on the simulation platform that has been enhanced with power and variability models as part of WP5
3. Refinement of the task model (independently, barrier synchronized tasks representative of embarrassingly parallel computation like as done in video processing algorithm)
4. Comparison against state-of-the-art policies: Rank Power/Rank Freq
5. Analysis of compensation capabilities using VAM-generated variability affected platforms.

The activity about Task 4.4 started in collaboration with ST. In particular, UNIBO is currently working on the optimization of the policies on the target multicore platform, provided by ST and on the target validation benchmarks defined in WP6, for which UNIBO is also performing the porting to the simulation platform as part of WP6.

The activity performed by UNIBO during the period M19-M24 in WP4 was focused on the completion of Task 4.4, concerning the optimization of the system level countermeasures for the specific hardware platform defined in WP5 and the benchmarks to be used for evaluation in WP6. More specifically, the activities have been:

1. The development of an optimized online version of the variability-aware task allocation policy exploiting a new formulation of Linear Programming problem that can be solved during application execution. This optimization is needed for the implementation of the task allocation policy on multimedia applications on a frame-by-frame basis.
2. The analysis of the impact of variability on the performance and energy consumption of multimedia applications, namely on the MPEG2 video decoder benchmark from ST (WP6). The application is parallelized so that some functions (i.e. IDCT and Decode Slice) are performed by various cores at the same time. This analysis provided information about the impact of speed and power consumption variations among the different cores on the energy and deadline miss rate.
3. The implementation of the optimized variability-aware allocation policy on the target platform running the MPEG2 video decoding benchmark.

More details and results related to this activities will be reported in D4.3 due on M27.

WP5: Design flow, integration, proof of concept (WP leader: ARM)

This Work Package coordinates and carries out the evaluation of the different project components. It is the place where the components of the project come together and will involve developing methodologies and test platforms to enable the evaluation to take place. It is responsible for assessing the severity of the un-compensated situation, and quantifying the improvements that result from the application of techniques identified in other Work Packages. It is also responsible for identifying the techniques that prove to be unsuccessful (and why), as well as to point to other techniques that might be worth investigation (beyond this project).

In a first phase we defined the system platforms and the IP blocks in which we will evaluate the developed techniques. Some initial developments on the xSTream and the ARM system platforms have already started in the first period.

The second period has seen a ramping up of the integration activity. The flow integration started on the first period on several cells has been extended to a full library. The work has been focused on the VAM flow from IMEC. A 32nm library composed of 80 cells is used as bases of the validation work. A full variability analysis has been performed on this library. Thanks to the deployment of a Research Island inside ARM a strong cooperation on the variability analysis of the VAM flow was undertaken. IMEC could hereby get access to the ARM926 design and the 32nm library.

In the scope of the variability characterization a ARM memory critical path has been characterized for different memory cut sizes. One size was chosen to perform a benchmarking of memory design coming out from the WP3 developments. Memory VAM was also applied to the memory developed by KUL.

The ALU of the ARM926 was chosen as the test vehicle for the Active Body Biasing scheme evaluation. UniBO started the adaptation of its methodology using a 45nm library provided by ST. The 32nm library, including back biasing information, became available at the end of the period allowing testing this technique on the 32nm node as well.

On the xSTream platform an important effort has been spent in the development of the simulation infrastructure of the system level design. An adaptation of an in house flexible model has been done in order to be able to simulate the xSTream processor and the xPE IP blocks including variability information. The variability impact seen on the system will be modelled by the "back of the envelop" approach proposed by UniBo. This approach is based on equation providing the relationship between corner variations and the system performances. A calibration of the variability information will be done using the VAM information on the ARM926. In order to account for the variability information at the system level during the simulation, specific adaptations of the software infrastructure had to be made.

Finally a monitoring system has been integrated to the xSTream platform. The system is based on a library component: Monitoring Micro IP. The information coming out from the IP can be accessed either by a Process Monitoring block which controls the knobs on the system or directly read out during the testing of the system.

This second period has seen a lot of activity in this work package. Most of the integration work has been done and is described in the delivery D5.3 which paves the path to the assessments done in WP6.

WP6: Validation and assessment of results (WP leader: ST)

This work package is the place were most of the results, methodologies, flows, IPs developed and/or leveraged in the other work packages come together for validating the project's goal of "build reliable systems with unreliable components".

The WP tasks are designed to validate and assess the project results through the benchmarking of individual IP blocks along with the identification and porting of a set of industrially relevant applications. The general focus is the leverage of IPs and applications along with their integration and mapping onto the integrated application platform developed with contributions from WP3,4,5. The output of the work package is the evaluation both in terms of NRE, final product cost, and in general advantages over the uncompensated case, of the benefit stemming from the methodologies, techniques and components developed by the project.

During the last six months of the second year of execution of WP6 activities, the work has progressed mainly for tasks T6.4, T6.5.1 and T6.5.2, allocation of resources to task has been aligned to expected levels from

the DoW. Tasks T6.2 and T6.3 have been completed during the first six months of this year and reported in the previous Periodic Activity Report.

In the context of WP6 validation tasks, as reported in the last Periodic Activity Reports, the partners of REALITY have agreed to validate the technologies and methodologies developed with two separated flows for the multimedia (STM) and general purpose (ARM) platform components.

The ARM926 test case has been applied towards the validation and benchmarking of both variability aware circuits and design and analysis flows; the process was driven by the availability of 32nm silicon technology data complemented by advanced variability analysis techniques at the atomistic level and up to devices, standard cell libraries, circuits and memories and whole netlists.

The major output of the period is the release of the report associated to D5.3; in this report are detailed many of the validation and benchmarking activities and results carried out by the partners on the different IPs and analysis flows deployed in the project.

For the multimedia scenario, a suitably defined simulation platform based on the REALITY platform definition tasks of WP5 has been made available. Such simulation platform provides a set of parallel media acceleration engines from STM (called xPEs) and an STM proprietary host processor, ST231, supporting Linux and a suitable run-time environment for the accelerators.

Objectives for the period 2, Project M13 until M24

The reporting Period 2 covers the project time-schedule M13 until M24, i.e. starting from 1st January 2009 until 31st December 2009. This report is a mid year progress report for such period.

Description of the performance / research indicators (all targets for Y2 have been met!)

WP	After year 1	After year 2	At end of project
WP1 Device variability	Physical modeling and understanding of the variability at 45/32 nm technology nodes (TN). First statistical compact models.	Compact models that accurately capture the variability and the reliability issues at 32 nm.	Models fine tuned. Feedback from device measurements incorporated.
	Preliminary version of a RDR std. cell library [32nm]. Flow definition and framework set up for variability characterization. Correlated variability energy timing flow definition and set up.	Variability characterization of a [32nm] RDR std cell library. Exploitation of the variability aware modelling flow on the driver application vehicle, including a solution for IP blocks and memories.	Methodology fine tuned. Feedback from benchmarking acknowledged.
WP3 Mixed design	Description of the variability and reliability analysis methods at circuit level	Demonstration of the developed method on SRAM and analog circuits	Validation of the developed method
WP4 Algorithm	Software techniques for flexible data and workload allocation for migration (the base flexible RTSM support)	Control algorithms for system level reliability and variability management (exploiting of the base RTSM support)	Porting, optimization and tuning for the target evaluation platform of: (a) the flexible RTSM, (b) the control algorithms
WP5 Integration	Definition of characterization blocks, macrocells, and system level architecture	Validation and application of methods to macrocells and integration into system	Final system integration, validation feeding into WP6 benchmarking
WP6 Benchmarking	Identification of relevant industrial applications and associated requirements and evaluation metrics	Definition of the validation plan. Benchmarking of block level IPs	Benchmarking of system level platform. Evaluation of results and impact according to validation plan criteria

12. Work progress and achievements during the period

12.1. WP1: Device variability and Reliability Models (WP leader: UoG)

Note: In this work package there is data that has been provided by STM to UoG and covered under the NDA between these two parties, e.g. device structures and TCAD I-V characteristics which will not be shown hereby.

Due to the initial unavailability of the 32nm structure information and TCAD simulation results, further investigation of reliability in the 45nm devices was done. Most device reliability problems are associated with generation of fixed charges or the trapping of electrons and/or holes in defect states in the gate stack during circuit operation. Using experimental data for the stress dependence of the average density of the stress generated charge and defect states, and their spatial positions, we had carried out a detailed 3D simulation of the statistical distribution of the corresponding changes in device characteristics due to microscopic manifestations of particular device defect configurations.
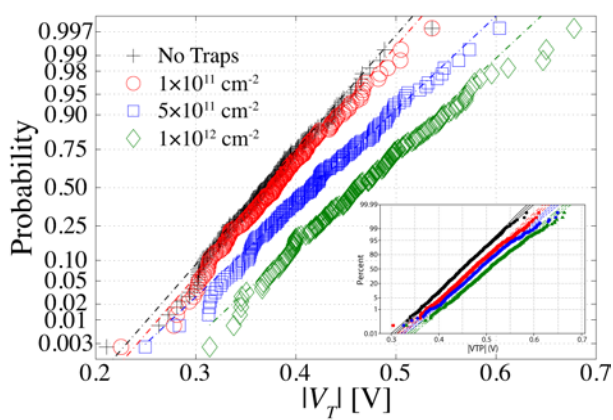
Figure 1. A normal probability plot of the threshold voltages, VT of 200 microscopically different 45nm p-channel devices. Plots for devices with no traps, and with trap sheet densities of 1×10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 1×10^{12}cm^{-2}, are shown. The inset shows experimental results for a similar device from STM.
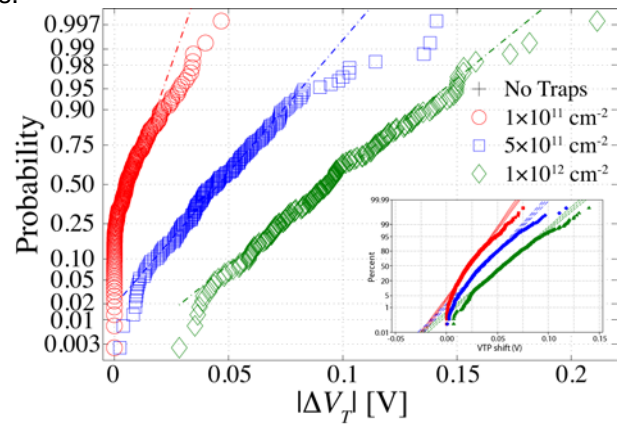
Figure 2. A normal probability plot of the increase in threshold voltages, ΔVT, of 200 microscopically different 45nm p-channel devices when trapped charge is introduced at the Si/SiO2 interface. Plots for devices with trap sheet densities of 1×10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 1×10^{12}cm^{-2} are shown. The inset shows experimental results for a similar device from STM.

The fresh devices include random discrete dopants (RDD) and line edge roughness (LER). The threshold voltages are extracted, based on a current criterion, and their distribution for the fresh devices is plotted with black crosses in Figure 1. Three different levels of NBTI degradation are investigated corresponding to positive interface charge densities of 1×10^{11}cm^{-2}, 5×10^{11}cm^{-2} and 1×10^{12}cm^{-2}, and Figure 1. also shows the threshold voltage distributions corresponding to these three different charge densities. Apart from the average increase in the threshold voltage associated with NBTI degradation in large transistors, a marked change in the slope of the distribution is observed in Figure1, indicating an increase in the spread with the increase in trap density. Figure 1 also clearly indicates that the threshold voltage distributions are not strictly Normal (which would present as a straight line on the plot), and the departure from normality is larger in the tails. For each of the 200 devices simulated, the change in V_T as a result of the NBTI degradation is shown on a normal probability plot in Figure 2 for the same three levels of degradation. For low trap sheet density (1×10^{11}cm^{-2}) there are many devices that show no increase in threshold voltage at all. In these cases the traps (if there are any) are not occurring at locations within the channel where there is significant current flow, as dictated by the distribution of discrete impurities.

Figure 3 illustrates results of the simulation of one particular microscopically unique pMOSFET that includes random dopants and LER (a) without and (b) with additional trapped charges. Both the colour mapped hole concentration and the positions of the random dopants are shown (acceptors in blue, donors in red). One iso-concentration surface is included providing a clear visual impression of the non-uniform channel formation due to the discrete random dopants and LER.

(a)   (b)
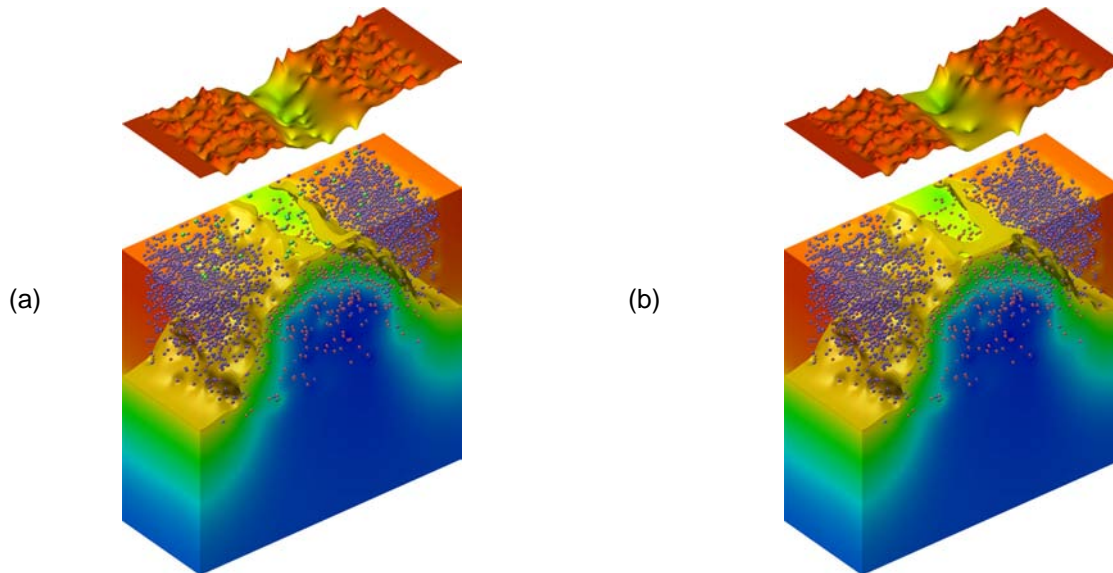
Figure 3. Hole concentration in one particular microscopically different p-channel device that includes random dopants and LER (a) with and (b) without additional trapped charges with a sheet density of $5 \times 10^{11} cm^{-2}$. Acceptors are shown in blue and donors in red, while trapped charges are green. One iso-concentration surface is included, and the surface plot above shows the hole concentration in a sheet through the channel.

On 28th April 2009, STM provided UoG with the Technology Computer-Aided Design (TCAD) data for the IBM 32nm low power devices. This consisted of device structure files (compatible with the Synopsys Sentaurus simulation package), which provided device geometry and doping profiles, and also I_D-V_G characteristics. Further clarification of specific material parameters was also provided when requested.

UoG has introduced the provided device structures into the UoG 'atomistic' device simulator. The profiles of each dopant species are mapped onto the simulation mesh used by the simulator, and saved as doping files to be read in upon execution of the simulator. The next step was to run the simulator to produce I_D-V_G characteristics at low and high drain voltage and calibrate the simulations to match the TCAD simulation results provided by STM. This is done by adjusting parameters in the mobility models (such as the saturation velocity) to obtain the correct current levels, and the metal gate workfunction can be adjusted to match the threshold voltage. The mobility models used are a doping concentration dependent model to account for ionised impurity scattering, a perpendicular electric field model to account for surface roughness scattering and a longitudinal electric field model to account for velocity saturation. Good agreement between the UoG simulator and the provided current-voltage characteristics has been obtained for both n- and p-channel devices.

Once the simulator has been calibrated to match the provided data, the different sources of variability that are important for this particular bulk MOSFET technology can be introduced. For both the n- and p-channel devices the sources included are random discrete dopants (RDD), line edge roughness (LER) and workfunction variation due to metal gate granularity (MGG). As a preliminary investigation, simulations to calculate the variability in the threshold voltage were performed including different sources of variability, alone and in combination. The UoG 'atomistic' simulator has been modified as part of this project to include MGG for the first time. This allowed the impact of MGG to be estimated, as this source of variability had not previously been examined. The effect of the average diameter, $\overline{\varnothing}$, of the grains in the gate was investigated, looking at the change in V_T distribution and V_T variability. It was observed that σV_T increases with increasing grain size and starts to saturate as the average grain diameter approaches the dimensions of the channel. Figure4a presents the V_T distributions for different $\overline{\varnothing}$ showing that the distributions are bounded by the threshold voltages corresponding to the two different workfunctions that can occur in the TiN gate. Figure4b presents the distributions for different sources of variability showing that the spread in V_T due to MGG is as large as that due to random dopants. It is also clear that the V_T distribution with all sources is not Gaussian, and making the assumption that it is could affect the validity of, for example, statistical circuit and timing simulations.

(a)   (b)
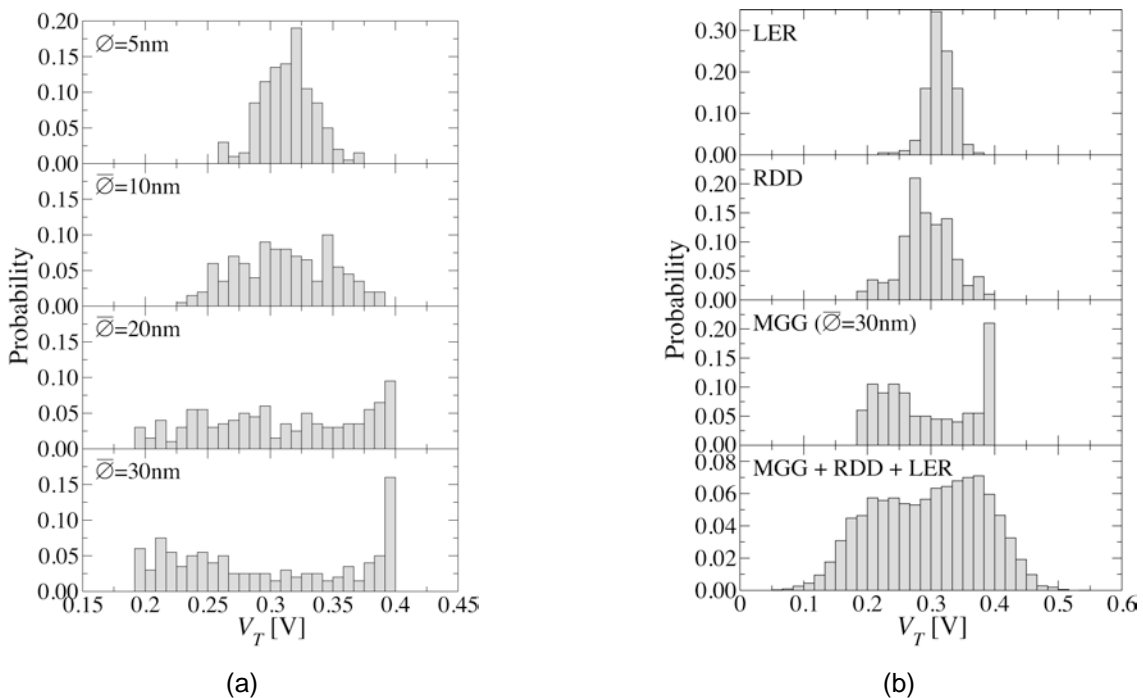
Figure 4 Distribution of threshold voltages for 200 devices (a) each with a different gate grain pattern, for different average grain diameters, and (b) with each of the three individual sources of variability considered here (MGG, RDD and LER) and also with all three sources combined. For the final case of all sources combined, 10,000 devices have been simulated.

Following discussions with STM it was decided to use an average grain diameter for the gate material taken from literature (22nm). This produced very close to the same σV_T as published data for IBM 32nm technology giving confidence in the results of the simulator. Then full I_D-V_G characteristics for ensembles of 200 'atomistically' different devices were simulated, for both n- and p-channel devices at high (V_D=1.0V) and low (V_D=0.05V) drain voltage.

On obtaining the 32nm process design kit (PDK) from STM it was found that the I-V characteristics obtained from Spice simulations with the PDK did not closely match those supplied from the TCAD simulations to which the UoG simulator had been calibrated due to the difference in release number between the PDK SPICE models and the TCAD data that has been transfer to UoG. If UoG were to extract compact models directly from the variability simulations these would not be consistent with the compact models in the PDK being used by the other project partners. An alternative method for the propagation of variability information from the device models to the circuit level was proposed and agreed upon. STM agreed that UoG may provide the I-V characteristics from their device simulations to IMEC who would extract *variability injectors* which can be incorporated into any compact modelling strategy. In this way the variability obtained from the UoG simulations can be included within statistical circuit simulations based on the STM 32nm PDK while at the same time providing a level of abstraction from the original information provide by STM to UoG under the NDA.

IMEC extracted variability injectors from two sets of I_d-V_{gs} curves (atomistic simulations) provide by UoG. UoG built atomistic transistor models based on the low-level technological information provided by ST and performed 200 atomistic simulations for nmos and pmos-type transistors each. IMEC applied the s2v (statspice to VAM) tool implementing extraction methodology and derived statistical populations (DV_{th}, Db) for random variations. Figure 5 shows the results for *nfet* - n-type MOSFET model – and *pfet* - p-type MOSFET model.
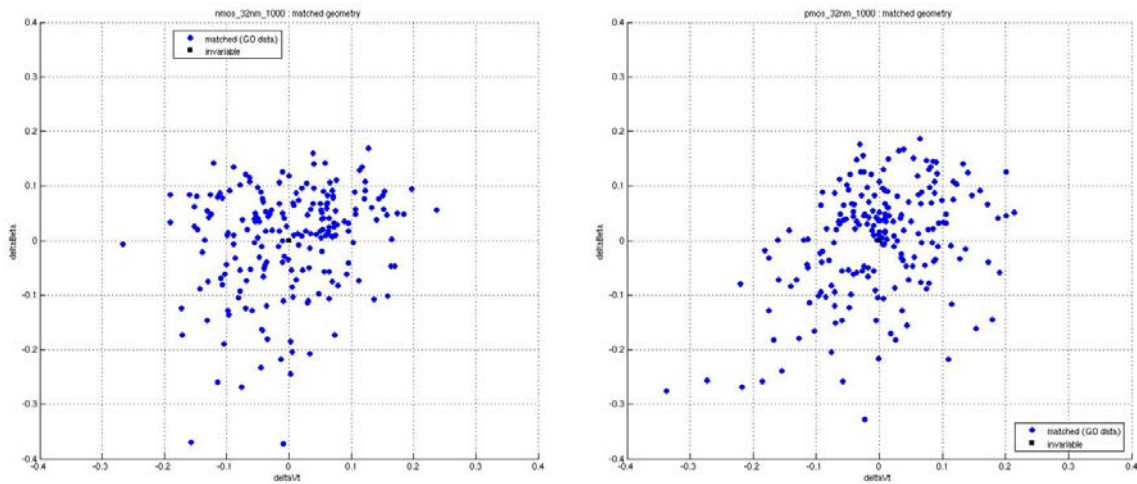
Figure 5: The random variations (DV_{th}, Db) of *nfet* and *pfet* type transistors (extracted from the family of I_d/V_{gs} curves coming from atomistic simulation)

IMEC analysed variability clouds extracted from UoG atomistic simulation data. Table 1 summarise the results for random process variations. It shows the standard deviation values of DV_{th} and Db for two basic transistor models - *pfet* and *nfet* – having minimal size (*w*=32nm, *l*=32nm).

	sigma DV_{th}	**sigma** Db
nfet **(nmos type)**	9.04382E-02	9.65812E-02
pfet **(pmos type)**	9.05554E-02	1.00704E-01

Table 1. Standard deviation values for DVth and Db parameters

Because the UoG atomistic model and simulations take care of process variation sources at the atomistic level and also add some additional variation sources not included in the statistical compact spice model of ST, the standard deviation values are expected and reasonable.

IMEC has made the variability injectors available to project partners so they can be used in statistical circuit simulations.

Use of resources

Partner	Planned effort (MM)	Actual effort (MM)
UOG	12	39.6(*)
IMEC	4.4	4.4
UNIBO	0	0
ST	2	2.35
KUL	0	0
ARM	0.2	0.2
TOTAL	18.6	46.55(*)

(*) The actual number of PMs for UoG is much higher than planned because UoG had to develop the methodology for simulation of metal grain variability which was not envisaged at the beginning of the project. Therefore we had to deploy significant additional manpower. This became possible due to the favorable exchange rate for the Euro and by deploying PhD students at lower rate than a normal research associate. The additional man power was also used to explorer in details the accuracy of different compact model strategies that will be reported in the next deliverable.

12.2. WP2: System and circuit characterization and sensitivity analysis (WP leader: IMEC)

This section describes the status of all WP2-related activities.

Task 2.1: Development and characterization of a standard cell library under variability impact

- Objective: To develop analysis and simulation techniques for statistical characterization of standard cell libraries;
- Input: Transistor-level netlist of each standard cell to be characterized;
- Output: Techniques for statistical characterization of a standard cell library.

ARM has kept on developing with his EDA partner the characterization tool capable of generating a CCSA-VA liberty file with a high enough accuracy. A good correlation between analysed variability and Monte Carlo simulation was finally achieved. A 80 cell library has been characterized and will be evaluated on a system level design. The main remaining issue in the field is the validation of the characteristics of a complex cell, especially flip-flops which characterization is incompatible with the traditional Monte-Carlo methodology applied in HSPICE.

For ST, in the reporting period the statistical characterization of device random mismatch for industrial standard cell libraries in ST's CMOS065LP (65nm low-power) technology has progressed in line with the plans. For device mismatch characterization, ideally every single transistor should be exposed to characterization, thus introducing a larger characterization time that given the typical size of industrial standard cell libraries has rapidly become unaffordable. Therefore, speed-up techniques are mandatory to reduce the characterization runtime.
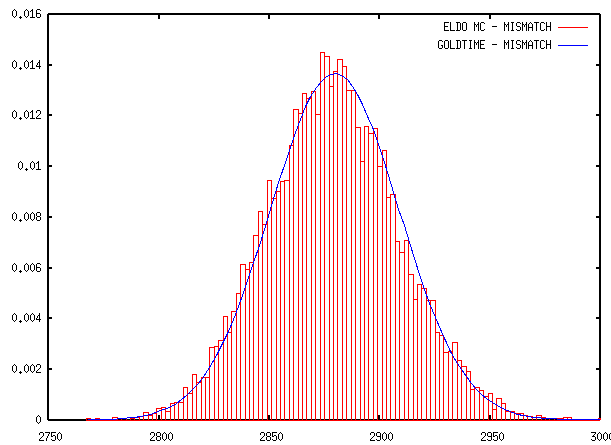
Figure 6 SSTA (GOLDTIME) vs. Monte Carlo (ELDO MC\)
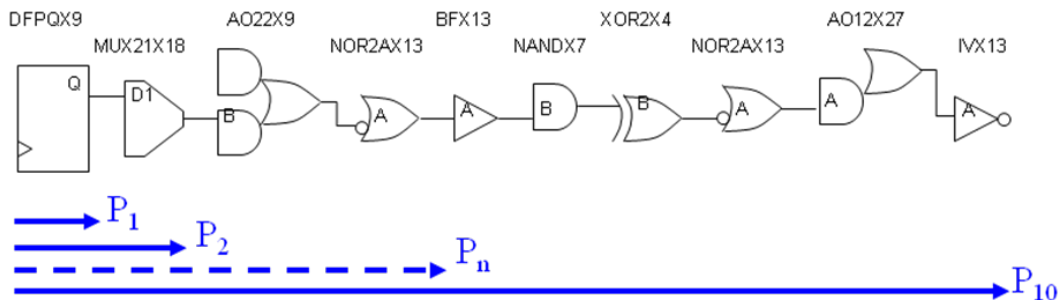
Figure 7. Timing path in CMOS065LP technology

A practical, yet accurate, technique to reduce the mismatch characterization time that was developed and validated during the reporting period, is based on the simultaneous identification of the transistors impacting the cell performances, on the reduction of the characterization grid size, and on the identification of a restricted set of transistor parameters that largely impact on the device performances, since it would not be feasible to consider all the parameters present in typical transistor compact models. The parameters that confirmed the most significant impact on cell delay were the threshold voltage and mobility.

The approach developed for random mismatch characterization was validated by comparing statistical static timing analysis (SSTA) against transistor-level Monte Carlo analysis on several path delays extracted from industrial digital blocks in CMOS065LP technology designed at ST. The experimental results reported in Figure 6 demonstrate an excellent agreement between SSTA and Monte Carlo analysis, thus validating the proposed technique for mismatch statistical characterization.

Furthermore, a design-level analysis on the extracted timing paths was performed. The statistical timing analysis carried out on the timing path depicted in Figure 7 are reported in Figure 8, and demonstrate that mismatch is impacting only short paths, since for longer paths the random nature of device mismatch cancels out.
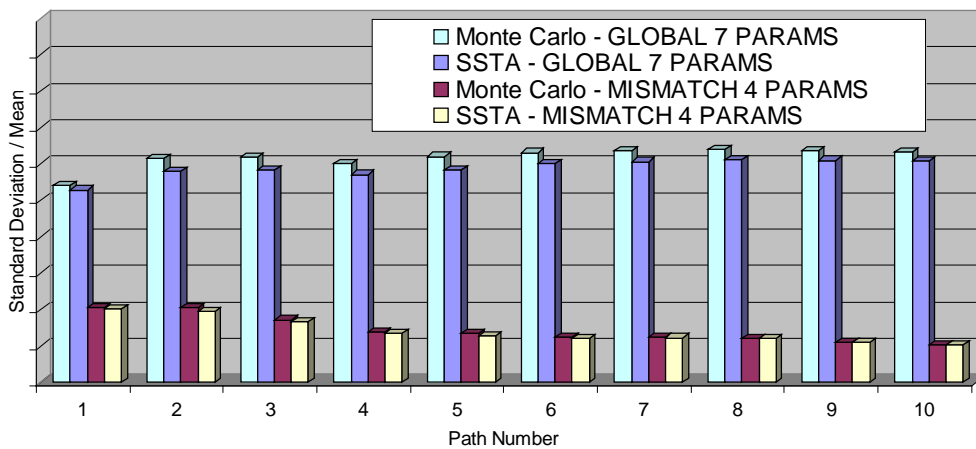
Figure 8 Device mismatch impact on path delay

Again, the statistical analysis performed both on global parameters and on mismatch parameters shows an excellent correlation with respect to Monte Carlo analysis, thus validating our approach.

The statistical characterization performed in CMOS065LP was also extended to CMOS045LP (45nm low-power) technology, which is today the most advanced CMOS nanometer technology in production, and the same characterization methodology and flow were used. An important factor to be considered is the non-linear dependence of cell delay on process variations, which was characterized in CMOS045LP. Poly CD, as well as threshold voltage, exhibits a non-linearity (more significant in PMOS devices) as shown in Figure 9. Poly CD non-linearity was known in CMOS065LP, but threshold voltage was observed in CMOS045LP, likely due to large deviations coupled with low voltage and temperature.

Other cell timing characteristics were analyzed. In particular, we considered the propagation delay and output slope, whose behavior against process variability are reported in Figure 10 and Figure 11 respectively, where both propagation delay and output slope variations for different timing arcs (~2900) of various standard cells with different driving strengths follow a well-defined trend vs. delay and slope values, for a given voltage and temperature condition.
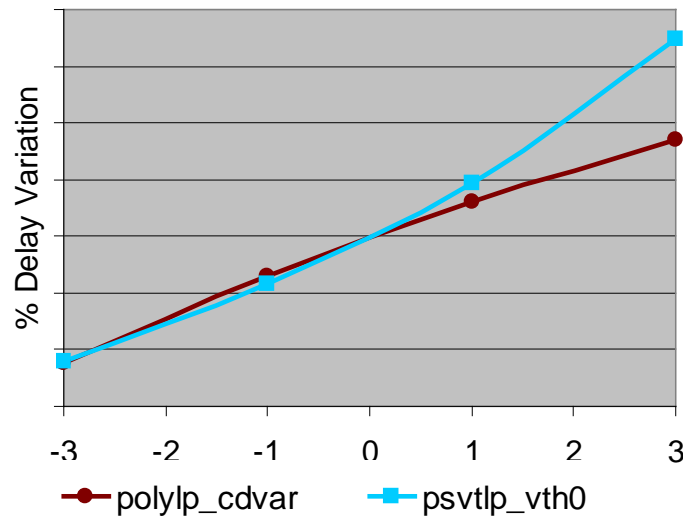
Figure 9 Poly CD and threshold voltage non-linearity

We also analyzed the impact of device mismatch in CMOS045LP, with the same approach validated for CMOS065LP. With the increase in the number of stages along the delay path, the sigma/mean ratio follows a similar relationship to what was observed in CMOS065LP.

Finally, statistical characterization was also performed on standard cell libraries in CMOS045, exploiting commercial tools currently available in the ST design flow. In particular, local mismatch libraries were generated around the corners:

- "Slow-Slow" min VDD;
- "Fast-Fast" max VDD.

Liberty-NCX tool was used to perform this characterization. The tool contains smart algorithms to avoid running a full Monte Carlo analysis, since as it was demonstrated from the activity in CMOS065LP, that many simulations for a single slew/load pair are needed, and consequently the characterization runtime is too large. As a result, the statistical characterization runtime was drastically reduced and with respect to deterministic library characterization, the overall overhead was significantly less than 4X.
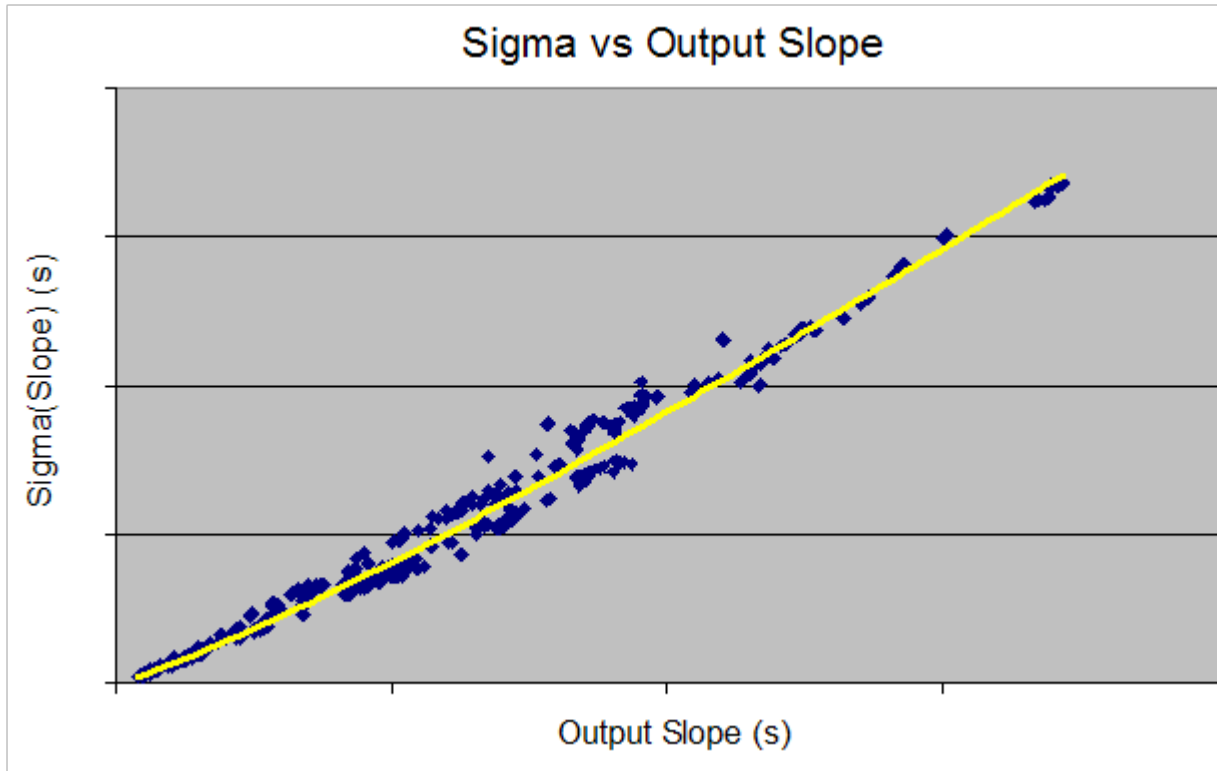
Figure 10. Output slope variation trend
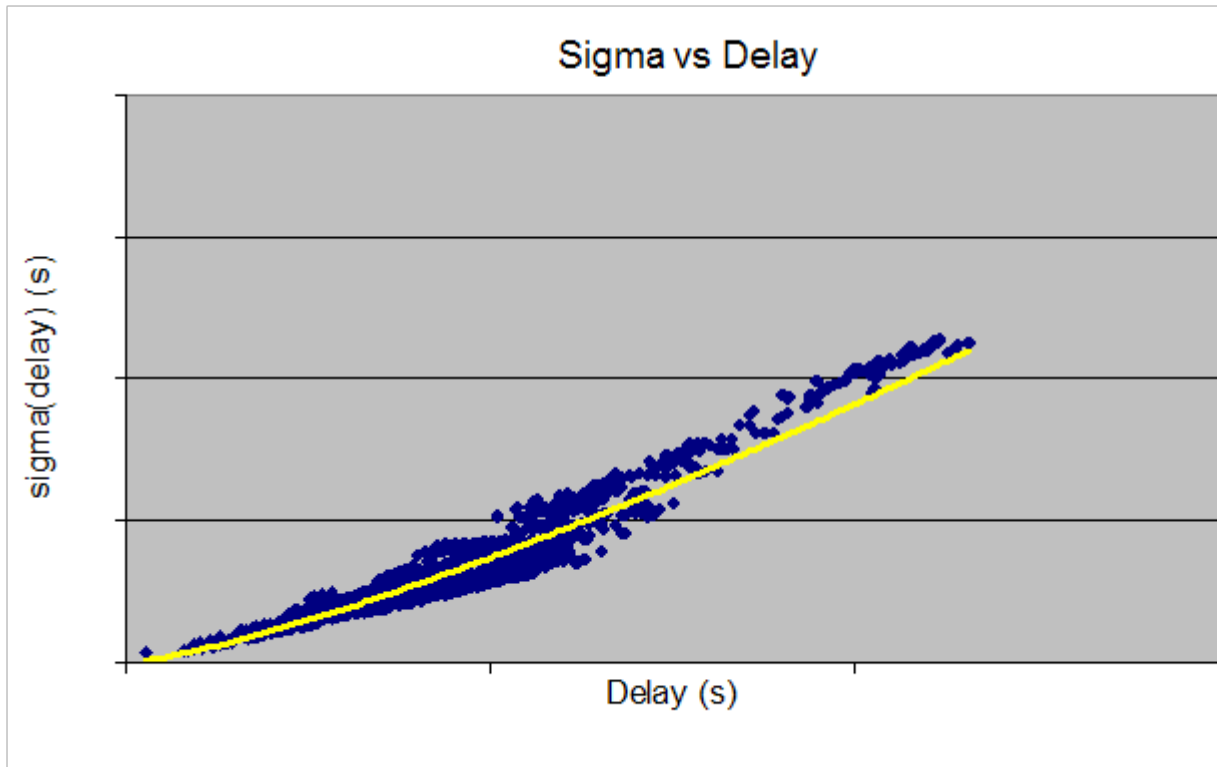
Figure 11. Propagation delay variation trends

The statistical libraries thus obtained are currently under exploitation for the statistical timing analysis of digital blocks and SoCs.

Task 2.2: Statistical Characterization of Macro-Blocks

The memory created for D3.2 was adapted and prepared to be tested by the MVAM tool. Test benches were created to test energy use, memory delay and setup and hold time for the data input. The work necessary to prepare the memory was larger then it should be. A few reasons for this can be given. 1) The memory had to be shrunk to 1/8 of its original size (from 8KB to 1KB) making it suboptimal. This had to be done to make a more fair comparison with the ARM memory. 2) More fundamental, the MVAM tool uses sliced netlists (netlists in which idle components are cut to reduce computational overhead). Making a correct sliced netlist for a complex memory is far from trivial. 3) To increase simulation speed, memory access cycles used to set bit data, precharge voltages etc. and replaced by complex initial conditions, which have to be added manually. 4) Energy calculations on sliced netlist are particularly difficult to implement as energy multiplication factors differ from subcircuit to subcircuit and are different for active and leakage power. KUL will continue this work in 2010 to make the comparison with the current ARM solution possible.

The characterization of memory blocks using the Extreme Value Statistics has first been adapted to the write margin issue. A methodology has been defined to evaluate the worst case of the traditional static write margin scheme. Since our office is also focusing on SOI technology, we developed new dynamic techniques to find the real worst case write margin taking into account SOI effects. To achieve this goal a monitoring of the body potential is done and re-injected in the simulations after then. The technique has been applied for first test on a 45nm bitcell. In the meantime transient simulations schemes have also been investigated to accurately imitate the behaviour of the cells during the actual usage in read and write mode.

In the read mode, for example a simple worst case cell has been modelled using the previously extracted Extreme Values distribution. The accuracy of this simulation has not been proven yet.
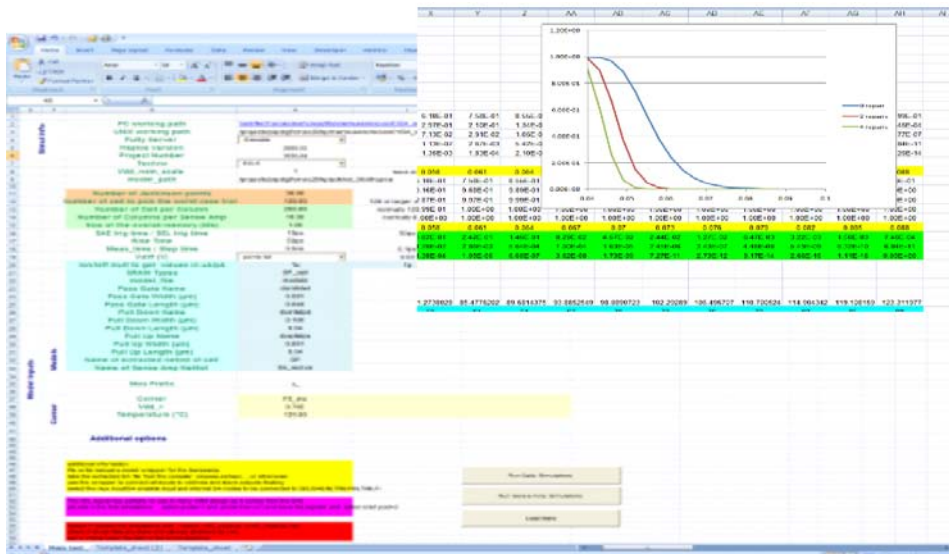
Figure 12: Snapshots of the "push button" margining

In parallel a push button tool has been developed for the designers to easily apply the read current characterization. The tool is based on an XL file which contains all the necessary simulation information for the simulation. Once the spice simulation is completed the output data are loaded and the Extreme Value distribution is automatically fit.

From these data a Yield curve with different scenarios are shown to the designer. Despite this interface effort designers are reluctant to use this methodology since the mathematical background appears too heavy and they find the traditional sigma parameters they were using for ages.

Task 2.3: Hybrid (corner/statistical) Statistical Analysis flow of for Digital Blocks

- <u>Objective</u>: To develop an innovative yet practical solution for statistical analysis and process variability evaluation of large SoC designs in advanced nanometer technologies and targeted towards industrial exploitation;

- <u>Input</u>: Statistical standard cell library, gate-level netlist of digital blocks. Industrial standard cell corner libraries; industrial STA tools, derating factors (for on-chip variations, i.e., OCV), device compact models and process parameter variations;

- <u>Output</u>: Statistical timing information of the digital block, critical path, and statistical information for average/worst-case timing. Statistical libraries with local device mismatch, reduced OCVs, hybrid statistical analysis flow.

Statistical analysis solutions for random within-die (WID) variations available today are quite complex for an effective industrial exploitation. Most approaches for WID variations are focused on systematic mismatch, which can be ameliorated by means of manufacturing-driven improvements (regularity, restricted design rules, resolution enhancement techniques). In REALITY we demonstrated that Statistical Static Timing Analysis (SSTA) is a good estimator of random WID variations, but in general, it lacks ease of deployment in an industrial environment, and requires a lot of efforts to characterize the statistical libraries, as it was demonstrated with the work previously carried out in WP2. Moreover, it also true that chip designers in an industrial environment, who have to satisfy tough turn-around-time requirements, and have to meet strict time-to-market windows dictated by an increasingly fierce competition, do not want to change the traditional sign-off methodology for timing verification based on deterministic static timing analysis.
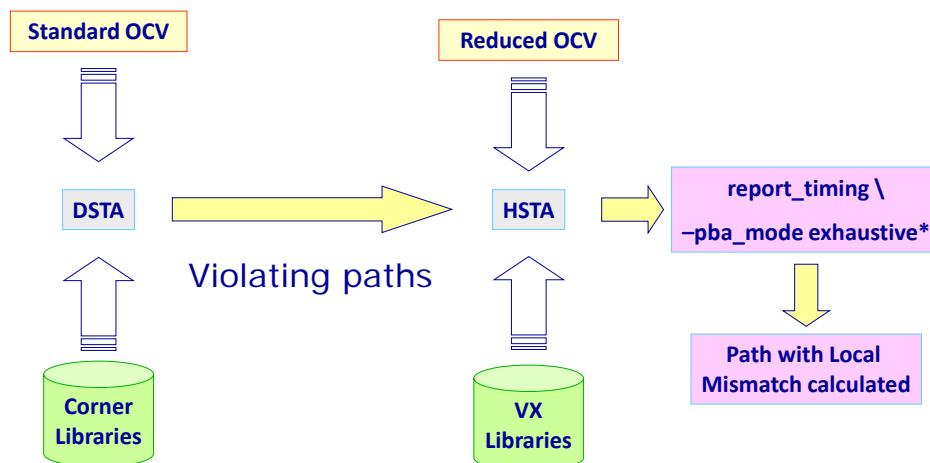
Figure 13 Hybrid statistical analysis flow

Therefore, it is necessary to develop a rapidly deployable solution based on existing and reliable commercial CAD tools and an industrial digital design flow, which also uses industrial models to reduce the impact of random intra-die variations at the cell level. Moreover, it is necessary to define the basic set of process parameters to effectively characterize the standard cell libraries. The objective of this activity (Task 2.3) is to develop a *hybrid statistical analysis flow* based on commercial Deterministic Static Timing Analysis (DSTA) tools and a new technique to consider the impact of random WID variations (i.e., device mismatch characterized in Task 2.1.2). By means of this approach it will be possible to analyze the local random variations without using the traditional design margins (based on derating factors) that we demonstrated with the previous work in WP2 to be either pessimistic or risky. The hybrid flow will allow reducing the design margins and removing some pessimism, without changing the digital sign-off flow and methodology. To enable this hybrid flow, new techniques to characterize statistical libraries including the contribution of local device mismatch have been defined and developed. Furthermore, new characterization techniques based on innovative algorithms will be developed and exploited, in order to avoid running a full Monte Carlo analysis, which is extremely time-consuming as it was demonstrated by the previous work carried out in WP2.

The Hybrid Statistical Timing Analysis (HSTA) flow developed during the reporting period is outlined in Figure 13.

A traditional DSTA based on corners is carried out using the tools currently available in the digital sign-off flow. Based on the results obtained in WP2, where we demonstrated that this approach introduces unnecessary design margins, we developed a statistical-based technique to remove part of this pessimism. After DSTA, we considered the critical paths violating the timing constraints and also we considered those paths that were "potentially" critical, i.e., whose timing slack was very small and subject to the detrimental impact of process variability. During this analysis, OCVs were taken into account by means of derating factors (which can be overly pessimistic as it was demonstrated during the previous WP2 activities).

After selecting the critical/violating paths, on one side we reduced the OCV margins (based on process variability data) and we also carried out a path-based SSTA (HSTA) based on the statistical libraries characterized in Task 2.1.2. Following this approach it was possible to single out the paths which were most critical, to carefully analyze them considering the random WID variations, and to optimize those paths by removing the timing violations without taking unnecessary margins.

This approach was used to evaluate the impact of random mismatch variations on digital designs in CMOS045LP (45nm low-power) technology.

Task 2.4: Statistical Analysis of SoC Architectures
The objective of this activity is to develop analysis and simulation techniques for statistical analysis of computing architectures. This Task depends on Tasks 2.1.2, 2.3, and 2.4, which have been the main target in 2009 1H. Hence, it is necessary to complete the activities planned in these Tasks before addressing the statistical analysis of SoC designs. A prototype of IMEC's system level variability collapsing technique is has been developed and implemented in MATLAB and JAVA. Testing and verification is ongoing. Sample results exists.

Task 2.5: Variation Aware Information Format:
An electronic information format (IF) that is parallel to the classical top-down and bottom-up design flow was developed. It provides the data interface for variability information between several levels of the design flow. For the interface between each level of abstraction of modeling or simulation a particular information chapter is defined. In particular, transistors, standard and non-standard cells, as well as macro blocks and entire SoCs are supported.

Imec continuously extends the specification towards new requirements that appear in the scope of the project. Examples are advanced TDDB and BTI models, or the capability to perform block-level sensitivity analysis of local random variations in circuit blocks, or features in the plot browser to comfortably colour several aspects of the populations such as GO/NOGO flags.

Use of resources

Partner	Planned effort (MM)	Actual effort (MM)
UOG	1.5	1.5
IMEC	10.8	10.8
UNIBO	0	0
ST	15	15
KUL	3	1
ARM	10	10
TOTAL	40.3	38.3

12.3. WP3: Mixed mode countermeasures (WP leader: KUL)

Task 3.1: Development of a formal method to analyze the effect of device level variability/reliability at the circuit level

This task was finalized and delivered at T0+12M. As such there is no further progress to be reported here.

Task 3.2: Design of variability/reliability-resilient memory IP blocks

This task is divided in two parts: a first section extends the work done in T3.1 to include variability awareness to the reliability simulation. In a second section, this knowledge is used to design a variability/reliability resilient memory IP block.

T3.2a: Variability-aware reliability simulation

Input from KUL

Aggressive scaling to nanometer CMOS technologies causes both analog and digital circuit parameters to degrade over time due to die-level stress effects (i.e. NBTI and HCI). Additionally failure-time dispersion increases due to increasing process variability. The purpose of this task is finding an efficient simulation method to analyze the reliability of electronic circuits.

Deliverable D3.1 (T0+12M) reported a software methodology developed to predict and analyze the impact of reliability degradation on electronic circuits. Accurate models suitable for each degradation effect have also been developed. The method developed in T3.1 is used as an input for T3.2a.
In year 2 of the project a methodology to simulate electronic circuit reliability including process variability has been developed. It incorporates a chi-square goodness-of-fit test to optimize failure-rate analysis. Advantages over current state of the art reliability simulators include, among others, the possibility to perform a failure-rate analysis with the ability to correctly and holistically account for the effects of complex time-varying stress signals.

Results show that taking time-varying stress signals into account provides circuit reliability information not visible with classic DC-only reliability simulators. In addition, variability-aware reliability simulation results indicate a significant percentage of early circuit failures compared to nominal design failure-time results.

Current research is focused on finding a more efficient (i.e. faster and more accurate) way to implement the variability-aware part of the simulator.

T3.2b: Design of variability and reliability resilient memory IP blocks

Input from IMEC:

Imec setup the environment and run the statistical characterization flow on the KUL SRAM memory. The flow environment requires preparation of several input files describing memory architectural and circuit properties in well defined format. KUL, as the memory design owner, had to deliver the critical path netlist of their 32kbit high-performance SRAM memory design and the set of testbenches. The results of statistical characterization are stored in the XML VAMIF cell chapter and in the LIBERTY format compliant set of memory cell libraries.

Imec setup the environment and run statistical characterization, represented by the MemoryVAM tool, on the KUL 32kbit high-performance SRAM memory design.
To setup and run characterization flow imec had to prepare set of input files. The following list enumerates the most important ones: ***Circuit islands definition***; the principal setup file contains the definition of circuit islands identified by corresponding spice subcircuits together with some other properties attached to it.

#name	subcircuit	gamma	multiplicity	divider	redundancy	
c_w	sa|d2hgbl	0	32	1	0	#dimension1: cells in a word
w_b	-	0	16	1	0	#dimension2: words in a block
b_bs	-	0	2	1	0	#dimension3: blocks in a blockset
bs_bc	-	0	16	1	0	#dimension4: blocksets in a block column
bc_m	vgbl2hgbl|enai|enbi|bcs	0	2	1	0	#dimension5: block columns in a memory
b	local_control	0	b_bs*bs_bc*bc_m	1	0	#local blocks in a memory
w	lwl_driver	0	w_b*b_bs*bs_bc*bc_m	1	0	#words in a memory
c	cell	0	c_w*w_b*b_bs*bs_bc*bc_m	1	0	#cells in a memory
lbl	lbl_driver|lbl_precharge	0	b_bs*bs_bc*bc_m*c_w	1	0	#local bit lines in a memory
bsbl	gbl_driver	0	c_w*bs_bc*bc_m	1	0	#blockset-gbl connections
br	brs	0	b_bs*bs_bc	1	0	#block rows
r	gwl	0	b_bs*bs_bc*w_b	1	0	#rows in a memory

Figure 14: The islands definition for the KUL 32kbit SRAM memory

The Figure 14 shows the content of such setup file for the KUL memory. ***Variability scaling rules***; the setup file defining scaling rules applied to the extracted performance metrics in the process of translating the multiple path performances into an observation of the memory performance. ***VAMIF compact model chapter***; this input file contains the statistical population of variability injectors (DV_{th}, Db) for all transistor models used in a memory design. ***VAMIF cell chapter;*** the VAMIF chapter with the top level configuration container, where user has to specify all pathnames of required input files and parameters that control the overall run of MemVAM characterization.

KUL, as the memory design owner, had to deliver the critical path netlist of their 32kbit high-performance SRAM memory design and the set of testbenches. ***Memory critical path*** contains one representative path, i.e. one instance of every block, and some additional circuitry to capture the layout influence across a chip. ***Measurement testbenches*** probe certain performance and stability metrics (commonly called performance metrics). We defined seven testbenches enabling extract the set of timing performance parameters – Q to CLK delays and DATA to CLK setup and hold times – and the set of power parameters – cell leakage power and CLK rise/fall power.

The output results from the characterization run are stored in VAMIF cell chapter and also as a collection of LIBERTY compliant memory cell libraries.

Input from KUL:

The challenge for both low power and variability aware design lies in the fact that this type of design does not fit in the classical top-down or bottom-up design methods. A design flow which looks over the edges of the classical abstraction levels is needed as design decisions on one level have profound effects on other levels. At this time, hardly any design methods or automated tools exist that can cope with this cross-level design. In this work, the design of an SRAM in 32nm CMOS technology is taken as a case study for a new design methodology.

Designing an SRAM memory is designing in between the architectural and the circuit levels of abstraction. Process technology can also be considered (litho-aware design...), but in this case this is limited to the use of statistical device models. The connection between the architectural level and the circuit level of design can be made by using statistical behavioural models. These models should incorporate the energy-variability trade off which is extremely important in the design of memories in DDSM technologies. This way, it is possible to optimize for energy consumption at the architectural level.

The memory IP blocks under consideration in this project are: memory cells, sense amplifiers, decoders, data busses and timing control blocks. As in all low power design, the following general design parameters constitute a trade of: activity, speed (frequency), capacitance (size), supply voltage and swing. All of them are strongly related to variability.

Options to improve the energy/variability properties of memory cells include: use of a specific architecture: (5T, 6T, 8T...), use of a sleep mode, use of different word line voltages, back gate biasing, use of high threshold transistors and the use of other bit line precharge voltages. The design of a bit line data bus is very closely connected to the cell architecture of choice. Important techniques used are: use of a divided bit line architecture (closely related to SNMTRAN, a new way to assess stability), use of charge recycling techniques, use of write-after-read schemes, the choice between single-ended and differential signalling,

buffer type, etc. For the other data busses, low swing signalling, signal gating and divided word lines are possible ways to limit energy consumption. Sense amplifier design choices include: the degree of SA sharing between different bit lines, the architecture, sizing, and use of tuning, compensation or (asymmetric) redundancy.

After significant delay due to the lack of device models, simulations were performed to prove the validity of the proposed circuit techniques. For stability, a combination of HVT SRAM cells with a divided bit line structure is promising. Using the obtained results, a 32KB SRAM memory was designed and simulated. A speed of 1GHz was obtained. The memory uses about 1.2pJ/access. The distribution of energy consumption the memory is showed in Figure 15.
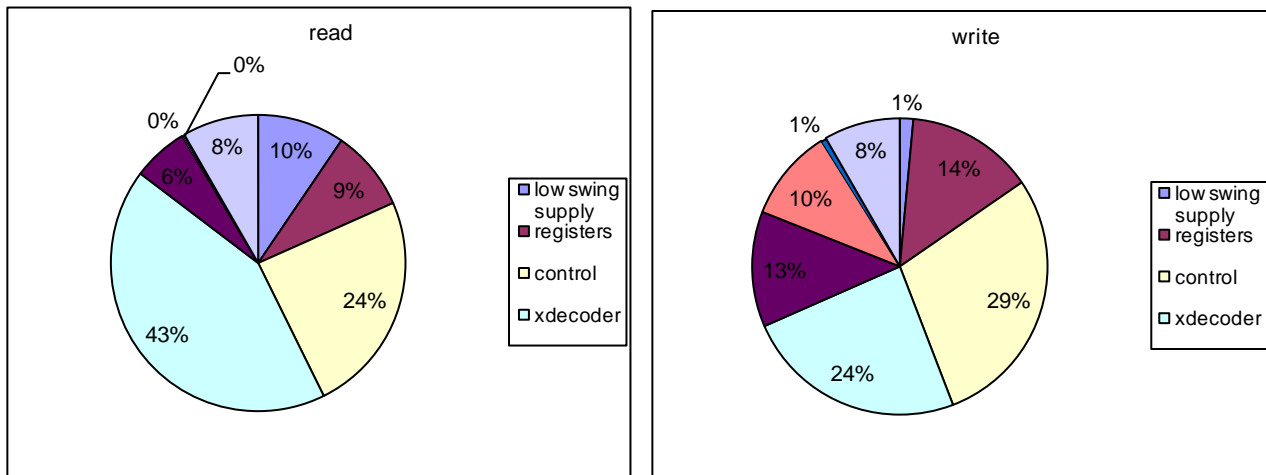
Figure 15 Ddistribution of energy consumption for different memory parts of the designed memory.

Task 3.3: Development of architectural solutions for variability management of data path and controllers

This task was finalized and delivered at T0+12M, as such there is no further progress to be reported here.

Task 3.4: Development of architectural solutions for variability management in on-chip interconnect fabrics

Input from Unibo

In M13-M24 UNIBO activities within WP3 have been concentrated on the completion of T3.4, whose results have been reported in D3.4. More specifically:

1. Analysis of the impact of variability on chip interconnect, considering both systematic and random variations considering both AVS and FBB.
2. Design and implementation architectural solutions for compensating variability effects.
3. Experiments to show the impact of the implemented techniques in terms of link delays and power consumption.
4. Completion of the deliverable D3.4 delivered on M24.
5. Design of speed/leakage meters to be used for runtime monitoring of variability effects.

Networks on Chip (NoC) links are essentially global point-to-point interconnects, which are evolving into complex communication channels with drivers and receivers, in an attempt to mitigate the effects of reverse scaling and reduce power.

In M13-24 UNIBO has performed characterization of the performance spread of these links due to variations, and started the exploration and assessment of power-aware compensation techniques for them is becoming

a key design issue. The effectiveness of ABB vs ASV has been compared on two on-chip point-to-point link architectures: a traditional full-swing and a low-swing signaling scheme for low-power communication. Extensive characterization experiments have been performed with the

goal of obtaining guidelines for the post-silicon variability compensation of these communication channels, while considering realistic layout effects. In particular, the implications of cross-coupling capacitance on the effectiveness of variability compensation have been considered.

Use of resources

Partner	Planned effort (MM)	Actual effort (MM)
UOG	0	0
IMEC	0	0
UNIBO	7	21(*)
ST	1	1
KUL	40.4	26(**)
ARM	0	0
TOTAL	48.4	48

(*) The actual number of actual MMs effort is for UNIBO much higher than initially planned because we used much more junior resources than expected that resulted in more PMs. As a consequence, there is not impact on the budget; rather UNIBO is currently in an under-spending condition.

(**) Due to the large delay in delivering the 32nm data, KUL had to delay its activities in task T3.2, resulting in incomplete work in this task by the planned finishing date in the previous DOW, as well as in personnel under-spending in KUL. Since the results of task T3.2 are an important input for WP6, KUL proposes to continue and finalize the work by extension of Task T3.2 into 2010, in close collaboration with the activities in WP6. KUL will report this extended work in an updated version D3.2b of the Deliverable D3.2. An updated DOW is requested to the project coordinator by KUL to reflect this change.

12.4. WP4: System level countermeasures (WP leader: UNIBO)

The main activities performed by UNIBO between M0 and M18 are related to Task 4.1, 4.2 and 4.3. The results of these activities are reported in D4.1 and D4.2 delivered on time at M9 and M18 respectively. Below we give an overview of the activities for each task.

Task4.1 and Task 4.2 (M0-M9): These tasks have been carried out to implement the workload allocation, migration and data allocation infrastructure. The results achieved in this task allow to perform workload allocation among the cores of the variability affected platforms. In addition, a task migration technique has been implemented that will be used in Task4.4 and Task4.5 for implementing workload management policies on the validation benchmarks.

Task4.3 (M9-18):
In this task we developed system level policies for compensation of variability effects on a multicore processor. The work in this task exploits the software infrastructure implemented in task 4.1 and 4.2.

The policies focus both on performance and energy as optimization metrics. They leverage workload allocation and idleness distribution. This choice has been made mainly because of its generality. Indeed, any multicore platform can support idleness distribution. On the other side, other policies based on dynamic voltage and frequency scaling could be explored and there a few papers in literature that propose this approach. In this project we wanted to focus on a industrial realistic platform case study, in view of the final porting of the presented policies on the target multicore demonstrator (WP5).

To accomplish the work in this task we considered a workload made of a set of independent tasks. Next-generation set-top-boxes will support very high resolution, high-frame rate video rendering with complexv3D GUIs and stereoscopic visualization support. These applications require extensive image processing and enhancements functions which are embarrassing parallel and will be distributed on the VLIW accelerator array as a large number of barrier-synchronized tasks. We assume that an estimate of the workload for each task is available at release time, and that tasks only synchronize on the barrier at the end of their execution. A global deadline, dictated by the frame rate, is specified for the task set. The total energy for frame processing should be minimized to reduce system production and ownership cost and reduce the likelihood of thermal failures.

In Task 4.3 and 4.4, we will focus on porting and optimizing the policies for the specific target benchmarks defined in the validation plan (WP6), consisting of more complex task graphs with dependencies.

Variability effects in multicore lead to performance and power variations among the cores. As such, we focused on workload allocation techniques to compensate for core-level performance and power variability.

In this variability-affected context, workload allocation based on nominal performance level for all cores is not a robust approach, in fact if a slower core is given the same workload as faster cores, it will execute in more time and it will become the bottleneck for barrier release. Furthermore, energy efficiency concerns would push for increasing utilization of slower cores which are characterized by lower leakage and, consequently, lower static power.

The main contribution of the work achieved during the last period of the project is the definition and experimental validation of optimal non-uniform workload allocation policies that compensate for platform variability both in terms of predictability and energy efficiency.

More in detail, we addressed the problem of distributing tasks onto accelerators with the primary objective of minimizing deadline violations and the secondary goal to minimize energy consumption. This goal ordering is dictated by the fact that frame-rate violations may severely degrade the user quality of experience and should be avoided as much as possible. First we define a static allocation policy where globally optimal allocation is computed with a computationally intensive integer-linear programming (ILP) solver. This approach is useful as a design-time lower-bounding analysis step to assess optimality losses of on-line policies, or it can be at used at application start-up time if the number of accelerators is not large and thus ILP solution time on the CPU is smaller than a couple of seconds. Second, we define a two-phase approach based on linear programming (LP) and bin packing (BP). This algorithm is sub-optimal but it is much faster and can definitely be applied at application start-up even for large coprocessor arrays. Allocation policies computed at application start-up are applicable when the workload does not change significantly on a frame-by frame basis, as in the case of image enhancement applications, which perform very regular pixel operations (e.g. Gaussian filtering, color-space conversion, etc.).

We explored the design space in terms of numbers of cores, and we tested a large set of different workloads and tightness levels of deadline constraints. . In our experiments a key parameter is the tightness of timing constraints. These constraints have been selected to obtain variable platform utilization. These constraints are referred as tconstr_1, tconstr_2, tconstr_3, tconstr_4. They are listed in order of tightness of the constraint.

We also compared with state-of-the-art solutions for variability-aware energy minimization, namely Rank Power and Rank Frequency policies, to demonstrate that our policies are much more robust in terms of real-time predictability while providing competitive energy savings The results about energy comparison among the policies demonstrate that the proposed ILP solution provides better results in terms of energy consumption and deadlines are always met. Our policies are able to save energy when the time constraint is more relaxed. Rank based policies spend the same energy independently from the constraints (they do not take them into account) and violates the deadlines in most of the cases.

In this task we considered variability effects acting independently on critical path delay, leakage power, and dynamic power. As a consequence, the critical path delay, leakage power, and dynamic power of each core can be identified by a point in a 3D space where coordinates represent the entity of variations. Variability distribution data have been obtained through IMEC's VAM tool flow, which provides distribution of critical path delay, leakage and dynamic power. VAM tool flow is the main tool flow used in this project for variability modelling work performed in WP5.

During the work done in this task, we also studied the variability compensation capability across a number of platforms generated using VAM. The proposed policies are much more effective in compensating performance impact of variations with respect to RF and RP, as shown in Figure 16.

Here we can observe that our policies compensate variations by reducing time violations due to variability effects and lead to predictable performance results. Indeed, the execution times provided by LP+BP and ILP are very close but lower than 0.040000 seconds independently from the platforms, which is the time constraint we used for these experiments. On the other side, rank policies lead to much more variable execution times. It must be noted that, by considering each single platform, our policies provide always lower energy while matching time constraints.

Finally, it must be noted that for our policies the energy spread is slightly larger, but mainly because our policies are aimed at minimizing energy (indeed the minimum energies are provided by our policies), not to match a given energy budget.
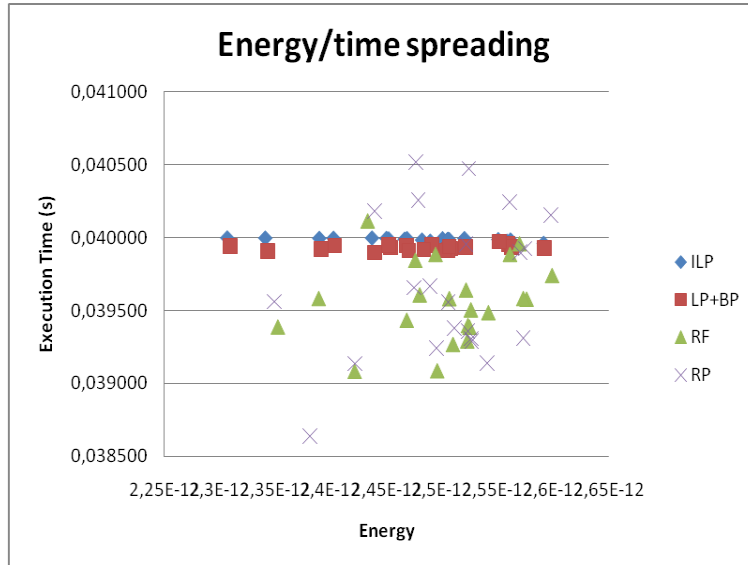
Figure 16 Execution time vs energy consumption per cycle.

During M19-M24 UNIBO developed an optimized version of the variability-aware task allocation policy, suitable to be applied to the MPEG2 benchmark used for validation in WP6. The new version is characterized by an optimized implementation of the LP part of the allocation algorithm, that was the main bottleneck. The new version is much more faster and scalable than the previous one and can be applied online, i.e. on a frame-by-frame basis. The execution times of the new version of LP are reported in Table 2:

execution time[usec]	3slaves	6slaves	9slaves	12slaves	16slaves
LP	202	402	617	851	1189
BP (8 tasks)	6.45	20.70	64.25	108.69	168.13
BP (16 tasks)	13.47	36.80	63.66	111.81	158.60
BP (32 tasks)	35.53	85.87	153.12	239.57	421.27
BP (128 tasks)	271.13	429.01	676.78	1092.81	1728.76

Table 2 Execution time of the optimized LP version and BP algorithms for an increasing number of processors and tasks

The LP algorithm does not take tasks into account so there is only a single line. On the other side the BP execution times depends on the number of tasks. In both cases it can be observed that execution times are on the order of microseconds for a wide range of slaves and tasks. If we compare this number with the typical execution time for a frame decoding, which is on the order of milliseconds, we can conclude that the allocation policy (composed by LP+BP) can be applied online. As a consequence, the allocation of the parallel tasks performed to decode a single frame can be decided frame by frame.

Another activity performed in the second period of the year is related to the analysis of the MPEG2 benchmark when the platform where it is running it is subject to variability. This activity has been performed with the collaboration of ST Microelectronics, as they provided the benchmark code and studied the feasibility of the task allocation policies.
This variability impact is important to study the effectiveness of the proposed policy and eventually perform focused optimizations. The completion of the policy optimization is foreseen by M27, but here we report first how we apply the task allocation policy on the selected use case.
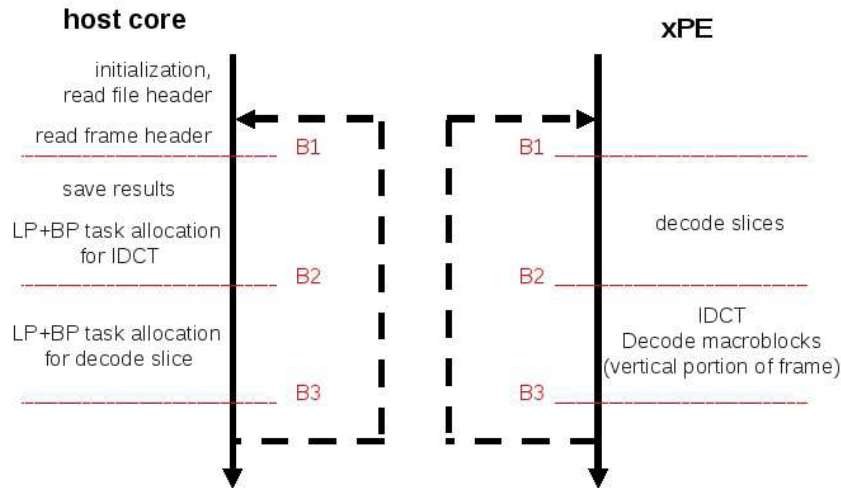
Figure 17 Task allocation policy applied to the MPEG2 benchmark.

Figure 17 summarizes how the task allocation policy is applied to the MPEG2 benchmark. More specifically, there are two functions parallelized that are IDCT and decode slice. These two functions generate a number of tasks, which is a parameter. For each of the two functions the task allocation policy (LP+BP) is applied (phases B2 and B3).

Use of resources

Partner	Planned effort (MM)	Actual effort (MM)
UOG	0	0
IMEC	0	0
UNIBO	6	20,75(*)
ST	2	2
KUL	0	0
ARM	0	0
TOTAL	8	22.75(*)

(*)The actual number of actual MMs effort is for UNIBO much higher than initially planned because we used much more junior resources than expected that resulted in more PMs. As a consequence, there is not impact on the budget; rather UNIBO is currently in an under-spending condition.

12.5. WP5: Design flow, integration, proof of concept (WP leader: ARM)

The first year of the project was dedicated to the definition of the system level platform from ARM and ST on which the integration work has to be done. This work was fulfilled in tasks 5.1, 5.2 and 5.3.
Task 5.4: Implementation and analysis of statistical characterization flow
ARM and IMEC have integrated within a production flow a statistical aware flow. We have focused this work on two methodologies available: the SSTA classical flow proposed by the EDA vendors and the VAM flow partly developed by IMEC within REALITY. Other components of the VAM flow developed outside the project have been provided by imec as background IP to complement the flow and the activities described further on. For each flow two phases were adopted. First a feasibility work was performed on several standard cells before starting the ramp-up phase with the still reduced standard cell library composed of 80 cells.
In order to catch the accuracy of the tools, ARM has developed internally a validation tool capable of testing different variability information and correlating them. The tool named SC3 (Standard Cell Cross Check) is provides the ability to make comparison across different library types, different technologies or different PVT corners. It has proven to be a quite strong tool to challenge the EDA vendors on the accuracy of their variability aware tools. The first results of our investigations showed quite great discrepancies between the standard deviation incorporated in the libraries and the Monte Carlo simulations taken as the golden standard. This difference could be understood and corrected in the latest versions of the tools.

The accuracy concerns lead us focusing on the VAM flow from IMEC. The Weighted Monte Carlo based flow shows a good correlation with the traditional HSPICE simulations at the cell level.

Task 5.5: Block level evaluation

The imec VAM flow was in the context of Reality project applied to the test vehicle based on ARM926. The VAM application on the mention test vehicle include all abstraction levels starting from technology input.

Technology input: the *statspice to VAM* (s2v) tool extracts populations of DV_{th} and Db pairs – variability injectors - for different MOSFET types from a foundry provided statistical device compact model library. In the context of the REALITY project we have applied the s2v tool to obtain the variability injectors from the ST 32 nm statistical device models that were used to characterize the subset of ARM's standard cell library.

Variability injection: the variability injection denotes the process of transforming a spice level netlist with any number and type of transistors into *N* variants of the same. These variants differ to the original netlist in such way, that variability injection sources are added to the MOSFET instances of a cell. The VACCinate tool responsible for variability injection was applied to the subset of ARM standard cell library chosen for the synthesis of the test vehicle based on the ARM926.

Variability aware characterization of memories: the methodology of statistical memory characterization relies on an importance sampling based sensitivity analysis of the different memory building blocks followed by a second sampling stage that combines these sensitivity results to memory path observations. The MemoryVAM tool, implementing the characterization procedure, was applied on all seven embedded memories that are parts of the test vehicle based on the ARM926 to get variability aware memory cell libraries.

Variability aware calibration of digital blocks: the goal of this flow level is to analyze and simulate each of digital blocks' Verilog netlists to provide correlated timing, activity and power reports. The corresponding VAM tool - DigiVAM - accepts the input from cell abstraction level (standard cells and memories) and delivers statistical models of IP blocks (such as controllers, multipliers, or whole processor cores). In the context of the REALITY project we have applied the DigiVAM on the test vehicle built around ARM 926 with all necessary inputs generated by the lower levels of VAM flow (standard cell variability aware libraries, memory variability aware libraries…)

In parallel all the legal issues on the ARM926 RTL delivery have been solved and the initial investigation on the Adaptative Body Biasing scheme developed by UNIBO could start on the ARM926 core. The first investigations were done using a 45nm library from ST. A first analysis done on the 45nm technology showed the ALU was the main element in the design critical path. This results have been confirmed by ARM using a 32nm library. As a consequence, for practical reasons UniBo focused on the ALU of the ARM core.

The legal discussion for the delivery of a 32nm library containing the Back Biasing conditions could be resolved as well. The full back biasing characterization on the 80 cells library could be done and was delivered at the end of the period. The final investigations on the ARM926 will be done in the next period.

The XPE processor was mapped and synthesized on 32nm CMOS technology libraries. A back-annotated simulation environment was built to investigate the static and dynamic power dissipation of the core at different working conditions. The necessary 32nm library characterization files and the core netlists were generated based on ST internal data at different working condition corners and a specific testbench for a single programmable accelerator was implemented with Verilog.

The testbench that has been used allowed the test environment to run a single application on one programmable accelerator without the intervention of a host core.

Two test applications have been implemented to analyze the dynamic power dissipation at medium and high workload: the medium workload application, mainly using flow control, scalar loads and stores, and integer arithmetic operations, and the high workload application, mainly utilizing wide vector arithmetic operations and vector load and stores executed concurrently on both execution lanes.

During the simulation of both applications, the signal activity reports were extracted and used to determine the dynamic power dissipation with both workloads.

Task 5.6: Integration of the building blocks

On the xSTream system platform, the RTL implementation for the system has been completed and successfully tested with embedded Linux running on the host processor and various image processing test applications running concurrently with 16 threads on all 8 programmable accelerators when mapped on an FPGA emulation board. The system has been integrated with control and sensor blocks that emulate the adoption on variability issues at system level, and those blocks have been used by the application software running on the host core for controlling the tasks running on the xPEs.

ST and UniBO implemented a device for computing overall statistics on (per core) power consumption and estimated lifetime, and punctual information about (per core) Vt, temperature, dynamic energy, static energy and clock frequency, computed according to the analytical model defined in the validation plan.

The model was integrated with the xSTream processor simulation platform to analyse the variability impact at the system level. The xSTreamISS is a flexible simulator developed for modelling of multiprocessors and can be adapted to different cores architecture. It can therefore be adapted to simulate the xPE engine of the xSTream processor itself. The simulator has been designed to support interface or behaviours for user defined device. The simulator can provide different levels of accuracy. Many features have been extended and or implemented anew; among them the ability to model variable frequency and multiple clock domains, dynamic change of the operating frequency for each core and other devices at runtime, a GUI which allows monitoring of the cores and the main devices (e.g. the memory blocks) and to interact dynamically with the simulation (e.g. activate tracing, stopping and resuming simulation, etc).
The variability information included in the simulations are based on a "back of the envelop" methodology. The method proposed defines equations to extrapolate the power/speed when V_{dd}, V_t, f are altered with respect to a "reference condition", and it uses fitting constants to tight up equations to available measured data. The variability information needs to be calibrated. In the scope of the reality project the calibration will be made thanks to variability extractions done on the ARM926 using VAM. the simulation platform analytical models for variability have been extended with a preliminary support for a simplified thermal model for the multiprocessor array of programmable accelerator

STMicroelectronics has developed a Monitoring Macro IP which is a real library cell and can be implemented in a system. The Macro IP can be accessed in two ways: either it can provide information during the test either it can bring the variability information directly to the system.
The IP Featuresare
- Test
    - Integrated JTAG IEEE1149.1 interface
    - Controllable using on-chip jtag port
    - Full-scan block except TAP controller which is non – scan by default
- APB Bus Interface
    - Integrated APB Interface, with address and data bus size of 4 bytes
    - Zero Wait states in APB read/write operations
- Parallel Interface
    - Integrated Parallel interface to directly access User Defined Registers.
- Multiple micro sensor for different process options
-
- Three Modes for each µSensor are available
    - Leakometer to monitor process leakage
    - Speedometer to monitor N mos process speed
    - Speedometer to monitor P mos process speed

To integrate this IP to a system design a Process Monitoring Control block has been developed. The block has a distributed architecture and can be connected to multiple Monitoring Macro IPs distributed across the chip.

Use of resources

Partner	Planned effort (MM)	Actual effort (MM)
UOG	0	0
IMEC	2.88	2.88
UNIBO	1	2(*)
ST	8	8
KUL	0	0
ARM	6.4	6.4
TOTAL	18.28	19.28

(*)The actual number of actual MMs effort is for UNIBO slightly higher than initially planned because we used much more junior resources than expected that resulted in more PMs. As a consequence, there is not impact on the budget; rather UNIBO is currently in an under-spending condition.

12.6. WP6: Validation and assessment of results (WP leader: ST)

Fo a summary of the WP6 activities in the first six months of 2009 we refer to deliverable D7.5 "Semi-annual periodic activity report."

For the second half of second year of execution of WP6 activities, the work has progressed mainly for tasks T6.4 and T6.5, allocation of resources to task has been aligned to expected levels from the DoW. Task T6.2, T6.3 have been completed during the first year and first half of second year as reported in the previous Periodic Activity Reports.

Objective in task Task 6.4
Evaluation and benchmarking of the block level IPs integrating components and design flows produced in WP2, WP3, and WP4 as defined by the validation plan and application scenarios. This task might for example include ARM processors cores and programmable accelerators from ST retrofitted with such technologies (ARM/ST/UoG/UniBo).
Work progress in Task 6.4

This task has been one of the most intensive of the whole period and a lot of the project IP and flow validation and benchmarking was either carried out or reported here.
The work was structured in 5 main activities, the first on the results obtained from on 32nm standard cell libraries and the associated statistical analysis with two complementary techniques; the first being a statistical static timing analysis (SSTA) and the other the advanced monte-carlo based VAM characterization flow developed by IMEC. Both accuracy and comparison with standard methods are provided along with a description of their integration in a standard industrial design flow environment.
The second on device characterization methodology and impact of different variations. Results were obtained by using the methodology built in the project, capable of transforming all the technology related variation sources to a two parameter process variation aware compact device model. A comparison of variability injectors extracted from the statistical spice and atomistic model simulations is also provided.
The third on the extensive set of benchmarking and analysis performed on the ARM926 platform. Results were obtained for the statistical analysis on the core netlist and from the application of variability aware design techniques such as back-biasing applied to the processors ALU.
The fourth was about the memory blocks and circuits benchmarking spanned from the outcomes of the statistical memory characterization to the comparison between different kinds of memories, the ones designed from KUL for the project and the preliminary industrial design in 32nm.
The last has been a short analysis of the cost of deploying system level monitoring blocks as the ones speculated to be available and modelled for the REALITY system level activities. STM has designed a flavour of such an IP whose system interfaces were described in D5.3 that has been mapped and validated on real silicon in 65nm technology. Results from this silicon test vehicle are going to be used as input to extrapolate the cost (in terms of area and power) to augment the analysis that are going to be performed in the last phase of the REALITY project.
Some of the results were very preliminary, and as such some additional experiments might have to be carried out to fully justify some of the conclusions; we expect to include the outcomes of those additional characterizations in the future report for D6.4.
So it's expected that some additional work on T6.4 remains to be finalized in the third year.

To summarize major findings of block and analysis flow level investigations on how transistor level variability propagates to product level variability. The first impression when we first look at the variability from device to device, is bad, regardless whether predicted by the works of the University of Glasgow, or the IBM model (probably based on Si measurements) provided to the consortium by ST: the variability of any P- or N-devices outreaches. We see a 3-sigma value for example of the threshold voltage of about 3x90mV in the local random case.
The exact nominal Vt value is not public but with a -270mV variation it is certainly close to zero, which can render the transistor inoperative (always-on) or leaky, while with +270mV, we operate in sub-threshold (always off or very slow). If we look at how this translates to digital circuit and finally system level, we see some cancelling out in local random case, whereas in global random case not.
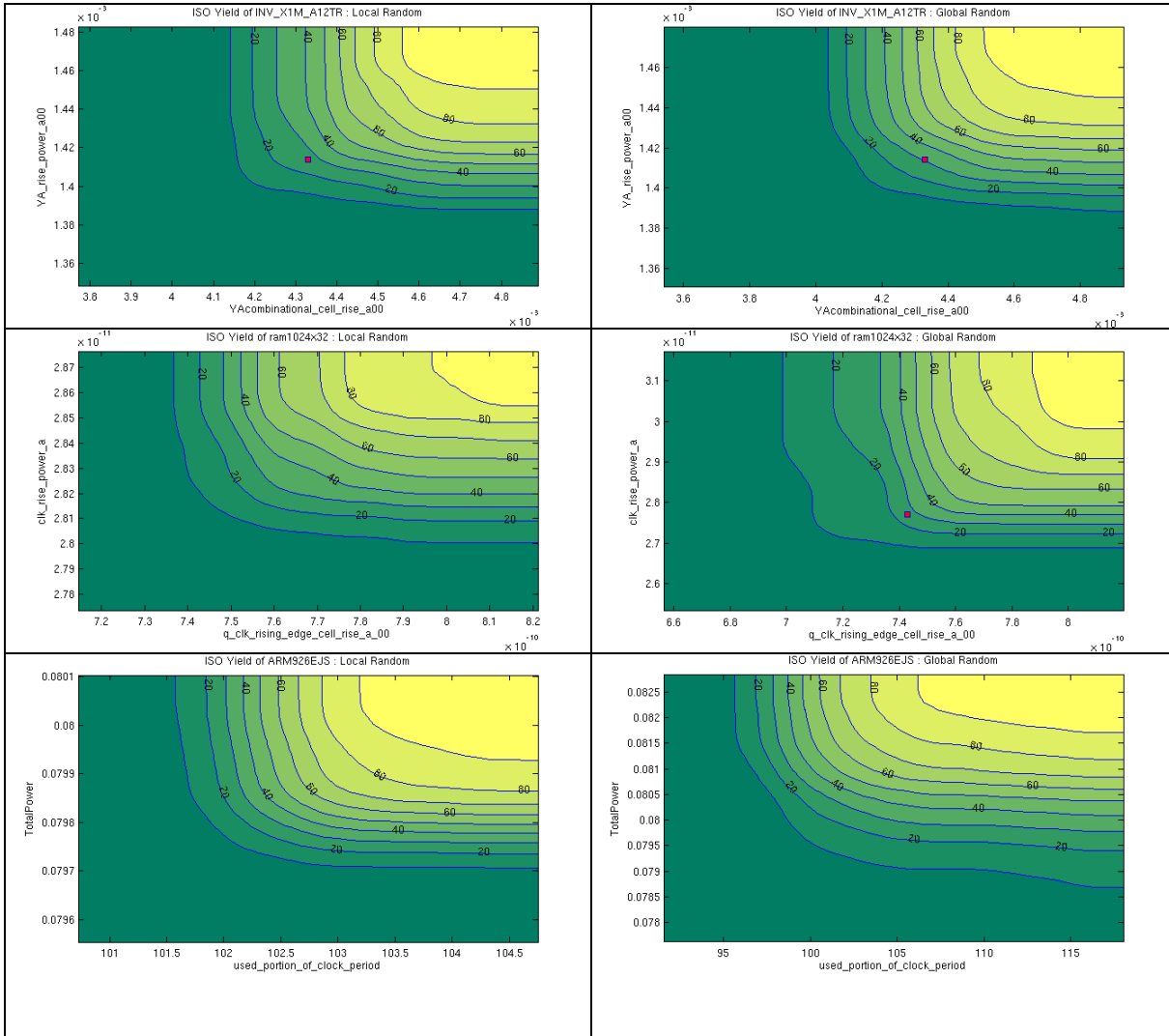
Figure 18: Variability as ISO-Yield MAP for: small gate (TOP), memory (MIDDLE), Processor (BOTTOM).

A general observation that can be made regardless of cell, memory, or processor is that global variability is higher, but local variability also exhibits an additional shift towards worse values, according to the amount of parallelity in the design. What is worse, this shift magnifies the closer we get to product level. This clearly visible in the following table:

	Nominal timing	Max Yield under Local Variations	Max Yield under Global Variations
DEVICE	-	-	-
CELL	4.3ps	40%	60%
MEMORY	740ps	10%	40%
PROCESSOR	1.5 ns (100%)	0%	55%

Finally we read the variability, expressed in percentiles, from the graphs. The thought one-sigma line is about half way between the 80 and 90 percentile lines in the graphs. If we assume unlimited power budget, we read the timing value for on the x-axis where the thought one-sigma line becomes vertical (top of each graph). The conversion to three-sigma works by taking the difference of the 1-sigma to the 0-sigma case, multiplying this difference with three and adding up to the 0-sigma value. In other words, we report what margin must be set, to guarantee 99.89% yield is in the following table:

	Nominal value	3-sigma point Local Random	3-sigma point Global Random

DEVICE (ST)	300mV (*)	90% (**)	-
DEVICE (UOG)	300mV (*)	60% (**)	15% (***)
CELL	4.3ps	11%	12%
MEMORY	740ps	10%	14%
PROCESSOR	1.5 ns (100%)	4.8%	15%

(*) estimated
(**) minimum transistor sizes
(***) transistor size independent

As expected, the local random variability decreases as we move closer to the product due to cancelling-out, extreme value theory, and Pelgrom's rule (not all transistors are at minimum dimensions, effectively reducing local random variability). The global random variability remains constant. Notice that all experiments used the ST device variability as input model, so that we should expect larger variations when using the UoG models in future experiments.

Since in reality, there is always a local and a global component, we foresee a convolution of the two distributions in the upcoming reporting period. This will have the advantage of a fast analytic "collapsing" of local rand and global random data, but will not capture non-linear effects at corner-cases. Therefore, a comparison to a local random variability analysis around a worst global corner seems an interesting parallel approach. Fur sure, local random timing variability around Slow-Slow corner with worst-case VDD, such as 0.9V, will show a dramatic increase as compared to our current data (Nominal-Nominal, 1.1V, resp. 1.0V for the memories).

Af for the memory characterization, a comparison between a low power memory designed by KUL with a regular one provided by ARM (preliminary) was carried out. Results show reduction in power by a factor of ten for a single read access noteworthy, despite the about 30% longer access time, which we believe can be brought to even with the ARM memory without sacrificing all the power achievements. There is still room for improvement, since the KUL design was not optimized for this particular size. Whether the ARM design was at its best or not is unknown. Both use the same technology library and test benches.
Regarding variability, the KUL memory shows a little bit more robustness than the ARM memory. We noticed also an inverted correlation between timing and power when comparing ARM and KUL memories: The slower an ARM memory, the higher its power consumption and the opposite is true for the KUL memory. This may have important implications for design trade-offs at system level.

On the monitoring IP activity, the STM silicon test vehicle demonstrated the full functionality of the sensors implemented in 65/55 nm technology, it also shows a very good potential for providing valuable information as an embedded monitoring block for both speed and leakage at the instantiation location on a SoC. The amount of intra wafer local variation across different dies suggest that tapping those statistics can be leveraged statically for wafer level test and dynamically can indeed be leveraged to trade off performance, power and yield. The area cost associated to the blocks seem to be compatible with their deployment in a multiprocessing platform like the one defined for the REALITY system level validation given that already in 65/55nm the footprint of a complete block is only 0.04mm2. The power consumption of the block should be further reduced to optimize the idle energy consumption

Objective in Task 6.5.1

Porting of application benchmarks selected in T6.1 for both the host ARM926 and the subsystem composed of STM's xPE accelerators to the system level simulation platform. This task includes application mapping and partitioning onto the multiple platform IP blocks and integration with the SW runtime heuristics and countermeasures defined in WP4 (ST/UniBo)

Work progress in Task 6.5.1
This task has been completed.

The first step of porting the MPEG2 decoder to the xSTream platform done by ST and UniBO has been to parallelize the application using pthreads. The second step has been to translate pthreads operations into operations for loading tasks on the xPE accelerators, for starting the execution of the tasks on the xPEs, and for checking if an xPE is running or has completed its task. This has been arranged in a sort of 'framework' that can be reused for translating pthreads into functions (implemented on the GPE) for loading and executing tasks on the xPEs. The last step has been the optimization of this parallelized application since the application was not able to decode video sequences in real time. Part of this optimization has been a further parallelization, consisting in letting the GPE save the results related to the previous frame while the xPEs are decoding the slices of the current frame.

The first step of porting of the AC3 decoder to the xSTream platform has been done parallelizing the application using pthreads. The next step has been done (almost without efforts) reusing the 'framework' developed for the MPEG2 decoder for translating the pthreads into operations for loading and executing tasks on the xPEs

Objective in Task 6.5.2
Evaluation and benchmarking of the system level integration of the building blocks from WP3, and WP4 as defined by the validation plan. This will also include evaluation of the SW heuristics and integrated HW/SW mechanisms that interact and interface to low level controls as defined in WP4, this will be achieved by modeling and simulation methodologies as defined by the validation plan, but wherever practical and possible via simulation on suitable platforms (ST/ARM/UniBO).

Work progress in Task 6.5.2
The device implemented by ST and UniBO for monitoring cores' activity, power consumption and aging, and scaling their frequency accordingly is being used in the xSTreamISS platform simulating the MPEG2 decoder and the AC3 decoder. Variability of cores in the xSTream platform is simulated using the VAM tables, and 'normalizing' the values of a (randomly chosen) row in the VAM table with the nominal values characterizing the xPE processor. ST and UniBO are performing a number of simulations with different values taken from the VAM table.

Use of resources

Partner	Planned effort (MM)	Actual effort (MM)
UOG	0	0
IMEC	0	0
UNIBO	1	0
ST	9	9
KUL	0	0
ARM	3	3
TOTAL	13	12

WP7: Project management (WP leader: IMEC)

A description of the work in this work package can be found in section 14 on project management.

Use of resources

Partner	Planned effort (MM)	Actual effort (MM)
UOG	0.6	0.6
IMEC	4.8	4.8
UNIBO	1	0.25
ST	0.2	0.2
KUL	0.5	0.5
ARM	0.3	0.3
TOTAL	7.4	6.65

(*) Please note that, according to the DoW, UNIBO has 1p/m in WP7

12.7. WP8: Exploitation and Dissemination (WP leader: IMEC/ARM)

A description of the work in this work package can be found in deliverable 8.3 which is the dissemination and use plan. This deliverable contains the work of all partners.

In addition numerous technical articles have been submitted to various conferences. Many of them already accepted for presentation at international forums.The list below gives an overview of all published technical articles published in 2009.and invited presentations:

Invited Presentations and manuscripts contributions

- Concerning invited presentations, Miguel Miranda, project coordinator gave an overview of the project status of REALITY on his talk: ***Design for Variability Efforts in Europe – REALITY project*** at the 2nd NMI International Conference on CMOS Variability: ICCV 2009, Wednesday, 13th May 2009 in London-UK (http://www.nmi.org.uk/conference/index.html)
- A. Asenov, Statistical variability and reliability in next generation CMOS technologies and the ITRS response. 2nd NMI International Conference on CMOS Variability: ICCV 2009, Wednesday, 13th May 2009 in London-UK (http://www.nmi.org.uk/conference/index.html)
- Davide Pandini, Statistical Static Timing Analysis: A New Approach to Deal with Increased Process Variability in ***Europe – REALITY project*** at theAdvanced Nanometer Technologies, 2nd NMI International Conference on CMOS Variability: ICCV 2009, Wednesday, 12th-13th May 2009 in , London-UK (http://www.nmi.org.uk/conference/index.html) (invited)
- D. Pandini, "Variability in Advanced Nanometer Technologies: Challenges and Solutions," (Keynote Speech) PATMOS, Sep. 2009.
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Use of resources

Use of resources Partner	Planned effort (MM)	Actual effort (MM)
UOG	1.5	1.5
IMEC	1.6	1.2
UNIBO	1	1
ST	1.5	1.3
KUL	1.6	1.6
ARM	1.1	1.1
TOTAL	8.3	7.7

13. Deliverables and milestones tables

Planned Deliverables between T0+13M and T0+24M (All delivered)

	TABLE 1. DELIVERABLES								
Del. no.[1]	**Deliverable name**	**WP no.**	**Lead beneficiary**	**Nature [2]**	**Dissemination level [3]**	**Delivery date from Annex I (proj month) [4]**	**Delivered Yes/No**	**Actual / Forecast delivery date**	**Comments**
D2.1.2	Report on small standard cell library	WP2	IMEC	R	CO	T0+18M	Yes	T0+M21	Delivered Initially planned for M18, this report has been delivered on M21. Work was completed on time but with a delay associated to have in place the necessary legal clearances allowing to distribute the report among partners.

[1] Deliverable numbers in order of delivery dates: D1 – Dn
[2] Please indicate the nature of the deliverable using one of the following codes:
R = Report, **P** = Prototype, **D** = Demonstrator, **O** = Other
[3] Please indicate the dissemination level using one of the following codes:
PU = Public
PP = Restricted to other programme participants (including the Commission Services)
RE = Restricted to a group specified by the consortium (including the Commission Services)
CO = Confidential, only for members of the consortium (including the Commission Services)
[4] Month in which the deliverables will be available. Month 1 marking the start date of the project, and all delivery dates being relative to this start date.

D3.2	Design report on the variability/reliability resilient memory IP blocks	WP3	KUL	R	PU	T0+24M	Yes	T0+24M	Delivered
D3.4	Report: techniques for enhancing interconnect variability tolerance	WP3	KUL	R	PU	T0+21M	Yes	T0+21M	Delivered
D4.2	Report on Control Algorithms for System Reliability and Variability Management	WP4	UNIBO	R	CO	T0+18M	Yes	T0+M18	Delivered
D5.2	Sample Implementation Flow	WP5	ARM	R	PP	T0+18M	Yes	T0+M18	Delivered
D5.3	Delivery of block level and system evaluation report	WP5	ARM/ST	R	PP	T0+21M	Yes	T0+24M	Delivered Initially planned for M21, this report has been delivered on M24 to accommodate for the delay associated to the delay associated to the delivering of the 32nm data and to having in place a research island needed to allow IMEC to get around liability requirements to access the ARM core. New timing Reflected in the latest DoW update
D6.2	Validation and Assessment of Results:	WP6	ST	R	PU	T0+18M	Yes	T0+18M	Delivered

	Validation Plan								
D6.3	Block level evaluation report as specified by the validation plan	WP6	ST	R	PP	T0+21M	Yes	T0+M24	Delivered Initially planned for M21, this report has been delivered on M24 to accommodate for the delay in D5.3 and its dependency.
D7.5	Semi-annual project progress report	WP7	IMEC	R	PU	T0+19M	Yes	T0+19M	Delivered
D7.6	Annual project progress report	WP7	IMEC	R	PU	T0+24M	Yes	T0+24M	Delivered

Table 3 List of planned Deliverables for Year 2

Planned Milestones between T0+M13 and T0+24M

MILESTONES							
Milestone no.	**Milestone name**	**Work package no**	**Lead beneficiary**	**Delivery date from Annex I**	**Achieved Yes/No**	**Actual / Forecast achievement date**	**Comments**
M3	Definition of Evaluation platform for system integration	WP3, WP4, WP5	ARM	Month 18	Yes	Month 17	Achieved
M4	System wide benchmarking of the integrated system on evaluation platform	WP3, WP4, WP5, WP6	ST	Month 24	Yes	Month 24	Achieved
M5	System wide yield assessment of variability impact at 32nm	WP1, WP2, WP6	ST	Month 24	Yes	Month 24	Achieved

Table 4 List of planned Milestones for Year 2

14. Project management

14.1. Consortium management tasks and achievements;

The Project Coordination and related Management tasks are a vital part of the successful execution of the REALITY project. The applied management approach is fully embedded into the daily operations of the REALITY project. This section describes the achievements and organization in the REALITY project during the first reporting period. This way of working will be continued throughout the entire project timeline. The project coordination and management aims at providing the necessary infrastructure to support the complicated task of decision making and communication between the REALITY partners. The organizational structure of the REALITY project management is presented in Figure 19:
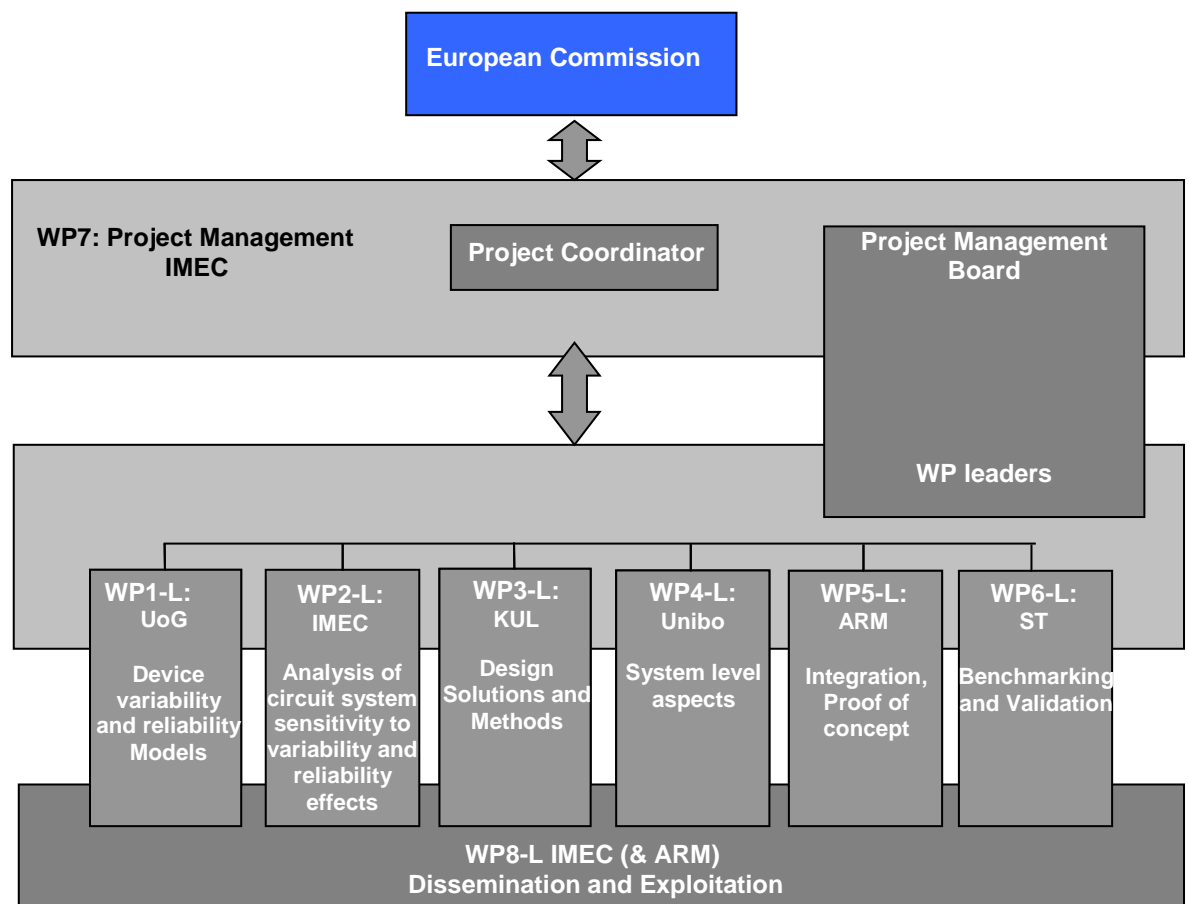
Figure 19 REALITY project team and coordination

IMEC acts as the project coordination of the **REALITY** project. IMEC oversees the day-to-day management and acts as the liaison between the project and the EC.

A Snapshot of the main management tasks :

- Keeping the global overview of the project.
- Communication list compilation and keeping it up-to-date.
- The technical management of the project, oversight and steering the scientific and technological development in the project.
- Keeping the actiontracker and follow-up the timely closure of actions.
- Keeping and follow-up of the Decisions list.
- Organizing the Risk Management.
- Monitoring deliverables and milestones, organizing the proper review of deliverables.

- Measuring the actual progress against technical objectives.
- Recommendations about major changes in the planned work.
- Chair the Project Management Board.
- Organization of the Project Management Board meetings and Project Technical meetings, including definition of the Agenda and key topics.
- Driving the dissemination and use (see deliverable report D8.3) activities
- Collection and submission of cost statements, overview of budget situation
- Promotional flyers and posters
- Organizing Contract negotiation for consortium agreement
- Update of the Description of Work, version v2.0

The Project Management Board is comprised of one member from each partner (WP leaders) and is chaired by the project coordinator. The input from the respective organization of each member regarding coordination, planning, monitoring and reporting will be disseminated in the board. Finally, the board is responsible for all the strategic decisions regarding the direction of the project. These responsibilities include:

- Strategic planning
- Managing assets complementary to innovation: budget, addition of new partner
- Contract negotiation for consortium agreement
- Set up of Non Disclosure Agreement (NDA)
- Contracts and licensing agreements resulting from the valorization initiatives
- Protection of intellectual property
- Technology transfer

For practical reasons, the project management board meetings and project team meetings – except the technical workshops – have been combined in the first reporting period.

The Work package leaders are responsible for the coordination and execution of the tasks and the deliverables within their respective work package. They have reported all technical results regarding the project (deliverables, publications, etc.) to the project coordinator.

14.2. Problems which have occurred and how they were solved or envisaged solutions

14.2.1. REALITY Top Risks to date:

There is a continuous evolution in problems occurring. Some major risks which were identified at the project kickoff have materialized and proper actions have made sure the impact was mitigated. Some other risks which were identified did not come true or the priority (severity or probability) was much lower than expected, and finally a few new risks popped up during the course of the first reporting period.

A continuation we provide a brief summary on the risks identified at the beginning of the project and updates related their evolution along the different reporting periods: M1-M12, M13-M18, M19-M24

Top risks and their evolution reported during the different reporting periods

1. Availability of process data in 32nm cannot be guaranteed:

    Period 1 (M1-M12) – See Deliverable D7.4

    During 2008, STM, the partner responsible for the availability of technology dataset to the consortium communicated the difficulties on making such dataset available (32nm). The difficulties originated on the decision at STM corporate level to stop manufacturing operations at the 32nm technology node. Thus, STM had to rely on an external technology provider, IBM. Since IBM would be one of the foundries that would process STM products in such advanced nodes. STM needed to wait for IBM to make such data available, thus affecting the execution and planning of the project.

Close to the end of period 1, STM communicated it could make available process data from IBM to selected partners and estimated the first quarter of period 2 as possible time frame for such transfer. The data delivering did actually take place in period 2 but in a much later time frame than initially expected.

First half Period 2 (M13-M18) – See Deliverable D7.5

STM Process data in 32nm was made available on April 2009 to one of the partners: Univ. of Glasgow with the purpose performing atomistic TCAD simulations. A statistical device compact model card was still missing to UoG and other partners (imec, ARM, UNIBO and KUL). On M17 STM communicated their strong commitment to deliver the remaining information at week 38 at the latest on exchange of a 4-way NDA involving the affected partners but ARM. In the meanwhile, ARM clarified having no need to access such data as they already had it via IBM directly. NDA was signed on M19.

Second half Period 2 (M13-M18) – This deliverable

The statistical device compact model card was made available to the remaining partners (imec, ARM, UNIBO and KUL) at M22, hence resolving the risk. As a consequence of the accumulated delay, deliverables D5.3 and D6.3 required an extension in their due date to (see Section 13). A DoW update was issued in month M24 to reflect this delay. Fortunately, such delay did not affect the completion of the milestones proposed for period 2.

However, KUL had to delay its activities in task T3.2, resulting in incomplete work in this taks by the planned finishing date, as well as in personnel effort under spending. Since the results of task T3.2 are an important input for WP6, KUL proposes to continue and finalize the work by extension of Task T3.2 into 2010, in close collaboration with the activities in WP6. KUL will report this extended work in an updated version D3.2b of the Deliverable D3.2. An updated DOW is requested by KUL to the project coordinator to reflect this change. Overall, at this point of time (end of period 2) we can safely say that this risk has been mitigated on time. The project coordinator trust that it will not affect the overall outcome of the project.

2. Availability of ARM926 softcore is not guaranteed.

Period 1 (M1-M12) – See Deliverable D7.4

During period 1 the project team identified two test vehicles to be used in the project. One of them requires an ARM test vehicle containing the ARM926 core. The availability of the ARM926 softcore was identified as a top risk as this is sensitive information that can only made available to partners under restrictive legal conditions.

The main roadblock developed mainly between imec and ARM (not with other partners though) due to too restrictive legal conditions in which ARM would facilitate the soft core to imec under unlimited liability while imec could only accept limited liability (one million euros)

On M13, after a visit of an imec delegation to ARM headquarters in Cambridge, a solution was found to sort out this road block. In 2009 a research islands (a legally neutral SW environment controlled by ARM where both partners could access and work on common without actually exchanging intellectual property) would be setup to perform the planned work on the ARM926 soft-core. Such common workplace or research island would become complemented with stages of IMEC engineers at ARM. This solution would also allow earlier access to the imec engineers toward the 32nm dataset already available at ARM..

First half Period 2 (M13-M18) – See Deliverable D7.5

On M18 the research island was not yet available. Few practical problems limited its deployment. A special machine with sufficient memory was ordered and its delivering suffered of some delay. Also the availability of licenses for the different SW tools for simulation and analysis of the ARM926core delayed its deployment..

Second half Period 2 (M13-M18) – This deliverable

On M22 the research island became fully operational. Deliverables D5.3 and D6.3 required an extension in their due date to accommodate the delay in the deployment of the island, also of the availability of the 32nm dataset to imec engineers. Still, overall, this risk is now fully eliminated without affecting the milestones planned for period 2 and overall the outcome of the project.

3. The developed methodologies in WP3 and flows may become not be integrated in the project.

Period 1 (M1-M12) – See Deliverable D7.4

At the beginning of the project it was observed that the drafting of the DoW did not included a path for integration of the activities resulting of WP3 in the overall project assessment plan propose in WP6. Quicly the risk of having a part of the project without connection to the rest was identified by the consortium. Still no special correction mechanism was taken in period 1, partly due to the fact that the integration and benchmarking activities (WP5 and WP6 respectively) where still under definition.

First half Period 2 (M13-M18) – See Deliverable D7.5

On M17, an update of the REALITY DoW was issued wherein imec, KUL and ARM defined a new activity in WP3 and WP5 consisting on benchmarking KUL's memory design techniques developed against exiting ARM memory products. KUL would provide the new memory circuits in WP3. Imec would benchmark the memory using its statistical memory analysis environment within WP5. IMEC and ARM would do similarly for the ARM product. ARM would benchmark the outcome of the analysis in WP6. The new activity was drafted to be devoted to evaluate the feasibility or unfeasibility of the implementation of the techniques developed in WP3 in an industrial context also allowing an assessment to be produced within deliverable D6.3.

Second half Period 2 (M13-M18) – This deliverable

Due to the large delay in delivering the 32nm data, KUL had to delay its activities in task T3.2, especially those involved on the benchmarking memory design techniques developed on WP3 until M24. Still at this point of time the planned benchmarking activities have been partially completed and a mid way assessment has been provided in deliverable D.6.3 (recently submitted). Indeed this risk has been almost completely eliminated without having a negative impact in the overall outcome of the project.

14.2.2. Status of the 32nm data set – history of developments

This section is added to this document to address the explicit request of the reviewers and project officer after the first review meeting. The description below summarizes the history of communications made by ST regarding the availability of the 32nm process data set. For details of the impact item on the project execution and planning please refer to Section 14.2.1.

- [October 2008] STM communicates restrictions to IMEC on the access of 32nm data set

- [December 2008] ARM and IMEC agree using IBM technology for developing projects tasks that depends of technology data availability

- [January 2009] ARM and IMEC agree on porting VAM environment to ARM facilities so IMEC does not need to be exposed to IBM's 32nm data set.

- [March 2009] STM and UoG sign bilateral NDA to STM facilitate 32nm process data to UoG

- [March 2009] VAM deployment at ARM starts and finalizes a month later
- [April] UoG confirms having received STM 32nm data set. However no device compact model yet.

- [May 2009]: STM agrees facilitating 32nm data set to KUL, UoG and IMEC and initiates a 4-way NDA on May 15th 2009

- [May 2009] IMEC has completed the library characterization work at ARM while the 32nm data set has not been made available yet to IMEC and KUL

- [June 2009] STM, IMEC, KUL and UoG sign 4-way NDA to allow the data that UoG will generate with the STM 32nm tech data will be used in the project by ST, IMEC, and KUL.

- [September 2009]; STM confirms making available the 32nm device compact model to all undersigning partners of the 4-way NDA by week 38 of 2009

- [October 2009] STM makes available the a 32nmLP statistical model card to imec and Imec distributes the information among the 4-way undersigning partners.

14.2.3. <u>Consolidated Changes in the Description of work:</u>

The description of work was updated with version 2.5, on May 6th 2009 reflecting the changes in the consortium and updates and clarification in the original D.O.W. A second update, version 3.4 followed on December 8th 2009, reflecting mainly the delays required to mitigate the risks described Section 14.2. The following Tables 5 and 6 below shows the overview of the justifications of the updates.

Please note: No manpower was changed; the total budget of the project remains the same. The project objectives remain the same.

Partner	WP	Changes	Explanation if needed
ST	WP6	Task 6.6 and Deliverable 6.6 have been deleted	Task 6.6 was similar to Task 6.5. Therefore Task 6.6 and accompanying Deliverable 6.6 has been deleted.
		Due date of deliverable 6.5 has been postponed to M30	Deliverable 6.5 coincides with deliverable 6.6 which original due date was M30.
IMEC	WP2	Name change of Miguel Miranda to Paul Zuber as WP2 leader	Paul Zuber is now WP2 responsible. Miguel Miranda is the technical project responsible.
	WP5	Name of the target platform has been inserted.	Original DoW was not specific concerning the target platform.
		Risk management part has been updated.	As requested by the EC during the review meeting. A detailed description of the risks + mitigation actions have been added.
		D2.4 confidentiality level has been changed to confidential	Due to possible confidentiality issues, the confidentiality level is changed.
		CV of Paul Zuber has been added	
		Change of project effort forms	Due to effort change, project forms are updated
		Name change of responsible: Bart Dierickx to Miguel Miranda	Bart Dierickx has left IMEC. Miguel Miranda is the main responsible for the project.
		Gantt chart and task linking graph is updated	Original gantt chart and task linking graph was outdated due to change of deliverables and task.
UoG	WP1	Effort was decreased from 36MM to 33MM	Due to effort increase in WP6, effort was decreased in WP1.
	WP6	Effort has been increased from 0 MM to 3 MM	Due to typo in original DoW UoG had no manpower allocated in WP6. 3MM have been transferred from WP1 to WP6 to ensure manpower allocation in this WP.

Table 5: Update of the DoW version 2.5 (May 2009)

Partner	WP	Changes	Explanation if needed
STM	WP2	Effort of ST in WP2 is largely reorganized. ST reduces effort in Task 2.2 from 5PM to 0PM. While in Task 2.1.2 ST increases their effort from 10PM to 15PM.	Due to internal strategy adjustments ST decides to take a more industrially viable approach to the problem of statistical static timing analysis. The new approach is based on a hybrid of existing and state-of-the-art techniques. Such new focus requires a re-allocation of efforts from Tasks 2.2 to Task 2.1.2. Tasks 2.2 remain being covered by ARM and KUL.
		Changed on the flow that will be used for statistical characterization of the standard cell library and for the evaluation of the demonstration activities. Page 40.	As consequence of change item 3. The variability aware modeling flow that has to be used to statistically characterize the standard cell library resulting from D2.1.2 will not result from WP2 but will be provide by IMEC's background to the project on exclusive use of IMEC
	WP6	Deliverable D6.3 due date is changed from T0+M21 to T0+24M.	Reflects the original dependency with D5.3 with both deliverables having the same due date. A delay of this deliverable until T0+M25 was granted by Mr. Anton Chichkov, current EC Project Officer for REALITY.
		Added clarification to the focus of deliverable D6.6.	Deliverable D6.6 is the last technical deliverable of the project, as such it should provide a comprehensive "reflection" from our industrial partners on the value added created by REALITY in their context. Such clarification has been added to the DoW
		ST effort in Task 6.3 moves to Task 6.4. Total ST effort in WP6 remains unchanged. ARM become lead beneficiary of deliverable D5.3.	Reflects ST being main contributor to the system level activities in Task 6.4 while ARM in cooperation with IMEC UNIBO, KUL and UoG is main coordinator of the efforts in Task 6.3 block level activities.
UoG	WP1	Dissemination level of deliverable D1.2 is changed from PU to CO (Confidential).	Consequence from the 4-way agreement put in place by ST in T0+M18 which prohibits public disclosure of the data made available to the consortium and of any of the results obtained therewith.
		UoG shifts 1PM from WP4 to WP1.	UoG appears to have 1PM in the overall table effort in WP4. However such effort was never detailed within the task structure. We believe this was mistake present in the original document, Instead UoG prefers to shift this effort toward WP1 since UoG has identified extra simulation work to be done with the introduction of the metal gate and the development of the corresponding simulator features
	WP5	The outcome of WP1 will be also integrated in the integration activities of WP5.	On a November 25th meeting between ST, UoG and IMEC, ST has confirmed to the project coordinator and the leader of WP1 that it is acceptable for all project partners (including those who are not part of the 4-way NDA) to make use of the variability injector modeling approach using variability injectors provided by IMEC that were derived from the simulations of UoG. The compact models with which the variability injectors will be used will be provided as output from WP1 by IMEC.
ARM	WP2	Deliverable D2.1.2 due date is changed to from T0+18M to T0+21M.	This delay reflects the additional time needed by ARM to obtain permission from IBM for distributing libraries within the consortium. This delay was already granted by Mrs. Isabel Vergara, EC project officer of REALITY during the month of July 2009
	WP5	Deliverable D5.3 due date is changed from T0+21M to T0+24M.	Reflects the delay associated to the deployment of ARM's Research Island (RI) initially planned for T0+M16 and actually deployed in T0+M21. The RI is a virtual space

| IMEC | WP7 | The project activity report D7.7 at the end of the project (T0+M30) is removed it gets replaced by report D7.8 (Final project report also at T0+M30). Consequently D7.8 gets renamed by D7.7 and D7.9 gets renamed by D7.8. | Given the short duration of the project in Year3 (6 months), the coordinator believes that the content of the two deliverables planned on T0+M30 – D.7.7 and D.7.8 will largely overlap. Hence we recommend to replace D7.7 (project activity report) by D7.8 (final project report) |

Table 6: Update of the DoW version 3.4 (December 2009)

14.3. Overview of changes in the project plan for period 2

As identified in section 15.2.2, some risks have materialized. Therefore corrective actions have been planned, resulting in a change of the original work plan. All changes in the original work plan have been identified in Table 6.

TOP RISK	Corrective action and implication on workplan
Availability of process data in 32nm cannot be guaranteed	During 2008 the project team has spent effort in making a 32nm dataset available to the consortium. Because the delay of this dataset originated on external technology provider to STM, the work plan has changed. The following steps have been taken to reduce this risk: - Due dates of deliverables have been delayed. This has been reported to the EC. The due dates of these new deliverables will be respected. - Currently an NDA has been signed to make the 32nm dataset available to University of Glasgow, KUL and IMEC. STM has confirmed allowing now that IMEC to receive this information not to ARM. Such data is expected to be provided in week 38 in 2009. - The split of deliverable D2.1 on the design of standard cell library in two sub-deliverables. The first sub-deliverable provides an early version of such a library which is a design using a public domain 32nm device model and using linearly scaled dimensions. A second one being the originally planned once the 32nm dataset becomes available D2.1.2 has been completed but its delivering has been delayed for 3 months to allow ARM to get agreement from IBM proceed disseminating such results - KUL had to delay its activities in task T3.2, resulting in incomplete work in this taks by the planned finishing date, as well as in personnel effort under spending. Since the results of task T3.2 are an important input for WP6, KUL proposes to continue and finalize the work by extension of Task T3.2 into 2010, in close collaboration with the activities in WP6. KUL will

	report this extended work in an updated version D3.2b of the Deliverable D3.2. An updated DOW is requested by KUL to the project coordinator to reflect this change. Overall, at this point of time (end of period 2) we can safely say that this risk has been mitigated on time. The project coordinator trust that it will not affect the overall outcome of the project. - The statistical device compact model card was made available to the remaining partners (imec, ARM, UNIBO and KUL) at T0+M22, hence resolving the risk. - As a consequence of the accumulated delay, deliverables D5.3 and D6.3 required an extension in their due date to (see Section 13). A DoW update was issued in month M24 to reflect this delay. Fortunately, such delay did not affect the completion of the milestones proposed for period 2.
Availability of ARM926 softcore is not guaranteed	During the project the project team has identified two test vehicles that will be used in the project. The ARM test vehicle contains the ARM926 core. The availability of the ARM926 softcore was identified as a top risk and therefore corrective action was taken during 2008. Even when the softcore can be made available the legal conditions to do so are too restrictive. The following steps have been taken to reduce this risk: - In 2009 a research island between ARM and IMEC will be setup to perform the planned work on the ARM926 soft-core complemented with stages of IMEC personnel at ARM. This will solve all current pending legal issues including the availability of the 32nm data set to IMEC by making the 32nm data set only available to the ARM engineer. By September 2009 such research island has not yet been made available. Hence the execution of task 5.3 becomes affected and a delay of deliverable D5.3 will be requested to accommodate for this timing dependency. - Finally the research island became fully operational from as from T0+M22 - Split of the demonstration activities in two main vehicles: one focused above the RTL level using STM processors (hereafter called system level) and one below (hereafter called RT-level) using ARM processors. A back of the envelope model have been developed to connect the two vehicles. - All tasks in WP5 are now on track and its deliverables submitted during this second reporting period
The developed methodologies in WP3 and flows being may become not integrated in the project	From the original work plan it was not clear how the developed methodologies in WP3 would be implemented in the project. The following steps have been taken to reduce this risk:

	- The original work plan has changed in order to use the developed memories in WP3 in the test vehicle. IMEC will analyse the memories in WP3 and benchmark them against ARM memories. - By T0+M18 KUL was still waiting for STM to make available its 32nm device compact model to design such memories. The project coordinator expects however that final delivering due date of such work may not need corrections, given the commitment of ST to provide such model by week 38. - The statistical device compact model card was made available to the remaining partners (imec, ARM, UNIBO and KUL) at T0+M22 - As consequence of the accumulated delay, Task 3.2 and its corresponding deliverable will require an extension beyond reporting period of Y2. Deliverable D3.2 was submitted on time but an update (D3.2b) will be submitted in Y3. An request for an upcoming DoW update will be proposed to reflect such extension

Table 7: Summary of changes with respect to the original project plan for period 2

14.4. List of project meetings, dates and venues in period 2:

Table 8 shows an overview of the meetings held in the first reporting period (project month M13 until M19. One room project meetings with having all consortium partners to join (work package leaders and scientific key members), are typically held each 6 months or more frequently when necessary. For efficiency reasons it was decided by the consortium partners to combine as much as possible the milestone meeting with the project management board meeting and the technical review. When necessary, separate and dedicated technical meetings were organized with specific topics. Conference calls were planned monthly during the first year of the project.

Meeting name	Meeting Purpose	Meeting Type	WP's	Date	Venue
1st review meeting with EC PO and reviewers	Official review meeting with EC Evaluate if project follows proposed DoW Decide if payments proceed	REVIEW meeting with PO and reviewers	WP1 until WP8	March 6, 2009	IMEC offices, Leuven Belgium
Monthly conference call	• Handle administrative issues • Keep track of deliverables and delivery dates • Follow up of the action tracker • Clarify technical contributions from partners • Any other business	Administrative and TECHNICAL	WP1 until WP8	Monthly	Conference call
Partner Meeting 3 (Pm1)	• Measure and ensure a constant level of information sharing about the progress in all the Work Packages. • Get a common understanding of the technical status and priorities • Align the work packages, milestones, timelines and (administrative) reporting • Assessment of all the risks, including definition of alternative actions • Escalation path if necessary, • Update of the DoW • Clarify the expectations of all partners • Review and approval of the deliverable report • Team building	MILESTONE M3 PROJECT MANAGEMENT BOARD + TECHNICAL	WP1 until WP8	26 May, 2009	University of Bolgna, Bologna, Italy
Partner Meeting 4 (Pm2)	• Review of the Dissemination and Use Plan. • Review of the planned objectives. • Get a common understanding of the technical status and priorities • Align the work packages, milestones, timelines and reporting. • Start preparing the 1st Annual Review by the EC. • Update of the DoW • Re-Assessment of all the risks, including definition of alternative actions. • Team building	MILESTONE M4, M5 + PROJECT MANAGEMENT BOARD + TECHNICAL	WP1 until WP8	Planned: 13 or 20 October 2009 (tentative dates!)	ARM offices, Grenoble, France

Table 8: Overview of project meetings

14.5. Impact of deviations materialized from the planned milestones and deliverables

Table 9 shows an overview of the committed deliverables in the first reporting period which were submitted to the EC. All of the scientific and dissemination deliverables were provided on time as planned. Some deliverables were postponed. This was also communicated towards the EC and the suggested planning updates approved via successive DoW revisions.

List of Deliverables submitted for review to the EC						
Del. no.[5]	Deliverable name	WP no.	Lead beneficiary	Nature [6]	Dissemination level [7]	Delivery date[8]
D2.1.2	Report on small standard cell library	WP2	IMEC	R	CO	T0+M21
D3.2	Design report on the variability/reliability resilient memory IP blocks	WP3	KUL	R	PU	T0+24M
D3.4	Report: techniques for enhancing interconnect variability tolerance	WP3	KUL	R	PU	T0+21M
D4.2	Report on Control Algorithms for System Reliability and Variability Management	WP4	UNIBO	R	CO	T0+18M
D5.2	Sample Implementation Flow	WP5	ARM	R	PP	T0+18M
D5.3	Delivery of block level and system evaluation report	WP5	ARM/ST	R	PP	T0+24M
D6.2	Validation and Assessment of Results: Validation Plan	WP6	ST	R	PU	T0+18M
D6.3	Block level evaluation report as specified by the validation plan	WP6	ST	R	PP	T0+24M
D7.5	Semi-annual project progress report	WP7	IMEC	R	PU	T0+19M
D7.6	Annual project progress report	WP7	IMEC	R	PU	T0+M24

Table 9: List of deliverables submitted to the EC

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[5] Deliverable numbers in order of delivery dates: D1 – Dn
[6] Please indicate the nature of the deliverable using one of the following codes:
R = Report, **P** = Prototype, **D** = Demonstrator, **O** = Other
[7] Please indicate the dissemination level using one of the following codes:
PU = Public
PP = Restricted to other programme participants (including the Commission Services)
RE = Restricted to a group specified by the consortium (including the Commission Services)
CO = Confidential, only for members of the consortium (including the Commission Services)
[8] Month in which the deliverables will be available. Month 1 marking the start date of the project, and all delivery dates being relative to this start date.

No major deviation exists in the planning of deliverables, nor the execution of the REALITY that may affect the final outcome of the project compared to the original schedule. Whenever necessary, practical constraints have been taken into account in the precise definition of meetings and in providing deliverables. However few deliverables timing needed adaptation to accommodate to dependencies associated to above identified risks, all still delivered within the second year of the project. In concrete:

Del. no.[9]	Deliverable name	WP no.	Lead benefici ary	Nat ure [10]	Diss emin ation level [11]	Delivery date from Annex I (proj month) [12]	Del ive red Ye s/N o	Actual / Forecas t delivery date	Comments
D2.1.2	Report on small standard cell library	WP2	IMEC	R	CO	T0+18M	Yes	T0+M21	Work completed on time but with delay associated to have in place the necessary legal clearances for distributing the report.
D5.3	Delivery of block level and system evaluation report	WP5	ARM/ST	R	PP	T0+21M	Yes	T0+24M	delay associated to having in place by ARM the research island needed to allow IMEC to get around liability requirements to access the ARM core
D6.3	Block level evaluation report as specified by the validation plan	WP6	ST	R	PP	T0+21M	Yes	T0+M24	Delayed to accommodate timing dependency with D5.3

Table 10 List of Deliverables with actual modifications with respect to the DoW existing at the beginning of period 2.

[9] Deliverable numbers in order of delivery dates: D1 – Dn
[10] Please indicate the nature of the deliverable using one of the following codes:
R = Report, **P** = Prototype, **D** = Demonstrator, **O** = Other
[11] Please indicate the dissemination level using one of the following codes:
PU = Public
PP = Restricted to other programme participants (including the Commission Services)
RE = Restricted to a group specified by the consortium (including the Commission Services)
CO = Confidential, only for members of the consortium (including the Commission Services)
[12] Month in which the deliverables will be available. Month 1 marking the start date of the project, and all delivery dates being relative to this start date.

14.6. Development of the Project website :

The www.fp7-reality.eu website is online since april 2008 and contains a Public area. It is the official homepage of the project and that serves as a public repository for all project related information. Consortium restricted information and project related documents (action trackers, deliverables, meeting slides…) are stored on a dedicated wiki page (http://www-micrel.deis.unibo.it/~reality/wiki/index.php/Main_Page).

The public web site gives interested users access to a number of public pages providing a description of the project objectives, news, announcement of upcoming events, links to exhibitions where the REALITY project will be represented, contact information and reports or specifications.

Further details on the website and its statistical monitoring information can be found in **deliverable report D8.3**

14.7. Use of foreground and dissemination activities during this period :

Within the REALITY consortium all partners contribute to a large extend equally to the dissemination of the project results. Extensive details on the dissemination approach and achievements can be found in deliverable report D8.3 submitted to the EC in February 2009.

IPR, Access rights and licensing have been made explicit and described in an elaborate way in the Consortium Agreement which was signed by all consortium partners.

14.8. Coordination activities comment – key message :

The key message regarding the REALITY coordination activities can be summarized as follows :

- **Deliverables have been achieved on time as planned.**
- **Numerous Scientific Publications have been achieved.**
- **Information has been shared within the consortium, but individual partners have also become active in a bilateral context. In particular, ARM/IMEC, ST/UNIBO**
- **True collaboration exists within the consortium, as well as outside the** REALITY **context.**
- **The** REALITY **research topic has and will remain to have industrial relevance.**
- **Furthermore, the** REALITY **research topic is at the core of the industrial partners activity.**
- **All main roadblocks threatening an efficient implementation of the proposed poject plan have been successfully overcome.**

Based upon this observation, it can be concluded that the REALITY project is in a good shape to finalize with the planned activities for the next period and to inititiate the assessment, valorization and dissemination activities typical of the last phase of a project.

15. Explanation of the use of the resources

15.1. ST Microelectronics

Table : Personnel, subcontracting and other major cost items for Beneficiary "ST" for period 2			
STM	Item description	Amount	Explanations
	Personnel costs	318,507	1 Manager, 5 R&D eng, 5,439.08 hours total 0.19MM Management 13MM senior engineers 25.66MM engineers. In detail the following persons in RTD: • Giuseppe Desoli (R&D manager)

			• Andrea Ornstein (R&D engineer) • Francesco Papariello (Senior R&D engineer) • Luca Pezzoni (R&D engineer) • Cristiano Forzan (Senior R&D engineer) • Davide Pandini (R&D manager) • Guido Angelo Repetto (R&D engineer)
	Travels	1,175	Project and review meetings: 25-26/05/2009 Bologna 19-20/10/2009 Grenoble 14-16/10/2009 Participation to ESTIMedia Workshop in Grenoble (REALITY publication)
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		319,682	

Adjustment to period 1

Table : Personnel, subcontracting and other major cost items for Beneficiary "ST" for period 1 – Adjustment			
STM	**Item description**	**Amount**	**Explanations**
	Personnel costs	-12,666	Applied actual updated hourly personnel cost engineer For Mngt and engineer
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		-12,666	

15.2. IMEC

Table : Personnel, subcontracting and other major cost items for Beneficiary "IMEC" for period 2			
IMEC	**Item description**	**Amount**	**Explanations**
	Personnel costs	€195,085.09	RTD Personel costs of 11.80MM (E1 type) engineers and 11.88MM (E2 type) senior engineers) and 3.60 (E3 type) senior engineers. Management cost of 4.8MM. . In detail the following persons in RTD: • Zuber Paul (researcher) • Dobrovolny Petr (Senior researcher) • Miranda Corbalan Miguel (Senior Scientist) In detail the following persons in Management: • Tassignon Tom (engineer)
	Consumables	€0	
	Travels	€6,283.79	Travel cost of prospective valorization meeting IMEC/ARM at Cambridge (UK), organization of first REALITY review meeting at imec, travel cost for stage of 1 week of 1 imec engineer at ARM locations in Grenoble for joint work, travel costs for invited presentation of coordinator at ICCV-2009 workshop on REALITY and peer review presentation at PATMOS conf., travel costs for two milestone project board meetings at Bologna

			and Grenoble, travel costs to Eindhoven for consultancy valorization meeting with Dr. Berkelaar
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€201,368.88	

Adjustment to period 1

Table : Personnel, subcontracting and other major cost items for Beneficiary "IMEC" for period 1 – Adjustment			
IMEC	**Item description**	**Amount**	**Explanations**
	Adjustment on overhead costs for RTD and Management	€20,467.20	The overhead costs computed in period 1 where based on rates of 2007. This adjustment reflects the computation of the 2008 overhead costs using the 2008 overhead rates available in 2009
	Adjust to personnel cost (RTD and management) from average rate to actual rates	€10,753.48	The personnel costs computed in period 1 where based on average rates. This adjustment reflects the computation of the 2008 personnel costs using actual rates rather than average rates.
	TOTAL DIRECT COSTS AS CLAIMED ON FORM C	€31,220.68	

15.3. University of Glasgow

Table : Personnel, subcontracting and other major cost items for Beneficiary "UoG" for period 2			
UoG	**Item description**	**Amount**	**Explanations**
	Personnel costs	€112,059.03	26.68 MM PDRAs 12 MM PhD students. In detail the following persons in RTD: • Asen Asenov (professor) • Scott Roy (professor) • William Allan (researcher) • Andrew Brown (Senior researcher) • Antonio Martinez (researcher) • Negin Moezi (researcher) • Noor Ain Kamsani (researcher) • Stanislav Markov (researcher)
	Travel	€19,036.10	Project meetings and conferences
	Consumables	€742.34	Modest computer consumables
	Other	€4,895.98	Computer hardware
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€136,733.46	

15.4. Katholieke Universiteit Leuven

TABLE 3.1 PERSONNEL, SUBCONTRACTING AND OTHER MAJOR DIRECT COST ITEMS FOR BENEFICIARY KUL (KATHOLIEKE UNIVERSITEIT LEUVEN) FOR THE 2ND YEAR (01FEB09-31JAN10)

Work Package	Item description	Amount	Explanations
WP 2, 3, 7, 8	Personnel costs	**145.215,29 EUR**	*28,6 MM of scientific researchers + 0.3 MM of a professor.* In detail the following persons in RTD: • Stefan Cosemans (senior researcher) • Nele Reynders (researcher) • Ben Geeraerts (senior researcher) • Yi Ke (researcher) • Jean-Michel Redoute (researcher) • Wim Dehaene (professor) • Georges Gielen (professor)*
	Subcontracting		
WP 2, 3, 7, 8	Major cost item 'travel'	**6.024,32 EUR**	*Technical meetings, conferences*
WP 2, 3	Major cost item 'consumables'	**10.102,72 EUR**	*Small components & computing costs*
	Remaining direct costs		
TOTAL DIRECT COSTS		161.342,33	

(*) Professor Gielen has worked on the project but without costs

15.5. University of Bologna

Table : Personnel, subcontracting and other major cost items for Beneficiary "UNIBO" for period 2			
UNIBO	**Item description**	**Amount**	**Explanations**
WP3/4/5/7/8	Personnel costs	95.014,57	Four grants for research are activated with four young graduated collaborators in order to carry out the activities foreseen for UNIBO in the REALITY project, corresponding to 39 person/month. Dr Andrea Acquaviva is involved in this project through a research collaboration contract to cooperate on all project related activities and in particular on WP4, his activities in this second year, correspond to 4 p/m. Prof. Luca Benini and Prof. Michela Milano are involved in the research activities foreseen within WP3 and 4 for a total of 2 person/month. Due to the unavailability of a senior researcher at the beginning of the project, the number of PM has been higher and at low cost than foreseen because the activities have been performed by junior researchers. In detail the following persons in RTD: • Loi Igor (junior researcher) • Pullini Antonio (junior researcher) • Paterna Francesco (junior researcher) • Paci Giacomo (junior researcher) • Kakoe Mohammad Reza (junior researcher) • Benini Luca (professor) • Milano Michela (professor) • Acquaviva Andrea (senior researcher)

WP3/4/8	Major cost item 'Travel & Subsistence'	6.318,03	Reimbursements of travel and subsistence cost for their participation to the following events: • Project and review meetings; • Participation to DATE conference 2009 and workshop in Nice.
WP4/8	Major cost item 'Other Costs'	773,32	These costs are incurred: • for the registration fee to DATE 2009 Conference • Hosting of Bologna meeting • Dissemination material
WP4	Consumables	114,14	The consumables purchased are PC accessories (such as DVDROMs)
WP4	Equipment	99,97	The cost incurred refers to the depreciation of the PC QUAD660.
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		102.320,05	

Adjustment to period 1

Table : Personnel, subcontracting and other major cost items for Beneficiary "UNIBO" for period 1 – Adjustment

UNIBO	Item description	Amount	Explanations
WP4	Personnel costs	4.649,87	1p/m of Dr Andrea Acquaviva
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		4.649,87	

15.6. ARM

Table : Personnel, subcontracting and other major cost items for Beneficiary "ARM" for period 2

ARM	Item description	Amount	Explanations
	Personnel costs	€185,868	1 manager, 3 engineers working part time on the project: 20pm spent during the period. In detail the following persons in RTD: • Yves Laplanche (R&D manager) • Virgile Javerliac (Senior R&D engineer) • Selma Laabidi (R&D engineer) • Emmanuel Pacaud (EDA engineer)
TOTAL DIRECT COSTS AS CLAIMED ON FORM C		€185,868	

16. Financial statements – Form C and Summary financial report

The form C has been uploaded to the NEF online webtool by all partners.

17. Certificates

There is an audit certificate from imec that will be provided as update of this deliverable as soon as the audit process gets completed.