7th RTD Framework Program

REALITY

Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

Contract No 216537

Deliverable D8.3

Dissemination and Use Plan

(initial version, at the first reporting period)

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The REALITY Consortium consists of:

Interuniversity Microelectronics Centre (IMEC vzw)	Prime Contractor	Belgium
STMicroelectronics S.R.L. (STM)	Contractor	Italy
Universita Di Bologna (UNIBO)	Contractor	Italy
Katholieke Universiteit Leuven (KUL)	Contractor	Belgium
ARM Limited (ARM)	Contractor	United Kingdom
University Of Glasgow (UoG)	Contractor	United Kingdom

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1. Disclaimer

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2. Acknowledgements

The author acknowledges contributions by all work-package leaders of the REALITY consortium.

3. Document revision history

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4. Preface

The scope and objectives of the REALITY project are:

- Development of design techniques, methodologies and methods for real-time guaranteed, energy-efficient, robust and adaptive SoCs, including both digital and analogue macro-blocks

The Technical Challenges are :

- To deal with increased static variability and static fault rates of devices and interconnects.
- To overcome increased time-dependent dynamic variability and dynamic fault rates.
- To build reliable systems out of unreliable technology while maintaining design productivity.
- To deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.

Focus Areas of this project are :

- “Analysis techniques” for exploring the design space, and analysis of the system in terms of performance, power and reliability of manufactured instances across a wide spectrum of operating conditions.

- “Solution techniques” which are design time and/or runtime techniques to mitigate impact of reliability issues of integrated circuits, at component, circuit, architecture and system (application software) design.

The REALITY project has started its activities in January 2008 and is planned to be completed after 30 months. It is led by Dr. Miguel Miranda of IMEC. Five contractors (STM, ARM, KUL, UoG, UNIBO) participate in the project. The total budget is 2.899 k€.

5. Abstract

The goal of this document is to provide the details regarding the deliverable “D8.3 Dissemination and Use Plan (DUP)” for the REALITY Project (IST-216537).

The DUP aims at describing the planned strategy for the internal and external dissemination of the project’s objectives and also at stating a preliminary approach to the market analysis and exploitation of the REALITY project’s results and outputs.

The DUP is conceived in conjunction with all the Consortium partners in order to give way to the most effective strategy and to obtain the highest return in terms of mass-knowledge on the project’s topics and of economic gain. This deliverable in particular, addresses specific dissemination actions and proposes an approach to the future exploitation of the REALITY project results and outputs.

This document is issued in the second year (M13) after the project kick-off and is just the starting point of defining and executing the strategy. Updates will be made in future, as described in the work plan, and the planned strategy will be matured and fine-tuned gradually.

Follow-up actions, including meetings and discussions, will continue for the duration of the project to ensure that the REALITY consortium proceeds in addressing the proper objectives. The Dissemination and Use Plan will be used as a guideline and as a reference by the members of the consortium for the duration of this project.
More detailed analysis and market/business modelling activities will be performed after the delivery of this document and its guidelines, the outcomes of which will be documented and described in deliverables D8.5 (“Dissemination and use plan (second issue)”)

After an introduction to the general aims of the dissemination and preliminary exploitation planning, D8.3 is subdivided into two main sections. The first chapter offers a detailed description of the dissemination activities performed and planned for promoting and spreading the REALITY results among and to the international academic and industrial organizations. The second chapter provides an overview of the planned exploitation activities and initial strategy.

Within the REALITY consortium all partners contribute to a large extend equally to the dissemination of the project results.

IPR, Access rights and licensing have been made explicit and described in an elaborate way in the Consortium Agreement which was signed by all consortium partners.

6. Introduction

The REALITY project has started its activities in January 2008 and is planned to be completed by the end of June 2010. It is scientifically led by Dr. Miguel Miranda of IMEC. The Project Coordinator is Ing. Tom Tassignon. The total budget is 2,899,882.50€.

This FP7 funded project is the base for collaboration between major industrial players in this field, research institutes and academic partners: ST, ARM, University of Glasgow, University of Bologna, KU Leuven and IMEC.

The selected target test vehicles for REALITY project comes from the two industrial partners: ST and ARM.

The “REALITY” project activity provides solutions for coping with variability and reliability issues that occur when scaling to and beyond the 32 nm technology node. A system-level solution is provided by focusing on two main axes: Analysis Techniques and Solution Techniques.

7. Dissemination Activities

7.1. Dissemination Strategy

The dissemination will ensure the spreading of the project's outcome among other industrial and academic organizations so that the methodologies and tools developed can be used in these sectors.

This objective will be achieved by using multiple different strategies.

In general terms, the dissemination of the REALITY project adopts the following principles:

- Dissemination of project results to the international research and design community, which is a crucial aspect for the effective exploitation of the project results in the community and outside the consortium. This objective will be achieved through scientific publications, participation to conferences, and the maintenance of the project website and wiki.

- The organization of training actions/workshops complements and strengthens the dissemination. The mobilization of resources of REALITY (most of which will be invested in R&D activities) coupled with the expertise of the partners involved, guarantees that innovative technologies in the area of reliability and variability will be created during the execution of the project.

- The dissemination of project results by the consortium partners as well as by the broader community of designers will vary depending on the specific technological results obtained in REALITY and the specific business segments addressed by the partners. Dissemination opportunities will be created by advertising to the right audience and communities.

7.2. Internal Project communication / dissemination

7.2.1. **Internal website and wiki**

At the start of the REALITY project, IMEC has created and hosts an internet website (www.fp7-reality.eu) which is up and running since April 2008. The goal of this site is to share research results among the general public and enhance the visibility of the research activity. A wiki (http://www-micrel.deis.unibo.it/~reality/wiki/index.php/Main_Page) has been setup by the University of Bologna. The primary goal of the wiki is to stimulate the effective communication within the project consortium. It is also intended as a way to limit the circulation of files and paper as much as possible.

The REALITY consortium registered and acquired the right to use an ".eu" domain name for the project website : www.fp7-reality.eu

During the course of the project, the REALITY website contents will be progressively enriched in order to provide an up-to-date view of the research progress.

Access to the wiki is password protected and meant for keeping internal project data like:

- action trackers
- confidential presentation material
- risk management plan and updates
- document templates
- deliverables (non public), and related draft work documents
- scientific reports, in case they are for restricted use
- communication lists

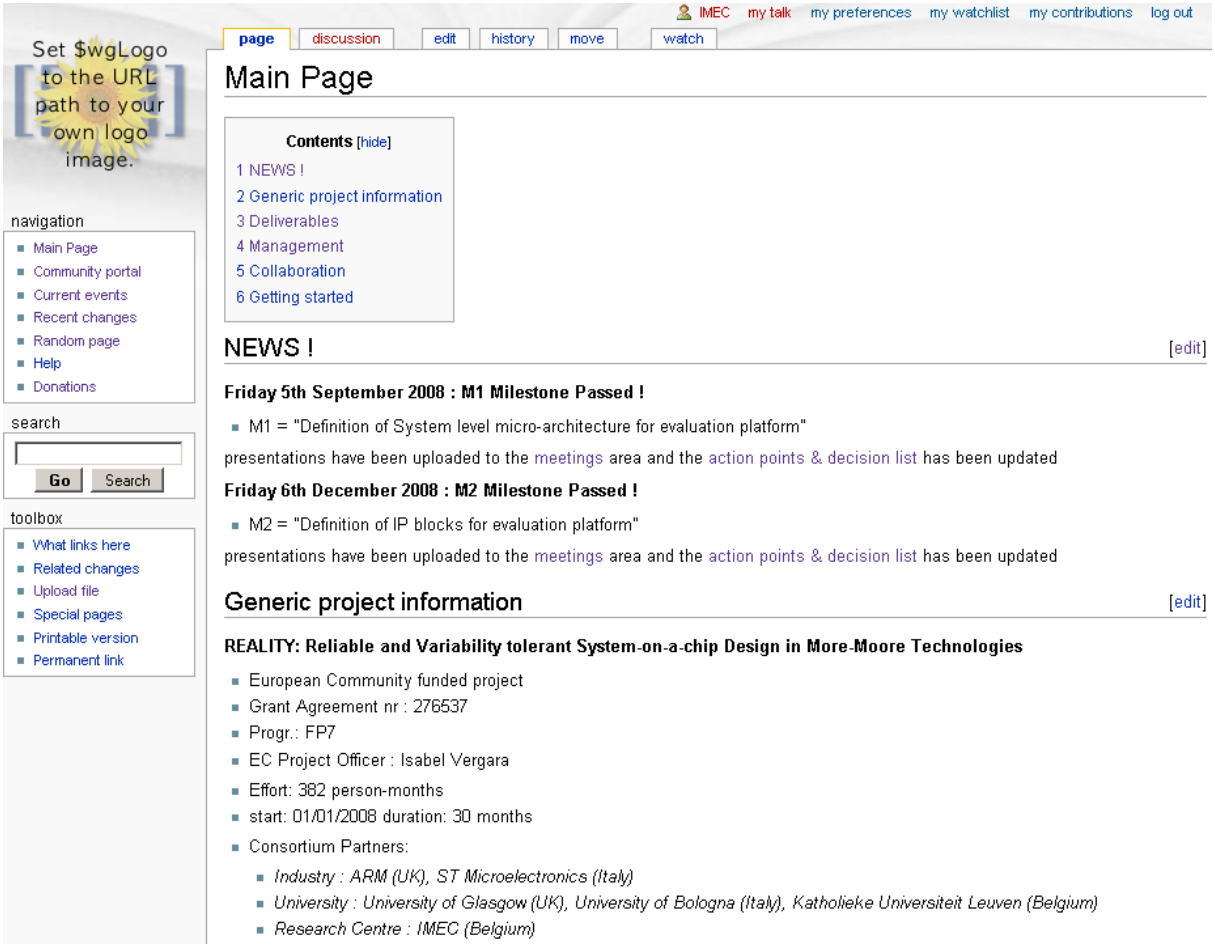

Figure 1: Screenshot of the wiki page for internal communication purposes

The contents and objectives of the public website can be found below.

7.2.2. **Project meetings**

One room project meetings with having all consortium partners to join, are typically held each six months. A fixed item on the meeting agenda is a brief status review by each of the individual consortium partners on their realized and planned dissemination activities. Also the outlook for new scientific publications in the next half year is being shared. Finally, tactics and approach towards dissemination of the potential project results to industrial companies outside the consortium is being discussed. In this way a close monitoring of the joint dissemination activities can be realized as well as the possibility to anticipate to the definition and fine-tuning of near term actions.

Besides the regular consortium meetings, another path that is being followed is the internal scientific dissemination. This action aims to exploit the REALITY results towards the academic consortium partners in order to advance relevant research in the corresponding

laboratories of these academic partners and to support their teaching activity through enrichment of the relevant courses or the introduction of new ones.

7.2.3. **Communication list**

An integral part of project management is team organization and communication. The REALITY project team has setup a simple but effective communication list which features all the team member names, their role in the project or function, and their coordinates.

This communication list is updated or reviewed on a regular base, typically each month.

The use of this list obviously enables proper communication among the consortium and to the relevant stakeholders. More importantly it makes sure no valuable information gets lost, stakeholders are informed about project events and the persons responsible for dissemination are clearly identified.

The communication list is available to all the partners via the project wiki page.

7.3. External communication / dissemination

7.3.1. **Public Web site**

The www.fp7-reality.eu website contains also a Public area that is the official homepage of the project and that serves as a public repository for all project related information.

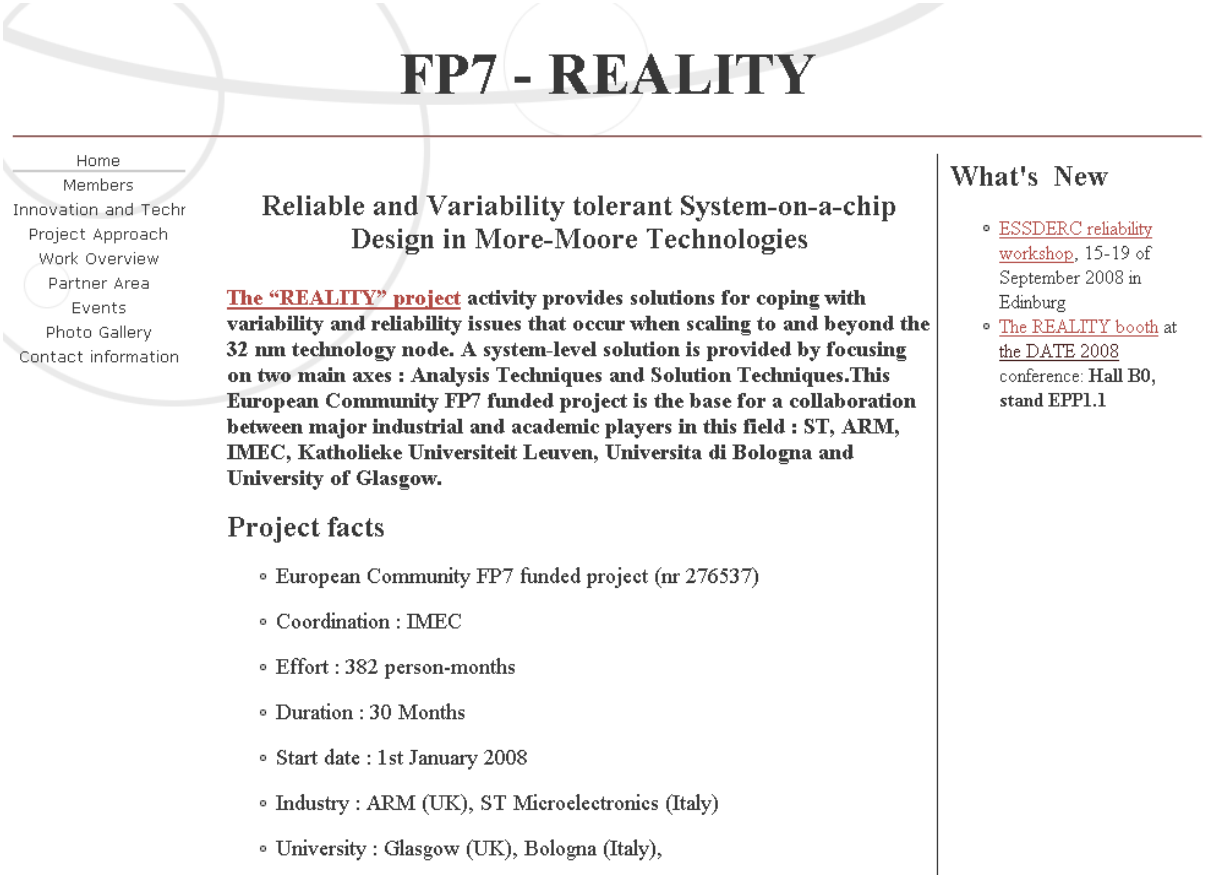

Figure 2 : The REALITY web homepage

The web site gives interested users access to a number of public pages providing a description of the project objectives, news, announcement of upcoming events, links to

exhibitions where the REALITY project will be represented, contact information and reports or specifications.

The www.fp7-reality.eu website contains a statistical monitoring function which allows the host to analyse the website traffic. In the course of the project it will help the project team to gain a better view of the interested audience and fine-tune the available information and contents of the website.

Relevant information which is monitored :

- traffic tracking
- amount of page views
- visitors and their geographical location (country of origin)
- the way visitors came to the site
- comparison of traffic per month and intensity

7.3.1.1. Statistical information

This statistical information can be accessed at all times via the following link: http://webstats.motigo.com/stats?AETKZALB7G6GmCZQTm2KB0i8F7cQ

Access statistics of the web site are as follows: The statistics demonstrating the total accesses of the REALITY website have been marked since the 22nd of April 2008, and especially after the first ten days of the website's settlement and functionality. The statistics are based on ***Motigo Webstats*** (http://webstats.motigo.com). The Motigo Webstats engine is employed to let the external visitors of the Website have access on the visits and the access rates of the website and has been chosen, because, it does not require that the visitor has any username and password in order to demonstrate the web statistics.

In this report, the statistics of the REALITY website accesses are obtained from ***Motigo Webstats*** engine and they are demonstrated below, in the following table, namely *Table 1*, given separately for each month, starting from March of 2008. For the months of January, February and March of 2008, there are no statistics available, as the website has been properly settled since the last days of April and therefore, the scripts of the Web statistics engine has been functioning since April. The statistic metrics of *Table 1* covers the website usage and highlights the total number of visits (accesses) per month, the website page views.

Table 1 : Statistics of the web accesses of the REALITY website per month.

Month	***Visits***	***Page views***
January	N/A	N/A
February	N/A	N/A
March	N/A	N/A
April	17	30
May	24	28
June	35	43
July	37	50
August	32	40
September	31	40
October	35	46
November	26	28
December	29	40

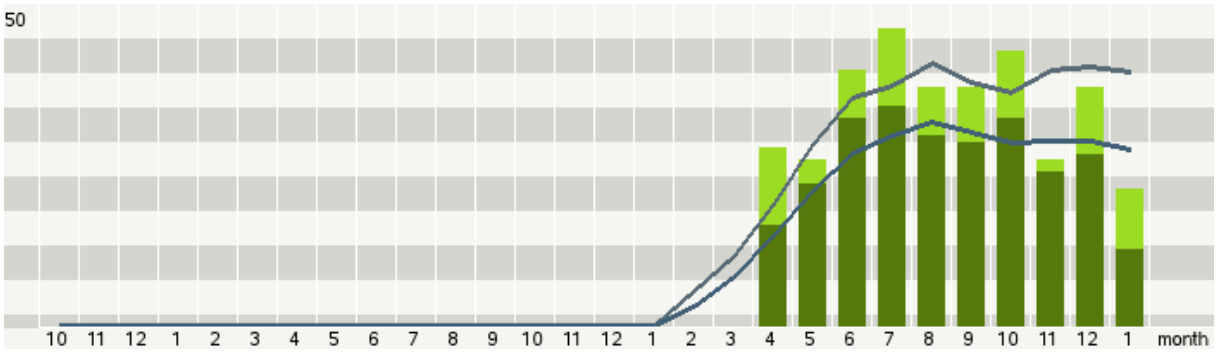

Figure 3: Overlapping overview of visits and page views

It must be noticed that, in Table 1, the metric of the number of new visits demonstrates the number of visitors that have accessed for the first time the REALITY website for the first time during the current month and they are named as *Non-Returning visitors* by the Motigo Webstats engine reports, while the rest of the visitors of the certain month are characterized as *Returning*.

7.3.1.2. Extra statistical information

In the two following figures, the screenshots of Motigo Web pages for the REALITY website are shown, for the duration April 2008 – January 2009. These figures are given to demonstrate the format of these Web tracking engines and the way of showing the information about the web accesses of a certain website.

Country of origin

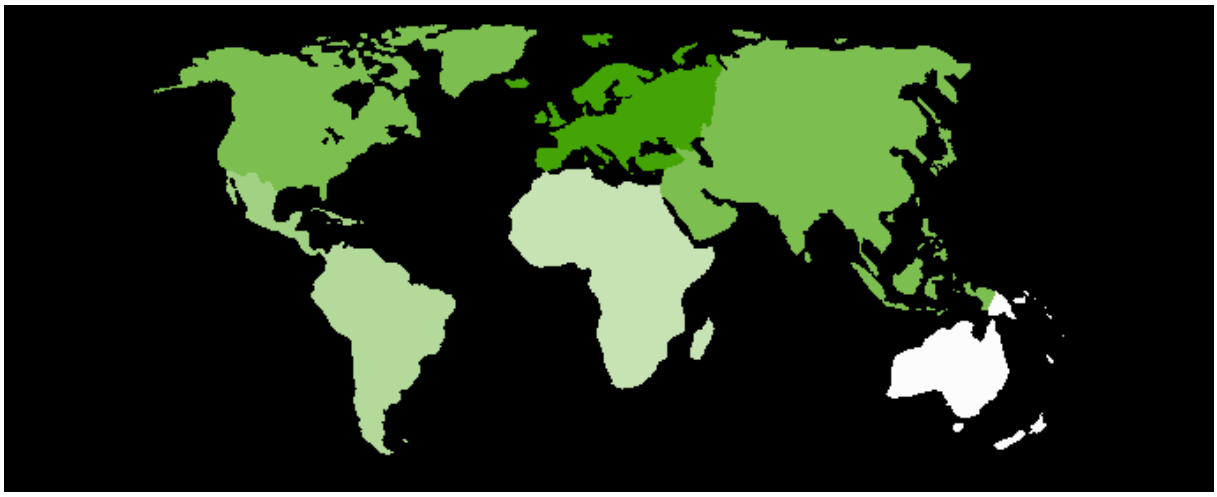

Figure 4: Overview of worldwide website traffic

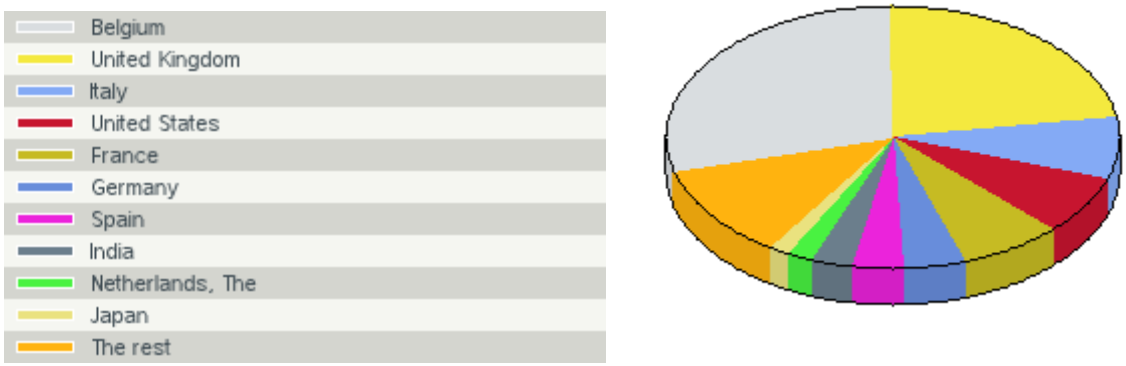

Figure 5: Table pie of website traffic in countries worldwide

1.	Belgium	104	28.3 %
2.	United Kingdom	81	22.0 %
3.	Italy	27	7.3 %
4.	United States	26	7.1 %
5.	France	26	7.1 %
6.	Germany	16	4.3 %
7.	Spain	13	3.5 %
8.	India	10	2.7 %
9.	Netherlands, The	7	1.9 %
10.	Japan	5	1.4 %
11.	Singapore	5	1.4 %
12.	Greece	5	1.4 %
13.	Cyprus	5	1.4 %
14.	Korea	4	1.1 %
15.	Slovakia	3	0.8 %
16.	Sweden	2	0.5 %
17.	Brazil	2	0.5 %
18.	Romania	2	0.5 %
19.	Mexico	2	0.5 %
20.	Switzerland	2	0.5 %
21.	Indonesia	1	0.3 %
22.	Turkey	1	0.3 %
23.	Croatia (Hrvatska)	1	0.3 %
24.	Puerto Rico	1	0.3 %
25.	Liechtenstein	1	0.3 %
	The rest	16	4.3 %
	Total	**368**	**100.0 %**

Table 2: Overview of traffic in specific countries worldwide

Statistical information in Europe

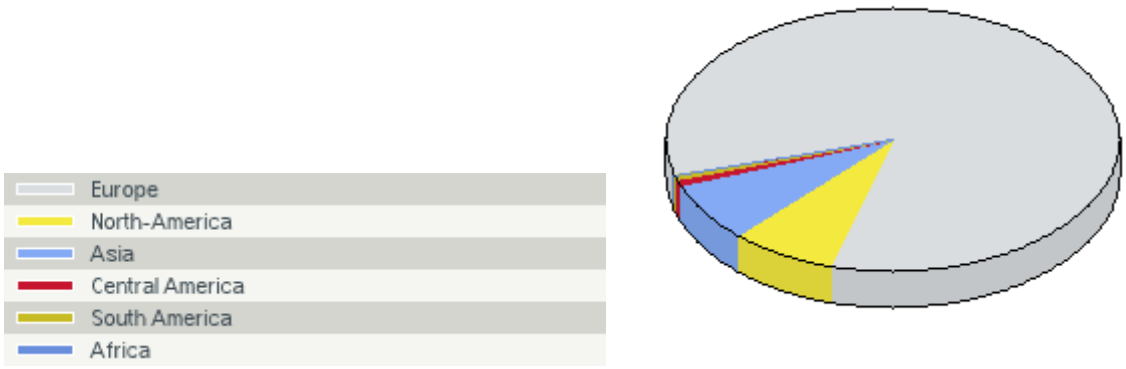

Figure 6: Table pie of website traffic in Europe

The statistics information given in this paragraph includes the most prevalent metrics, which could let someone have a clear enough picture of the total visit rate during the year 2008. The Web tracking engine installed on the website derives several other metrics and features

On request, this information can be delivered to the REALITY Consortium partners via the common communication channels (via email, wiki or website)

7.3.2. **Promotion at exhibitions and conferences**

During the first reporting period a multitude of occasions were exploited with the aim to make the start of the REALITY project public and to explain the target objectives to the general public. These actions are a part of a broader dissemination strategy.
The path which was rolled out by the consortium is a mix of dedicated promotion activities combined with key note lectures and presentations at renowned conferences.
The result is clear: the presence of the REALITY project team was observed by a broad audience both general public and specialists. This yields a number of contacts showing interest in the REALITY research topic. On top of this, the start of the REALITY project has been picked up by the press resulting in a variety of press articles.

Exhibitions and conferences fulfil a complementary role as a fast medium for diffusion of results. All the REALITY consortium partners will definitely continue in the next period to join or target exhibitions as much as possible in order to show the benefits of the developed methodologies and tools.

- **Project Booth at DATE '08 & Press Release**

The Design, Automation, and Test in Europe (DATE) conference is one of the worlds premier conferences dedicated to electronic and embedded systems. It was held at the ICM in Munich, Germany at 11-12-13th March 2007.

DATE is sponsored by the European Design and Automation Association, the EDA Consortium, the IEEE Computer Society : (TTTC), (CEDA), ECSI, RAS and ACM SIGDA.

The year 2008 was the first time that the DATE organization put into place a special area for European funded projects.

REALITY project Booth :
The REALITY project team decided to participate with a dedicated project booth (Hall B0 Stand EPP 1.1). This booth consisted of a small cubicle, white hard-coated wall panels on 2 sides with the posters, a reception counter & stool, a meeting space and a facility of hosting a 'fringe' meeting. Figure 7 gives an impression.

Figure 7 : Project Booth at DATE '08

The project booth was staffed during the full extend of the conference by the REALITY project coordinator and the IMEC WP leader, with presence of some of the consortium partners. The main purpose was to announce to the audience the start of the REALITY project, explain the objectives and find potential industrial interest in the results of the project.

The IMEC corporate booth hosted a facility for press conferences and interviews with the press. IMEC's press officer Ms. Katrien Marent was available for interaction with the press.

One of the main reason's for the REALITY project team to participate with a dedicated booth at the renowned DATE '08 conference is the interesting mix of attendees: press, professionals and captains of industry.

Table 3 : DATE '08 Attendee Statistics

Total Registrations	**4700**
Conference	1420
Exhibition (Visitors + Exhibition Personnel)	3231
Press	49

Table 4 : Geographical Breakdown

Europe	**75%**
Germany	36%

France	9%
UK & Ireland	8%
Benelux	7%
Others	15%
North & South America	**19%**
M. East, India, Africa	**2%**
E.Asia & Australasia	**4%**

- **ESSDERC and ESSCIRC 2008 in Edinburgh**

REALITY team members were present at the ESSDERC and ESSCIRC 2008 in Edinburgh.

The 38th European Solid-State Device Research Conference (ESSDERC) and the 34th European Solid-State Circuits Conference (ESSCIRC) were held in Edinburgh from 15 - 19 September 2008.

The aim of the ESSDERC and the ESSCIRC conference is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits.

In this conference Prof. Asen Asenov (University of Glasgow, leader of WP1) was the presenter of the workshop on “CMOS variability research in Europe: from atomic scale to circuits and systems”. More info on this workshop can be found in the section on training and workshops.

- **6th Technology Aware Design Seminar: Avoidance vs. Adaptability for Variability and its Time-dependency: Who Will Win?**

On 24-25 November 2008 the central theme of the CALIT event on “Technology Aware Design” was how to overcome the Variability and Reliability technology scaling walls.

The topics discussed in this seminar were related to the research topics in REALITY projects. REALITY research topics were presented by some of the consortium partners (Asen Asenov, University of Glasgow; Georges Gielen, KU Leuven).

More info on this workshop can be found in the section on training and workshops.

7.3.3. **Organization of training - workshops**

The organization of training - workshop actions complements and strengthens the dissemination. The mobilization of resources of REALITY (most of which will be invested in R&D activities) coupled with the expertise of the partners involved, guarantees that innovative technologies in the area of the REALITY project will be created during the execution of the project.

7.3.3.1. ESSDERC-ESSCIRC

With respect to the REALITY FP7 project, a workshop was organized at ESSDERC-ESSCIRC 2008. The 38th European Solid-State Device Research Conference (ESSDERC) and the 34th European Solid-State Circuits Conference (ESSCIRC) were held in Edinburgh from 15 - 19 September 2008. The conference is sponsored by an impressive list of industrial companies and was an excellent opportunity to disseminate results from the REALITY project to the public and in specific to the representatives of the industrial companies active in this domain.

Figure 8: Overview of sponsors of the ESSDERC/ESSCIRC 2008 conference

Overview of this workshop

The increasing variability in CMOS transistor characteristics has become a major challenge to scaling and integration. Statistical variability related to the fundamental discreteness of charge and matter, which cannot be eliminated by tighter process control, is becoming the major component of CMOS variability. The increasing device variability demands fundamental changes in the way that future integrated circuits and systems are designed. Strong links must be established between circuit design, system design and fundamental device technology to allow circuits and systems to accommodate the individual behaviour of every transistor on a chip. Design paradigms must change to accommodate the increasing variability.

This Workshop presented the status of CMOS variability related research in Europe conducted in three European and two national projects including:

- *NANOSIL*: Silicon-based nanostructures and nanodevices for long term nanoelectronics applications (EU FP7)
- *PULLNANO*: Pulling the limits of nanoCMOS Electronics (EU FP6)
- ***REALITY*: Reliable and variability tolerant system-on-a-chip design in More-Moore technologies (EU FP7)**
- *NanoCMOS*: Meeting the design challenges of nanoCMOS electronics (UK EPSRC)
- *NanoMat*: Meeting the material challenges of nanoCMOS electronics (UK EPSRC)

The workshop covered a broad range of technology, devices, design aspects of the CMOS variability from atomic scale to circuit and system level.

The Keynote Speaker, Professor Toshiro Hiramoto from Tokyo University, introduced the subject and presented the concerted research effort, supported by the MIRAI Project in Japan, in characterising and understanding the sources of statistical CMOS variability.

Programme of the workshop

09.00 Welcome and introduction, R. Clerc (NANOSIL)
09.10 Measuring and understanding device variability. Keynote, T. Hiramoto, Tokyo Univ. (MIRAI)
09.40 Link between 'ab initio' material simulation and variability, A. Shluger, UCL (NanoMAT)
10.10 Simulation of statistical variability introduced by discreteness of charge and matter, A. Asenov, University of Glasgow (NanoMAT)
10.40 Coffee break
11.00 Measuring and simulation of device variability at 45 nm technology generation, A. Cathignol, STMicroelectronics/IMEP (PULLNANO)
11.30 Measurement and simulation of statistical variability in FinFETs, A. Mercha, IMEC (PULLNANO)
12.00 Variability in novel device architectures, G. Iannaccone, IU.NET (NANOSIL)
12.30 Lunch
13.30 Reliable and variability-tolerant system-on-chip design strategies, B. Dierickx & M. Miranda, IMEC (REALITY)
14.00 Grid technology to support statistical device and circuit simulation, S. Roy, University of Glasgow (NanoCMOS).
14.30 Impact of variability on multicore processor architectures, S. Furber, Manchester University (NanoCMOS)
15.00 Hardware-software interactions in variability and reliability aware design, L. Benini, University of Bologna (REALITY)
15.30 Coffee break
16.00 Brainstorming session: Practical solution for Variability resistant devices, circuits and systems (A. Shluger, A. Asenov, G. Ghibaudo, S. Furber, B. Dierickx, industry representatives)
17.00 Close

A complete overview of this workshop, including slides, can be found at http://www.nanocmos.ac.uk/essderc/.

7.3.3.2. CALIT Visionary Workshop

On 24-25 November 2008 the central theme of the CALIT event on “Technology Aware Design” was: “how to overcome the Variability and Reliability technology scaling walls”.

It is IMEC’s intention to build CALIT into an internationally foremost school where managers, policy-makers, scientists and practicing engineers can meet regularly to discuss and exchange their views on these selected topics of high future interest to the international community.

The 2008 CALIT event on “Avoidance vs. Adaptability for Variability and Its Time Dependency” consisted of 2 parts. Part 1 was the “CALIT Visionary Workshop” that was held on Monday 24 November 2008.

The CALIT Visionary Workshop on “Technology Aware Design - Performance and Power Scaling Beyond 32nm: Game Over?” on Tuesday 24 November 2008 brought together invited panel members who have renowned themselves in various areas of knowledge closely related to this year’s themes and a limited number of guests. The purpose was to hold brainstorm discussions on a selected number of topics.

Programme of part 1 of the workshop

1.30pm	*Welcome – CALIT - Objectives of the Workshop (Herman Maes)*
1.45pm	*Panel Discussion* *Theme: Performance and Power Scaling Beyond 32nm: Game Over?* *Moderator : . Prof.Wim Dehaene, Katholieke Unv. Leuven, Belgium* *Panel Members: **A.Asenov (Univ. Of Glasgow, UK)**, J.Cortadella (Elastix Corp., USA), **B.Dierickx (Vrije Univ. Brussels and IMEC, Belgium), G.Gielen (Katholieke Unv. Leuven, Belgium)**, K.Flautner (ARM Ltd. UK), S.Nassif (IBM Research, USA), M.Pelgrom (NXP, The Netherlands)*
3.30pm	*Coffee Break*
4.00pm	*Conclusions of the workshop*
4.30pm	*Social Event (only panellists and organizers)*
5.30pm	*Reception at The Lodge (only panellists and organizers)*
6.30pm	*Dinner at The Lodge (only panellists and organizers)*

Part 2 was the CALIT Symposium on Tuesday 25 November 2007 that was held in the IMEC Auditorium.

Programme of part 2 of the workshop

9.00	*Welcome and General Intro* *Miguel Miranda, IMEC, Belgium*
09.10	*The Limits and Opportunity of Adaptability* *Sani R. Nassif, IBM Austin Research Laboratory, US*
10.00:	***Statistical Variability and Reliability in Nano CMOS transistors*** ***Asen Asenov, Glasgow University, UK***
10.50	*Coffee Break*
11.10	***Circuit modeling of ageing and reliability degradation effects*** ***Georges Gielen, Katholieke Univ. Leuven, Belgium***
12.00	*Lunch*
13.20	*From worst-case design to statistical design.* *Marcel Pelgrom, NXP Research, The Netherlands*
14.10	*Surfing over variability* *Jordi Cortadella, ELASTIX Corp., USA*

15.00 Coffee break
15.20 The Wall Ahead is Made of Rubber
Krisztian Flautner, ARM Ltd., UK
16.10 Debate with panel: Design Time versus Run Time Design Solutions for Variability and Reliability
Panelists: A.Asenov, J.Cortadella, G.Gielen, K.Flautner, S.Nassif, M.Pelgrom
Moderator: TBD
17.30 End of program

An overview of this workshop can be found at http://www2.imec.be/imec_com/tad-sem.php.

7.3.4. **Promotional Flyer and Bulletin**

A brochure (leaflet) has been compiled containing the key information about the REALITY project : funding, start-end date, consortium partners, objectives, methodologies, benefits and target achievements.
The brochure has been printed and distributed in the different events in which the consortium partners will participate. During the first reporting period the REALITY flyers were distributed at DATE '08 (March 2008, Munich - Germany).

Needless to say that in future where ever possible, the consortium partners will distribute the brochure in the numerous scientific and industrial oriented events.

The below figure shows a selected page from the brochure as an example.

REALITY Project Sheet

Reliable and Variability tolereant System-on-a-chip Design in More-Moore Technologies

The "REALITY" project activity provides solutions for coping with variability and reliability issues that occur when scaling to and beyond the 32 nm technology node. A system-level solution is provided by focusing on two main axes : Analysis Techniques and Solution Techniques.
This European Community FP7 funded project is the base for a collaboration between major industrial and academic players in this field : ST, ARM, IMEC, Katholieke Universiteit Leuven, Universita di Bologna and University of Glasgow.

Scope

- As miniaturization of the CMOS technology advances, designers will have to deal with increased variability and changing performance of devices. Intrinsic variability of devices, which begins to be visible in 65nm devices, already will become much more significant in smaller technologies. Soon it will not be possible to design systems using current methods and techniques. Scaling beyond the 32 nm technology node brings a number of problems whose impact on design has not been evaluated yet. Random intra-die process variability, reliability degradation mechanisms and their combined impact on the system level parametric quality metrics are becoming prominent issues. Dealing with these new challenges will require an adaptation of the current design process: a combination of design time and runtime techniques and methods will be needed to guarantee the correct functioning of Systems on Chip (SoC) over the product's lifetime, despite the fabrication in unreliable nano-scale technologies.
- The objective of this project is to develop design techniques and methods for real-time guaranteed, energy-efficient, robust and self-adaptive SoC's.

Technological challenges

- Build reliable systems out of unreliable technology while maintaining design productivity.
- How to cope with increased static variability and static fault rates of devices and interconnects during the circuit and system design phase.
- How to cope with increased time-dependent dynamic variability and dynamic fault rates during the circuit and system design phase..
- Design design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.

Figure 1 Random discrete dopants in a 35 nm MOSFET from the present 90 nm technology node.

Figure 2 Corresponding variations in the current-voltage characteristics of 100 transistors with different dopant distributions

Figure 3 Corresponding distribution of the static noise margins in 6T SRAM cells

Solutions

- Analysis techniques : for exploring the design space, and analysing of the system in terms of performance, power and reliability of manufactured instances across a wide spectrum of operating conditions (thermal, noise, soft).
- Solution techniques : which are design time and/or runtime techniques to mitigate the impact of reliability issues (seen as time-dependent variability aspects) of integrated circuits at component, circuit, architecture and system level.

imec KU LEUVEN ST ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA ARM University of Glasgow

www.fp7-reality.eu

Figure 9 : the first REALITY Brochure

7.3.5. **Press Releases**

The start of the REALITY project has been noticed and picked-up by the press. Multiple contacts have led to several articles.

- One example of such a press announcement can be found at http://www.embedded-computing.com/news/db/?10348.

European Research Projects Exhibit at DATE´08 ICM, Munich, Germany 10 – 14 March, 2008
10 months 3 weeks 6 days ago

London, February 15 , 2008 – DATE as the leading global design event continues to enhance its unique combination of industrial exhibition and the most important conference on system design.

New at DATE´08, European research projects will enrich the exhibition by presenting and demonstrating the latest research results ready for utilization in system and semiconductor product development.

Facing strong global competition the future success of Europe's economy is determined by the ability to innovate and to turn research results into products. In response to this challenge Europe's industry collaborates in numerous research projects and teams up with research institutes and universities, supported by the European Commission and by national authorities.
…
The REALITY project develops design techniques, methodologies, and flows for real-time guaranteed, energy-efficient, robust and self-adaptive SoCs. Tackled technology and design challenges include static variability and rates of devices and interconnects, time-dependent dynamic variability and dynamic fault rates, building reliable systems out of unreliable technology while maintaining design productivity and deploying design techniques that allow technology scaleable, energy efficient SoC systems while guaranteeing real-time performance constraints.

- The partners published press releases and information on web pages.

For example, the project was announced together with two other projects at University of Glasgow (URL see : http://www.elec.gla.ac.uk/groups/dev_mod/index.php)

7.3.6. **Cross reference promotion**

- **Cross reference promotion within the REALITY consortium**

In order to increase the visibility on the ongoing project research work as well as to increase the traffic to the REALITY website, consortium partners have setup a link from their own website to the project website. In addition to these references, links from other project websites where the REALITY consortium partners participate in have been made to the REALITY URL (e.g. http://www.nanocmos.ac.uk/essderc/). Where ever possible the REALITY project URL is mentioned in publications, reports and conference presentations.

A search at Google yields :

Figure 10 : Cross reference promotion inside & outside the REALITY consortium

The acronym REALITY is a common English word. To maximize the search results, the term “variability” has to be added. The use of non-existing words as acronym would raise the number of relevant search results. This is an interesting fact for future European projects.

- **Cross reference promotion outside the REALITY consortium**

Clear signs of interest for the REALITY research progress have been shown by other project teams (this was very clear during the setup of new projects in this area, e.g. ENIAC initiatives). The REALITY consortium actively pursues to keep a good relation with these other project teams as it may be a potential channel for dissemination and future exploitation. Running activities in this area will be elaborated further in the next reporting periods.

7.4. Scientific dissemination

Publications in Journals
One of the main vehicles for diffusion of research results is, obviously, to publish in outstanding journals and conferences in the field of interest, appropriate presentations and publications will be encouraged to ensure wide visibility of the project results. Among the most renowned and suitable journals in the topics covered by the project goals can be cited the following:

- IEEE Transactions of Electron Devices
- IEEE Electron Device Letters

Also Newsletters of support & funding organizations like Artist, Hipeac, Does-it; DSP Valley, etc are a potential communication channel.

The partners promised to publish papers in conferences and journals of the related field. This promise has been kept. However, due to the time that it takes to design the concepts of the optimization approaches, to implement these approaches, to obtain results, to write papers and to have them reviewed, a ramp-up phase is required for publications. Despite the need for a ramp-up phase, already a large amount of papers have been published or submitted during the first reporting period :

IMEC:

- Papanikolaou, A.; Wang, H.; Miranda Corbalan, M.; Catthoor, F. and Dehaene, W. , “Reliability issues in deep deep sub-micron technologies: time-dependent variability and its impact on embedded system design”, VLSI-SoC: Research Trends in VLSI and Systems on Chip, Book chapter , 2008
- Combining system scenarios and configurable memories to tolerate unpredictability , Sanz Pineda, C.; Prieto, M.; Gomez, J.; Papanikolaou, A.; Miranda Corbalan, M. and Catthoor, F.“ ”, ACM, TODAES, 2008

- Wang, H.; Miranda Corbalan, M.; Dehaene, W. and Catthoor, F. , Design and synthesis of Pareto buffers offering large range runtime energy/delay trade-offs via combined buffer size and supply voltage tuning, IEEE Transactions on VLSI Systems, 2009

UoG:

- A. Cathignol, B. Cheng, D. Chanemougame, A. R. Brown, K. Rochereau, G. Ghibaudo, A. Asenov, “Quantitative Evaluation of Statistical Variability Sources in a 45 nm Technological Node LP N-MOSFET”, *IEEE Electron Device Letters*, Vol 29, No. 6, pp. 609-611 (2008).
- M. F. Bukhori, S. Roy and A. Asenov, “Statistical aspects of reliability in bulk MOSFETs with multiple defect states and random discrete dopants”, *Microelectronics Reliability,* Vol. 48, No 8-9, Pp. 1549-1552 (2008)
- M. F. Bukhori, S. Roy and A. Asenov, “Simulation of Statistical Aspects of Charge Trapping and Related Degradation in Bulk MOSFETs in the Presence of Random Discrete Dopants”, IEEE Transactions on Electron Devices, *submitted*

ST:

- C. Forzan and D. Pandini, “Statistical Static Timing Analysis: A Survey,” Integration, the VLSi Journal, in press.

UNIBO:

- Chakraborty, K. Duraisami, A. Sathanur, P. Sithambaram, L. Benini, A. Macii, E. Macii, M. Poncino. (2008). Dynamic Thermal Clock Skew Compensation Using Tunable Delay Buffers. (vol. Volume 16, Issue 6, pp. 639 - 649). IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. vol. Volume 16, Issue 6, pp. 639 - 649.

7.4.1. **Publications in conferences**

Conferences fulfil a complementary role as a fast medium for diffusion of results. A list of the most relevant conferences in the fields of interest for the project includes: DATE, ESSDERC/ESSCIRC, IEDM and IEEE International Symposium on Quality Electronics Design. All these conferences are targeted by all partners in order to show the benefits of the developed methodologies and tools.

IMEC:

- J. Martin-Martinez, B. Kaczer, N. Ayala, R. Rodriguez, M. Nafria, X. Aymerich, P. Zuber, B. Dierickx and G. Groeseneken, “Stochastic Piecewise modeling of post-BD gate currentoriented to circuit design”, Fringe poster at ESSDERC/ESSCIRC, Edinburgh 2008

- AbdelHamid, A.; Anchlia, A.; Dierickx, B.; Miranda Corbalan, M. and Zuber, P. “Postponing SoC death”, Fringe poster at ESSDERC/ESSCIRC, Edinburgh 2008

- Miranda Corbalan, M.; Dierickx, B.; Zuber, P.; Dobrovolny, P.; Kutscherauer, F.; Roussel, P. and Poliakov, P. , Variability Aware Modeling of SoCs: from device variations to manufactured system yield, IEEE International Symposium on Quality Electronics Design, San Jose, March 2009

KUL:

- A dual port dual width 90nm SRAM with guaranteed data retention at minimal standby supply voltageGeens, Peter; Dehaene, Wim; Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European;15-19 Sept. 2008 Page(s):290 – 293;Digital Object Identifier 10.1109/ESSCIRC.2008.4681849

- A 3.6pJ/access 480MHz, 128Kbit on-Chip SRAM with 850MHz boost mode in 90nm CMOS with tunable sense amplifiers to cope with variability, Cosemans, Stefan; Dehaene, Wim; Catthoor, Francky; Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European, 15-19 Sept. 2008 Page(s):278 – 281, Digital Object Identifier 10.1109/ESSCIRC.2008.4681846

- Emerging Yield and Reliability Challenges in Nanometer CMOS Technologies, Gielen, G.; De Wit, P.; Maricau, E.; Loeckx, J.; Martin-Martinez, J.; Kaczer, B.; Groeseneken, G.; Rodriguez, R.; Nafria, M.; Design, Automation and Test in Europe, 2008. DATE '08, 10-14 March 2008 Page(s):1322 – 1327,Digital Object Identifier 10.1109/DATE.2008.4484862

- A fully-integrated Wienbridge topology for ultra-low-power 86ppm/°C 65nm CMOS 6MHz clock reference with amplitude regulation, De Smedt, Valentijn; De Wit, Pieter;

Vereecken, Wim; Steyaert, Michiel; Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European, 15-19 Sept. 2008 Page(s):394 – 397, Digital Object Identifier 10.1109/ESSCIRC.2008.4681875

- Emerging Yield and Reliability Challenges in Nanometer CMOS Technologies, Gielen, G.; De Wit, P.; Maricau, E.; Loeckx, J.; Martin-Martinez, J.; Kaczer, B.; Groeseneken, G.; Rodriguez, R.; Nafria, M.; Design, Automation and Test in Europe, 2008. DATE '08, 10-14 March 2008 Page(s):1322 – 1327, Digital Object Identifier 10.1109/DATE.2008.4484862

UoG:

- A. Asenov, “Statistical device variability and its impact on low power digital circuit design”, Proc. FTFC 2008, pp. 31-34 (2008), *Invited*

- B. Cheng, S. Roy, A. R. Brown, C. Millar and A. Asenov, “Evaluation of intrinsic parameter fluctuations in 45, 32 and 22 nm technology node LP n-MOSFETs”, Proc. ESSDERC 2008, Edinburgh, pp. 47-50 (2008).

- A. Asenov, S. Roy, A. R. Brown, G. Roy, C. Alexander, C. Riddet, C. Millar, B. Cheng, A. Martinez, N. Seoane, D. Reid, M. F. Bukhori, X. Wang, U. Kovac, “Advanced simulation of statistical variability and reliability in nano CMOS transistors”, *IEDM. Tech, Dig. Pp*. 421 (2008). *Invited*

ST:

- Acquaviva A., Paterna F., Benini L, Olivieri M., Papariello F., Desoli G. "Adaptive Idleness Distribution for Non-Uniform Aging Tolerance in MultiProcessor Systems-on-Chip", submitted to Design, Automation & Test Europe conference, DATE 09 20-24 April, 2009 , Nice, France

UNIBO:

- S. Bonesi, D. Bertozzi, L. Benini, E. Macii. (2008). Process Variation Tolerant Pipeline Design Through a Placement-Aware Multiple Voltage Island Design Style. (pp. 967 - 972). Design, Automation and Test in Europe, 2008. DATE '08 . Design, Automation and Test in Europe, 2008. DATE '08. Munich, Germany. 2008. (pp. 967 - 972). ISBN: 978-3-9810801-4-8.

- Atienza, G. De Micheli, L. Benini, J.L. Ayala, P.G. Del Valle, M. DeBole, V. Narayanan. (2008). Reliability-aware design for nanometer-scale devices. (pp. 549 - 554). Design Automation Conference, 2008. ASPDAC 2008. Asia and South Pacific . Design Automation Conference, 2008. ASPDAC 2008. Asia and South Pacific. Seoul. 2008. (pp. 549 - 554). ISBN: 978-1-4244-1921-0

- G. Paci, A. Nackaerts, F Catthoor, L. Benini, P. Marchal How to Live with Uncertainties: Exploiting the Performance Benefits of Self-Timed Logic In Synchronous Design Proceedings of 11th Euromicro Conference On Digital System Design, DSD 2008, Parma, Italy, Sept 3-5, 2008.

- F. Paterna, A. Acquaviva, L. Benini, F. Papariello, G. Desoli, M. Olivieri, “Adaptive Idleness Distribution for Non-Uniform Aging tolerance in Multiprocessor Systems-on-Chip”, to be presented at Design and Test in Europe Conference, DATE 2009, Nice, France, March 2009.

7.4.2. **Workshops, seminars, tutorials and Keynotes**

Regarding section 7.3.3, academic project members have made efforts to advance the research in the area in the laboratories of the academic partners (as promised) and beyond. Toward this end, the partners have actively held tutorials and presented keynotes. The following is a list of keynotes and tutorials for the first reporting period:

IMEC:

- M. Miranda, B. Dierickx, P. Dobrovolny , P. Zuber , "Variability Aware System Modelling in Sub-32nm Design", Invited Tutorial at DATE 2008, Munich, Germany
- M. Miranda, B. Dierickx, P. Dobrovolny , P. Zuber , "Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies", Invited Presentation at AENEAS Workshop on "Design Methods and Tools for Nanoelectronics, Milano, 2008
- B. Dierickx, M. Miranda, "Reliability and variability aware system on a chip design strategy", ESSDERC/ESSIRC Workshop on CMOS variability research in Europe: From Atomic Scale to Circuits and Systems, 19 September 2008, Edinburgh

UoG:

- A. Asenov, "Statistical Variability and Reliability in Nano CMOS and Impact on Design", CANDE, San Francisco (November 2008)
- A. Asenov, "Statistical variability and reliability in Nano CMOS transistors", CALIT, IMEC, Leuven (Nov 2008)
- A. Asenov, "FD SOI Variability issues", Tutorial, EurSOI, Grenoble (November 2008)
- A. Asenov, "Statistical variability and statistical reliability are already here: Are we ready for them?", NMI DfM Technical Network, Cambridge (Oct. 2008)
- A. Asenov, "Variability in Nanoelectronics", SINANO Modelling Summer School, tutorial, Bologna (September 2008)
- A. Asenov, "Simulation of statistical variability introduced by discreteness of charge and matter", ESSDERC Workshop "Variability research in Europe", Edinburgh (September 2008)
- A. Asenov, ESSDERC 2008 tutorial, Edinburgh (September 2008).
- A. Asenov, "Variability and its impact on design", Grand Challenges in Electronic Design Meeting, NXP (Southampton 2008)
- A. Asenov, "Performance of ultra-short MOSFET with different channel materials", IPRM, Versailles (May 2008).
- A. Asenov, "NanoCMOS: Impact of device variability on design", AENEAS meeting, Milan (May 2008).
- A. Asenov, "Statistical device variability and reliability: Where we stand now?", UKDF, Manchester (April 2008).

- A. Asenov, “Statistical device variability and its impact on design”, Synopsys seminar, Mountain View (April 2008).
- A. Asenov, “Advances in the simulation of statistical variability”, Synopsys seminar, Mountain View (April 2008).

ST:

- G. Desoli, panelist at CMOS Variability conference “Integration and Collaboration in the Era of Design for Variability (DfV)”, Oct. 23rd, 2007 Royal College of Physicians, London
- D. Pandini, “Statistical Static Timing Analysis: A New Approach to Deal with Increased Process Variability in Advanced Nanometer Technologies,” (Keynote Speech) *PATMOS*, Sep. 2007.
- D. Pandini, G. Desoli, and A. Cremonesi, “Computing and Design for Silicon Manufacturing,” Invited talk at HIPEAC 2009 Task Force on Reliability and Availability, Paphos, Cyprus, Jan. 2009

UNIBO:

- Luca Benini, “Hardware-software interactions in variability-aware design”, Oct 17, 2008, Universidad Complutense Madrid.
- Luca Benini, “Robust and scalable Power Management for Multicore Platforms”, Feb 8, 2008, Intel Braunschweig.

7.4.3. **Education**

Again relating to task 6.2 academic team members have actively been involved in courses related to the topic of the project. The following courses were held by the partners:

IMEC:

- B. Dierickx, M. Miranda, IDESA lecture on Variability Modeling, 27 oct 2008, IMEC

8. Initial Use Plan (exploitation strategy)

The objective of defining the exploitation strategy is to identify the results from the project that can be used or exploited by partners. Therefore, an initial market analysis will be assessed on the exploitable results. Based on these results, an exploitation strategy will be defined. Both the academic and industrial partners are interested in using the methodologies and tools developed during the project course as soon as these results become available.
On the one hand, the academic partners are interested in the results of the project because they could be used in a near future to continue some of their active research lines.
On the other hand, the project results are crucial to improve the design flows and production processes of the industrial partners, since the specific technical area of the project belongs to some of the leading edge business cases of these companies. In this sense, to address an exploitation and use plan of the technologies developed in this project will be an appropriate task.
Finally, the exploitation phase aims to develop and market new design techniques and methods for future SoC's and to use these results in the design flow of the industrial companies resulting in real-time guaranteed, energy-efficient, robust and self-adaptive SoC's.

8.1. Use by industrial partners in proprietary products

The use of the REALITY project results in products will be useful for the major industrial partners in this project: ARM and ST

The participation of STMicroelectronics and ARM to this project is motivated by both the strong impact of the research activities and topics addressed, which are critical for a leading company like ST and a leader in microprocessor Intellectual Property like ARM, and by the outstanding competence and scientific reputation of the participating scientific partners.

The major impact expected from REALITY is to develop such tools that on the one hand will link process technology and design and on the other hand will address process issues by offering design solutions.

8.1.1. **ST Microelectronics**

STMicroelectronics has extensive collaborations and links with many CAD and EDA vendors aimed at fostering and improving the design flows deployed within the company to address increasingly more demanding constraints of sub-nanometer design nodes and very large volumes products. Trough these links ST can stimulate the R&D of those tools and design flow providers to focus on the relevant problems and address new methodologies and technologies such as the ones developed within the REALITY consortium.
In order to disseminate the knowledge of the benefits of the REALITY methodologies and techniques, STM will organize internal audits and workshops inviting product architects and designer as well as partners of the REALITY consortium.

Moreover, the design flows and methodologies for statistical timing analysis and variability impact evaluation will be included into the top-down design flow currently used at ST. In particular, the statistical timing analysis tool used in REALITY will be deployed to perform sensitivity-based optimization to reduce the pessimistic design margins that significantly reduce the potential benefits and advantages introduced by technology scaling. The automatic internal standard cell library characterization tool will be extended with the techniques for statistical characterization developed and validated in REALITY, to include the impact of process variations in the characterization of industrial libraries.

Finally, exploiting the variability data and statistical device compact models developed in REALITY, a path ranking based on statistical timing analysis will be generated during sign-off to provide a better correlation with at-speed testing and to improve the parametric yield using the statistical optimization methods defined in REALITY.

8.1.2. **ARM**

The impact at the system level of random variations observed on the transistors of the most advanced technologies is quite difficult to analyse. Acquiring a good knowledge on variability issues through the whole development flow and developing an accurate methodology to percolate the variability information from the device level up to the SoC is fundamental to develop the next generation processors. As a consequence the dissemination of the knowledge acquired during the project is one of the main challenges for the ARM team.

We foresee the exploitation of the outcome of the project in three different ways:

1. Transversal team work organisation

To address the specific transversal needs of the project ARM has build up a project team with engineers coming from different horizons:

- Device
- Physical IP
- System design

A strong synergy between these three fields is becoming mandatory to understand the challenges we will face at each step of development of the next generation nodes. Within the project the team is developing characterisation methods as well as innovative design solutions to address the random variation issues in the designs. The ability to produce useful solutions will validate the transversal team organisation.
The team will survive the project and take advantage of this specific organisation to address new challenges we will face in the future technologies.

2. Internal knowledge spreading

The project is the place of a strong cooperation between ARM engineers and well known European researchers. The links drawn are essential for ARM to build a strong knowledge in variability phenomenon, characterization methods and remedial solutions.
Workshops and tutorials are organised at ARM enabling fruitful exchanges between partners and in house engineers. These events are profitable for both parties:

- ARM gets through these discussions a deeper understanding of the troubles they will face in the future technologies. This is especially done with the cooperation with University of Glasgow and IMEC who develop a good synergy to forecast the random effect on advanced devices.
- We provide our partners with a better understanding of the industry constraints we are facing both in the Physical IP field and in the System level development era. This is outstanding information to lead the frontend researches toward investigations closer to the applications.

This cooperation between universities, research institutes and ARM gives us a strategic understanding of the issues and allow to better target our research efforts by knowing the industrial constraints as well as the fundamental physics issues we will face.

Beyond the knowledge exchange organized with our partners, the engineers involved in the project are building an internal know how for ARM. They are participating to quarterly meetings with their peers inside ARM to internal research teams with information on the result of the project and discuss the interesting way to lead their technical work.
To train the development engineers, internal conferences involving engineers from all divisions of the company are organised within ARM. Technical presentations in these events are also proposed.
Finally the knowledge built during the project will be the basis of broader publication in conferences or tutorials in order for us to advertise towards our potential customers on our strategic understanding of the issue.

3. Production phase of tools and methodologies developed during the project

ARM is directly interested by the Variability Aware Methodology developed during the project. As a consequence a demonstration of the methodology on an ARM926 processor was proposed. The method will therefore be exploited within ARM. The ultimate demonstration of the methodology will be an application on more advanced processors to address the most power demanding applications.
The demonstration of the methodology is a crucial phase which really opens the door to exploit the method more widely inside the company if we feel it will provide us with a strategic differentiator toward our competitors.

ARM engineers are also developing internal tools to analyse accurately the variability impacts at the physical IP level as well as at the system level. The tools developed are not supposed to compete with any EDA vendor tool but aims at providing the most accurate information on variability for punctual analysis. One the one hand the information of these tools will be exploited either to provide accurate information on some specific designs. On the other hand this tool will be quite useful to validate the accuracy of the commercially available characterization tools since the statistical analysis is supposed to provide a more exact description of the design electrical behaviours then classic methodologies.
At the end of the project, the R&D team will provide the development engineers with prototypes. They will therefore have the capability to test the concepts on their own designs and analyse how the tools can be integrate in their production flow. Once the prototypes validated the tools will be handed over the design automation group to incorporate it in the production tools pool available inside ARM.

The tools and methodologies investigated within will allow analysing the impact of the statistical variations. The wanted impact of these tools is to allow engineers to analyse the robustness of their design, simple or complex, in a reasonable timeframe towards the effects of random variability. As a side effect, we expect the project to provide us with the necessary information to develop more robust systems and efficient resilient systems.
What is more, the accurate analysis of random variability will also pave the way to a better understanding of systematic variability. The comparison between the different effects on the new technologies gives a good understanding where to put our development efforts.

8.2. Use by academic partners to advance relevant research

8.2.1. **University Of Glasgow**

The capability has been developed to simulate statistical reliability in nanoCMOS devices. Validation in respect of experiment has increased confidence in using particular sources of variability to explain experimental variability measurements in real devices.

8.2.2. **KULeuven**

Exploitation is through the dissemination effort described below. The software results could be exploited through KUL's spinoff company later on, but it is too early at the moment.

As dissemination effort; KUL has spent 1 person month in total in 2008.
This includes :

- A paper in a special session at DATE 2008. Georges Gielen was organizer and presenter.
- A subset of slides on reliability and variability has been included in the tutorial which Georges Gielen gives as part of the analog design flow course of IDESA (another European project), with the aim to make people aware about the problems and how to deal with them.
- Preparation for and participation to the TAD workshop organised by and at IMEC in November 2008, with both a participation to the panel (one member (prof. dr. ir. Georges Gielen), one moderator (prof. dr. ir.Wim Dehaene)), and a tutorial presentation (prof. dr. ir. Georges Gielen) which includes material from the Reality project
- regular technical papers

8.3. Use by Research Institution IMEC

- The Main Exploitation Target is 2-fold :

  1. *Inclusion of results in its IP portfolio (IIAP)*

Main Exploitation Target : inclusion of results in its IP portfolio (IIAP) and more specifically in the Apollo research program, which is the successor of the M4 research program.

IMEC is one of the few research institutes in the world, with proven experience on bringing together top-tier industry partners for cooperation into a shared research program. IMEC has been very successful in deploying this model of shared research.

IMEC vzw's business strategy is based upon its 'IP Portfolio'. The exploitable results from the REALITY project will be included in this portfolio and will be exploited through:

- IMEC vzw's Industrial Affiliation Program (IIAP)' partnerships;
- Bilateral contracts with national and international industry and universities, and;
- Technology transfers and licensing of proven technology to industry and spin-off companies.

Each industrial partner joins the IIAP research program on a bilateral basis, with clearly defined technical scope and deliverables, allowing the partner to tune the bilateral project to some of its industrial needs. An industrial resident can be delegated to IMEC by the partner to join IMEC's research teams, typically for one year.

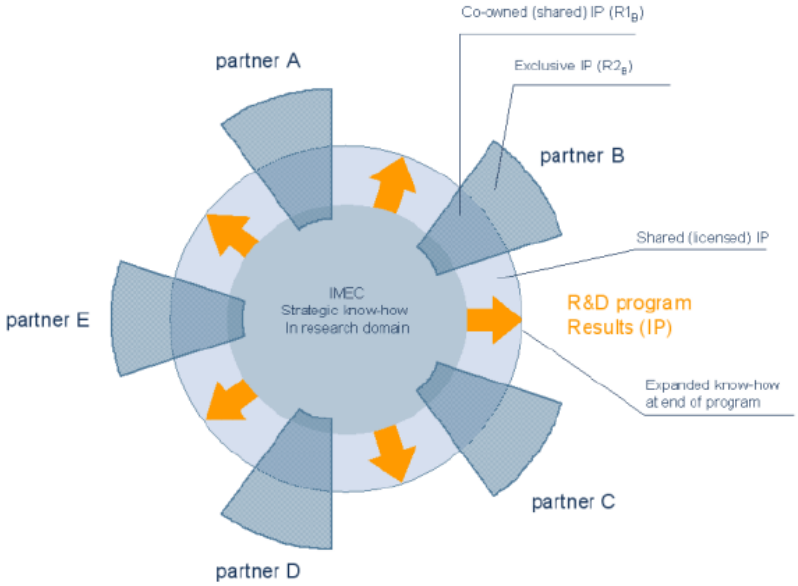

Figure 11 REALITY results can be licensed through the IIAP business model

- Type R1: The more generic or methodological type of project results, based on IMEC's strategic know-how (background information, R0) are co-owned by both IMEC and the industrial partner, without any accounting to each other;

- Type R2: Company-specific results or confidential information are the exclusive ownership of the industrial partner;
- Type R0: Results owned exclusively by IMEC are available for licensing, providing full user rights for the industrial partner. This type of IP relates to more fundamental, generic technologies;

In addition, the industrial partner gets access to IMEC's background information in the research domain specific to the IIAP, and the R0 and R1 results of the other industrial partners in the same IIAP.

Benefits:

- The industrial partner gets access to strategic IMEC background information at an early stage;
- The industrial partner gets access to other R0 and R1 (shared) results from other partners in the same IIAP;
- The industrial researcher (resident) is taken up into the IMEC mixed research team to execute the IIAP program. This intensifies the process of technology transfer and shortens the learning curve;
- The program induces a flexible interaction between the research team at IMEC (including the industrial researcher) and the industrial headquarters;
- Each IIAP contract is conducted on a bilateral basis, allowing for tuning and confidential information (exclusive R2) as described in the bilateral agreement;
- Each IIAP contract is standard as well as the corresponding prices.

Leverage effects:
Joining an IIAP program induces:

- A pricing leverage, through the cost-sharing principle of R0 and R1 results;

- An information leverage, as each industrial partner gets access to much more information (project info, IMEC's background information, R0 and R1 of other program partners) than its financial commitment;
- A cross-fertilization leverage, through the sharing of R0 and R1 results and through a good combination by IMEC of leading-edge partners, also coming from complementary fields (e.g. foundries, equipment or materials suppliers) but interested in the same research topic;
- A time-to-market leverage, as the industrial partner gets a competitive advantage in both strategic results and rapid time-to-market.

IMEC has a proven transfer record in the running APOLLO initiative (long term research program) in the domain of nomadic embedded system (Samsung, CoWare, Mentor Graphics, Arteris, …). This type of program is aimed to drive strategic cooperation between IMEC and the industry on the field of nomadic embedded systems. Hereto, IMEC has made a strong investment, bringing together the needed critical research mass of almost 150 researchers in this field. Based on this work, IMEC is also building up more extended networking and cooperation relationships with other European universities, which can contribute on complementary know-how creation. As a result, IMEC positions itself as centre-point in the chain for providing leading know-how and research to the industry. By the tight interaction with IMEC's partners, they are optimally prepared to exploit the know-how into leading solutions in their specific markets. It is anticipated that the results of REALITY will be instrumental to build the next generation solutions targeted by the long-term roadmap of its Apollo research program initiative. Research performed in REALITY will also create new opportunities for extending IMEC research cooperation with leading academic and industrial partners.

2. *Academic dissemination of the results by talks and* tutorials in conferences, organisation of training events and seminars at IMEC via the Microelectronics Training Centre (the public are PhD students and invited industry)

As dissemination IMEC has contributed in:

- The DATE ’08 booth on which REALITY project has been presented with posters.
- ESSDERC/ESSCIRC workshop on “CMOS variability research in Europe: from atomic scale to circuits and systems”
  - “Reliable and variability-tolerant system-on-chip design strategies, B. Dierickx & M. Miranda”
  - Member of the programme committee
- IMEC organized the CALIT TAD event on “Avoidance vs. Adaptability for Variability and its Time-dependency: Who Will Win?”

IMEC is also investing in the exploitation of its IP towards the industrial partners of the REALITY consortium. Discussions between IMEC-ST-ARM are at the moment ongoing.

9. Conclusions

Conclusions will be added in the second version of the deliverable at the end of the project.

10. List of Abbreviations

REALITY	Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies
CAD	computer aided design
DLC	
DMT	discrete multi-tone
DSP	digital signal processing
TAD	Technology aware design
IP	Intellectual Property
FFT	fast Fourier transform
HW	hardware
IC	integrated circuit
QoS	quality of service
SoC	system on chip
SOHO	small office/home environment
SW	software

