Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

REALITY Project Sheet

The "REALITY" project activity provides solutions for coping with variability and reliability issues that occur when scaling to and beyond the 32 nm technology node. A system-level solution is provided by focusing on two main axes : Analysis Techniques and Solution Techniques.
This European Community FP7 funded project is the base for a collaboration between major industrial and academic players in this field : ST, ARM, IMEC, Katholieke Universiteit Leuven, Universita di Bologna and University of Glasgow.

Scope

- As miniaturization of the CMOS technology advances, designers will have to deal with increased variability and changing performance of devices. Intrinsic variability of devices, which begins to be visible in 65nm devices, already will become much more significant in smaller technologies. Soon it will not be possible to design systems using current methods and techniques. Scaling beyond the 32 nm technology node brings a number of problems whose impact on design has not been evaluated yet. Random intra-die process variability, reliability degradation mechanisms and their combined impact on the system level parametric quality metrics are becoming prominent issues. Dealing with these new challenges will require an adaptation of the current design process: a combination of design time and runtime techniques and methods will be needed to guarantee the correct functioning of Systems on Chip (SoC) over the product's lifetime, despite the fabrication in unreliable nano-scale technologies.
- The objective of this project is to develop design techniques and methods for real-time guaranteed, energy-efficient, robust and self-adaptive SoC's.

Technological challenges

- Build reliable systems out of unreliable technology while maintaining design productivity.
- How to cope with increased static variability and static fault rates of devices and interconnects during the circuit and system design phase.
- How to cope with increased time-dependent dynamic variability and dynamic fault rates during the circuit and system design phase..
- Deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.

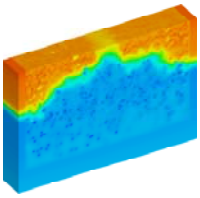

Figure 1 Random discrete dopants in a 35 nm MOSFET from the present 90 nm technology node.

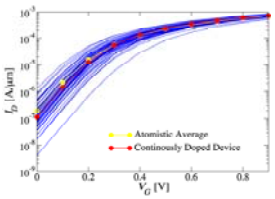

Figure 2 Corresponding variations in the current-voltage characteristics of 200 transistors wit h different dopant distributions

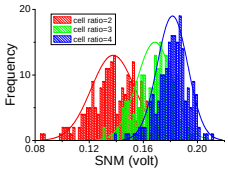

Figure 3 Corresponding distribution of the static noise margins in 6T SRAM cells

Solutions

- Analysis techniques : for exploring the design space, and analyzing of the system in terms of performance, power and reliability of manufactured instances across a wide spectrum of operating conditions (thermal, noise, age).
- Solution techniques : which are design time and/or runtime techniques to mitigate the impact of reliability issues (seen as time-dependent variability aspects) of integrated circuits at component, circuit, architecture and system level.

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Progress beyond state-of-the-art

- **Development of a methodology for variability and reliability analysis from device to system :**

  It should be capable of propagating the statistical effects of reliability and variability issues all the way from the technology level to the application level. Special focus is required on modelling how design parameters influence the final reliability.

- **Development of novel failure-resistant analogue circuit design and analysis techniques :**

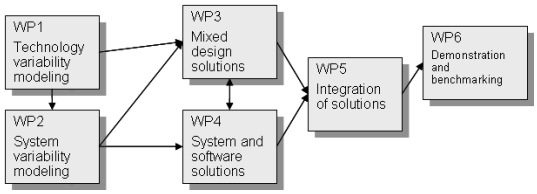
  Coping with variability and time-varying degradation mechanisms by means of reconfiguration and recalibration rather than redundancy.
  This requires monitoring or measuring the effects on the chip after fabrication, and then changing the circuits through reconfiguration and/or recalibration.

- **Creation of IP-wrapping abstractions that facilitate the composition of self-monitoring components at SoC level :**

  The information flowing through the boundaries of the different levels will be classified and standardized. The interfaces to be monitored, the control knobs to apply and the associated metrics will be standardized.

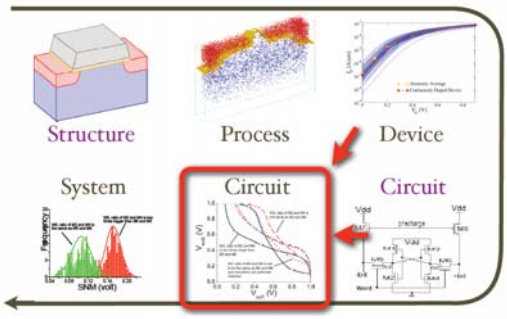
- **To develop support and policies for distributed dynamic resource management at the OS/middleware that work in closed loop :**

  Workload, memory and communication will be run time reallocated to optimally match the evolving state of the hardware in order to ensure reliable computation at a sustainable cost in terms of performances and energy. Policies based on feedback control loops will be employed at this level too.



Project Approach

- **Workpackage 1 :** Physical modeling and understanding of the variability at 45/32 nm technology nodes.
- **Workpackage 2 :** Flow definition and framework set up for variability characterization. Correlated variability energy timing flow definition and set up.
- **Workpackage 3 :** Description of the variability analysis methods at circuit level. Demonstration of the development method on SRAM circuits
- **Workpackage 4 :** Software techniques for flexible data and workload
- **Workpackage 5 :** Integration, definition of characterization blocks, macro-cells and system level architecture
- **Workpackage 6 :** Identification of relevant industrial applications, associated requirements and evaluation metrics



PROJECT FACTS

European Community FP7 funded project (nr 276537)	
Coordination :	IMEC
Effort :	382 person-months
Duration :	30 Months
Start date :	1st January 2008
Industry :	ARM (UK), ST Microelectronics (Italy)
University :	Glasgow (UK), Bologna (Italy), Leuven (Belgium)
Research Centre :	IMEC (Belgium)

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