REALITY

Reliable and Variability tolerant System-on-a-Chip Design in More-Moore Technologies

Scope:

- Scaling beyond the 32 nm technology
- Tackle the increased variability and changing performance of devices from device unto system level.

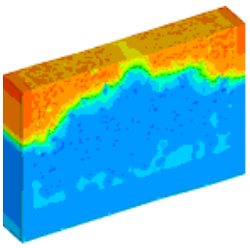
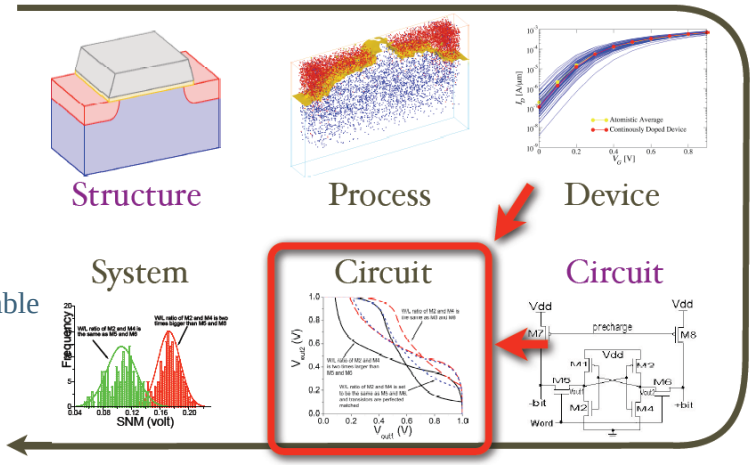


Figure : Random discrete dopants in a 35 nm MOSFET from the present 90 nm technology node.

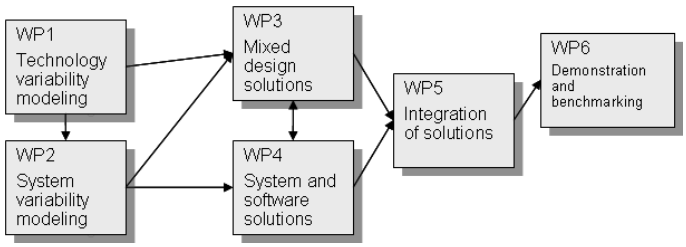
Challenges:

- Increased static variability and static fault rates of devices and interconnects.
- Increased time-dependent dynamic variability and dynamic fault rates.
- Build reliable systems out of unreliable technology while maintaining design productivity.
- Deploy design techniques that allow technology scalable energy efficient SoC systems while guaranteeing real-time performance constraints.



Proposed solution:

- System analysis of performance, power, yield and reliability of manufactured instances across a wide spectrum of operating conditions.
- Generally applicable solution techniques to mitigate the impact of reliability issues of integrated circuits, at component, circuit, and architecture and system design.



PROJECT FACTS

FP7 Project : European Community funded
Website : www.fp7-reality.eu

Industry : ARM (UK), ST Microelectronics (Italy)
University : Glasgow (UK), Bologna (Italy), Leuven (Belgium)
Research Centre : IMEC (Belgium)

Coordination : IMEC
Duration : 30 Months
Effort : 382 person-months
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