SysML-based modelling, architecture, exploration, simulation and synthesis for complex embedded systems - Project Outline
SATURN

- SysML based modelling, architecTuRe, exploRation, simulation and synNthesis for complex embedded systems

- SATURN’s goal is to bridge the current gap between modelling and verification/synthesis in UML based designs of Embedded Systems that are equally composed of HW and SW.

- To do this
  - MARTE is being evaluated for its complementary application with SysML
  - We are adding formal semantics of different Models of Computation for integrated modelling and verification environments
Objectives

- To close the gap between MDA-based modelling and simulation by the integration of OMG SysML modelling tools with simulator-based run-time environments (RTEs).

- To bring SysML and MARTE into industrial application based on two real industrial case studies (Smart Cameras, broadband wireless telecom system) considering all facets of embedded systems design including system level design, hardware dependent software, RTOS, and hardware aspects.

- To push European-based tool vendors and directly exploit project results into existing commercial products, the consortium combines European-based tool vendors (Artisan, Extessy) with leading European system houses (Intracom Telecom, Thales Security Systems).
Project Implementation

- 3 technical WPs
  - WP3 Verification Technology Development
  - WP4 Prototype Tool Specification and Development
  - WP5 Application Test Cases and Validation
- WP1 Project Management
- WP2 Requirements Definition
- WP6 Exploitation and Dissemination
What tools are we using and developing?

- Plan is to allow users to input their design in to Studio in SysML with consideration to augmenting this with MARTE
- In addition there will be a profile for SystemC that enables SystemC specific constructs to be modelled. This will be discussed later.
- There will be code generation capability from Studio to Synthesisable SystemC along with standard Studio C/C++ capability
- Some modelling will be done in Simulink
- This will be passed to the Extessy EXITE ACE tool to enable cosimulation of the whole system
- The Synthesisable SystemC will be translated to VHDL for transfer to the FPGA
- C/C++ will be compiled/loaded to the microprocessor element
The SATURN Tool Chain

- This graphic shows the tool chain being implemented in the project
- This is related to the methodology defined in D3.2