Milestones

This table lists all milestones due during the second project period (starting M13).

MILESTONES							
Mile-stone no.	**Milestone name**	**WP no.**	**Lead beneficiary**	**Delivery date (from Annex I)**	**Achieved Yes/No**	**Actual / Forecast achievement date**	**Comments**
M03.1	Tape out 1st selective RX ADC (simulation result of test-chip available)	WP03	LU	M18	Yes	29.07.2011	
M03.2	Tape out 1st RF ΔΣ ADC (simulation result of test-chip available)	WP03	IMEC	M18	Yes	29.07.2011	
M03.5	Tape out of first class-C VCO	WP03	LU	M24	Yes	31.01.2012	
M04.1	Power Amplifier tape out 1, simulated extracted view available	WP04	KUL	M18	Yes	29.07.2011	
M04.3	Digital modulator and driver lab demonstrator 1	WP04	KUL	M18	Yes	29.07.2011	
M05.2	Tape out f. first prototypes, error free GDSII in time	WP05	IFAT	M18	Yes	29.07.2011	
M06.5	2nd periodic report delivered to EC	WP06	TEC	M24	Yes	03.04.2012	
Major Milestone							
MM02	*CMOS Building Block Design and Implementation*			*M24*	*Yes*	31.01.2012	