Publishable Summary

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Project acronym:	**DRAGON**
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1 Publishable summary

Project Name: **DRAGON** *Start Date*: February 1, 2010
Grant Agreement: **248277** *Duration:* 36 months
Project Website: http://www.dragon-project.eu
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Mission of DRAGON

"The main idea of the DRAGON project is to research and use new design methodologies and architectural innovations, based on reconfigurability and state-of-the-art digital CMOS technology, in order to break the barriers imposed by the lack of scaling properties of analog components. With this concept, distinct reductions in cost, size and energy consumption for multi-standard cellular handsets can be achieved, while higher demands on data rate can be met. Data rates are increasing every day, therefore, the energy consumption per transmitted or received data bit has to be reduced in order to save energy and avoid thermal problems. Wireless data services will become an attractive low-cost alternative to be used in novel applications."

The DRAGON Project

In the DRAGON project a design platform comprising multi-standard transceiver specifications and novel flexible architectures is developed. The number of required external components, like analog filters are replaced by reconfigurable digital (CMOS Complementary Metal Oxide Semiconductor) circuitry; and critical building-blocks are implemented to demonstrate proof of concept, both of the architecture and design methodology. All critical building-blocks are fabricated, tested, and demonstrated in state-of-the-art CMOS technology. The project results are also being provided to standardisation bodies, allowing an alignment of requirements to technology limits.

Objectives

The performance offered by wireless standards has improved steadily over the last decades. There are two main reasons:

1. Society today increasingly asks for wireless systems since they have the potential to enhance comfort and pleasure. More importantly even, wireless technologies can help to support independent living and save costs in health care for an ageing society.
2. Industrial progress relies on continued growth of wireless capacity. Not only more and more people count on mobile broadband services in their professional activities, also the number of objects connected by wireless interfaces is dramatically increasing.

Objective 1 – Miniaturisation of Complex Radio Systems
Future terminals will need radios that support multiple standards and data rates up to 1 Gbit/s. In order to avoid a serious impact on cost, size and weight of the terminal due to increasing numbers of radios and their capacity, miniaturization through design of innovative reconfigurable architectures in nanoscale technologies is crucial.

Objective 2 – Design Methodologies for Energy Efficient Solutions for High Performance Systems
The new, innovative designs should be capable of reaching the same level of average power consumption as dedicated solutions. DRAGON aims at obtaining a 50% energy reduction compared to classical systems.

Objective 3 – Multi-Functional / Multi-Purpose Devices
The proposed multi-functional designs in DRAGON should allow paying off non-recurring engineering costs (NRE) in chip design by re-using the same system in a broad range of applications. Further, DRAGON aims at supporting more than two standards in one building block, which is currently the maximum number that can be achieved.

Objective 4 – Proof of Concept by Silicon Demonstrators
The design of innovative architectures in the most advanced commercial CMOS technologies should not only be used to illustrate and prove the DRAGON project results, but, more importantly, should give European companies the confidence that the disruptive design paths are ready for adoption, and convince them of their significant added value.

Overall Strategy

The results of DRAGON are achieved in multiple steps and marked by three major milestones, which constitute central points in the course of the project and span across the technical work packages.

Milestone 1 – Architectural Exploration
Architectural innovative ideas are identified, explored and used as a high level tool to realise project targets. The focus of the according design experiments is being defined.

Milestone 2 – CMOS Building Block Design and Implementation
The most critical building blocks for the targeted multi-standard radio systems with novel architectures are implemented and measured, using state-of-the-art digital CMOS technology.

Milestone 3 – System Demonstration
Silicon system demonstrators are realised and measured. The overall project results are consolidated and contrasted with the initial goals.

The above objectives and milestones are to be achieved within the three main project phases as displayed in Figure 2 below.

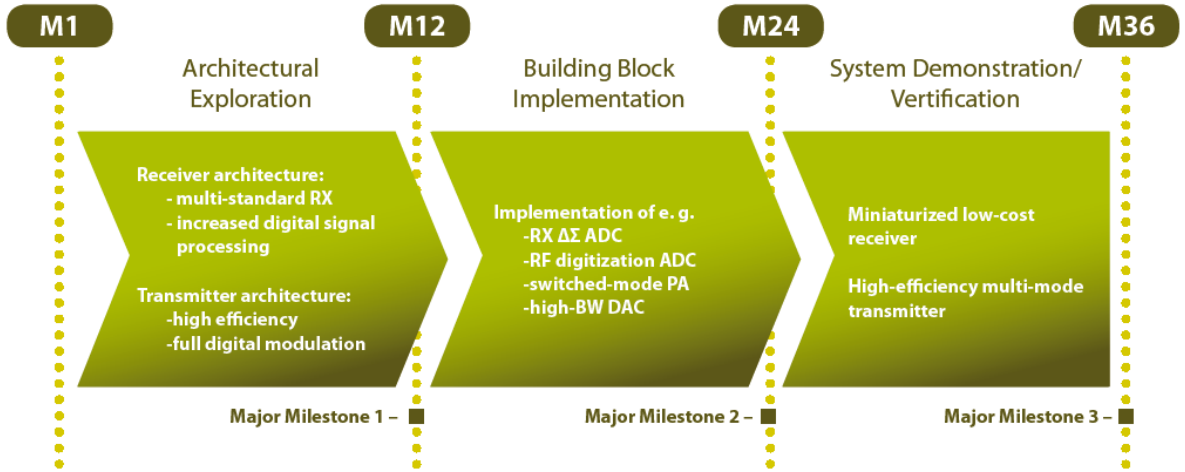

Figure 1: DRAGON Project stages

Technical Approach

The project work in DRAGON is divided into five technical and one project management work packages listed hereafter, including the following sub tasks structure:

WP01: *Requirements and Standardisation:* use cases and target applications; definition of scope and compilation of link budget; propose and evaluate architecture solutions; standardisation.

WP02: *Low Power Concept and Architecture:* receiver architecture; transmitter architecture.

WP03: *Innovative Miniaturised Receiver Design:* selective RX ADC; miniaturised digital RF receiver.

WP04: *Smart Transmitters and Power Amplifiers: design of burst-mode switched-mode power amplifiers; design of high bandwidth modulator and digital driver.*

WP05: *Proof of Concept and Verification:* organization of test chips on state-of-the-art silicon technology; lab setup and silicon verification.

WP06: *Project Management and Dissemination:* project management; dissemination; IPR and exploitation framework.

Description of the work performed and results until now

The DRAGON project started in February 2010 and is going to run for 36 months.

The overall strategy of the project is to define a common system specification and use this in the initial architecture exploration and building block design, as outlined in Major Milestones 1 and 2. The defined specification is based on the state-of-the-art LTE release 10 3GPP standard. By using this standard as a basis we assure that results are relevant for the project industry partners. We have then applied the requirements as well as constraints and features from state-of-the-art CMOS technology to arrive at a forward-looking architecture as well as circuit level requirements for the critical building blocks. Finally, after the first round of circuit fabrication the measured block performances have been feed into a system level simulation and verified against the specification as well as the individual block targets.

The progress achieved by all work packages within the first and second project year is in line with the initial plan and can be summarized as follows.

WP01 (Requirements and Standardisation) has delivered two documents (D01.1 "System specification (first version)" and D01.2 "System specification (second version)") in the first year and one document (D01.3 "System evaluation (first)") in the second year according to stated commitments and time schedule in Annex-I. Beyond that, a system specification for both RX and TX was compiled, reviewed, and agreed upon among project members in Project Year 1, a document serving as over-all requirements, providing targets that aim to justify the project output both for academia as well as industry. Besides, feedback regarding trends and early assumptions in 3GPP was provided to all project members. In Project Year 2, a first system analysis for both RX and TX has been carried out and documented, reviewed, and presented to the other project members.

During the first project year, within ***WP02 (Low power concept and architecture),*** the receiver architecture and the transmitter architecture were investigated and defined according to the work plan. Timely, the architectural choices were delivered in D02.1 "Receiver Architecture" and D02.2 "Transmitter Architecture" and milestones M02.1 "Receiver Architecture" and M02.2 "Transmitter Architecture" were reached in M12. According to the time plan, the involved partners started to refine the architectures including the first feedback from the circuit designs and more detailed simulation results. For the second project year, there are no further deliverables planned within WP02. The progress of the WP is according to the work plan and the involved partners are confident that milestones M02.3 "Receiver architecture optimised" and M02.4 "Transmitter architecture optimised" (both due M26) will be reached successfully on time.

Within ***WP03 (Innovative miniaturised receiver design),*** focus of the work during the first project year were the designs of the selective RX ADC and the bandpass ΔΣ ADC, resulting in the achievements of milestones M03.1 "Tape out 1st selective RX ADC" and M03.2 "Tape out 1St RF ΔΣ ADC" in M18. Currently, new versions of the receiver prototypes are under investigation and are to be designed and processed within the third project year.

In the first project year, ***WP04 (Smart transmitters and power amplifiers)*** made major progress on the identification of the TX and PA bottlenecks being translated to the TX and PA specifications and shared with the other partners. Two PAs were designed in line with the design concepts of DRAGON, one targeting for high output power, the other as a Doherty PA especially targeting for high efficiency at power back-off. Both designs were taped out in UMC 90nm-technology in the first project year. The measurements of these PAs provided an excellent starting point for the objectives of the WP and for the development of multi-level burst-mode architecture. Besides, the major bottlenecks for the generation of multi-level burst-mode signals were identified and a lab demonstrator was built.

During the second project year, deliverable D04.1 "Power amplifier topology: version 1 description and design", deliverable D04.3 "Digital modulator and driver: version 1 description and design" as well as milestones M04.1 "Power amplifier tape-out 1" and M04.3 "Digital modulator and driver tape out 2" have been met. The technical outcomes are in line with the time schedule. The measurement results from hardware implementations and chips give valuable feedback to the consortium. Using the measurement results achieved so far WP04 activities will move forward to the third project year, improving the burst-mode architectures, PA architectures and digital modulator architectures, as well as driving for a higher degree of integration.

Within ***WP05 (Proof of concept and verification),*** during the first project year a feasible policy for silicon access for all implementing partners as well as access to Infineon PDK was established. The

technology for the tape-out of the first test chips was defined. Furthermore, first prototype PAs were implemented to identify the different research lines for the proof-of-concept demonstrators. The first prototype receiver front-end was taped out so that the first tape-out milestone (MS05.2) was reached successfully in the second project year (M18). Besides, all planned test chips for the first half of the project have been implemented and successfully characterized. Results have been compiled and reported as defined in the project plan.

During year two of the project access for 40nm CMOS technology could be provided to additional partners via Europractice. This will enable the project also to implement TX-blocks in 40nm CMOS technology. Feedback from the first prototype test chips will be considered in the 2nd series of prototype test chips for the addressed TX- as well as for the RX-blocks. The schedule for the second prototype run has been drafted and the tape-outs should be completed around M30 of the project.

As stated above, all the relevant overall project objectives for the reporting period have been successfully achieved. The project made excellent progress and is consistent with the original planning. This paves the way for a successful third project year without any deviations from the original schedule.

The final result of the project will be a set of critical building blocks; both for cellular transmit and receive paths. These building blocks will meet key requirements for an industrial standard like LTE. Some results achieved are already state-of-the-art and published at the most prestigious IEEE conferences and journals The designs and design reports will be useful for the industry partners when designing future cellular, and other wireless, transceivers, and the fact that the designs are verified to the system specifications will simplify adoption by industry.

The DRAGON Consortium

The DRAGON consortium brings together partners and competencies from Europe's leading companies in the areas of nano electronics and wireless communications, one research institute and three universities, with radio chip designers and system experts. The consortium is covering the full design chain from customer requirements over system integration to hardware design. Top universities are included to achieve optimum innovation and move the current boundaries of the state-of-the-art. This unique combination of skills guarantees the high quality and optimal industrial exploitation of the project outcomes. This will strengthen the European telecom equipment and semiconductor industry.

Figure 2: The DRAGON Consortium

DRAGON Disclaimer

All public information will be marked with the following DRAGON project disclaimer:

The information in this document is provided "as is", and no guarantee or warranty is given that the information is fit for any particular purpose. The user thereof uses the information at its sole risk and liability.