Milestones

This table lists milestones that were due during the whole project duration.

MILESTONES							
Mile-stone no.	Milestone name	WP no.	Lead beneficiary	Delivery date (from Annex I)	Achieved Yes/No	Actual / Forecast achievement date	Comments
MS11	Consortium review held for a detailed WP definition containing an identification of the target applications and key performance parameters to be used to assess the progress of the project	WP1	EAB	M04	Yes	27.05.2010	
MS12	First version of the system specification is released	WP1	EAB	M06	Yes	30.07.2010	
MS13	Second version of the system specification is released	WP1	EAB	M12	Yes	31.01.2011	
MS14	Final evaluation of improvements w.r.t. scaling and other DRAGON objectives	WP1	EAB	M40	Yes	05.06.2013	
MS21	Receiver Architecture	WP2	TUGraz	M12	Yes	31.01.2011	
MS22	Transmitter Architecture	WP2	TUGraz	M12	Yes	31.01.2011	
MS23	Receiver Architecture optimised	WP2	TUGraz	M26	Yes	29.03.2012	
MS24	Transmitter Architecture optimised	WP2	TUGraz	M26	Yes	29.03.2012	
MS31	Tape out 1st selective RX ADC (simulation result of test-chip available)	WP3	LU	M18	Yes	29.07.2011	
MS32	Tape out 1st RF Delta-Sigma ADC (simulation result of test-chip available)	WP3	IMEC	M18	Yes	29.07.2011	
MS33	Tape out 2nd selective RX ADC (simulation result of test-chip available)	WP3	LU	M30	Yes	21.08.2012	

MILESTONES							
Mile-stone no.	Milestone name	WP no.	Lead beneficiary	Delivery date (from Annex I)	Achieved Yes/No	Actual / Forecast achievement date	Comments
MS34	Tape out 2nd RF Delta-Sigma ADC (simulation result of test-chip available)	WP3	IMEC	M30	Yes	21.08.2012	
MS35	Tape out of first class-C VCO	WP3	LU	M24	Yes	31.01.2012	
MS36	Tape out of second class-C VCO	WP3	LU	M30	Yes	21.08.2012	
MS41	Power Amplifier tape out 1, simulated extracted view available	WP4	KUL	M18	Yes	29.07.2011	
MS42	Power Amplifier tape out and hardware validation 2, simulated extracted view available	WP4	KUL	M30	Yes	21.08.2012	
MS43	Digital modulator and driver tape out 1, simulated extracted view available	WP4	KUL	M18	Yes	29.07.2011	
MS44	Digital modulator and driver tape out and hardware validation 2, simulated extracted view available	WP4	KUL	M30	Yes	21.08.2012	
MS51	Workflow for silicon production established	WP5	IFAT	M03	Yes	30.04.2010	
MS52	Tape out f. first prototypes, error free GDSII in time	WP5	IFAT	M18	Yes	29.07.2011	
MS53	Tape out f. Second prototypes, errof free GDSII in time	WP5	IFAT	M30	Yes	21.08.2012	
MS54	Evaluation completed	WP5	IFAT	M40	Yes	05.06.2013	
MS61	Project start and kick-off, all legal requirements ready	WP6	TEC	M01	Yes	08.03.2010	Receipt of originals of signed Accession Forms to the Grant Agreement and Consortium Agreement forms delayed
MS62	Dissemination environment available	WP6	TEC	M03	Yes	30.04.2010	
MS63	Project dissemination plan completed	WP6	TEC	M06	Yes	30.07.2010	

Milestones							
Mile-stone no.	Milestone name	WP no.	Lead beneficiary	Delivery date (from Annex I)	Achieved Yes/No	Actual / Forecast achievement date	Comments
MS64	1st periodic report delivered to EC	WP6	TEC	M12	Yes	29.03.2011	
MS65	2nd periodic report delivered to EC	WP6	TEC	M24	Yes	03.04.2012	
MS66	3rd periodic report delivered to EC	WP6	TEC	M40	Yes	13.06.2013	first version
Major Milestones							
MM01	*Architectural Exploration*			*M12*	*Yes*	31.01.2011	
MM02	*CMOS Building Block Design and Implementation*			*M24*	*Yes*	31.01.2012	
MM03	*System Demonstration*			*M40*	*Yes*	05.06.2013	

Table 3: Milestones table