Publishable Summary of the DRAGON project

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2 Publishable summary

Project Name: **DRAGON** *Start Date*: February 1, 2010
Grant Agreement: **248277** *Duration:* 36 months
Project Website: http://www.dragon-project.eu
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Mission of DRAGON

"The main idea of the DRAGON project is to research and use new design methodologies and architectural innovations, based on reconfigurability and state-of-the-art digital CMOS technology, in order to break the barriers imposed by the lack of scaling properties of analog components. With this concept, distinct reductions in cost, size and energy consumption for multi-standard cellular handsets can be achieved, while higher demands on data rate can be met. Data rates are increasing every day, therefore, the energy consumption per transmitted or received data bit has to be reduced in order to save energy and avoid thermal problems. Wireless data services will become an attractive low-cost alternative to be used in novel applications."

The DRAGON Project

In the DRAGON project a design platform comprising multistandard transceiver specifications and novel flexible architectures is developed. The number of required external components, like analog filters, are replaced by reconfigurable digital CMOS Complementary Metal Oxide Semiconductor) circuitry; and critical building-blocks are implemented to demonstrate proof of concept, both of the architecture and design methodology. All critical building-blocks are fabricated, tested, and demonstrated in state-of-the-art CMOS technology. The project results are also being provided to standardisation bodies, allowing an alignment of requirements to technology limits.

Objectives

The performance offered by wireless standards has improved steadily over the last decades. There are two main reasons:

1. Society today increasingly asks for wireless systems since they have the potential to enhance comfort and pleasure. More importantly even, wireless technologies can help to support independent living and save costs in health care for an ageing society.
2. Industrial progress relies on continued growth of wireless capacity. Not only more and more people count on mobile broadband services in their professional activities, also the number of objects connected by wireless interfaces is dramatically increasing.

Objective 1 – Miniaturisation of Complex Radio Systems
Future terminals will need radios that support multiple standards and data rates up to 1 Gbit/s. In order to avoid a serious impact on cost, size and weight of the terminal due to increasing numbers of radios and their capacity, miniaturization through design of innovative reconfigurable architectures in nanoscale technologies is crucial.

Objective 2 – Design Methodologies for Energy Efficient Solutions for High Performance Systems
The new, innovative designs should be capable of reaching the same level of average power consumption as dedicated solutions. DRAGON aims at obtaining a 50% energy reduction compared to classical systems.

Objective 3 – Multi-Functional / Multi-Purpose Devices
The proposed multi-functional designs in DRAGON should allow paying off non-recurring engineering costs (NRE) in chip design by re-using the same system in a broad range of applications. Further, DRAGON aims at supporting more than two standards in one building block, which is currently the maximum number that can be achieved.

Objective 4 – Proof of Concept by Silicon Demonstrators
The design of innovative architectures in the most advanced commercial CMOS technologies should not only be used to illustrate and prove the DRAGON project results, but, more importantly, should give European companies the confidence that the disruptive design paths are ready for adoption, and convince them of their significant added value.

Overall Strategy

The results of DRAGON are achieved in multiple steps and marked by three major milestones, which constitute central points in the course of the project and span across the technical work packages.

Milestone 1 – Architectural Exploration
Architectural innovative ideas are identified, explored and used as a high level tool to realise project targets. The focus of the according design experiments is being defined.

Milestone 2 – CMOS Building Block Design and Implementation
The most critical building blocks for the targeted multistandard radio systems with novel architectures are implemented and measured, using state-of-the-art digital CMOS technology.

Milestone 3 – System Demonstration
Silicon system demonstrators are realised and measured. The overall project results are consolidated and contrasted with the initial goals.

The above objectives and milestones are to be achieved within the three main project phases as displayed in Figure 2 below.

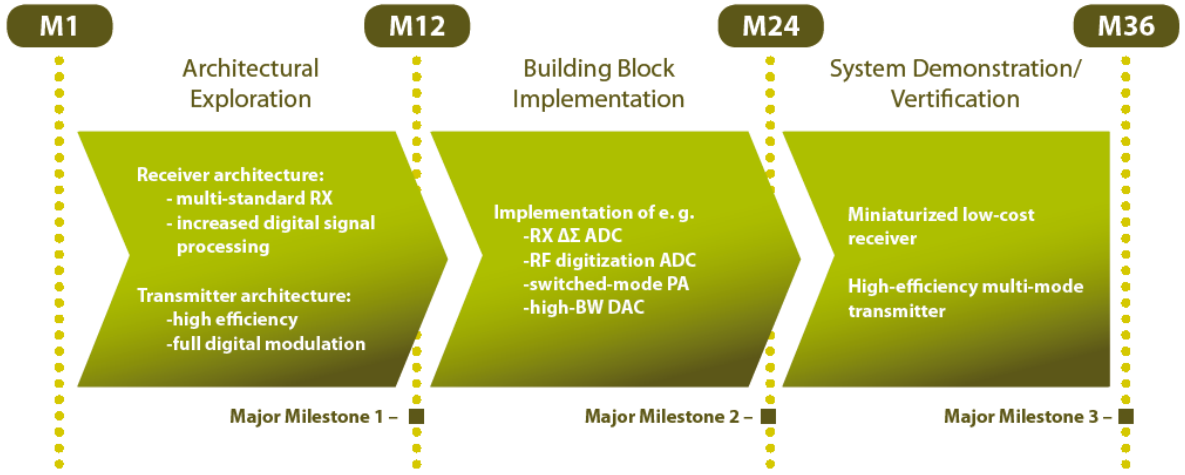

Figure 1: DRAGON Project stages

Technical Approach

The project work in DRAGON is divided into five technical and one project management work packages listed hereafter, including the following sub tasks structure:

WP01: *Requirements and Standardisation:* use cases and target applications; definition of scope and compilation of link budget; propose and evaluate architecture solutions; standardisation.

WP02: *Low Power Concept and Architecture:* receiver architecture; transmitter architecture.

WP03: *Innovative Miniaturised Receiver Design:* selective RX ADC; miniaturised RF digisation receiver.

WP04: *Smart Transmitters and Power Amplifiers: design of burst-mode switched-mode power amplifiers; design of high bandwidth modulator and digital driver.*

WP05: *Proof of Concept and Verification:* organisation of test chips on state-of-the-art silicon technology; lab setup and silicon verification.

WP06: *Project Management and Dissemination:* project management; dissemination; IPR and exploitation framework.

Description of the work performed and results in the first project period

The DRAGON project started in February 2010 and is going to run for 36 months. During the first project phase, corresponding to the first project year, the focus was put on the architectural exploration. The main aim was to identify, explore and use architectural innovative ideas as a tool at a high level to realize project targets. The focus of the according design experiments was defined.

At the beginning, major effort was put into the successful launch of the project. The major goal was to establish a sound basis for a good and fruitful cooperation of the project partners towards the research objectives. This could be realized through providing all the relevant management components like contractual, financial, legal, technical, administrative and ethical issues as well as catching upcoming obstacles well ahead of time. Furthermore, a public project website and the internal IT communication infrastructure have been established as well as a dissemination plan for the entire project duration has been compiled.

The progress achieved by all work packages within the first project year is in line with the initial plan and can be summarized as follows.

The status of ***WP01 (Requirements and Standardisation)*** can be summarized as follows:

- The work package has delivered two documents according to stated commitments and time schedule in Annex-I (D1.1 “System specification (first version)” and D1.2 “System specification (second version)”).
- A system specification for both RX and TX has been compiled, reviewed, and agreed upon among project members. This document will serve as over-all requirements, providing targets that aim to justify the project output both for academia as well as industry.
- Feedback regarding trends and early assumptions in 3GPP has been provided to all project members.

Within ***WP02 (Low power concept and architecture)*** the receiver architecture and the transmitter architecture have been investigated and defined according to the work plan. Timely, the architectural choices have been delivered in D2.1 “Receiver Architecture” and D2.2 “Transmitter Architecture” and milestones M02.1 “Receiver Architecture” and M02.2 “Transmitter Architecture” have been reached in M12. According to the time plan, the involved partners started to refine the architectures including the first feedback from the circuit designs and more detailed simulation results. Everything is on track to reach milestones M02.3 “Receiver architecture optimised” and M02.4 “Transmitter architecture optimised”, i.e., optimised receiver and transmitter design, in M26.

Within ***WP03 (Innovative miniaturised receiver design)*** the design for the selective RX ADC is already done down to the layout level. The design of the bandpass ΔΣ ADC is on track and tape-out is expected for this year. Hence, no problems are expected to reach milestones M03.1 “Tape out 1st selective RX ADC” and M03.2 “Tape out 1st RF ΔΣ ADC” in M18.

WP04 (Smart transmitters and power amplifiers) made major progress on the identification of the TX and PA bottlenecks (KUL, IFX and TUG). These were translated to the TX and PA specifications and shared with the other DRAGON partners.

Two PAs have been designed that are in line with the design concepts of DRAGON. One design is targeting for high output power, while the other is a Doherty PA and especially targets high efficiency at power back-off. Both these designs have been taped out in UMC 90nm-technology in the beginning of July 2010. The measurements of these PAs will provide an excellent starting point for the objectives of this WP. Furthermore, these results are also important for IFAT and TUG/FTW for the development of multi-level burst-mode architecture.

We have identified the major bottlenecks for the generation of multi-level burst-mode signals and have made good progress to build a lab demonstrator.

The collaboration between the different WP partners is excellent. Information is shared about the possibilities at the circuit-level on one hand, and possibilities at the architecture level on the other hand.

The status of ***WP05 (Proof of concept and verification)*** after the 1st project year comprises the following points:

- A feasible policy for silicon access for all implementing partners has been established. IMEC will implement on 40nm all other implementing partner will use 65nm technology.
- Access to Infineon PDK established and all implementing partners have the design environment for the first tape out in place.
- First prototypes PAs have been implemented to identify the different research lines for the proof-of-concept demonstrators.
- First prototype receiver front-end has been tape out.
- Technology for the tape-out (M16) of the first test chips is defined.

The draft timeline and the intermediate steps until the first tape-out in M18 has been set and is in line with the overall project schedule.

The DRAGON Consortium

The DRAGON consortium will bring together partners and competencies from Europe's leading companies in the areas of nano electronics and wireless communications, one research institute and three universities, with radio chip designers and system experts. The consortium is covering the full design chain from customer requirements over system integration to hardware design. Top universities are included to achieve optimum innovation and move the current boundaries of the state-of-the art. The combination of all this guarantees the high quality and optimal industrial exploitation of the project outcomes. This will strengthen the European telecom equipment and semiconductor industry.

Figure 2: The DRAGON Consortium

DRAGON Disclaimer

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