

# STEEPER

## Steep Subthreshold Slope Switches for Energy Efficient Electronics

**Grant Agreement Number:** 257267  
**Project Acronym:** STEEPER  
**Project Title:** Steep Subthreshold Slope Switches for Energy Efficient Electronics  
**Funding Scheme:** Collaborative project  
**Thematic Area:** Information and Communication Technologies  
**Project start date:** 01/06/2010

<b>Deliverable D5.1:</b> Device Requirements and specifications for tunnel FETs
---

**Nature<sup>1</sup>:** R

**Dissemination level<sup>2</sup>:** PU

**Due date: Month:** M6

**Date of delivery:** M12

**Partners involved:** GLOBALFOUNDRIES, Intel Mobile Communications

**Authors:** Juergen Faul, Reinhard Mahnkopf, Thomas Schulz

**Document version:** V1.0

---

<sup>1</sup> R = Report, P = Prototype, D = Demonstrator, O = Other

<sup>2</sup> PU = Public, PP = Restricted to other programme participants (including the Commission Services), RE = Restricted to a group specified by the consortium (including the Commission Services), CO = Confidential, only for the members of the consortium (including the Commission Services)

## Revision history

Version	Date	Author	Comment
0.1	15.07.11	J. Faul, R. Mahnkopf, T. Schulz	First full version
1.0	29.07.11	A. Ionescu	Update and approval
1.0	29.07.11	P. Dainesi	Final quality control and formatting

## Table of contents

Revision history.....	2
Executive summary .....	4
Chapter 1: Target Setting Methodology.....	5
1.1. Targets for digital circuits .....	5
1.2. Targets for analog / mixed signal devices and circuits .....	7
Chapter 2: Significant results .....	11
Chapter 3: Benchmark.....	14
Chapter 4: Different Tunnel-FET Scenarios .....	16
Conclusion.....	18
References .....	19

## Executive summary

In this deliverable specifications and targets for tunnel FET devices are derived. To that extend the ITRS roadmap serves as a guideline. Detailed specifications are assessed for digital applications. For analog applications we determine the same main specifications, because there is no evidence reported in literature that tunnel FETs behave differently than conventional MOS FETs with respect to analog/RF properties.

We analyse and illustrate "CMOS replacement" and "CMOS add-on" scenarios based on tunnel FETs in case of advanced technology nodes (sub-20nm) for both digital and analog/RF applications and support our statements with quantitative estimations and industrial benchmarking.

As an outcome of the analysis tunnel FETs are well suited for applications in low standby as well as low operating power applications. For high performance circuits an application of tunnel FETs features only minor benefits since the inherent advantage of steep sub  $V_t$  slopes is therefore not relevant.

## Chapter 1: Target Setting Methodology

Goal of the present deliverable is to define Requirements and Specifications for tunnel FETs. Both, digital and analog / mixed signal specifications are investigated.

### 1.1. Targets for digital circuits

The process of target definition for tunnel FET devices is based on the most recent ITRS roadmap which serves as a first guideline throughout the targeting process. The present project ends in 2013. Assuming a two years timeframe for implementation into manufacturing environment the roadmap predictions for 2015 need to be considered. For that year the latest ITRS revision from 2010 predicts for multi gate FET's the following specifications [1]:

Table 1: ITRS predictions for 2015

Prediction for 2015 (Multi Gate FET's)			
	HP	LSTP	LOP
EOT electric [nm]	1.17	1.5	1.2
L [nm]	17	17	17
Vdd [V]	0.81	0.81	0.63
Vt [V]	0.26	0.467	0.292
Ion_n / Ion_p	1.22	1.22	1.22
Ion [mA/ $\mu\text{m}$ ]	1.49	0.632	0.772
Ioff [nA/ $\mu\text{m}$ ]	100	0.01	5
Cg for CV/I [fF/ $\mu\text{m}$ ]	0.68	0.57	0.669
CV/I [ps]	0.37	0.73	0.55
Tau (FoM) [ps]	2.78	5.11	4.06

In Table 1, HP stands for high performance logic, LSTP for low standby power and LOP for low operation power applications. Although the roadmap denotes in the timeframe considered also specifications for ultra thin body FD SOI devices the predictions of the multi gate devices were taken as reference since those values are more advanced.

By looking at the predicted supply voltages targets need to be defined for supply voltages below the roadmap values of 0.81 and 0.63V. Especially, in the light of steeper sub Vt slopes for tunnel FETs (i.e.  $\sim 40\text{mV/dec}$ ) a further reduction of Vdd over the roadmap predictions seems to be indicated. To account for that the assessment is done for Vdd=0.5 / 0.6V.

For performance assessment of real circuitry both, DC and AC performance matter. High DC currents are needed to drive signals over long metal loaded wires where, only transistor Ion matters. On the other hand, high AC performance is required for gate load dominated circuits such as inverter chains. Besides the simple C\*V/I for each transistor type nowadays the so called figure of merit (FoM) assessment is employed throughout the semiconductor industry [2]. In this metric, a

gate delay per stage for an inverter type of ring oscillator is calculated. Both assessments are included in Table 1. Inherent to the approach gate delays for the inverter based FoM are slower.

In addition to performance also the consumed power is an important measure, especially for low operation power applications. To that extend the ratio of performance over power serves for comparison. For the power calculation values for both, static and dynamic power are obtained with the following equations:

$$\tau = C_{load} * V_{dd} / I_{dsum}$$

$$\text{Static Power} = I_{off}(\text{total}) * V_{dd}$$

$$\text{Dynamic Power} = 1/\tau * C_{load} * V_{dd}^2$$

$$\text{Total Power} = 1/3 \text{ static} + 2/3 \text{ dynamic Power} \quad (\text{rough estimate for both, HP and LOP logic})$$

$$\text{Performance / Power} = 1/\tau / \text{Total Power}$$

Applying these methods for power calculations on the ITRS roadmap we obtain for high performance logic device applications the following power development over time:

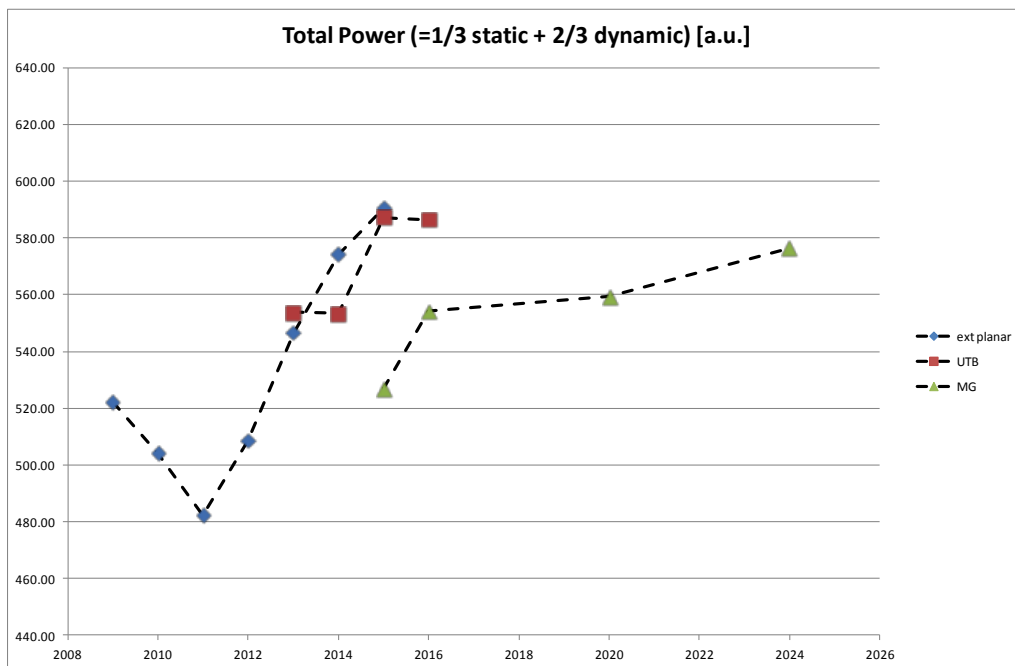


Figure 1: Total power consumption over time

The data displayed in Figure 1 show that within a given device architecture the power consumption slightly increases over time. The trend is broken by introducing a new architecture. So, the power consumption increase is thus moderate over time. Looking at the ratio Performance over power, a different picture is obtained:

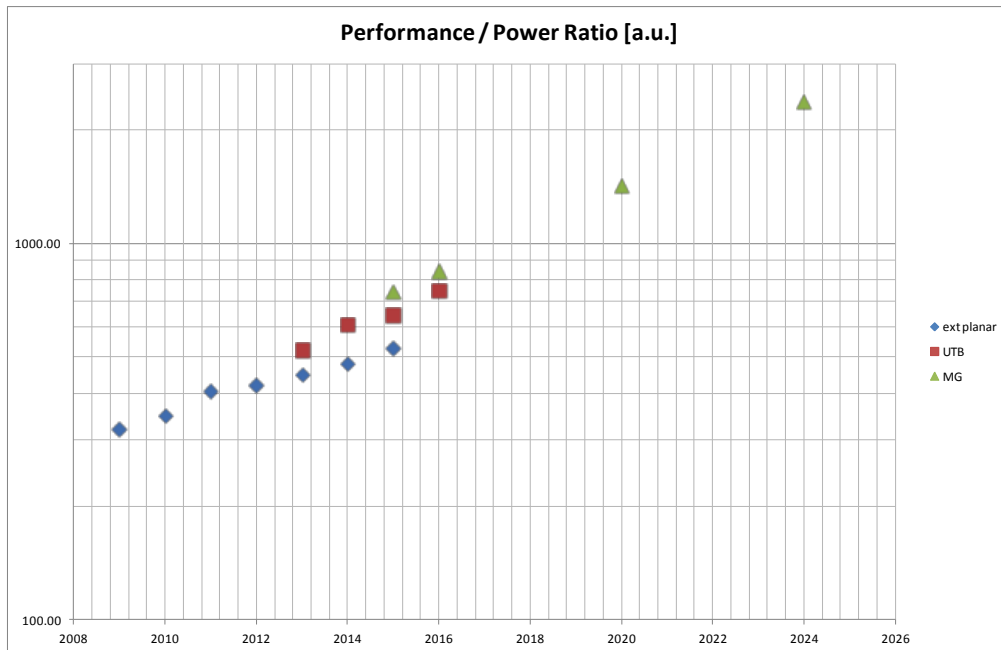


Figure 2: Performance to Power ratio over time

In Figure 2, the ratio of performance over power is increasing with a slope of  $\sim 30\%$  every 2 years. This slope will be applied as guideline for the target definition. Especially in this metric it is expected to see a tremendous benefit of the tunnel FET devices over existing roadmap predictions due to their steep sub  $V_t$  slope characteristics.

Performance over power is the primary measure for LOP devices. The maximum performance for a given power consumption specification is sought for. For LSTP, the static power consumption is the most important parameter. In these applications devices are operating in stand by or idle mode for most of the time. In both cases, the semiconductor industry is striving for long battery life times.

Three different scenarios for tunnel FET applications have been discussed, i.e. full replacement, add-on or niche scenario. The requirements for the different scenarios are different. Whereas a full replacement requires similar or exceeding specifications of conventional CMOS devices, an add-on or niche scenario can concentrate on the inherent benefits of low voltage application or certain tunnel FET features only. The different scenarios will have different requirements.

## 1.2. Targets for analog / mixed signal devices and circuits

In general on hand side digital, and on the other hand analog mixed signal (A-MS) with radio frequency (RF) circuitry parts show different system trends and are driven by different kinds of device parameter optimization. As an example Figure 3 shows the system on chip integration (SOC) of a GSM (Global System for Mobile Communications) phone in standard CMOS for 130nm technology generation. At that point in time the analog part was minor and consumed roughly one third of the total die size. But because the analog part is scaling less aggressive as the digital part over time the relative die size for low cost GSM phones is now in actual technology generations dominated by the analog part as shown in Figure 4.

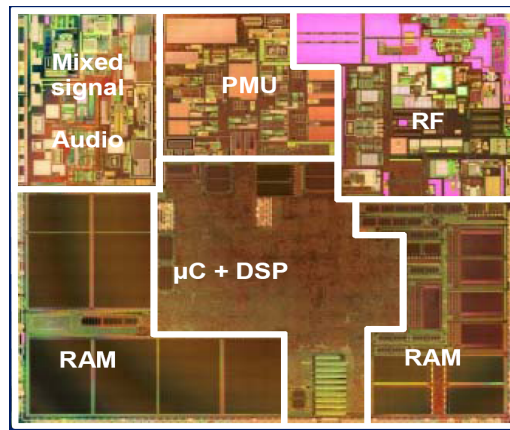


Figure 3: SOC integration in standard CMOS example: GSM phone on a chip

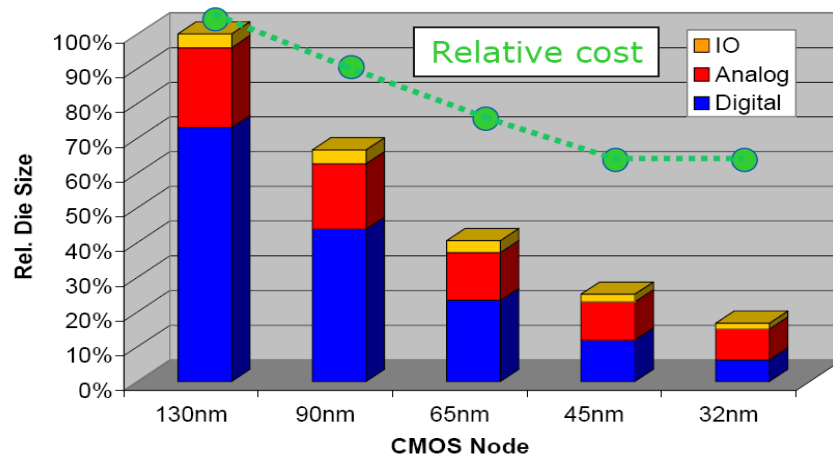


Figure 4: Different trends in area scaling for digital and analog parts of a circuitry.

Digital parameters of a transistor describe how good a transistor is acting as a switch that means how good is the transition of a defined off state towards a defined on state, therefore parameters like the leakage current, the drive current, the threshold voltage and the slope of the IV curve are the key digital parameters besides the area footprint of the device as discussed before. Otherwise in analog circuits the signals do not allow huge fluctuations in parameter values and differences in between equally designed devices. Therefore the electronic noise which defines the random fluctuation in an electronic signal is more important for analog applications and should be reduced to achieve better signal to noise ratios (SNR). The device ability of signal amplification is often reported as intrinsic gain which is the ratio of the mutual (input) transconductance and the output transconductance. Because the gain in signal amplification depends also on the signal frequency the bandwidth defines a range of frequencies for which the amplifier gives amplification above one. The upper limit of the bandwidth is the transit or cut-off frequency, where the voltage is degraded to the value of  $1/\sqrt{2}$  and the voltage level is damped to  $20 \times \log(1/\sqrt{2}) = (-) 3$  dB. The noise factor (F) and the noise figure (NF) of a device specifies how much additional noise the device will contribute to the noise already from the source. Classical MOSFETs are dominated by flicker noise which is increasing over the



technology generations and is dependent on random dopant fluctuations and traps, but due to highly doped pn junctions and the tunneling effect Tunnel FETs might see an increase in shot noise.

Typical requirements for figure of merit (FOM) of A-MS/RF devices are summarized as follows:

- Analog specific figure of merit
  - High mutual transconductance  $g_m$
  - High output resistance  $R_{out}$  (= low output transconductance  $g_{DS}$ )
  - High intrinsic (voltage) gain  $A_v$  (=  $g_m * R_{out}$ )
- RF specific figure of merit
  - High transit/cut-off frequency  $f_T = f_c = 1/\text{gate delay} = g_m/(2\pi (C_{gd}+C_{ds}))$ 
    - Reduced gate resistance  $R_G$
    - Reduced capacitances  $C$
  - High maximum oscillation frequency  $f_{max}$  (Power amplification = 1 = 0 dB)
  - Reduced noise figure NF in [dB] and noise factor F in [1]:
    - $N = \text{total input noise power} / \text{input noise power from source only}$
    - $NF_{min} = 10 \log_{10} (F)$  dB
  - Reduced flicker noise (1/f noise),  $S_{vgate}$
  - Linearity (VIP3), an ideal amplifier would be a totally linear device, but real amplifiers are only linear within limits.
  - Reduced parameter mismatch, especially threshold voltage.  $A_{VT} = \sigma_{\Delta VT}^2 / (WL)$

In contradiction to the digital target specifications the analog / mixed signal target specifications are more similar to conventional MOSFET devices. Therefore in agreement with the MOSFET figure of merit the expected intrinsic device gain for Tunnel FETs is around 30 and the one over frequency noise is approx. 50 [ $\mu V^2 \mu m^2 / Hz$ ]. In a replacement scenario a Tunnel FET has to achieve a peak transit frequency of around 520 GHz and a peak maximum oscillation frequency of approx. 600 GHz as summarized in Table 1b.

Table 1b: SOC integration in standard CMOS example: GSM phone on a chip

	AMS/RF ITRS 2010	scenario 1 Replacement
	2015	2015
gm/gds [1]	30	30
1/ f noise [ $\mu V^2 \mu m^2 / Hz$ ]	50	50
peak fT [THz]	0.52	0.52
peak fmax [THz]	0.6	0.6

Figure 5 shows that different final applications usually work at a much lower system frequency than the needed device transit frequency. But nevertheless Si-RF CMOS has to cover a wide spectrum from below 1GHz towards 77GHz for RADAR applications.

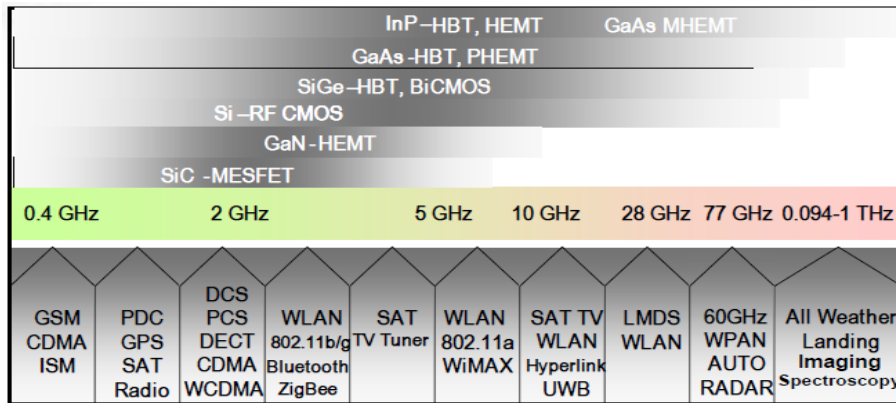


Figure 5: Application spectrum: ITRS2010, Wireless Working Group

At the moment we have no evidence that the Tunnel FET device is behaving differently as the conventional MOSFET regarding most analog/RF parameters but known issues to achieve specific FOM are as follows:

- Short channel effects (SCE) degrade  $R_{out}$  as we scale  $L_G$ 
  - Different Tunnel FET behavior is expected due to the channel length independence.
- Drastic reduction in intrinsic gain
  - Potential benefit: TFET is not sensitive to channel length, therefore less parameter variability
- Increasingly difficult to achieve both high gain and high  $f_T$
- Increasingly difficult to achieve low gate resistance  $R_G$  & low capacitances
  - Can TFET's provide any advantage regarding  $R_G$  or capacitances ? (→ measurements required)

A current issue is that typical analog/RF parameters are not reported in TFET publications. Therefore measurements of the above mentioned parameters are needed for future assessments of analog/RF properties.

## Chapter 2: Significant results

The goal of the present project is the development of devices featuring steep sub  $V_t$  slopes at the end of the project in 2013. Considering a time frame of two years for integration into manufacturing the project scope corresponds to a manufacturing start in 2015. For that particular period the roadmap predicts  $V_{dd}$ 's of 0.81V for HP / LSTP and 0.63V for LOP, respectively as devoted in Table 1.

Tunnel FET's feature steep sub  $V_t$  slopes in the range of 40mV/dec compared to  $\sim 90$ mV/dec for conventional devices at  $V_{dd}$  and gate lengths according to the roadmap predictions. Taking this slope difference into account the following threshold voltages can be estimated for given off currents in the LSTP and LOP case:

Table 2:  $V_t$  estimation considering sub  $V_t$  benefit for tunnel FET's

		Conventional FET	Tunnel FET $V_t$
LOP	$I_{off} = 5\text{nA}/\mu\text{m}$	0.29V	0.17V
LSTP	$I_{off} = 10\text{pA}/\mu\text{m}$	0.47V	0.28V

The HP case was not considered since its specified off-state current of  $100\text{nA}/\mu\text{m}$  would result in a small  $V_t$  reduction only. According to Table 2, for tunnel FET's the threshold voltages can be lowered by about 120mV for LOP and for LSTP by even 190mV, respectively. The different amount of  $V_t$ -reductions is a consequence of the application specific off current requirements. In case of LSTP with its extremely low  $I_{off}$  of  $10\text{pA}/\mu\text{m}$  the sub  $V_t$  slope improvement results in a higher  $\Delta V_t$ .

Again, the HP process is not considered further for the reason described above, due to a small benefit in  $V_t$  well below 100mV. Also, for those applications a reduction of operating voltages is not in focus. Therefore, this process flavour is not thought to be a primary candidate for the application of tunnel FET's. The possible threshold voltage reduction for LSTP and LOP however, enable a reduction in supply voltage for those applications.

For the target setting the ITRS roadmap data serve as inputs and were scaled to the boundary conditions of tunnel FET's. This approach implies that tunnel FET's and CMOS FET's are assumed to achieve comparable drive currents for a given geometry and  $V_t$ . The target definition is derived from the ITRS drive currents by normalization to the reduced threshold voltages noted in table 2 and to target  $V_{dd}$  settings. Unlike the roadmap the present assessment considers for both process options the identical electrical EOT of 1.5nm. Please note that for LSTP and LOP different supply voltages were considered due to the  $V_t$  difference of about 100mV. LSTP features lower leakage specifications and thus, higher  $V_t$  levels. To account for this delta the LSTP application was assessed for 0.6V whereas LOP done for  $V_{dd}=0.5\text{V}$ . This difference is necessary to obtain an equivalent circuit performance. To that end a comparable gate overdrive is required and thus the operating voltages need to be chosen differently.

Table 3 shows the outcome of the targeting exercise. For the calculations a gate length of 20nm and an electrical EOT of 1.5nm was assumed. The table consists of two parts. The left hand part contains the assessments for LSTP, the right hand part the estimates for LOP. In both parts, the left

column denotes the scaled CMOS devices violating the off current requirements. This device serves as an intermediate step for the drive current definition. The right column in the table shaded in orange colour lists the obtained values for the tunnel FET’s of each process option. As expected, both scaled devices of the intermediate step for LSTP and LOP violate the target specifications due to a shallower sub Vt slope for conventional devices.

Table 3: Target assessment based on scaled ITRS devices

	Replacement in LSTP			Replacement in LOP		
	"CMOS" scaling	TFET target		"CMOS" scaling	TFET target	
EOT electric [nm]	1.5	1.5		1.5	1.5	
L [nm]	20	20		20	20	
Vdd [V]	0.6	0.6		0.5	0.5	
Vt [V]	0.29	0.29		0.17	0.17	
Ion_n / Ion_p		1.43			1.43	
Ion [mA/μm]	0.501	0.501		0.614	0.614	
Ioff [nA/μm]	0.111	0.01		84	5	
Cg for CV/I [fF/μm]	n/a	0.638		n/a	0.638	
CV/I [ps]	n/a	0.76		n/a	0.52	

In summary, we obtain the following targets for LSTP and LOP applications:

LSTP – targets:

EOT=1.5nm, L=20nm, Vt=0.29V, Ioff=10pA/μm

➔ Ids=0.5mA/μm @ Vdd=0.6V  
CV/I = 0.76ps

LOP – targets:

EOT=1.5nm, L=20nm, Vt=0.17V, Ioff=5nA/μm

➔ Ids=0.6mA/μm @ Vdd=0.5V  
CV/I = 0.52ps

By comparing the obtained gate delays in the simple CV/I metric from above with the roadmap values in Table 1 nearly similar performances are obtained to the ITRS proposal. Whereas the gate delay for LSTP is with 105% only slightly slower than the roadmap values LOP is with 94% even a little faster.

The real benefit of Tunnel FET’s however, is seen by comparing the power estimates with the roadmap assumptions. To that extend Tab. 4 compiles a comparison for gate delay calculated by a figure of merit (FoM) approach, drive currents and Vt, the static, dynamic and total power as well as the performance over power ratio for both LSTP and LOP, respectively.

Table 4: Comparison of obtained tunnel FET design point with ITRS road map prediction

	Replacement in LSTP			Replacement in LOP		
	"ITRS" Prediction	TFET target		"ITRS" Prediction	TFET target	
Vdd [V]	0.81	0.6		0.63	0.5	
Tau (FoM) [ps]	5.11	5.61	110%	4.06	3.81	94%
Ion [ $\mu\text{A}/\mu\text{m}$ ]	0.632	0.501		0.772	0.614	
Vt [V]	0.467	0.29		0.292	0.17	
Static Power [a.u.]	0.0081	0.006	74%	3.15	2.5	79%
Dynamic Power [a.u.]	0.281	0.177	63%	0.267	0.181	68%
Total Power [a.u.]	188	118	63%	179	121	68%
Perf / Power	1	1.45		1	1.58	

As a first observation in Table 4 it is seen that also in the FoM assessment the performance evaluation for circuits based on tunnel FET’s and on conventional devices is similar. Here again, LOP circuits build on tunnel FET’s are assessed to be slightly faster than the roadmap device whereas in LSTP it is the opposite. Thus both, the simple CV/I metric and the more sophisticated FoM estimation agree quite well in the relative comparison between tunnel FET’s and conventional devices. The performance result as such is not a surprise since the proposed tunnel Fet drive currents are only about 20% off the roadmap targets for a supply voltage scaled with a similar amount.

As far as power consumption is concerned, circuits based on tunnel FET devices feature a tremendous benefit. Both, static and dynamic power are significantly reduced. As a consequence, the devices consume only about 2/3 of the conventional devices in averaged total power at the proposed target point with a comparable speed. Due to this big advantage, the performance to power ratio is looking very favourable for this new device type. There, a benefit of 50% is observed. Compared to a usual increase of 30% every two years this is tremendous. Based on this outcome the implementation of tunnel FET’s in LOP is even more favourable than the one in LSTP applications.

### Chapter 3: Benchmark

It is very clear that the conventional planar bulk MOSFET is the dominant semiconductor device in most electronic logic circuitry today and it is after 4 decades of device optimization the unbeaten champion regarding power vs. performance trade-off for current product applications. Nevertheless new requirements for very low supply voltages give a chance for emerging steeper slope devices as discussed above. But what has been really proven and what needs verification?

As starting point for the benchmark of a generic state of the art MOSFET with Tunnel FET’s from literature we compare the transfer characteristic of both device types which is the drive current  $I_D$  in [A/ $\mu\text{m}$ ] versus input voltage  $V_{GS}$  in [V]. A conventional planar bulk MOSFET shows typically a subthreshold slope around 80-90 mV/current decade, whereas more advanced fully depleted SOI MOSFETs or FinFETs can achieve 60-70 mV/current decade. This design space is indicated in Figure 6 as the family of different blue trendlines. To differentiate from this state of the art device type the novel device types should show subthreshold slopes of 40 mV/current decade or below which are indicated as red, orange, and yellow trendlines.

The following benchmark is based on data from the most important semiconductor device conferences (IEDM, VLSI, ESSDERC) of the years 2009 and 2010 as listed in Table 5. In this time period we see nine papers of interest regarding different Tunnel FET’s. Most papers at the ESSDERC conference show simulation results (dark green) whereas most papers from IEDM and VLSI show experimental results (light green). For simplicity the curves are shown by 2 fitting tangents.

**Steeper slope devices, trendlines normalized at  $I_{off}=1\text{nA}/\mu\text{m}$**

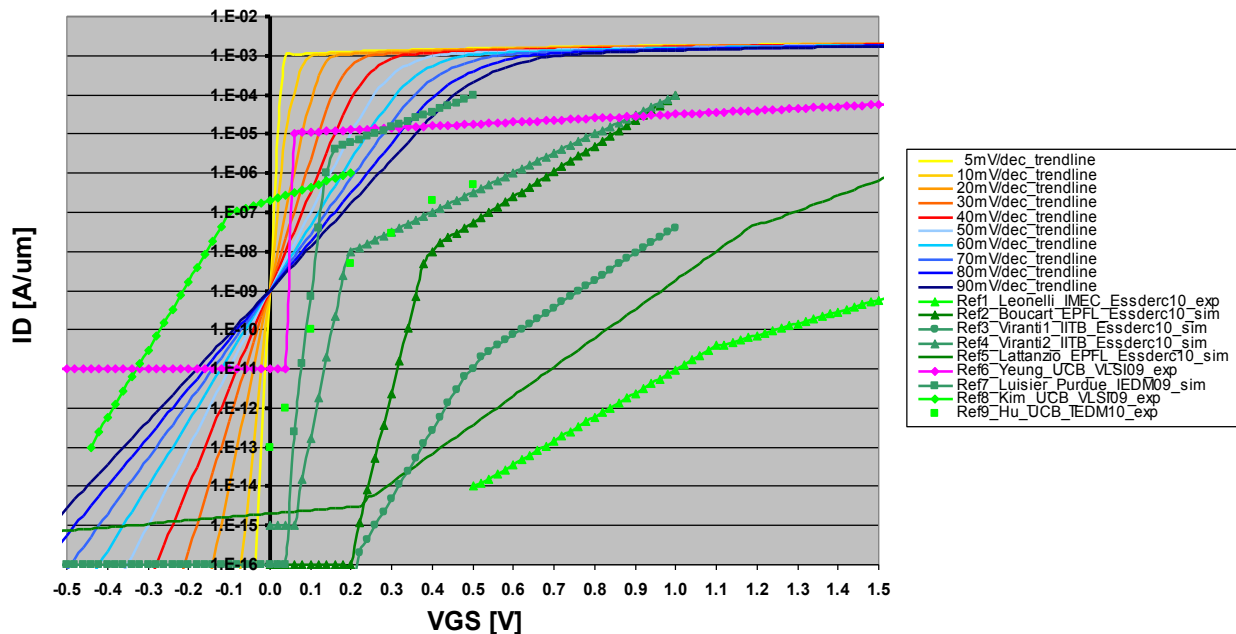


Figure 6: Tunnel-FET Benchmark based on the most important semiconductor device conferences (IEDM, VLSI, ESSDERC) for 2009-2010.

Table 5: Literature reference list corresponding to figure 3

Reference	Name	Author	Organization	Conference	Exp/Sim
[3]	Ref 1	Leonelli	IMEC	ESSDERC 10	Experiment
[4]	Ref 2	Boucart	EPFL	ESSDERC 10	Simulation
[5]	Ref 3	Viranti	IITB	ESSDERC 10	Simulation
[6]	Ref 4	Viranti	IITB	ESSDERC 10	Simulation
[7]	Ref 5	Lattanzio	EPFL	ESSDERC 10	Simulation
[8]	Ref 6	Yeoung	UCB	VLSI 2009	Experiment
[9]	Ref 7	Luisier	Purdue	IEDM 2009	Simulation
[10]	Ref 8	Kim	UCB	VLSI 2009	Experiment
[11]	Ref 9	Hu	UCB	IEDM 2010	Experiment

Based on the benchmark in Figure 6 we can draw the following conclusions:

- The comparison shows a wide spread of different subthreshold slopes but slopes around 40mV/current decade over some decades are experimentally demonstrated [10, 11].
- Paper Reference 6 [8] see pink curve, is not a Tunnel FET device but a similar designed device which is based on positive feedback (FBFET) due to stored charges in the gate sidewall spacers. It shows experimentally that subthreshold slopes below 1mV/current decade are possible.
- No experimental Tunnel FET device is able to compete with a MOSFET in the high performance regime above 1mA/ $\mu\text{m}$ . Therefore we need to discuss different scenarios with reduced drive currents as described in chapter 4.
- But other simulation papers (not shown here) [12] and e.g. Paper Reference 9 [11] show that with reduced bandgap material and tailored heterojunction tunnel region drive currents of 1mA/ $\mu\text{m}$  are possible at supply voltages below 0.5V. Because simulation results vary much and are often higher than later experimental proofs these point needs further verification.
- Different kind of Tunnel FETs can achieve much lower off currents than MOSFETs. This allows a new kind of logic circuitry if an Ion/Ioff current ratio of 6 decades could be obtained and parasitic capacitances could be reduced.

## Chapter 4: Different Tunnel-FET Scenarios

The target assessment of chapter 2 revealed for  $I_{on}=0.6\text{mA}/\mu\text{m}$  a similar performance to the ITRS prediction. At that setting, a huge benefit in power consumption was observed. But the benchmark in chapter 3 showed also that high drive currents for Tunnel-FETs are not demonstrated yet. Based on that we distinguish between the following scenarios and give guidelines for possible applications:

Table 6: Different possible scenarios for Tunnel-FETs in CMOS technologies.

	HP MOSFET ITRS 2010	LOP MOSFET ITRS 2010	LSTP MOSFET ITRS 2010	scenario 0 Intermediate	scenario 1 Replacement	scenario 2 Add-on	scenario 3 Niche
M1 HP [nm]	2015	2015	2015	2012	2015	2015	2015
L Gate [nm]	21	21	21	32	21	21	21
EOT_el[nm]	17	17	17	32	21	32	32
EOT_el[nm]	1	1,2	1,3	1,1	1,1	1,1	1,1
VDD [V]	0,81	0,63	0,81	0,8	0,6	0,5	0,4
Vth [V]	0,22	0,327	0,521	0,25	0,24	0,2	0,16
$I_{on}$ [mA/ $\mu\text{m}$ ]	1,67	0,679	0,596	0,1	1	0,1	0,01
$I_{off}$ [nA/ $\mu\text{m}$ ]	100	5	0,01	1	1	1	1
$I_{on}/I_{off}$	1,7E+04	1,4E+05	6,0E+07	1,0E+05	1,0E+06	1,0E+05	1,0E+04
SS [mV/dec]	80	80	80	50	40	40	40
Cg [fF/ $\mu\text{m}$ ]	0,76	0,66	0,62	0,8	0,7	0,8	0,8
CVI [ps]	0,37	0,61	0,84	6,40	0,42	4,00	32,00
Pact [mW/ $\mu\text{m}$ ]	1,353	0,428	0,483	0,080	0,600	0,050	0,004
Pleak [nW/ $\mu\text{m}$ ]	81	3,15	0,0081	0,8	0,6	0,5	0,4

As shown in Table 6 there are the already above discussed three ITRS MOSFET categories (HP, LOP, and LSTP) and additional 4 distinguished Tunnel-FET scenarios (0, 1, 2, 3). The intermediate scenario (0) is special because these targets are for a different point in time. The intermediate scenario is an early derivation for the year 2012 of the add-on scenario (2) which is for the year 2015. All other scenarios are also for the year 2015. The main distinction of the cases 1, 2, and 3 is the drive current. The replacement scenario (1) has a drive current of  $1\text{mA}/\mu\text{m}$  or more. This is the target guideline for full replacement for exceeding the performance, predicted by the ITRS. In the add-on scenario (2) the performance with  $I_{on}=0.1\text{mA}$  is below ITRS prediction. However, in low leakage circuitry a benefit can still be utilized by realizing speed critical circuits by conventional device architecture and leakage sensitive circuitry by tunnel FET's. In the niche scenario the performance is only around 1% of the ITRS prediction and only applications that utilize special tunnel FET inherent advantages are formed by tunnel FET's.

Some parameters are equal or do not differ much for the different scenarios but are mentioned in the Table 6 to allow following the power-performance calculations. For instance the electrical oxide thickness is 1.1nm for all cases and the capacitance does not vary much with 0.7-0.8 fF/ $\mu\text{m}$  for all cases. The  $I_{off}$  current is normalized to  $1\text{nA}/\mu\text{m}$  and comparable to the LOP MOSFET.

Some parameters differ more for the different scenarios therefore we have a second look on them: The supply voltage as chosen system input is similar for the ITRS and intermediate scenario around 0.8V but to take advantage of a steeper slope for Tunnel FETs the supply voltage is finally reduced



to 0.6V, 0.5V, and 0.4V for scenarios 1, 2, and 3, respectively. The threshold voltage is estimated from the subthreshold slope and the Ion/Ioff ratio and varies from 160 to 250mV.

Scenario 0: Is the intermediate scenario for the project partner working on the demonstrators till the end of the project 2012 with somewhat reduced requirements towards the average subthreshold slope. The subthreshold slope as the main differentiator towards conventional MOSFETs should be 50 mV/dec for short term and 40 mV/dec as base for the other scenarios.

Scenario 1: Is the replacement scenario which means that the conventional MOSFET in the year 2015 can be completely replaced by similar or better performing Tunnel FET devices. This scenario is highly unlikely because there is no experimental evidence that a Tunnel FET can achieve the required drive currents of above 1 mA/ $\mu\text{m}$ .

Scenario 2: Is the add-on scenario which means that next to the conventional MOSFET the Tunnel FET as additional flavour device is used like other MOSFETs with different threshold voltages. For this scenario the Tunnel FET should have a very similar process flow as the standard CMOS process with no or minor additional process steps needed to fully integrate the Tunnel FET devices.

Scenario 3: Is the niche scenario which means that there might be some special applications which do not fit in one of the other scenarios but take advantage of a special property of the Tunnel FET device which makes it attractive for an application despite the fact that other device properties are worse than standard devices. For instance an autarkic temperature insensitive low power application which do not need any high performance device because of a very low activity as for instance a meter or counter who has to send only one signal per day to a base station nearby. As consequence this scenario has the best active Power value but the poorest gate delay.

## Conclusion

In summary, a possible design point for tunnel FET's is proposed. Drive currents of  $500\mu\text{A}/\mu\text{m}$  ( $600\mu\text{A}/\mu\text{m}$ ) at  $0.6\text{V}$  ( $0.5\text{V}$ ) have been proposed for LSTP (LOP) applications. The device considered features a gate length of  $20\text{nm}$ , an electrical EOT of  $1.5\text{nm}$  and threshold voltages in compliance with the corresponding Off-current requirements. Guideline was to achieve a comparable performance to multi channel devices as being proposed in the ITRS roadmap. The proposed design point fulfils this requirement and shows for that setting a tremendous reduction in power consumption.

Due to the benefit in power consumption an application in low operating power applications is most favourable. Also in case of low standby power application a significant benefit can be observed. For high performance designs where power consumption does not play a major role a replacement of conventional devices by tunnel FET's is not paying off the inherent benefit of low power consumption is not sought after.

By achieving the derived targets all logic circuitry can easily be replaced by the new device type. Also driving long metal wires might be possible without a significant draw back in performance since the proposed drive currents are scaled similarly to the operation voltages.

By not achieving the targets tunnel FET's can still serve as add-on features. Then, digital circuitry could be formed in a state-of-the-art processing and tunnel FET's could be dropped in wherever their special properties are of benefit for the overall product performance. This approach, however, requires a high degree of compatibility in process integration. This aspect is part of the next deliverable of work package 5.

Based on the benchmark and the first experimental data we see that an add-on scenario is currently more likely than a replacement scenario. The situation might change if one of the discussed device optimizations like different materials or larger or more efficient tunnelling areas allow higher drive currents or if the parasitic capacitances can be greatly reduced.

## References

- [1]. International Technology Roadmap for Semiconductors (ITRS), update 2010, <http://www.itrs.net/links/2010itrs/home2010.htm>
- [2]. ULSI Devices, C.Y. Chang and M. Sze, John Wiley & Sons, 2000.
- [3]. D. Leonelli, et. al. “Optimization of Tunnel FETs: Impact of Gate Oxide Thickness, Implantation and Annealing Conditions”, ESSDERC Proceedings 2010
- [4]. K. Boucart, et. al. “A Simulation-based Study of Sensitivity to Parameter Fluctuations of Silicon Tunnel FETs”, ESSDERC Proceedings 2010
- [5]. H. Virani, et. al. “Impact of electron velocity on the ION of n-TFETs”, ESSDERC Proceedings 2010
- [6]. H. Virani, et. al. “Impact of electron velocity on the ION of n-TFETs”, ESSDERC Proceedings 2010
- [7]. L. Lattanzio, et. al. “Abrupt Switch based on Internally Combined Band-To-Band and Barrier Tunneling Mechanisms”, ESSDERC Proceedings 2010
- [8]. C. W. Yeung, et. al. “Programming Characteristics of the Steep Turn-on/off Feedback FET (FBFET)“, VLSI Proceedings 2009
- [9]. M. Luisier, et. al.” Performance Comparisons of Tunneling Field-Effect Transistors made of InSb, Carbon, and GaSb-InAs Broken Gap Heterostructures”, IEDM Proceedings 2009
- [10]. S. H. Kim, et. al.“ Germanium-Source Tunnel Field Effect Transistors with Record High ION/Ioff“, VLSI Proceedings 2009
- [11]. C. Hu, et. al. “Prospect of Tunneling Green Transistor for 0.1V CMOS”, IEDM Proceedings 2010
- [12]. Ram Asra, et. al. “A Binary Tunnel Field Effect Transistor with a Steep Sub-threshold Swing and Increased ON Current”, Japanese Journal of Applied Physics 49 (2010)