STEEPER

Steep Subthreshold Slope Switches for Energy Efficient Electronics

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Authors: WG

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[1] R = Report, P = Prototype, D = Demonstrator, O = Other

[2] PU = Public, PP = Restricted to other programme participants (including the Commission Services, RE = Restricted to a group specified by the consortium (including the Commission Services), CO = Confidential, only for the members of the consortium (including the Commission Services)

Revision history

Version	Date	Author	Comment
0.1	June 7 2012	W.G.	First issue
1	25June 2012	Adrian Ioescu	Approval without changes

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Executive summary

1st Steeper workshop "Simulation and Characterization of Steep-Slope Switches (SSS)" was organized as an integral part of the SISPAD Conference in Bologna, 9th September 2010. The workshop programme was scientifically coordinated by Professors Adrian M. Ionescu (Ecole Polytechnique Fédérale de Lausanne - EPFL) and Giorgio Baccarani (University of Bologna). Local organization and support was provided by Karin Jaymes (EPFL) and Rita Mambelli (ARCES, Bologna).

The workshop's goal was to generally introduce the FP7 Steeper Project, its technology, modeling and design goals and objectives but also increase public awareness of selected research topics related to the energy efficient and low voltage operation of advanced nanoelectronic circuits in the sub-0.5V regime. The Steeper Consortium members and the invited speakers have shared their experience discussing the technology impact of advanced tunnel FETs, planar and nanowire Si-TFETs as well as III-V heterojunction tunnel FETs; novel concepts for steep slope switches and sub-60mv/decade junction-less transistors; modeling and simulation challenges in tunnel FETs including its atomistic level simulation.

Workshop programme

The 1st Steeper workshop "Simulation and Characterization of Steep-Slope Switches (SSS)" was organized as an integral part of the SISPAD Conference in Bologna, 9th September 2010 with the following programme [1]:

Time	Topic/Speaker
08:15	Registration
08.30	Introduction: Welcome and general information on FP7 STEEPER initiative in Europe Adrian M. Ionescu (EPFL).
09:00	Tunnel FETs: impact of the fabrication process on the electrical performances (Keynote) Cyrille Le Royer (CEA LETI – MINATEC)
09:40	Planar and Nanowire Si-TFETs Qing-Tai Zhao, Siegfried Mantl (Forschungszentrum – Juelich)
10.00	Coffee break
10.40	Novel concepts for steep slope switches (Keynote) Sayeef Salahuddin (University of California at Berkeley)
11:20	Sub-60mv/decade switching in junction-less transistors Nima Dehdashti Akhavan, Jean-Pierre Colinge (Tyndall National Institute)
11:40	Steep-slope nanowire FETs: from concept to design Elena Gnani, Giorgio Baccarani (University of Bologna)
12.00	Buffet Lunch
13.30	Atomistic Simulation of TFETs: from Coherent to Phonon-Assisted Tunneling (Keynote) Mathieu Luisier (Purdue University)
14:10	Simulation challenges in tunnel FETs Pierpaolo Palestri (Univ. of Udine)
14:30	Modeling negative capacitance field effect transistor David Jiménez (Universitat Autònoma de Barcelona, Spain)
14.50	Coffee break
15.10	Nanowire tunnel FETs in silicon and III-V material systems (Keynote) H. Riel (IBM Research GmbH, Zurich Research Laboratory)
15:50	III-V heterojunction tunnel FETs Joachim Knoch (TU Dortmund)
16:10	Abrupt Hybrid Switches Using Internally Combined Band-To-Band and Barrier Tunneling Mechanisms Livio Lattanzio (EPFL)
16:30	Role of the transport in the channel for Ion optimization in Tunnel FETs David Esseni (University of Udine)
16.50	Close

Conclusion

The 1st Steeper workshop "Simulation and Characterization of Steep-Slope Switches (SSS)" goal was to generally introduce the FP7 Steeper Project, its technology, modeling and design goals and objectives but also increase public awareness of selected research topics related to the energy efficient and low voltage operation of advanced nanoelectronic circuits in the sub-0.5V regime. The Steeper Consortium members and the invited speakers have shared their experience discussing the technology impact of advanced tunnel FETs, planar and nanowire Si-TFETs as well as III-V heterojunction tunnel FETs; novel concepts for steep slope switches and sub-60mv/decade junction-less transistors; modeling and simulation challenges in tunnel FETs including its atomistic level simulation.

References

[1]. 1st STEEPR WORKSHOP Simulation and Characterization of Steep-Slope Switches (SSS) Bologna, 9th September 2010;
on-line proceedings http://sispad2010.arces.unibo.it/workshop-2