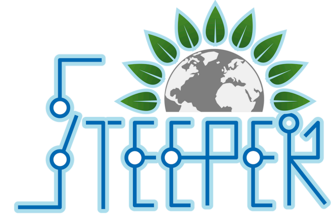

STEEPER

Steep Subthreshold Slope Switches for Energy Efficient Electronics

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Executive summary

The present deliverable report describes and evaluates ways of enhancing tunnel FET performance through engineering the injecting source contact. Since doping a nanostructure becomes increasingly difficult, we investigate the use of electrostatic doping to realize an n-i-p device structure. Two possible cases, first with gate underlap and second with a self-aligned process are investigated. If extremely thin source/drain gates can be manufactured and if an underlap in the range of a few nanometers only can be realized a device structure with gate underlap performs better than a self-aligned device structures. Further simulations, in particular with respect to a slightly modified device design that combines underlap and self-aligned design, are currently in progress. Together with our experimental investigations this will allow exploring the full potential of electrostatic doping for the optimization of TFETs.

Optimization of TFET Performance

TFETs are gated n-i-p structures with a degenerately n(p)-doped source contact, a gated intrinsic channel area and a p(n)-doped drain contact as illustrated in Fig. 1 (a). The conduction and valence

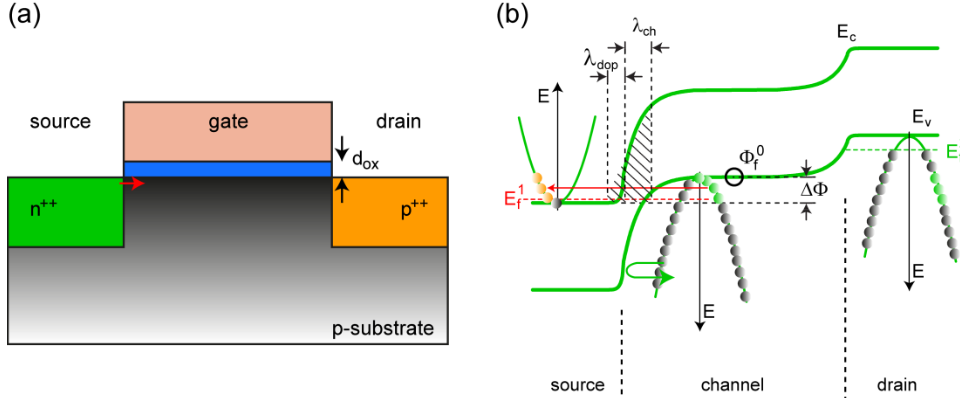

Fig. 1. (a) Device structure of a TFET. (b) Conduction and valence bands in a TFET in the device's on-state. Plotted are also the dispersion relations showing the carriers that contribute to the on-current within the energetic window $\Delta\Phi$.

bands along current transport direction in a TFET are shown in Fig. 1 (b) in the device's on-state. A drain current flows due to band-to-band tunneling (BTBT) once the valence band in the channel is moved above the conduction band in source. The current consists of electrons that tunnel from the valence band in the channel into the source contact where they find empty states in the conduction band and get thermalized. In order to understand the working principle of TFETs in more it is instructive to calculate the current through the device analytically. Approximating the source-side n-p-junction with a triangular-shaped potential barrier (as illustrated by the hatched area in Fig. 1 (b)) the WKB approximation can be used to calculate the transmission probability according to [1]

$$T_{\mathrm{WKB}} = \exp\left(-\frac{4\sqrt{2m^*}E_{\mathrm{g}}^{3/2}}{3h(eF)} \right). \qquad (1)$$

Here, F is the electric field across the n-p junction and m^* is the effective mass. The spatial extent of the junction is given by the sum of the screening lengths in the source contact due to the doping concentration λ_{dop} and the effective screening length within the channel λ_{ch} that depends on the channel layer thickness d_{ch}, the gate oxide thickness d_{ox}, the dielectric constants of channel and gate dielectric and the structure of the device. Since the electric field can be approximated as $qF \approx (E_{\mathrm{g}} + \Delta\Phi)/(\lambda_{\mathrm{dop}} + \lambda_{\mathrm{ch}}) = (E_{\mathrm{g}} + \Phi_{\mathrm{f}}^0)/(\lambda_{\mathrm{dop}} + \lambda_{\mathrm{ch}})$ [2] a small screening length in the channel as well as in the contacts is mandatory in order to obtain high band-to-band tunnelling probabilities. A small λ_{ch} is realized best in a device consisting of a nanowire with very thin diameter in a wrap-gate configuration with a high-k gate dielectric because $\lambda_{ch} = \sqrt{\varepsilon_{ch}/\varepsilon_{ox} \cdot d_{ch}^2 / 8\ln(1+2d_{ox}/d_{ch})}$. Since employing a thin nanowire with wrap-gate and high-k gate dielectric is necessary in order to suppress short channel effects in ultimately scaled devices there is no extra effort needed in a TFET. However, making λ_{dop} small involves much greater effort. The reason for this is the particular conduction/valence band profile in a TFET. In contrast to a conventional MOSFET, switching a TFET on yields an increase of the source depletion region which in turn results in a limited band-to-band tunnel probability since the tunnelling distance hardly gets smaller with increasing gate voltage (see Fig. 2 (a)). Therefore, the gate action on the source contact needs to be screened very well in a TFET. This screening is usually done by increasing the doping concentration of the source

contact. This scenario is shown in Fig. 2 (a) and (b) where conduction/valence bands in a TFET are shown for two different gate voltages in the case of low doping (a) and high doping concentration (b). However, a high doping concentration in the source contact is problematic.

First, increasing the doping concentration implies an increase in Fermi energy. This is particularly true for III-V semiconductors due to the low density of states in these materials. III-Vs on the other hand exhibit a number of desirable properties for TFETs such as low effective mass, a direct band gap that can be tuned with composition and the possibility of realizing heterojunction TFETs with a type II heterointerface. A large Fermi energy on the other hand yields a TFET that shows a switching behaviour that is at best around 60mV/dec [3,4]. The reason for this is shown in Fig. 2 (b): Current through a TFET flows when the valence band in the channel is shifted energetically above the conduction band in source (in case of a p-type TFET as considered here). However, on the case of a large Fermi energy carriers are injected from the Boltzmann part of the source Fermifunction leading to an inverse subthreshold slope of at best 60mV/dec. The optimum position of the Fermi energy is therefore close to the conduction band which yields a significantly reduced screening ability as discussed above (cf. Fig. 2 (a)).

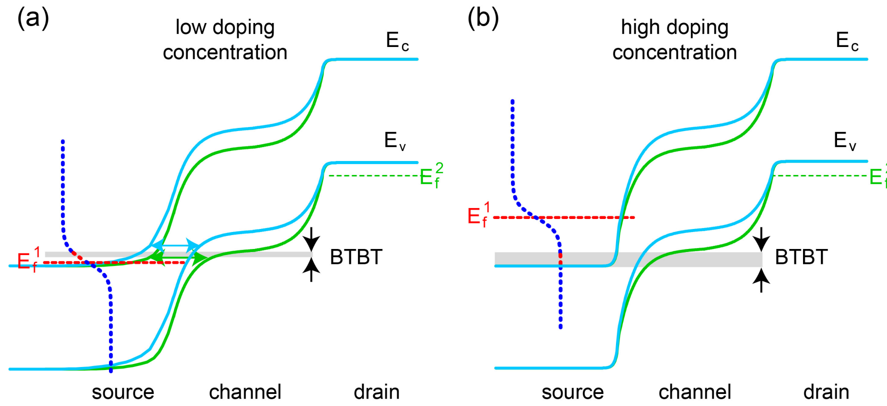

Fig. 2. Conduction/valence band profile along the direction of current transport in the case of a low source doping concentration (a) and a high doping concentration (b) [3,4].

Second, dopants in a nanostructure get deactivated as the size of the semiconducting nanostructure is scaled down. This deactivation was shown by measuring the specific resistivity of in-situ doped VLS-grown silicon nanowires (see Fig. 3 (a)) [5]. In order to exclude the impact of the surface states, the density of surface states was estimated and a depletion region due to charges in these surface states was substracted from the physical radius. Then plotting the resistivity as a function of the electronic radius r_{elec} (where πr_{elec}^2 is the area through which current flows) as is shown in Fig. 3 (b), one obtains a strong increase of as r_{elec} is scaled down due to the deactivation of dopants. It is therefore difficult to obtain a sufficiently high doping concentration providing the necessary screening in a TFET based on a nanowire with thin diameter.

Due to the reasons discussed above we study the use of electrostatic doping, i.e. using two or three individual gates in order to realize the n-i-p structure of the TFET. The major advantage of this is that a small screening length can be obtained in the same fashion as in the channel, i.e. by using a wrap-gate with a thin, high-k gate dielectric and at the same time the Fermi energy can be small since the screening is provided by the additional source gate electrode. However, the two gate electrode in source and channel need to be very close to each other in order to avoid any gate underlap that would decrease the achievable electric fields at the source channel interface and hence would limit the band-to-band tunnelling probability. Therefore, a self-aligned process needs to be

employed to accomplish this. On the other hand, bringing the source and channel gates close to each other will increase the parasitic capacitance and hence will limit the gate delay $\tau = C_g V_{dd} / I_d$. We therefore performed simulations of nanowire TFETs with different gate configurations in order to find the optimum device layout for TFETs with electrostatic doping.

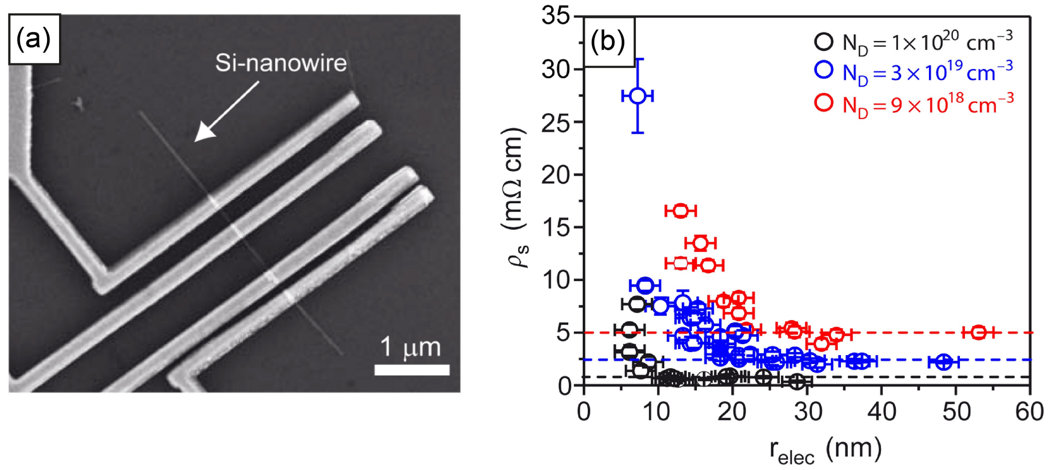

Fig. 3. (a) Scanning electron micrograph of an in-situ doped VLS grown silicon nanowire. (b) Specific resistivity as a function of electronic radius of the nanowire [5].

Electrostatic Doping in Nanowire TFETs

Device Structure and Simulations

For the following investigations we consider a device structure consisting of a nanowire bundle as schematically shown in Fig. 4. Each individual nanowire is surrounded by six adjacent nanowires such that a single nanowire device can be considered as being of cylindrical shape and with zero electric field in the source and drain regions due to symmetry reasons. A major benefit of the nanowire bundle device configuration is that the parasitic source/drain capacitances can be decreased by bringing the nanowires closer to each other, i.e. by scaling down d_{dev}. (cf. Fig. 4). In order to keep the computational burden as small as possible we will exclusively consider a single, cylindrical TFET.

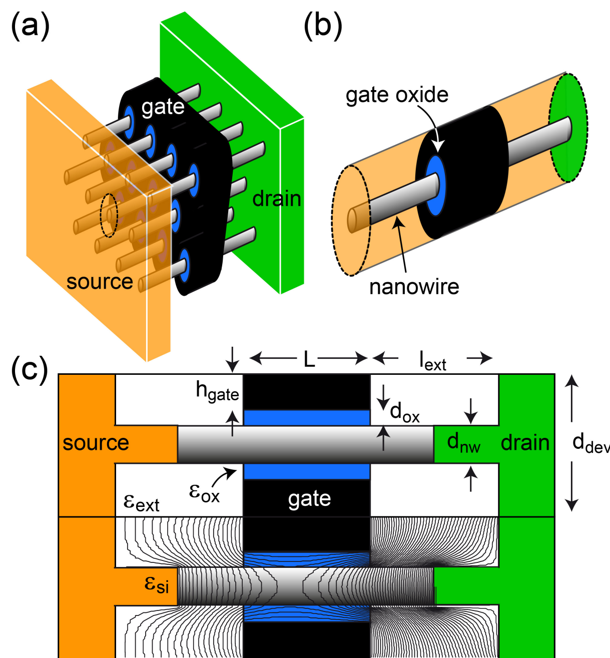

Fig. 4. Nanowire FET bundle. Each individual device is surrounded by six adjacent devices such that each transistor can be approximated with a cylindrically shaped nanowire device.

Our simulations are based on a self-consistent solution of the Schrödinger and Poisson equation using the non-equilibrium Green's function formalism on a finite difference grid [6]. While a one-dimensional approximation is made for the quantum transport equations, the electrostatics is solved in cylindrical coordinates in order to properly take parasitic source and drain capacitances into account.

For our investigation regarding electrostatic doping we consider two different device configurations: 1) an intrinsic nanowire is surrounded by a thin gate dielectric throughout its entire length. Three individual gates are then placed along the nanowire as illustrated in Fig. 5 (a). The three gates have to be placed apart from each other in order to avoid short circuits and to allow manufacturing such a device. Alternatively, we consider the device depicted in 5 (b): A thin metal layer such as aluminium is deposited on top of a thin SiO2. Subsequently, the metal layer is oxidized thereby creating a source and drain gate. The oxidized metal then serves as a high-k gate dielectric. We are currently working on an experimental realization of such a self-aligned method to create three individual gates. In the following the two device structures are referred to as "underlap-structure" for the device shown in Fig. 5 (a) and "self-aligned structure" for the TFET depicted in Fig 5 (b).

In all simulations we consider an InAs nanowire with a diameter d_{nw}=10nm; the total diameter of the device is $d_{dev} = 34nm$ in all cases. Due to quantization, the effective band gap is taken to be 0.6eB and the effective electron and hole masses are taken to be $0.04m_0$ and $0.41m_0$, respectively [7,8]. In order to compare the different devices with each other and to qualify the various geometries, we use the gate delay $\tau = C_g V_{dd} / I_d$, the I_{on}/I_{off} –ratio and the dynamic power consumption $P \propto C_g V_{dd}^2$ as relevant figures of merit. In order to calculate the gate delay we use for the total gate capacitance C_g the charge control capacitance, i.e. $\left(Q(V_g = V_{off} + V_{dd}, V_{ds} = 0) - Q(V_g = V_{off}, V_{ds} = V_{dd})\right)/V_{dd}$ and the effective current $\left(I_d(V_g = V_{off} + V_{dd}, V_{ds} = V_{dd}/2) + I_d(V_g = V_{off} + V_{dd}/2, V_{ds} = V_{dd})\right)/2$ as proposed in Ref. [9]. Note, that a fixed off-state current level of $I_{off} = 10^{-10} A$ was used in order to determine the gate voltage V_{off}; the supply voltage was set to $V_{dd} = 0.3V$.

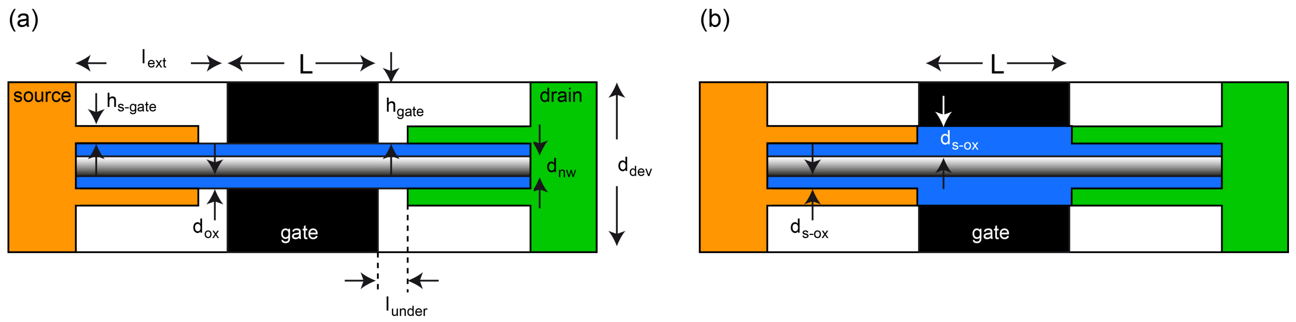

Fig. 5. Device structures under consideration. (a) shows the "underlap structure" where three individual gates are placed along the nanowires device. (b) shows a "self-aligned" TFET where the source drain metal gate is transferred into a gate insulator.

Investigations of the underlap-structure

For the investigation of the underlap structure we simulate the electrical characteristics of a TFET with L=25nm, $l_{ext} = 25nm$, $h_{s-gate} = 5nm$, $d_{ox} = 1nm$ and various gate underlaps l_{under}. Figure 6 shows the on/off-ratio and on-current (a), transfer characteristics (b), gate delay (c), the energy needed for switching (d) and the total capacitance (e). Obviously, the on-current, on/off ratio and gate delay improve as the gate underlap is decreased. A minimum in gate delay is found around an underlap (i.e. $l_{ext} - l_{under}$) of 2nm. The reason for the minimum is that the smaller the underlap, the higher the on-current due to an improved screening and thus due to an increased band-to-band tunnel probability (see band profiles in the inset of Fig. 5 (b)). However, for very small underlaps the parasitic capacitance dominates and the gate delay increases again. With increasing thickness of the source/drain gates h_{s-gate} the magnitude of the parasitic capacitance also increases. At the same time, the point of minimum gate delay will be shifted towards larger gate underlaps, i.e. the minimum achievable gate delays will be determined by the ability to fabricate source/drain side gates that are as thin as possible.

Investigations of the self-aligned structure

Simulations of self-aligned TFET device were also performed. Since in the self-aligned device structure a metallic electrode is deposited on a thin gate dielectric and subsequently oxidized the actual gate dielectric consists of the SiO2 and the metal oxide and thus is thicker than the source/drain-gate dielectric and also thicker than in the underlap device design. Therefore, a very

thin source/drain gate of $h_{s-gate} = 2nm$ was chosen in order to guarantee a good gate control of the actual channel and to avoid short channel effects.

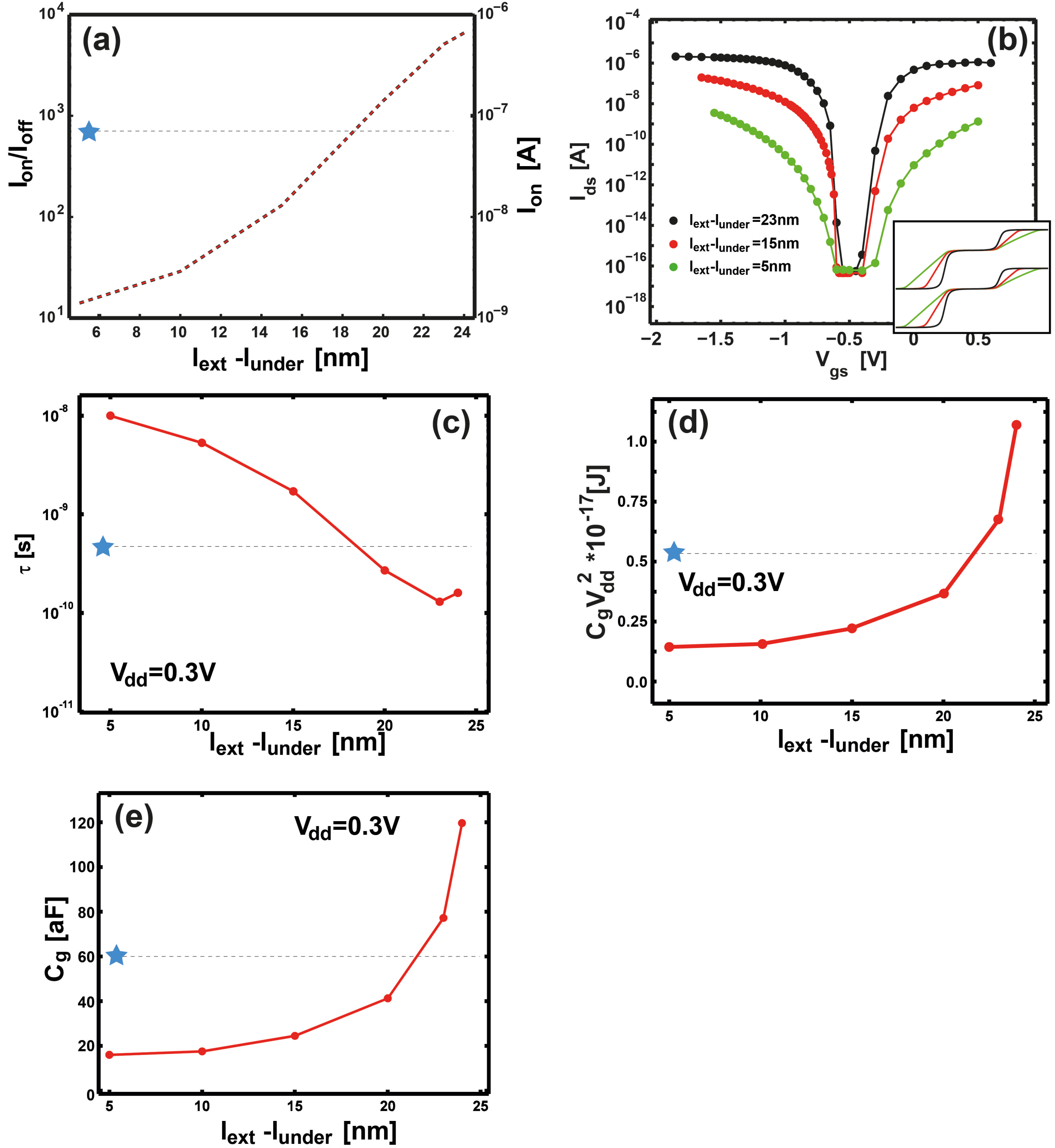

Fig 6. On-off ratio and on-current (a), transfer characteristics (b), gate delay (c), switching energy (d) and total capacitance as a function of gate underlap in an underlap device structure. The blue stars are values extracted from simulating the self-aligned device structure.

The results of this simulation are plotted in Fig. 6 as well (blue stars). Note that the structure is self-aligned and hence there is no gate underlap to be considered here. So the data point should in principle be placed at $l_{ext} - l_{under} = 0nm$. Obviously, the self-aligned structure outperforms the underlap device in the case of larger gate underlaps since the on-current is larger. However, for very small underlaps the performance of the underlap device becomes higher than the self-aligned TFET

since in this case screening in the channel and the source/drain areas of the underlap device is accomplished with a significantly thinner gate dielectric in the channel area. Again, the ability to realize a TFET with appropriate performance depends predominantly on the thickness of the source/drain gate electrodes h_{s-gate}. Further simulations are currently being performed in order to find out the optimum device design rules.

Conclusion

Proper functionality of TFETs with optimized on-currents requires appropriate screening of the gate action on the source contact. This is usually realized with a high doping concentration in the source contact. However, in order to obtain an inverse subthreshold slope steeper than 60mV/dec it is necessary that the Fermi energy is rather small. Particularly in materials such as III-V compound semiconductors with low density of states the trade-off between on- and off-state cannot be resolved. Therefore we investigated electrostatic doping as an alternative to doping where individual gates are employed to create the n-i-p structure of a TFET. Two different device designs were studied here: i) a device structure exhibiting a gate underlap in order to ensure an isulation between adjacent source/drain and channel-gates and ii) a self-aligned TFET structure. The two device designs were compared with each other employing the gate delay and on/off-ratio as the relevant figures of merit.

The advantage of the self-aligned structure is the absence of any gate underlap, however, at the price of a thicker gate insulator that limits the achievable on-current levels. Therefore, the source/drain gate metallization needs to be extremely thin since the oxidized metal will contribute to the channel gate dielectric's thickness. TFETs based on the underlap design show potentially a better performance compared to the self-aligned design. However, in order to realize this better performance, the gate underlap needs to be on the order of a few nanometers only. Further simulations, in particular with respect to a slightly modified device design that combines underlap and self-aligned design, are currently in progress. Together with our experimental investigations this will allow exploring the full potential of electrostatic doping for the optimization of TFETs.

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