# STEEPER

## Steep Subthreshold Slope Switches for Energy Efficient Electronics

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**Authors:** Wladek Grabinski, K. Leufgen, P. Ulrich based on the input of all partners

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[1] R = Report, P = Prototype, D = Demonstrator, O = Other

[2] PU = Public, PP = Restricted to other programme participants (including the Commission Services, RE = Restricted to a group specified by the consortium (including the Commission Services), CO = Confidential, only for the members of the consortium (including the Commission Services)

# Revision history

| Version | Date | Author | Comment |
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| 0.1 | 01.09.11 | Wladek Grabinski | First issue |
| 0.2 | April 2012 | Wladek Grabinski | Main revision based on partner input |
| 1 | May 2012 | P. Ulrich, K. Leufgen | Completion and formal aspects |
| 1 | June 2012 | A. Ionescu | Approval without changes |

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# 1 Executive summary

This report describes the status of the STEEPER dissemination and exploitation activities. It is a living document, which is continuously updated and the present deliverable is a snapshot at M24. Most of the dissemination activities during this first reporting period of the project have been oriented towards the setting up of tools, technology frameworks and structures that mainly help the internal circulation of information and provide the basis for the external circulation. As a first concrete achievement the project website was operational meeting its milestone. It is the main action to show publicly the objectives and organization of the project, the main project contacts and a continuous indication of activities, links, and results allowing the general public to gather information about our project. The web page also comprises a private place for the dissemination and exchange of documents, drafts, presentations, progress reports and ideas within the project. The consortium is being active, also, in the presentation of early research results and objectives of the project in various venues. An ad-hoc advertising poster and leaflet to facilitate the dissemination during public events have been published.

# 2 Introduction

The respective contributions have been regrouped under the following activities: general dissemination activities, specific dissemination activities, dissemination and use plan activities, organizational issues and preparation of next period events.

## 2.1 Scope of this document

Dissemination activities for STEEPER are performed in Task 6.1 (Dissemination and networking), use and exploitation activities are performed in Task 6.2 (Exploitation) and joint collaborative actions with similar FP7 projects in Task 6.3 (Training). The three tasks are scheduled to run for the whole duration of the project. The present deliverable is the first product of the project's dissemination activities and plan for the next phases of the project. This document covers all dissemination activities that were completed during the two first reporting periods (M1-M12, M13-24) and planned for the final one.

## 2.2 Related documents

Deliverable D6.1 "STEEPER website" was published (M4) in relation with its detailed description, use and characteristics. For details on this website, please refer to D6.1 and the continously updated site at www.steeper-project.org.

# 3 General dissemination activities

The STEEPER project Consortium distinguishes between internal and external dissemination actions, based on different channels adopted to distribute the knowledge created in the project. Each partner of the consortium will carry out, throughout the duration of the project, both individually and in cooperation with other partners, the dissemination actions for various purposes and different audiences.

## 3.1 Internal dissemination and use

This includes all the actions aiming at ensuring a good diffusion of information and documentation

among the project partners in order to increase the awareness. The internal dissemination has been achieved through the following channels: Private project website: the private website has been set up and is used to ensure for all the partners access to proper information and project progress. It is used as a database and collection for all the reports regularly generated by each work package team as well as general project information, including all the presentations and seminars worked by the Project Technical Committee and Project Management Boards. Access is restricted to partners of the Consortium and the EC and it is protected by user authentication. The internal website is regularly updated with all the information developed during the whole project.

Internal meetings and workshops: Two types of internal meetings and workshops are used in the development of the project: conference calls and face-to-face meetings. The meetings can also be classified as regular or specific. As stated in the Consortium Agreement document the regular meetings are the ones for the Project Steering Board (PSB), face to face, one every semester and the ones for the consortium conferences calls, organized quarterly. Both PMB and PTC may meet at any time; in fact this has been the case for the consortium several times so far. Industrial partners are working on the dissemination and use activities by involving their internal product groups and R&D teams.

Academic partners are working on the dissemination activities organizing internal seminars to train and attract PhD students in their respective locations.

## 3.2 External dissemination and use

External dissemination includes actions aiming at ensuring the visibility and awareness of the project and the results outside the Consortium. These actions are concentrated on the scientific community. During the development of the project we will also focus on organizations and companies. The main channels employed to ensure these dissemination goals are:

- Public project website, the STEEPER public web (http://www.steeper-project.eu) presents to the general public the objectives of the work, the organization, the partners composition, the internal and external events, and the scientific publications.
- First press release by IBM
  - http://www-03.ibm.com/press/us/en/pressrelease/32877.wss
- Related STEEPER project video is available on YouTube
  - http://youtu.be/7h9TGRrfZnY
- Additional photos on Flickr
  - http://www.flickr.com/photos/ibm_research_zurich/sets/72157625119452303/

Publication of research results is one of the key objectives of the STEEPER project. Papers will be submitted to competitive conferences relevant for the topic of the project all in an international framework.

Workshops and training courses, project partners plan to actively participate in workshops and training courses as a key way to disseminate and use the results of the project in the widest research community. These actions are concentrated on the beginning of the third year that will be a proper time to show the global project results of the STEEPER collaborative project.

**Table:** List of all dissemination activities (publications, conferences, workshops, web sites/applications, press releases, flyers, articles published in the popular press, videos, media briefings, presentations, exhibitions, thesis, interviews, films, TV clips, posters).

| LIST OF DISSEMINATION ACTIVITIES | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **NO.** | **Type of activities[3]** | **Main leader** | **Title** | **Date** | **Place** | **Type of audience[4]** | **Size of audience** | **Countries addressed** |
| 1 | Press release | IBM | First press release | | On-line | Medias | Open | EU |
| 2 | Films, TV clips | IBM | STEEPER project video | | On-line | Medias | Open | EU |
| 3 | Photos | IBM | STEEPER photos on Flickr | | On-line | Media | Open | EU |
| 4 | Workshop | EPFL | 1st workshop | Sept. 9, 2010 | Bologna | Scientific Community | Open | EU |
| 5 | Website | SCIPROM | STEEPER Website | 10Dec 2010 | Online | Scientific Comunity, Civil Society, Policy Makers, Media | Open | EU |

[3] A drop down list allows choosing the dissemination activity: publications, conferences, workshops, web, press releases, flyers, articles published in the popular press, videos, media briefings, presentations, exhibitions, thesis, interviews, films, TV clips, posters, Other.

[4] A drop down list allows choosing the type of public: Scientific Community (higher education, Research), Industry, Civil Society, Policy makers, Medias ('multiple choices' is possible).

## Significant publications and presentations

The project members have contributed to number of the journal articles, conference talks and posters presenting significant project results:

[1] L. Lattanzio, L. De Michielis and A. M. Ionescu, "Electron-Hole Bilayer Tunnel FET for Steep Subthreshold Swing and Improved ON Current", ESSDERC 2011.
[2] L. De Michielis, L. Lattanzio, P. Palestri, L. Selmi, A. M. Ionescu, "Tunnel-FET Architecture with Improved Performance due to Enhanced Gate Modulation of the Tunneling Barrier", DRC 2011 proceedings, pag 111-112;
[3] De Michielis, L., Iellina, M., Palestri, P., Ionescu, A.M., Selmi, L., "Tunneling path impact on semi-classical numerical simulations of TFET devices", 2011 12th International Conference on Ultimate Integration on Silicon, ULIS 2011, art. no. 5758002, pp. 146-149
[4] De Michielis, L., Iellina, M., Palestri, P., Ionescu, A.M., Selmi, L., "Effect of the Choice of the Tunneling Path on Semi-classical Numerical Simulations of TFET devices", S-State Electronics Journal.
[5] M. Schmidt, R. A. Minamisawa, S Richter, J.-M. Hartmann, R. Luptak, A. Tiedemann, D. Buca, Q. T. Zhao, S. Mantl "Impact of strain and Ge concentration on the performance of planar SiGe band- to-band-tunneling transistors" Proc. 2011 12th International Conference on Ultimate Integration on Silicon (ULIS), pp. 202-205, 2011
[6] Q. T. Zhao, C. Sandow, M. Schmidt, S. Richter, S.Mantl "Planar and Nanowire Si-TFETs" Workshop on Simulation and Characterization of Steep-Slope Switches, Bologna, Italy, 09.09.2010
[7] Q. T. Zhao, C. Sandow, M. Schmidt, S. Richter, S.Mantl (invited) "Silicon and Strained Silicon Planar and Nanowire Tunnel FETs" China Semiconductor Technology International Conference, Shanghai, China, March 13-14, 2011
[8] M. Schmidt, R. A. Minamisawa, S Richter, J.-M. Hartmann, R. Luptak, A. Tiedemann, D. Buca, Q. T. Zhao, S. Mantl "Impact of strain and Ge concentration on the performance of planar SiGe Band-to-band-tunneling transistors" 2011 12th International Conference on Ultimate Integration on Silicon (ULIS), Cork, Ireland, March 14-16, 2011
[9] S. Mantl (invited) "Concepts for energy efficient transistors" Workshop on Nanotechnology, Nanomaterials and Nanoreliability, Chemnitz, Germany, May 24, 2011
[10] E. Gnani, S. Reggiani, A. Gnudi and G. Baccarani, "Superlattice-Based Steep-Slope Switch", Proc. of the IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2010.
[11] E. Gnani, S. Reggiani, A. Gnudi and G. Baccarani, "Steep-slope nanowire FET with a superlattice in the source extension", Proc. of the European Solid-State Device Research Conference (ESSDERC), p. 380, 2010.
[12] E. Gnani, S. Reggiani, A. Gnudi and G. Baccarani, "Steep-slope nanowire field-effect transistor (SS-NWFET)", Proc. of the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), p.69, 2010.
[13] E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi and G. Baccarani, "Investigation on Superlattice Heterostructures for Steep-Slope Nanowire FETs", Proc. of the Device Research Conference (DRC), 2011.
[14] E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi and G. Baccarani, "An Investigation on Steep-Slope and Low-Power Nanowire FETs", ESSDERC 2011 Conference.

[15] E. Gnani, S. Reggiani, A. Gnudi and G. Baccarani, "Steep-Slope Nanowire FET with a Superlattice in the Source Extension", Solid State Electronics.
[16] M. T. Björk, H. Schmid, C. D. Bessire, K. E. Moselund, H. Ghoneim, E. Lörtscher, S. Karg, H. Riel. Si–InAs heterojunction Esaki tunnel diodes with high current densities. Applied Physics Letters, Vol. 97, 163501, 2010.
[17] C. D. Bessire, M. T. Björk, H. Schmid, A. Schenk, K. B. Reuter, and H. Riel Trap-Assisted Tunneling in Si-InAs Nanowire Heterojunction Tunnel Diodes. submitted.
[18] H. Schmid, K. E. Moselund, M. T. Björk, M. Richter, H. Ghoneim, C. D. Bessire and H. Riel. Fabrication of Vertical InAs-Si Heterojunction Tunnel Field Effect Transistors. 69th Device Research Conference Digest, 2011.
[19] P. Mensch, K. E. Moselund, S. Karg, E. Lörtscher, M. T. Björk, H. Schmid and H. Riel. C-V Measurements of Single Vertical Nanowire Capacitors. 69th Device Research Conference Digest, 2011
[20] K. E. Moselund, M. T. Björk, H. Schmid, C. D. Bessire, H. Ghoneim, P. Mensch and H. Riel Nanowire Tunnel FETs - From All-Silicon Towards Heterostructures. Wilhelm and Else Heraeus Seminar on III-V Nanowires – Growth, Properties and Applications, Bad Honnef, February 2011
[21] H. Riel. Semiconductor Nanowires for Future Electronic Devices. Schottky Seminar, TU Munich, May 2011
[22] H. Riel. Towards Ultimate Scaling and Beyond – The Importance of Research. DPG Industrietag of the German Physical Soceity, Dresden, March 2011.
[23] G. Signorello, S. Karg, E. Lörtscher, M. Björk, H. Schmid, B. Gotsmann, K. Moselund, and H. Riel Uniaxial Strain in Core/Shell III-V Nanowires: Correlation to Electronic Properties. MRS Spring Meeting, San Francisco, 27th April 2011.
[24] K. E. Moselund, M. T. Björk , H. Schmid, C. D. Bessire, H. Ghoneim, S. Karg, E. Lörtscher, P. Mensch and H. Riel Bottom-up Nanowire Tunneling Devices: Towards III-V Tunnel FETs on Silicon MRS Spring Meeting, San Francisco, 27th April 2011.
[25] C. Bessire, M. Björk, H. Schmid, K. Moselund, H. Ghoneim, S. Karg, H. Riel Si-InAs Heterojunction Esaki Tunnel Diodes with High Current Densities. Annual Meeting of the German Physical Society, Dresden, March 2011
[26] H. Riel, "The Future of Nanolectronics" Update Nano 2011, Helsingborg, 22.05.2011.
[27] S. Karg, G. Signorello, E. Lörtscher, M. Björk, H. Schmid, B. Gotsmann, K. Moselund, and H. Riel Uniaxial Strain in Core/Shell III-V Nanowires: Correlation to Electronic Properties. e-MRS Meeting, Nizza, May 2011.
[28] M. T. Björk, H. Schmid, K. E. Moselund, C. Bessire, M. Naterra-Comte, H. Ghoneim, S. Karg, E. Lörtscher, H. Riel Nanowire Tunnel FETs - From All-Silicon towards Heterostructures. MRS Fall Meeting 2010, November, Boston, USA
[29] H. Riel Towards Ultimate Scaling – Semiconducting Nanowires Frontiers of the Nanoelectronics, München, 08.09.2010
[30] H. Riel Nanowire Field Effect Transistors – Where do they belong to? SINANO-NANOSIL Workshop Seville, 17.09.2010
[31] H. Riel, K. Moselund, M. Björk, H. Schmid, H. Ghoneim, C. Bessire, E. Lörtscher, S. Karg, W. Riess Tunnel Field Effect Transistors based on Grown Nanowires. SISPAD Workshop – Simulation and Characterization of Steep-Slope Switches, Bologna, 09.09.2010
[32] Heike Riel, K. Moselund, M. Bjoerk, H. Schmid, H. Ghoneim, E. Loertscher, S. Karg, W. Riess VLS-grown Silicon Nanowires – Growth, Doping, and Tunnel FETs. 2010 IEEE Silicon Nanoelectronics Workshop, Honolulu, 13.06.2010
[33] W. Riess, "The Future of Nanoelectronics":
[34] W. Riess, "The Future of Nanoelectronics": Albert-Ludwigs Universität Freiburg, Technische Fakultät, Fakultätskolloquium, July 15, 2010

[35] W. Riess, “The Future of Nanoelectronics”: 457. WE-Heraeus Seminar, Graphene Electronics – Material, Physics and Devices, August 15-18, 2010
[36] W. Riess, “The Future of Nanoelectronics”: Physikalisches Kolloquium, Univeristät Basel, September 24, 2010
[37] W. Riess, “The Future of Nanoelectronics”: EPFL Kolloquium, 8 March 2010
[38] W. Riess, “The Future of Nanoelectronics”: Physikalisches Kolloquium, Universität Regensburg, January 24, 2011
[39] W. Riess, “The Future of Nanoelectronics”: Swedish Foundation for Strategic Research, Lindholmen Science Park, Göteborg, Sweden, May 9, 10, 2011
[40] C. Bessire, M. T. Björk, H. Schmid, K. Moselund, H. Ghoneim, P. Mensch, H. Riel, Nanowire Heterostructure Tunnel Devices for Future Transistors, IBM Binnig and Rohrer, Nanotech Center opening, May 2011.
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[42] Ph. Mensch, K. Moselund, S. Karg, M. Björk, H. Schmid, E. Lörtscher, and H. Riel. Capacitance Measurements of Vertical Wrapped-Gate Nanowire MOS Capacitors. Wilhelm and Else Heraeus Seminar on III-V Nanowires – Growth, Properties and Applications, Bad Honnef, February 2011.
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[44] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, “A Compact Capacitor-Less High-Speed DRAM Using Field Effect-Controlled Charge Regeneration”, IEEE Electron Device Letters, Vol 33, N° 2, February 2012, pp.179-182
[45] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, “Z2-FET: a steep switching device with gate-controlled hysteresis”, Proc. of the EuroSOI conference, 2012
[46] A. Villalon, C. Le Royer, M. Cassé, D. Cooper, B. Prévitali, C. Tabone, J.-M. Hartmann, P. Perreau, P. Rivallin, J.-F. Damlencourt, F. Allain, F. Andrieu, O. Weber, O. Faynot and T. Poiroux, “Strained Tunnel FETs with record Ion: First demonstration of ETSOI TFETs with SiGe channel and RSD”, 2012 SYMPOSIUM ON VLSI TECHNOLOGY (submitted)
[47] Pino D'Amico, Paolo Marconcini, Gianluca Fiori, Giuseppe Iannaccone "Interband tunneling in nanowires with diamond cubic or zincblende crystalline structure based on atomistic modeling" to submit to Appl. Phys. Lett.
[48] A. Revelant, P. Palestri and L. Selmi "Multi-Subband Semi-classical Simulation of n-type Tunnel-FETs" ULIS 2012
[49] E. Gnani, S. Reggiani, A. Gnudi, G. Baccarani, “Steep-Slope Nanowire FET with a Superlattice in the Source Extension”, Solid-State Electronics, vol. 65-66, pp. 108-113, November-December 2011.
[50] E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi, G. Baccarani, “Investigation on Superlattice Heterostructures for Steep-Slope Nanowire FETs”, Device Research Conference (DRC 2011), pp. 201-202, Santa Barbara CA, June 20-22, 2011.
[51] E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi and G. Baccarani, "An Investigation on Steep-Slope and Low-Power Nanowire FETs”,Proceedings of the European Solid-State Device Research Conference (ESSDERC), pp. 299-302, Helsinki, 13-15 September 2011.
[52] E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi, G. Baccarani, “Performance Limits of Superlattice-Based Steep-Slope Nanowire FETs”, Proceedings of the International Electron Device Meeting (IEDM), pp. 5.1.1-5.1.4, Washington DC, 5-7 December, 2011.

[53] Q.T. Zhao, J. M. Hartmann and S. Mantl, “An Improved Si Tunnel Field Effect Transistor with a Buried Strained Si1-xGex Source”, IEEE Electron Device Lett. 32, pp.1480-1482, 2011

[54] Q. T. Zhao, W. J. Yu, B. Zhang, M. Schmidt, S. Richter, D. Buca, J.-M. Hartmann, R. Luptak, A. Fox, K. K. Bourdelle, S. Mantl, “Tunneling Field-Effect Transistor with a Strained Si Channel and a Si0.5Ge0.5 Source”, 2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC), pp. 251-253, 2011

[55] M. Schmidt, R. A. Minamisawa, S Richter, J.-M. Hartmann, R. Luptak, A. Tiedemann,D. Buca, Q. T. Zhao, S. Mantl “Impact of strain and Ge concentration on the performance of planar SiGe band-to-band-tunneling transistors” Proc. 12th International Conference on Ultimate Integration on Silicon (ULIS), pp.202-205, 2011

[56] Q. T. Zhao, C. Sandow, M. Schmidt, S. Richter and S.Mantl (invited talk ) “Planar and Nanowire Si-TFETs” China Semiconductor Technology International Conference (CSTIC), Shanghai, March 13-14, 2011

[57] H. Schmid, K.E. Moselund, M.T. Bjoerk, M. Richter, H. Ghoneim, C.D. Bessire, H. Riel, "Fabrication of Vertical InAs-Si Heterojunction Tunnel Field Effect Transistors", Proc. Device Research Conference "DRC," Santa Barbara, CA (IEEE, June 2011)

[58] K. E. Moselund, M. T. Björk, H. Schmid, H. Ghoneim, S. Karg, E. Lörtscher, W. Riess, H. Riel, “Silicon nanowire tunnel FETs: Low-temperature operation and influence of high-k gate dielectric”, TED 2011

[59] P. Mensch, K.E. Moselund, S. Karg, M.T. Bjoerk, H. Schmid, E. Loertscher, H. Riel, "C-V Measurements of Single Vertical NW Capacitors", Proc. Device Research Conference "DRC," Santa Barbara, CA (IEEE, June 2011)

[60] C. Bessire, M. T. Bjoerk, H. Schmid, A. Schenk, K. B. Reuter, H. Riel, “Trap assisted tunneling inn Si-InAs Nanowire Heterostructure Tunnel Diodes”, Nano Lett. 2011

## 3.3 The STEEPER Logo

A project logo draft has been proposed to all partners by EPFL. When finally validated this logo should represent the project identity at a glance. It shall be used in all project dissemination activities including the project website, presentation in internal meetings but also for valorisation of the project outside the consortium. It is also used in all project official documents, deliverables, milestones and reports. An official version of the logo is stored in the template section of the document repository on the project website. The STEEPER consortium makes use of a characteristic logo, which should help raise the recognition of the project by the public and academic community throughout the different dissemination activities. The logo was defined at the beginning of the project and is used by the consortium in all the internal or external communications. The STEEPER logo was proposed by the coordinating institution to the rest of the Consortium and accepted just at the beginning of the project.


**Figure 1.** STEEPER logo.

## 3.4 The STEEPER WEB Pages

The URL of the STEEPER project website is http://www.steeper-project.org/ and it has been online since June 2010. The website is hosted and maintained by SCIPROM, a private R&D management company. The layout of the page design was also defined by by SCIPROM, the project partner. The integrity of the project data is ensured by daily backups that are maintained on safety storage servers keeping information of the last 6 months, and a monthly backup for the last 12 months. A screenshot of the home page of the STEEPER web site is shown in Figure 2.

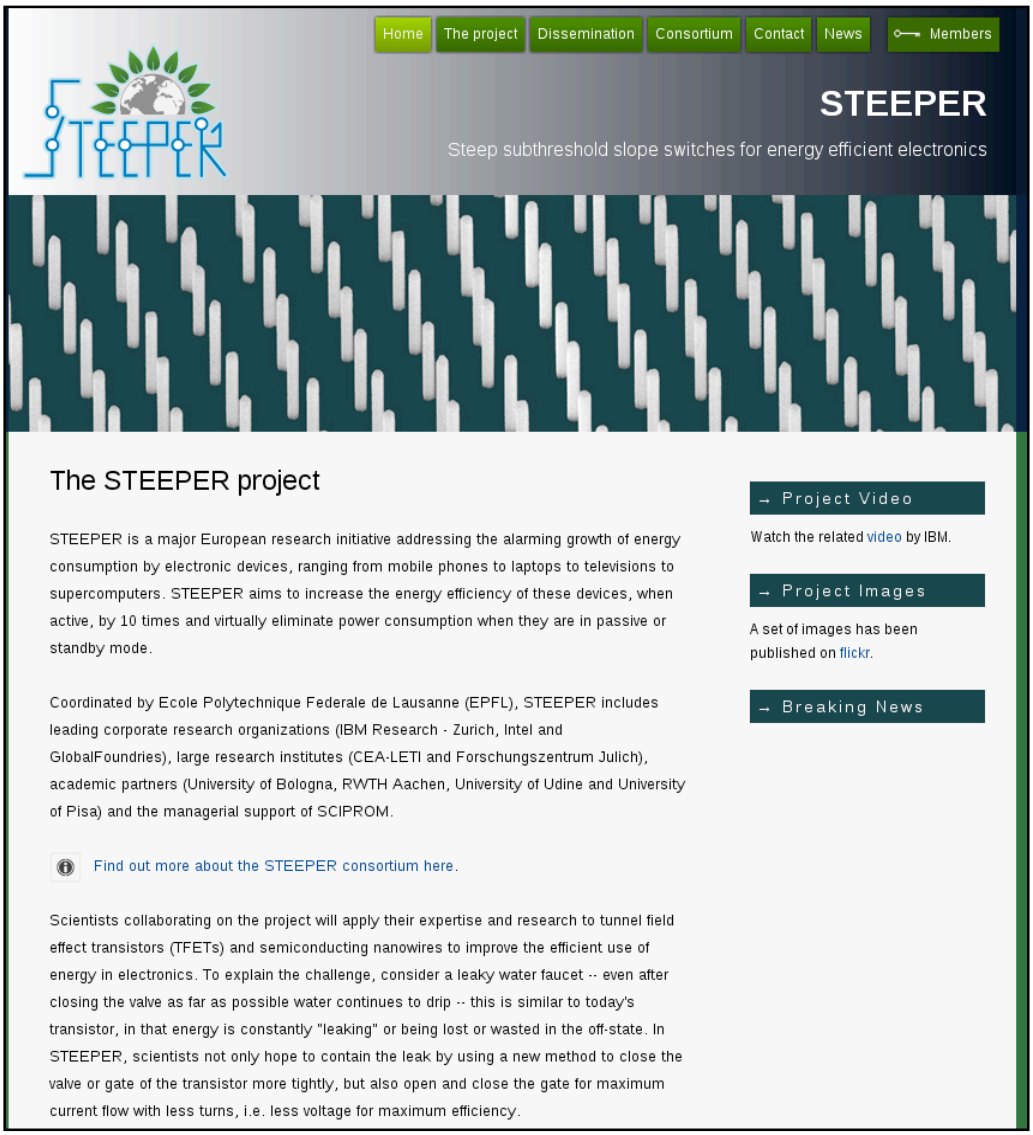


**Figure 2.** Screenshot of the home page of the STEEPER website.

The website is intended to provide a vision of the project to the general public. It is a key objective of WP6 on project dissemination. The site is continuously updated in order to give notice of the research publications of the Consortium as well as of the main activities of the project. The website includes a number of items of public information relevant for the project and useful for dissemination activities. The page also provides a private space reserved for the partners and the EC where the main documents of the project are stored as well as the collection of all presentations made during meetings. Access to the private page is restricted to partners of the Consortium and the EC and it is protected by user authentication.

## 3.5 Public site organization

The header of the STEEPER website is shown in Figure 3.

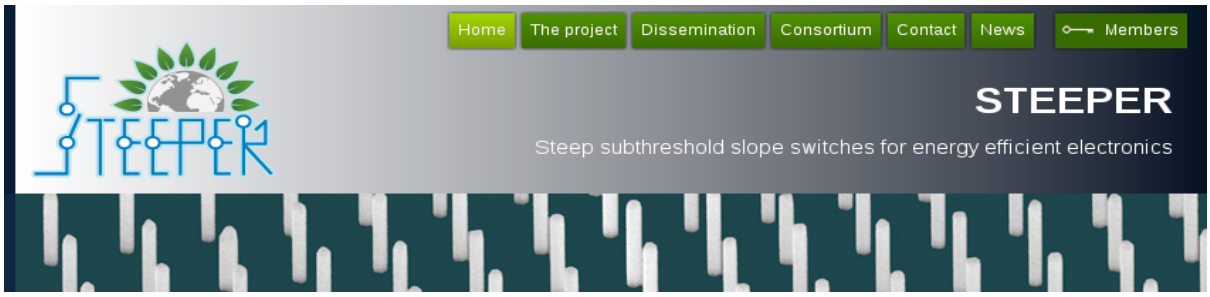


**Figure 3.** Header of the STEEPER public website

The website has the following main sections:

- Home/The Project: Objectives of the project, description of work foreseen, its structure in as stated in the Grant Agreement.
- Dissemination
- Consortium, description of the partner institutions, with contact details for the key people
- Contact, address and contact details for the coordinator and project administrative officer.
- Members: Private STEEPER project site

## 3.6 Private site organization

The private sitemap of the STEEPER website is shown in Figure 4. The website has the following main sections listed in Fig.4:

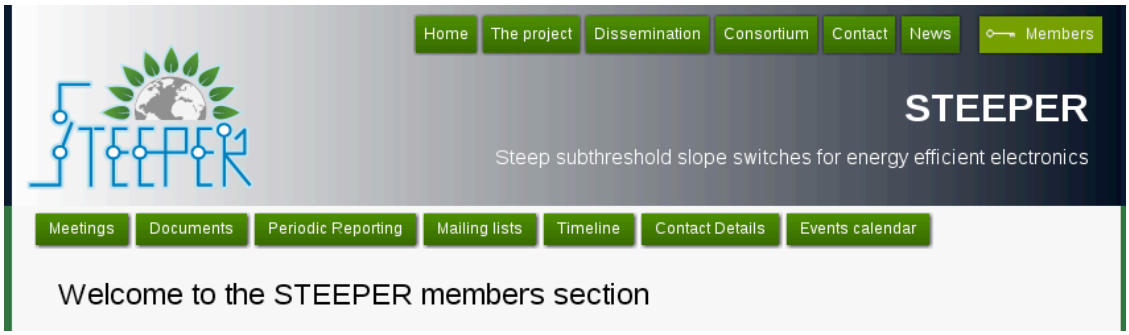


**Figure 4.** Header of the STEEPER private website

Planned actions, details about them as well as results. Internal documents by Workpackages (WP), this section is specific for each WP. The WP leader may use this space as shared storage and sharing place.
The reviewer area is reserved for the EC project officer and reviewers. It also stores all the deliverable documents in its most updated version. PMB and PTC meeting documents, collection of the documents for the project meetings including agendas, presentations (pdf, ppt) and conclusions.

## 3.7 Internal dissemination activities (within STEEPER consortium)

Due to the fact that STEEPER objectives cover the future semiconductor devices field at levels from devices to complex systems, passing by the different cells and circuit organization, internal dissemination sessions have been organized together with the regular PMB and PTC meetings. At each meeting all the work packages (WP) have presented their short term objectives, progress reports and results. This has been crucial for the project coordination and objective focus. All the presentations are shown in the intranet section of the project website. Meetings and consequently internal presentations have been organized in *{the meeting list}*

## 3.8 Confidential[5] or public applications for patents, trademarks, registered designs

At this time the STEEPER project consortium has no applications for patents, trademarks or registered designs. This might change in the course of the project and all information with be updated accordingly

| TEMPLATE B1: LIST OF APPLICATIONS FOR PATENTS, TRADEMARKS, REGISTERED DESIGNS, ETC. | | | | | |
|---|---|---|---|---|---|
| Type of IP Rights[6]: | Confidential Click on YES/NO | Foreseen embargo date dd/mm/yyyy | Application reference(s) (e.g. EP123456) | Subject or title of application | Applicant (s) (as on the application) |
| non | | | | | |

[5] Note to be confused with the "EU CONFIDENTIAL" classification for some security research projects.

[6] A drop down list allows choosing the type of IP rights: Patents, Trademarks, Registered designs, Utility models, Others.

# 4 Specific dissemination activities

All partners have taken advantage of their participation to renowned events to introduce STEEPER through their presentations when the topic covered was relevant to STEEPER

## 4.1 Articles in journals and conferences

Please refer to the list of publications above (section 2).

**TABLE OF SCIENTIFIC (PEER REVIEWED) PUBLICATIONS, STARTING WITH THE MOST IMPORTANT ONES**

| NO. | Title | Main author | Title of the periodical or the series | Number, date or frequency | Publisher | Place of publication | Year of publication | Relevant pages | Permanent identifiers[7] (if available) | Is/Will open access[8] provided to this publication? |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Electron-Hole Bilayer Tunnel FET for Steep Subthreshold Swing and Improved ON Current | L. Lattanzio, L. De Michielis and A. M. Ionescu | ESSDERC | Sept. 12-16, 2011. | ESSDERC | Helsinki | 2011 | pp | | Yes |
| 2 | Impact of strain and Ge concentration on the performance of planar SiGe band- to-band-tunneling transistors | M. Schmidt, R. A. Minamisawa, S Richter, J.-M. Hartmann, R. Luptak, A. Tiedemann, D. Buca, Q. T. Zhao, S. Mantl | ULIS | March 14-16, 2011 | ULIS | Cork | 2011 | pp. 202-205 | | Yes |
| 3 | Performance Limits of Superlattice-Based Steep-Slope Nanowire FETs | E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi, G. Baccarani | IEDM | Dec. 5-7, 2011 | IEDM | Washingotn DC | 2011 | | | Yes |
| 4 | C-V Measurements of Single Vertical NW Capacitors | P. Mensch, K.E. Moselund, S. Karg, M.T. Bjoerk, H. Schmid, E. Loertscher, H. Riel | DRC | June 2011 | DRC | Santa Barbara, CA | 2011 | | | Yes |
| 5 | Interband tunneling in nanowires with diamond cubic or zincblende crystalline structure based on atomistic modeling | Pino D'Amico, Paolo Marconcini, Gianluca Fiori, Giuseppe Iannaccone | Appl. Phys. Lett. | 2011 | Appl. Phys. Lett. | | | | | Yes |

[7] A permanent identifier should be a persistent link to the published version full text if open access or abstract if article is pay per view) or to the final manuscript accepted for publication (link to article in repository).

[8] Open Access is defined as free of charge access for anyone via Internet. Please answer "yes" if the open access to the publication is already established and also if the embargo period for open access is not yet over but you intend to establish open access afterwards.

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 6 | Multi-Subband Semi-classical Simulation of n-type Tunnel-FETs | A. Revelant, P. Palestri and L. Selmi | ULIS | 2012 | ULIS | Grenoble | 2012 | | | Yes |
| 7 | Strained Tunnel FETs with record Ion: First demonstration of ETSOI TFETs with SiGe channel and RSD | A. Villalon, C. Le Royer, M. Cassé, D. Cooper, B. Prévitali, C. Tabone, J.-M. Hartmann, P. Perreau, P. Rivallin, J.-F. Damlencourt, F. Allain, F. Andrieu, O. Weber, O. Faynot and T. Poiroux | VLSI symposium | June 12-15, 2012 | VLSI symposium | Honolulu | 2012 | | | Yes |

## 4.2 External exploitation activities performed individually by the STEEPER partners

### 4.2.1 Commissariat à l'Energie Atomique - Laboratoire d'Electronique et de Technologie de l'Information (CEA)

Carlo Reita - carlo.reita@cea.fr

CEA-LETI mission is the technology transfer from Academia to Industry and this is carried out in the form of both IP transfer and know-how transfer. CEA-LETI will carry out a proactive analysis of the technology developments realised for the STEEPER project in order to submit patents related to the TFET technology and include such patents in its IP portfolio. A large part of this portfolio is currently licensed to CEA-LETI industrial partners and we look at the TFET area as a one with strong potential to consolidate existing partnerships and attract new ones. At the same time, the know-how generated in the project, on materials, processes and integration will feed the industrial and academic programs on sub 20nm CMOS technology on the CEA-LETI 300mm platform. As a Research Institute, CEA-LETI will not develop products based on TFETs itself, but will support the European Industry in the prototyping phase if needed. Finally, at the end of the project and as it is done for most of them, an analysis to check the possibility of start-up creation will be performed.

### 4.2.2 Consorzio Nazionale Interuniversitario per la Nanoelettronica (IUNET)

Luca Selmi - luca.selmi@uniud.it
Giorgio Baccarani - gbaccarani@arces.unibo.it

The University of Bologna, as a third party of IUNET, is going to contribute to the dissemination of the obtained results by publishing on scientific journals and presenting at international conferences the most original achievements generated by the research work. In addition, we plan to exploit the main results of the STEEPER project predominantly from standpoint of education. We shall involve young students both in M.S. theses and in Ph.D. programs with the aim to make them familiar with the urging need to cut down significantly power consumption in electronic circuits and systems to the benefit of the environment. So doing, we shall solicit new and innovative ideas to be thoroughly investigated through the exploration of new materials, new device concepts and, whenever possible, by providing the proof of concepts of those ideas. The forthcoming Summer School we are organizing in Bertinoro is a further example in this direction. On the other hand, as a University, we are predominantly interested in the dissemination of knowledge and, as such, we do not envisage to directly pursuing the economic exploitation of IP rights. However, we are open to collaborate with European Industries and Research Institutes, and primarily with those who are participating in the project with manufacturing facilities, in order to help demonstrate by proof of concepts the new ideas we are pursuing.
The IUNET partner is currently exploiting the knowledge acquired during the STEEPER project to update a series of graduate level lectures and classes at the partner Universities on energy efficiency in electronics and electron devices. Moreover, the experience gained so far, and the networking with top-level players in the field of nanoelectronics available through STEEPER has been intensively exploited in the preparation of national projects on closely related subjects. One proposal involving IUNET-Bologna and IUNET-Udine has been submitted and funded by the Italian MIUR under the FIRB Futuro in ricerca 2011 programme. The proposal aims at the fabrication of a new concept of steep slope switch where a Bragg energy filter in III-V materials implemented at the source could make it possible to achieve extremely steep characteristics and high on-current at low voltage. A second proposal devoted to "Materials devices and circuits for VLSI digital circuits with high energy efficiency" has been submitted for the national MIUR PRIN

2010-2011 call.

**Table**: Development of innovative simulation tools for Tunnel-FETs

| STEEPER Partner | IUNET |
|---|---|
| **Describe the result:** | Two numerical models have been developed and implemented to simulate, respectively, Ultra Thin Body SOI and Nanowire Tunnel-FET. The former is based on semiclassical Multi Sub-Band Monte Carlo transport techniques. The latter is a full quantum simulator based on a k.p description of the energy relation and NEGF transport. |
| **Who will be the customer?** | In principle, potential customers are industrial research groups in the semiconductor and TCAD industry who may be willing to acquire access to the model source code for internal research purposes. Given the fact that Tunnel-FETs are not yet mainstream devices for industry, however, the expected number of potential customers is close to zero. |
| **What benefit will it bring to the customers?** | Assuming there are customers, the benefit will consist in the ability to simulate BTBT phenomena and Tunnel-FETs with much improved accuracy compared to existing TCAD for different device architectures and semiconductor channel materials. |
| **When is the expected date of achievement in the project (Mth/yr)?** | The simulators are expected to be fully developed and functional at month 24. Minor adjustments, debugging and integrations may be necessary during the last 12 months of the project. |
| **When is the time to market (Mth/yr)?** | No delivery to market is foreseen at the moment |
| **What are the costs to be incurred after the project and before exploitation?** | At present it is not possible to predict what the exact customer requests will be compared to what we have now, and therefore what the additional costs will be. |
| **What is the approximate price range of this result / price of licences?** | Not predictable at the moment |
| **What is the market size in Million € for this result and relevant trend?** | n.a |
| **How this result will rank against competing products in terms of price / performance?** | No direct ranking is possible on a fair ground. |
| **Who are the competitors for this result?** | Potential competitors for this result could be NEGF based full quantum transport simulators incorporating scattering mechanisms and suited for general purpose (UTB, wire, etc..) device architectures. |
| **How fast and in what ways will the competition respond to this result?** | Not predictable at the moment. Given that BTBT is becoming as serious source of leakage also for mainstream MOSFETs, it can be expected that TCAD companies may develop new and more accurate BTBT models compatible with existing TCAD platforms. |
| **Who are the partners involved in the result?** | None |
| **Who are the industrial partners interested in the result (partners, sponsors, etc…)?** | In principle the result can be of interest to researchers (both academic and industrial) |
| **Have you protected or will you protect this result? How? When?** | Being developed in an academic environment the result has been described in scientific publications. Aside from this due step, IUNET intends to protect the result by avoiding any |

| | |
|---|---|
| | disclosure of the source code to potential customers. |

### 4.2.3 Global Foundries Dresden Module One LLC & Co. KG (GF)

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Juergen Faul - Juergen.Faul@globalfoundries.com

The GLOBALFOUNDRIES (GF) mission is to create the unrivaled customer experience through deep collaboration, successful innovation, exceptional service and operational and manufacturing excellence. GF is the first foundry to ramp high volume manufacturing of High-k Metal Gate 32/28nm technology. GF ability to offer advanced process technology is powered by its highly successful and efficient collaborative R&D model centered on the joint development alliance (JDA) with several world leading product companies. Leading-edge technologies includes 45nm and smaller geometries with 32/28nm products in current production. Advanced technologies include 90nm and 65nm process geometries, and base technologies include 0.11um and larger geometries. Valued-Added-Solution process modules such as Non-Volatile Memories, High Voltage and RF are available across the various process geometries. GF Value-Added Solutions (VAS) are comprised of modules built on production-proven baseline technologies, structured into application-specific platforms that provide customers a faster time-to-market. FG VAS focuses on enabling customers' differentiation of their products in existing and new markets, while ensuring shortest time-to-market and minimal cost of ownership. Since VAS' earlier inception, multiple solutions have been launched to address needs in display drivers, ID and smart cards, Wi-Fi, Bluetooth applications, and power management.

### 4.2.4 IBM Research GmbH, Zurich Research Laboratory (IBM)

Heike Riel - Heike Riel hei@zurich.ibm.com

**Table:** Experimental exploitation activities

| LEAD PARTNER NAME | IBM Research GmbH, Zurich Research |
|---|---|
| Describe the innovation content of result | III-V on Si heterostructure nanowire TFETs are considered as excellent candidates for low-power devices. Furthermore, the nanowire geometry allows the integration onto a Si platform, which is essential for successful future utilization.<br>The III-V on Si TFET results achieved so far are according to plan and |
| Who will be the customer? | Semiconductor Manufacturers |
| What benefit will it bring to the customers? | The promise of the TFET as a steep slope device is to significantly reduce the operation voltage and thus the power consumption of electronic circuits. A decrease in power consumption will allow energy and thus cost savings, an extended battery lifetime etc. |
| When is the expected date of achievement in the project (Mth/yr)? | At the end of the project we would like to achieve a TFET with a operation voltage of below 0.5V. |
| When is the time to market (Mth/yr)? | The project targets a first experimental verification of theoretical promises that TFET can have a steep slope. If this is demonstrated at the end of the project there will further optimization be needed and the next step from the demonstration of single device to simple circuits has to be made, followed by more complex circuits. If all this is successful, a typical development time line for semiconductor devices of 5-8 years is expected. |
| What are the costs to be incurred after | The full costs of developing a new device technology are |

| | |
|---|---|
| the project and before exploitation? | needed. They are increasing with increasing technology nodes. |
| What is the approximate price range of this result / price of licences? | Not applicable |
| What is the market size in Million € for this result and relevant trend? | Semiconductor Technology market |
| How this result will rank against competing products in terms of price / performance? | Not applicable |
| Who are the competitors for this result? | A successful TFET is relevant for the entire semiconductor industry. Therefore all companies within this industry are competing for this result. |
| How fast and in what ways will the competition respond to this result? | Competitors such as Intel are also working on TFETs. |
| Who are the partners involved in the result? | |
| Who are the industrial partners interested in the result (partners, sponsors, etc…)? | |
| Have you protected or will you protect this result? How? When? | |

### 4.2.5 Intel Mobile Communications GmbH (IMC)

Reinhard Mahnkopf - reinhard.mahnkopf@intel.com

IMC is continuously monitoring the progress on TFET project activities and assessing the potential for implementation in future technology platforms for IMC products. Major IMC interest is on assessing the potential of TFETs for mobile communication products; for those low cost mainstream CMOS foundry standard technology is used in production -on bulk silicon with planar CMOS device architecture today and 3D trigate device architecture in future. With these technologies the TFET devices developed in STEEPER are compared with and measured against, at least conceptually with respect to their potential. Technology requirements have been derived for the IMC product portfolio and brought in into the project in year 1 as part of the respective WP5 activities. The IMC view on TFET application scenarios has been worked out and described in first year of the STEEPER project as well with associated figures-of-merit

1. The replacement scenario: TFET devices are replacing standard CMOS n/pFET.
2. Add-on scenario: TFET devices are co-integrated with CMOS because of specific unique TFET properties, on parameters in which they are superior to standard n/pFET.
3. Niche scenario: TFET figures-of-merit are relevant for a very narrow application segment only.

In the first two scenarios TFET's could still be exploited for mass production purposes, which is not true for scenario 3. As said above IMC focus was and still is on judging the potential of TFETs for system-on-a-chip (SoC) low power technology platforms. Based on the technical results achieved so far with the different TFET technology concepts pursued in STEEPER, there doesn't seem to be a fast track to bring TFET's into a competitive position to standard CMOS from device "performance" perspective in the near future. A replacement scenario seems to be unlikely from today's view. Therefore it is highly desirable to get TFET devices with a high degree of CMOS commonality from processing perspective, the TFET technology solution should be compatible to standard CMOS, and use silicon bulk substrate for cost reasons to enable scenario (2). STEEPER TFET device achievements so far point to the low voltage high latency (low frequency) application space, which is considered as a niche market today (scenario (3)), but significant growth might happen in this segment mid-term when taking into account the potential uplift in the health sector.

Based on these kinds of considerations IMC is exploiting the STEEPER results by trying to identify the technology which fits best for manufacturing IMC products, taking advantage of the potential proposition of TFETs developed. Therefore STEEPER results will influence –in one way or the other- IMC's device, technology and platform roadmap.

### 4.2.6 Research Center Jülich (FZJ), Peter Grünberg Institut (PGI9-IT)

Siegfried Mantl - s.mantl@fz-juelich.de

The FZJ as an academic partner plan to use the identified technical and scientific challenges of STEEPER to define new topics for PhDs and MS thesis to be offered. These PhDs will benefit from the access to the advanced technological and computational platforms available in the project. Due to the close interaction between FZJ and CEA-LETI with surrounding universities (the German Elite University RWTH Aachen and the Institute National Politechnique Grenoble, respectively) also the research centres will play a key role in helping to educate masters and PhD students, as well postdoctoral researchers in the field of nanoelectronics, thus contributing to counteract the lack of engineers and scientists in this field in Europe. In this perspective, the aim of the internship organized at the FZJ is to introduce students to current research topics in the field of nanoelectronics. Therefore, selected experiments allow to find real research equipment in a clean room environment. The internship program addresses students of physics, electrical engineering/ computer science, chemistry and materials science for the undergraduate / bachelor. From the very initial stage of the courses, the bases of the experiments are described in lectures. The following classes are introducing the experiments from different subject areas and are taught in small groups. Practical internship assignment is as follows:

- Fabrication and electrical characterization of Si component
- Quantum transport in semiconductor nanostructures
- Spin transport in magnetic nanostructures
- Non-volatile memory
- Cell-chip coupling of bioelectronic hybrids
- Resonant quantum tunneling structures
- Mechanically controlled junctions
- Molecular beam epitaxy of Ge quantum dots
- Carbon nanotubes
- Semiconductor Nanowires
- Production of multifunctional oxide films
- Transmission electron microscopy (TEM)

### 4.2.7 **RWTH Aachen University (RWTH)**

Joachim Knoch - knoch@iht.rwth-aachen.de

The long-term research strategy of the Institute for Semiconductor Electronics (RWTH Aachen) is to investigate energy independent nanosystems consisting of various components such as nanoscale thermoelectric generators, third generation photovoltaics, scalable energy storage and low power nanoelectronics devices. Therefore, the results gained within STEEPER on low power steep slope switches are one cornerstone of our research agenda. RWTH Aachen will exploit the knowledge on band-to-band tunneling to further develop concepts targeting at energy independent systems and explore possible combinations with e.g. energy efficient sensors. In addition, the results gained, particularly on the device physics aspects and working principles of steep slope switches will be incorporated into current and future advanced level lectures at RWTH Aachen making students. To be specific, about one third of the lecture "Nanoelectronics Devices" that will be held for the first time next summer term is devoted to steep slope transistors.

**Table:** Long term RWTH research strategy

| LEAD PARTNER NAME: | RWTH Aachen University |
|---|---|
| Describe the innovation content of result | Increasing the knowledge and understanding of tunnel FETs. Design guideline for tunnel FETs with optimized performance. |
| Who will be the customer? | Industry as well as academic partners and students. |
| What benefit will it bring to the customers? | Provide guidelines for designing and manufacturing optimized tunnel FETs. Education of students, exposing them to novel, energy efficient device concepts. |
| When is the expected date of achievement in the project (Mth/yr)? | June, 2013 |
| When is the time to market (Mth/yr)? | June, 2013 |
| What are the costs to be incurred after the project and before exploitation? | |
| What is the approximate price range of this result / price of licences? | |
| What is the market size in Million € for this result and relevant trend? | |
| How this result will rank against competing products in terms of price / performance? | |
| Who are the competitors for this result? | Groups worldwide working on tunnel FETs. |
| How fast and in what ways will the competition respond to this result? | |
| Who are the partners involved in the result? | FZ Jülich, IBM Zurich and IU-NET |
| Who are the industrial partners interested in the result (partners, sponsors, etc…)? | IBM |
| Have you protected or will you protect this result? How? When? | Several patents related to tunnel FETs have been filed (some of them are already granted) in 2005, 2009, 2010, 2011 |

### 4.2.8 **Ecole Polytechnique Fédérale de Lausanne (EPFL)**

Adrian Mihai Ionescu - adrian.ionescu@epfl.ch

The mission of the Nanoelectronic Devices Laboratory (NANOLAB) at EPFL is to innovate at device and technology level for advanced, state of the art nanoelectronics functionality. The NANOLAB is working on various subjects in the field of silicon micro/nano-electronics with special emphasis on the technology, design and modelling of nanoscale solid-state devices (including Silicon-On-Insulator devices, few-electron devices, hybrid SET/CMOS, single electron memory, nanowires and nanotubes), Radio Frequency MEMS devices for in- and above-IC and integrated optoelectronic devices. The results obtained within STEEPER project on low power steep slope switches design, fabrication and its applications are one of main, important feature of our teaching agenda. The NANOLAB delivers a series of the courses, including New Trends in Nano-Electronics, New Trends in Nano-Electronics, Nanoscale MOSFETs and beyond CMOS devices, RF MEMS for communications applications, where the students will benefit having access to the R&D results and findings of the STEEPER project.

# 5 Exploitation preparation

The STEEPER project addresses critical limitations caused by new technology nodes at sub-nanometer scale as well as new semiconductor device technology and its design paradigms for advanced IC systems with a key consideration of the impact of new device switching properties on the modern IC architectures. In particular the relevant topics addressed in the project are: The investigation of the impact of device operation and its integrations with available technologies approaching as well as going beyond the end of the ITRS devices, integrated circuits and systems. All these research lines are strategic for semiconductor companies so exploitation actions have been initiated within the different workpackages (WP). In particular, both Intel and GF and also LETI as industrial partners are evaluating the exploitation paths in STEEPER.

# 6 Joint collaboration actions with similar FP7projects

One of the STEEPER objectives is also to contribute to join activities (cluster meetings, training activities) with similar FP7 projects. We aim for joint publications, including contributions to a common portal, plan contributions to a FP7 conference, contribute to a common roadmap and strategy for future research in the domain, including cooperation with relevant national and international activities and enable the exchange of students/researchers between institutions and complementary collaborative dissemination actions. Thematic exchanges are foreseen with: GRAND: modeling approaches for quantum transport; DUALLOGIC: III-V integration on Silicon platforms; NEMSIC: circuit design with steep slope switches as sleep transistors for power management; as well as collaboration with other institutions, associations and networks including NANOSIL, NANOICT

# 7 Conclusions

This deliverable has presented the dissemination activities that have been performed by the STEEPER partners during the two first years of the project. Specific effort has been dedicated to the design of a project website website, project brochure, posters, distribution of press release and participation in project exhibitions to ensure the visibility of STEEPER to the European research community as a whole. The existence of the project, its objectives and consortium organization has been spread out through websites, press news, and brochure distribution at main conferences in Europe. Together with joint collaborative actions with similar FP7projects the aim of STEEPER for

the following period of the project is to present research results to the main conferences of the domain as well as among potential industrial users.