STEEPER

PUBLISHABLE SUMMARY

Grant Agreement number: 257267

Project acronym: STEEPER

Project title: Steep subthreshold slope switches for energy efficient electronics

Funding Scheme: Collaborative project

Date of latest version of Annex I against which the assessment will be made: 14 June 2011

Periodic report: 1st ☐ 2nd X 3rd ☐ 4th ☐

Period covered: from 1 June 2011 to 31 May 2012

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Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate) [1]:

  ☐ has fully achieved its objectives and technical goals for the period;

  X has achieved most of its objectives and technical goals for the period with relatively minor deviations.

  ☐ has failed to achieve critical objectives and/or is not at all on schedule.

- The public website, if applicable

  X is up to date

  ☐ is not up to date

- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 3.4) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 3.2.3 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: Mihai Adrian Ionescu

Date:

For most of the projects, the signature of this declaration could be done directly via the IT reporting tool through an adapted IT mechanism.

[1] If either of these boxes below is ticked, the report should reflect these and any remedial actions taken.

PUBLISHABLE SUMMARY

Objectives:

The project objectives have been addressed by the activities of various WPs that resulted in the full achievement of 2nd year deliverables and milestones. In terms of dissemination, we have organized in advance the 2nd STEEPER workshop and the consortium partners have published papers in 2nd year focusing on the main STEEPER topics. This is can be considered a true success and step forward towards the continuation of the project.

General objectives

• OBJ 1: Demonstrate energy efficient steep subthreshold slope transistors based on quantum mechanical band-to-band tunneling (tunnel FETs) able to reduce the voltage operation of advanced nanoelectronic circuits into sub-0.5V and their power consumption by one order of magnitude.

OBJ 2: Enable and demonstrate the power consumption benefits resulting from hybridization of tunnel FET and CMOS technologies and from tunnel FETs as stand-alone technology for digital, analog, RF and mixed-mode circuit applications.

Technology objectives

• OBJ 3: Develop a CMOS-compatible UTB SOI technology platform for tunnel FETs with ultra-low standby power by exploiting key additive boosters for enhanced performance: high-k dielectrics, SiGe source, strain

• OBJ 4: Study and identify advanced technology implementations for high-Ion tunnel FETs: III-V materials, nanowires, staggered versus broken band gaps, electrostatic doping

Simulation and modelling objectives

• OBJ 5: Develop accurate numerical simulation tools: semi-classical multi-sub-band Monte Carlo simulator and full-band quantum-transport simulation for in-depth study of UTB and nanowire tunnel FETs, respectively

• OBJ 6: Study the scaling, parameter sensitivity and variability on the characteristics of nanometer tunnel FETs

• OBJ 7: Develop and implement DC and AC compact models for the simulation and design of circuits based on tunnel FETs and or co-design with advanced CMOS industrial benchmarking: device and circuit

• OBJ 8: Benchmark tunnel FETs developed in STEEPER for low standby power logic, high speed, memory, RF and analog applications. Evaluate their energy efficiency against CMOS

Achievements during the 2nd year:

Concerning the technology:

All-Si TFETs

- Planar SiGe based Tunnel FETs cointegrated with CMOS on ETSOI: Lot 2.1: We demonstrate high performance HKMG Tunnel FET (cointegrated with FDSOI CMOS) by investigating tunnel boosters: electrostatics with low EOT (1.2nm), and ultrathin body channel (<7nm); band structures with SiGe source and/or channel; strain with cSiGe/SOI; junction abruptness with low temperature SD spike anneal. For the first time I_{ON} up to 428µA/µm in p mode with I_{ON}/I_{MIN} ratio large than 106 at VD=-1V are demonstrated, outperforming the TFET state of the art. Moreover we have obtained subthreshold slope Sw down to 33mV/dec and average Sw of 111mV/dec (over more than 3 decades of drain current).One can note that for the first time, the compressive strain (induced by SiGe epitaxy on ETSOI) has been evidenced at the device level (with 2D strain mapping obtained with HAADF STEM).
- (s)Si nanowire Tunnel FETs: sSi nanowire (10x50nm²) TFETs with 3.5nm HfO2 and 60nm TiN gate stack exhibit improved ON current (with a factor of 10) and subthreshold slope

(SSw=76mV/dec) with respect to previous SiO2/poly-Si gate stack (cf. M1.3).Optimizations of Source-Drain areas ("Implantation Into Silicide") have been shown to further improve the TFET performance: 6x30nm² sSi W-gated nanowire TFETs with 3nm HfO2/40nm TiN show SSw value down to 50 mV/dec (at VDS=0.18V).

- SiGe based nanowire Tunnel FET: 30nm wide nanowire TFETs have defined in Si/Si1-xGex/Si (5+12+12nm) with x = 35% and x = 50% (gate stack: 3.5 nm Al2O3 and 40 nm TiN). Due to enhanced tunnel injection (cSiGe), the ON currents are similar to the values obtained with sSi NW TFETs (in spite of degraded EOT

III-V TFETs

- A method for the catalyst-free selective area growth for the fabrication of axial III/V nanowire homo- and hetero-structures on silicon that is based on a nanowire template has been successfully developed at IBM.
- The n-type doping concentration of InAs has been increased to as high as $5 \cdot 10^{19}$ cm-3. Measurements of the Seebeck coefficient and modeling has been utilised to derive the carrier mobility
- The current in InAs-Si heterojunction tunnel diodes was boosted by improved doping at the interface to $6 \cdot 10^{6}$ A/cm2 at 0.5 V in reverse bias.
- First vertical InAs/Si heterojunction nanowire tunnel FETs were demonstrated.

Concerning modelling, simulation, and device optimization and novel structures:

Thanks to new relevant results from IUNET exploring the energy and the valence band effective masses for Si(1-x)Gex as a function of Ge molar fraction it is possible to simulate Tunnel-FETs of variable SiGe composition as used by the CEA-LETI and Juelich partners.

- Semiclassical and full quantum transport models for planar and nanowire, homo-junction and heter-junction Tunnel-FETs in Si, Si(1-x)Gex and InAs have been extended and verified against simulations (from literature and from partners - reference atomistic model) and experimental data (from literature and from partners - LETI, IBM)
- Scaling, optimization and sensitivity studies have been carried out for a variety of Si, Si(1-x)Gex, InAs, InAs/InAs/Si and InAs/Si/Si planar and NW TFETs
- An analytical DC Tunnel FET model has been completed. Mixed device circuit simulations and look-up table models have been extensively used to benchmark TFETs against alternative device architectures (FDSOI, bulk) in the context of energy efficient applications and aggressive VDD scaling.The IUNET-Bologna validated the quantum-simulation model by comparison with tight-binding simulated results on InAs TFETs available from the literature and with experimental data on hetero-junction InAs-Si Esaki diodes made available by IBM.
- The analytical p-n junction model developed by EPFL has been validated with FEM numerical simulation and experimental devices provided by STEEPER partners LETI and IBM.
- IUNET-Pisa has computed elastic band-to-band-tunneling rates for diamond cubic or zinc-blende nanowires with different materials and different cross sections up to a side of 3.4 nm using atomistic Hamiltonians based on sp3d5s*
- The analysis of this simple vehicle circuit and main results of IUNET-Udine mixed device-circuit simulations is an important step to obtain feedbacks about how the different electrical characteristics of Tunnel FETs and MOSFETs (already highlighted in part during the first year of the project) impact the performance of digital circuits operated at very low supply voltages.

Concerning novel device concepts and optimization ideas:

- Simulations of electrostatically doped source/drain tunnel FETs show the importance of screening the gate action on the source contact. The underlap between the gates in the source and channel regions can be made rather small since the gain in BTBT current overcompensates the increasing parasitic capacitance.
- A SiGe heterostructure tunnel FET including a strained silicon channel and a strained SiGe source contact have been realized and characterized by FZJ. The devices show an inverse subthreshold slope of 80mV/dec over more than two orders of magnitude and relatively large on-currents on the order of 1mA/mm. Furthermore, ambipolar operation of the devices can be suppressed by applying an appropriate back-gate voltage. Temperature dependent measurements show that tunnelling is the dominant carrier transport mechanism in the present devices.
- Optimized SL devices show very steep inverse subthreshold slopes and very high on-state currents. The resulting I_{ON}, namely 4.5 mA/μm at an I_{OFF} = 100 nA, exceeds the silicon CMOS performance, and is made possible at VDD = 0.4 V by the steep slope predicted by our simulations proving the huge potential of this particular device architecture.

Concerning benchmarking:

- The assessment 5.2 shows that both the Tunnel-FET System-on-Chip (SoC) co-integration on CMOS chips and also the multichip System-in-Package (SiP) system integration with Tunnel-FETs in a stand-alone chip have the potential to be integrated in an advanced conventional planar CMOS process flow. But there are also significant differences seen which will cause additional efforts needed to create a fully integrated circuit for the III-V TFET version.
- The SOI TFET version is an evolutionary extension of a common SOI process flow and the additional TFET device flavor can be treated as other MOSFET device flavours. The integration effort is similar and no principle roadblock is visible. If the SOI TFET is finally used depends first and foremost on the electrical figures of merit of these devices.