STEEPER

PROJECT PERIODIC REPORT

Grant Agreement number: 257267

Project acronym: STEEPER

Project title: Steep subthreshold slope switches for energy efficient electronics

Funding Scheme: Collaborative project

Date of latest version of Annex I against which the assessment will be made: 14 June 2011

Periodic report: **1st** X **2nd** ☐ **3rd** ☐ **4th** ☐

Period covered: from 1 June 2010 to 31 May 2011

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Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate) [1]:

  X has fully achieved its objectives and technical goals for the period;

  ☐ has achieved most of its objectives and technical goals for the period with relatively minor deviations.

  ☐ has failed to achieve critical objectives and/or is not at all on schedule.

- The public website, if applicable

  X is up to date

  ☐ is not up to date

- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 3.4) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 3.2.3 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: Mihai Adrian Ionescu

Date: .07/ 08/ 2011

For most of the projects, the signature of this declaration could be done directly via the IT reporting tool through an adapted IT mechanism.

[1] If either of these boxes below is ticked, the report should reflect these and any remedial actions taken.

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1. PUBLISHABLE SUMMARY

Objectives:

The project objectives have been addressed by the activities of various WPs that resulted in the full achievement of year 1 deliverables and milestones. In terms of dissemination, we have organized in advance the 1st workshop of the project and we have more than 40 publications in the first year centered on STEEPER topics. This is can be considered a true success and step forward towards the continuation of the project.

General objectives

- OBJ 1: Demonstrate energy efficient steep subthreshold slope transistors based on quantum mechanical band-to-band tunneling (tunnel FETs) able to reduce the voltage operation of advanced nanoelectronic circuits into sub-0.5V and their power consumption by one order of magnitude 1.
- OBJ 2: Enable and demonstrate the power consumption benefits resulting from hybridization of tunnel FET and CMOS technologies and from tunnel FETs as stand-alone technology for digital, analog, RF and mixed-mode circuit applications

Technology objectives

- OBJ 3: Develop a CMOS-compatible UTB SOI technology platform for tunnel FETs with ultra-low standby power by exploiting key additive boosters for enhanced performance: high-k dielectrics, SiGe source, strain
- OBJ 4: Study and identify advanced technology implementations for high-Ion tunnel FETs: III-V materials, nanowires, staggered versus broken band gaps, electrostatic doping

Simulation and modelling objectives

- OBJ 5: Develop accurate numerical simulation tools: semi-classical multi-sub-band Monte Carlo simulator and full-band quantum-transport simulation for in-depth study of UTB and nanowire tunnel FETs, respectively
- OBJ 6: Study the scaling, parameter sensitivity and variability on the characteristics of nanometer tunnel FETs
- OBJ 7: Develop and implement DC and AC compact models for the simulation and design of circuits based on tunnel FETs and or co-design with advanced CMOS

Industrial benchmarking: device and circuit

- OBJ 8: Benchmark tunnel FETs developed in STEEPER for low standby power logic, high speed, memory, RF and analog applications. Evaluate their energy efficiency against CMOS

Achievements during the 1st year

Concerning the technology:

All-Si TFETs

- **First experiments of Lot 1 (SOI based TFET & CMOS) delivered** by CEA LETI: **samples send to partners confirmed the interest of low EOT gate stack** for improving the subthreshold slope and the ON currents of TFETs. The measured values are in agreement with the state of the art.
- **The lot 2 was started based on promising results of lot 1** by CEA LETI**.** More technology booster have been decided: an aggresive EOT with high-K/Metal Gate, ultrathin Si film,trigate architecture, SiGe source.
- **Nanowire array TFETs using SOI and sSOI with SiO_2 and HfO_2 as gate dielectrics were successfully fabricated** by FZJ.

III-V TFETs

- **Epitaxial growth of InAs nanowires on Si<111> has been successfully established by IBM-ZRL without the use of a catalyst material and with high yield**. Moreover, the InAs-Si interface is abrupt and of high quality as required for high performance TFETs.
- **In-situ doping of InAs nanowires has been demonstrated** to lower the resistivity for as-grown InAs using Si as dopant.
- **A detailed study on InAs-Si heterojunction diodes has been performed** and Esaki diodes based on this material set have been demonstrated for the first time.

Concerning the modelling, simulation, device optimization and novel structures

- Major progress is reported **with the semi-classical transport model based on an available Multi Subband Monte Carlo transport solver** by IUNET-UD which has been extended to describe planar Tunnel-FET devices through the addition of a BTBT generation rate term.
- The development of a complete simulator for NW Tunnel-FETs based on quantum-transport to provide accurate modelling of the tunnelling processes in the devices under investigation is still in progress.
- The **first analytical dc compact models for Tunnel junctions and Tunnel FETs have already been implemented in MATLAB**.
- At circuit level, **the first simulation of digital inverters with mixed device-circuit simulation methodology using the calibrated input deck has been successfully achieved**.

Concerning novel device concepts and optimization ideas

- A **tool for the simulation of cylindrical nanowire tunnel FETs with electrostatically doped source contacts has been developed** by TU-D.
- The **impact of device parameters such as the source doping concentration and source-gate underlap on the performance of vertical wrap-gate III-V heterojuntion tunnel FETs** has been studied by TU-D.
- A SiGe heterostructure tunnel FET including a strained silicon channel and a strained SiGe source contact have been realized and characterized by FZJ. The devices show an inverse subthreshold slope of 80mV/dec over more than two orders of magnitude and relatively large on-currents.
- EPFL demonstrated by simulation the usefulness of the novel EHBTFET device concept, which is based on the carrier tunneling through a bias-induced EH bilayer in a silicon quantum well.
- IUNET(Bologna) demonstrated a novel steep slope device concept based on an energy filter created exploiting a miniband in a periodic heterostructure as the injecting source contact.

Concerning benchmarking

- A first possible design point for tunnel FET´s was proposed for LSTP (LOP) applications. The duideline was to achieve a comparable performance to multi channel devices as being proposed in the ITRS roadmap. The proposed design point fulfils this requirement and shows for that setting a tremendous reduction in power consumption.
- Low operating power applications have been identified as most favourable with significant benefits. By achieving the derived targets all logic circuitry can easily be replaced by the new device type. By not achieving the targets tunnel FET´s can still serve as add-on features.