



E3NETWORK

Energy Efficient E-band transceiver for
backhaul of the future networks

DELIVERABLE D4.2

Measurement report of the E3Network transceiver

Contract number :	317957
Project acronym :	E3NETWORK
Project title :	Energy Efficient E-Band Transceiver for Backhaul of the Future Networks

Deliverable number :	D4.2
Nature :	R- Report
Dissemination level :	PU (Public)
Report date :	30 June 2016

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The E3NETWORK project was funded by the European
Commission under the 7th Framework Programme (FP7) –ICT

Coordinator: CEIT

VERSION CONTROL

Version	Date	Contributors	Sections Affected
1	2016-02-11	All	All – document created
2	2016-02-26	All	All – results and discussions included
3	2016-05-12	CEIT	Update of results and discussions
4	2016-05-16	SIV	All – finalization of rev A
5	2016-06-28	CEIT	Final version
6	2016-06-30	FHG	All

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EXECUTIVE SUMMARY

D4.2 describes the testing of the transceiver demonstrator designed and assembled within T4.2 in the project E3network. D4.2 describes all the tests that have been considered mandatory to pass, in order to prove that the demonstrator is working as intended. A more comprehensive testing and comparison with the specifications is planned to be done in WP5, demonstrating that the system can be considered a commercial system, respecting the current normative an equipment shall meet in order to be put on the market. The goal of the work within T4.2 is that the demonstrator will be proven useful for the work within WP5.

The transceiver demonstrator described in D4.2 consists of three main units, one receiver (RX) unit and two transmitter (TX) units. D4.1 contains a detailed hardware description and can also be used as a manual to operate the demonstrator.

E-Band measurements on a loop-back setup using off-line demodulation are presented, showing successful transmission of a 10 Gbps signal. Additionally, online decodification of the signal is tested at baseband level with satisfactory results.

ACRONYMS AND ABBREVIATIONS

ADC	Analog-to-Digital Converter
ATPC	Automatic Transmit Power Control
BB	BaseBand
CW	Continuous Wave
DAC	Digital-to-Analog Converter
dB	decibel
DBB	Digital baseband
DEMODO	Demodulator
DPL	Duplexer
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate array
GHz	Gigahertz
IF	Intermediate Frequency
LO	Local Oscillator
mmW	millimeter-wave
MOD	Modulator
NF	Noise Figure
PA	Power Amplifier
PtP	Point-to-Point
QAM	Quadrature Amplitude Modulation
R&TTE	Radio and Telecommunications Terminal Equipment
RTPC	Remote Transmit Power Control
RX	Receiver
STREP	Specific Targeted Research Projects
TX	Transmitter
WG Att	Waveguide Attenuator
WG	WR12 waveguide

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1. INTRODUCTION

D4.2 describes the initial testing of the transceiver demonstrator designed and assembled within T4.2 in the project E3Network. An in-depth description of the hardware in the demonstrator is given in D4.1, which describes the overall demonstrator as well as its operation.

D4.2 describes all the tests that have been considered mandatory to pass, in order to prove that the demonstrator is working as intended. A more comprehensive testing and comparison with the specifications was initially planned to be done in WP5, demonstrating that the system can be considered a commercial system, fulfilling the current normative that a piece of equipment shall meet to be put on the market.

All the tests described in D4.2 are performed using a proper test method. The test bench used, the scope of the measurements and the test method are adequately described in each relevant section.

The transceiver demonstrator described in D4.2 consists of three parts, one receiver (RX) part and two identical transmitter (TX) parts. For most tests, transmitter #1 is connected to the receiver over a waveguide attenuator and will thus form an E-band "link".

D4.2 is also an important document for MS8, "Integrated E3Network transceiver technically tested". In the DOW, this milestone is described as "The integrated E3Network transceiver will have to fulfill the technical specifications in D1.2.3 and measurable project objectives O1, O2, O3 and O4". The project objectives are found in B1.1.3 in the STREP proposal.

Section 2 will describe the measurements done within T4.2 and compare them to the specifications in D1.2.3 where applicable. Section 3 will discuss project objectives O1-O4 and section 4 will conclude D4.2.

2. MEASUREMENTS OF THE TRANSCEIVER DEMONSTRATOR

The overall objective of the measurements reported in D4.2 is to verify that the transceiver demonstrator is suitable to be used within WP5, where a comprehensive characterization will be performed. These measurements are therefore considered to be enough to determine if the transceiver demonstrator is working as intended and then suitable for WP5.

Two identical transmitters are built and tested: transmitter #1 and transmitter #2. Transmitter #1 is comprehensively tested throughout D4.2. Transmitter #2 is fully tested for RF output power and partially with spectrum measurements. After this partial testing of transmitter #2, all partners involved are confident that transmitter #1 and transmitter #2 will have very similar performance and they are interchangeable within the work of WP5.

In the following sub-sections, simplified block diagrams of the overall transceiver demonstrator will be used to explain the different measurement setups. Figure 1 shows one of such block diagrams, with all the abbreviations explained. The following figures will use the same abbreviations. Figure 2 shows a photograph of the overall transceiver demonstrator.

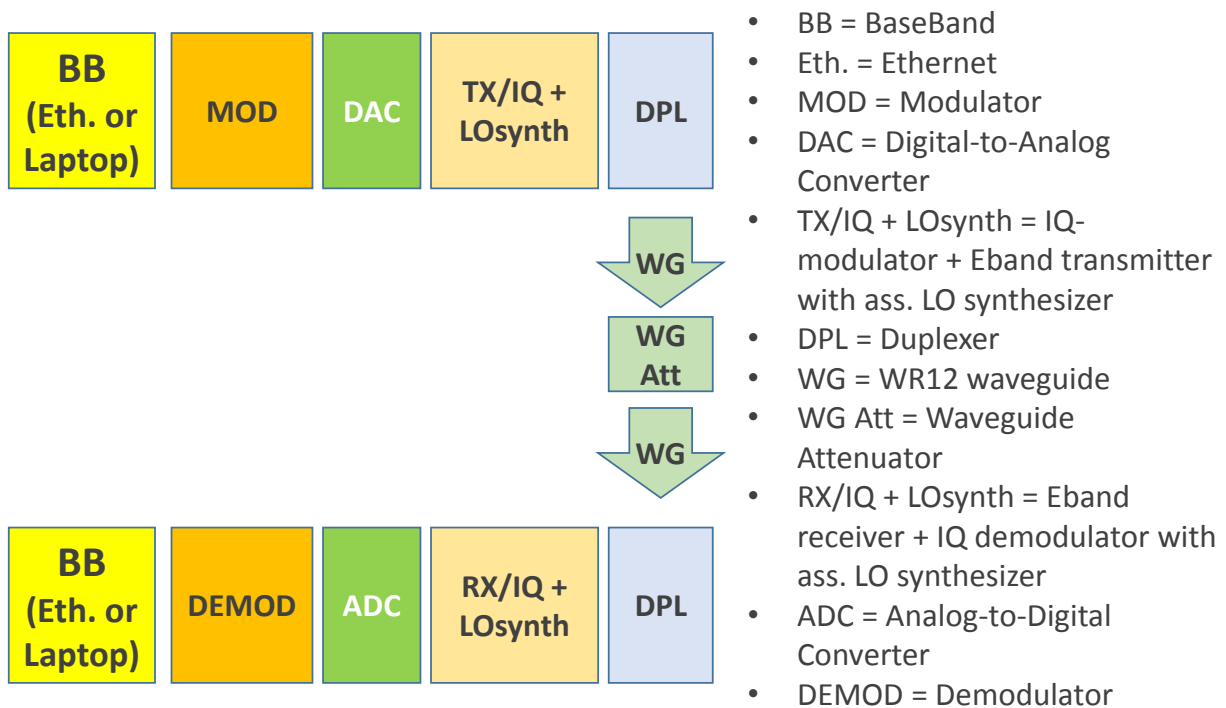


Figure 1. Simplified block diagrams of the overall transceiver demonstrator with abbreviations

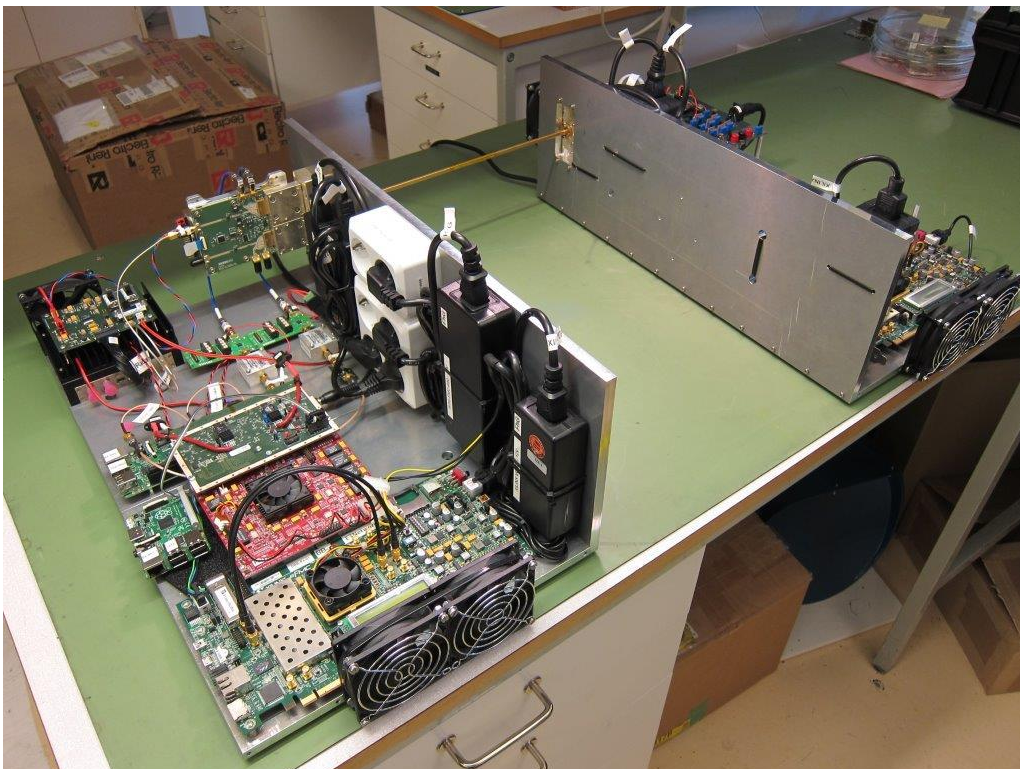


Figure 2. Photos of the overall transceiver demonstrator – transmitter (top) and receiver (bottom), external LO synthesizers and associated cables not shown for clarity

In most of the tests the TX is connected to the RX through a 300 mm long WR-12 waveguide in series with a 30dB attenuator. The total attenuation of this combination is typically 31 dB over the full 71-86 GHz band. A plot of the measured attenuation vs. frequency is shown in Figure 3.

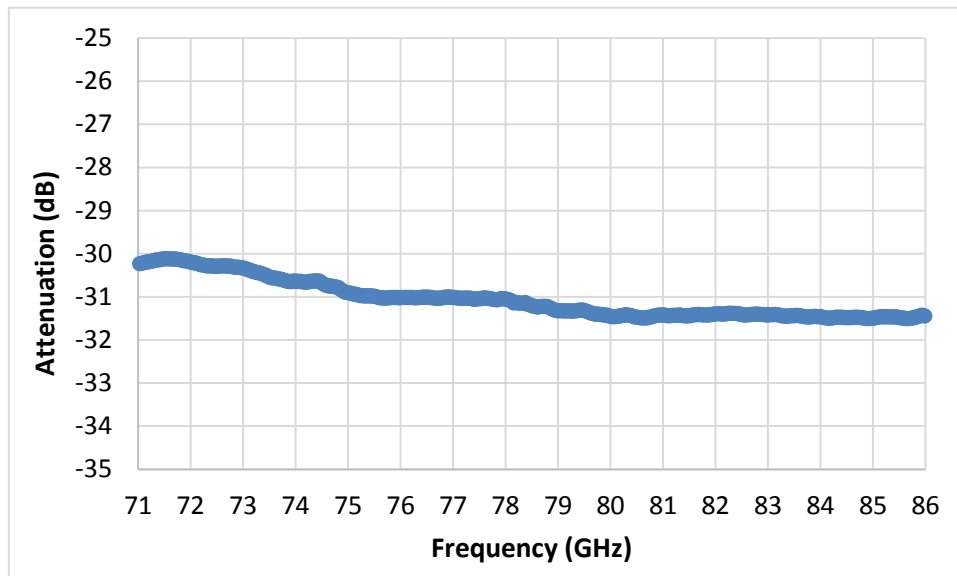


Figure 3. Attenuation of waveguide + fixed 30 dB attenuator used in the testing of the demonstrator

Many of the parameters are tested on different channels. If nothing else is stated, the channels tested correspond to the center frequencies found in Table 1. The bandwidth occupied is always 2000 MHz, independent on modulation.

Table 1. RF channels and they corresponding centre frequencies

F0	RF freq	Unit
CH 1	72.125	GHz
CH 2	74.625	GHz
CH 3	82.125	GHz
CH 4	84.625	GHz

The measurements in this chapter are outlined as follows: section 2.1 contains RF output power measurements for transmitter #1 and transmitter #2. Section 2.2 investigates the RF stability and spectral purity of the whole transmitter #1 connected to the mmW RX part (including diplexer). In section 2.3, base-band loop operation (DBB-Tx, DAC, ADC, DBB-Rx) performing the appropriate connection between transmitter #2 and the receiver is verified. In section 2.4 the whole transmitter #1 is again connected to the mmW RX part to check the E-Band loop performance.

2.1 Transmitter RF output power

Introduction:

Measurements are performed at room temperature and in four different channels for every transmitter module. The channels are outlined in Table 1.

Objective:

Verify that the maximum *useable* output average RF power measured at TX PCB and Duplexer output is within the [ReqEqu044] value defined in D1.2.3. Note that this is not the maximum *possible* output average RF power (=saturated RF power) but rather the maximum RF power that is suitable for 64QAM transmission including back-off etc.

At this stage, this Ptx value has been defined with back-off considerations and to prove the performance of the link.

Test instruments:

- WR12 RF Power sensor (ELVA-1 DPM)

Test configuration:

The power sensor is connected directly to the diplexer output port in order to measure the RF output power as seen in Figure 4. No additional waveguides or attenuators are needed for this test. The RF signal is a 10 Gbps 64-QAM modulated signal with a bandwidth of 2 GHz, generated in baseband in the TX FPGA, converted to analog using the DAC board and then up-converted to the E-Band.

The output power from the TX PCB can be numerically calculated by de-embedding the known losses of the diplexer and waveguide connecting the PCB to the diplexer (a total of 1 dB).

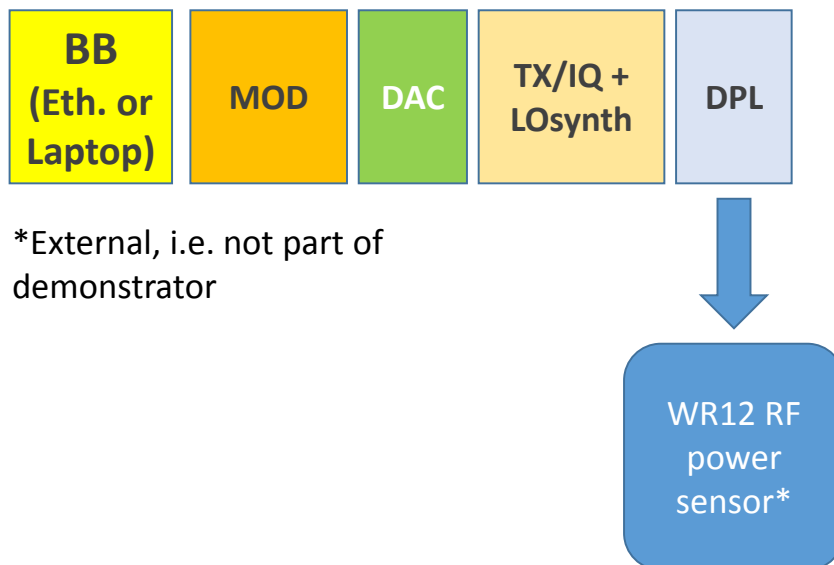


Figure 4. Transmitter RF output power at TX PCB and Duplexer output – test setup

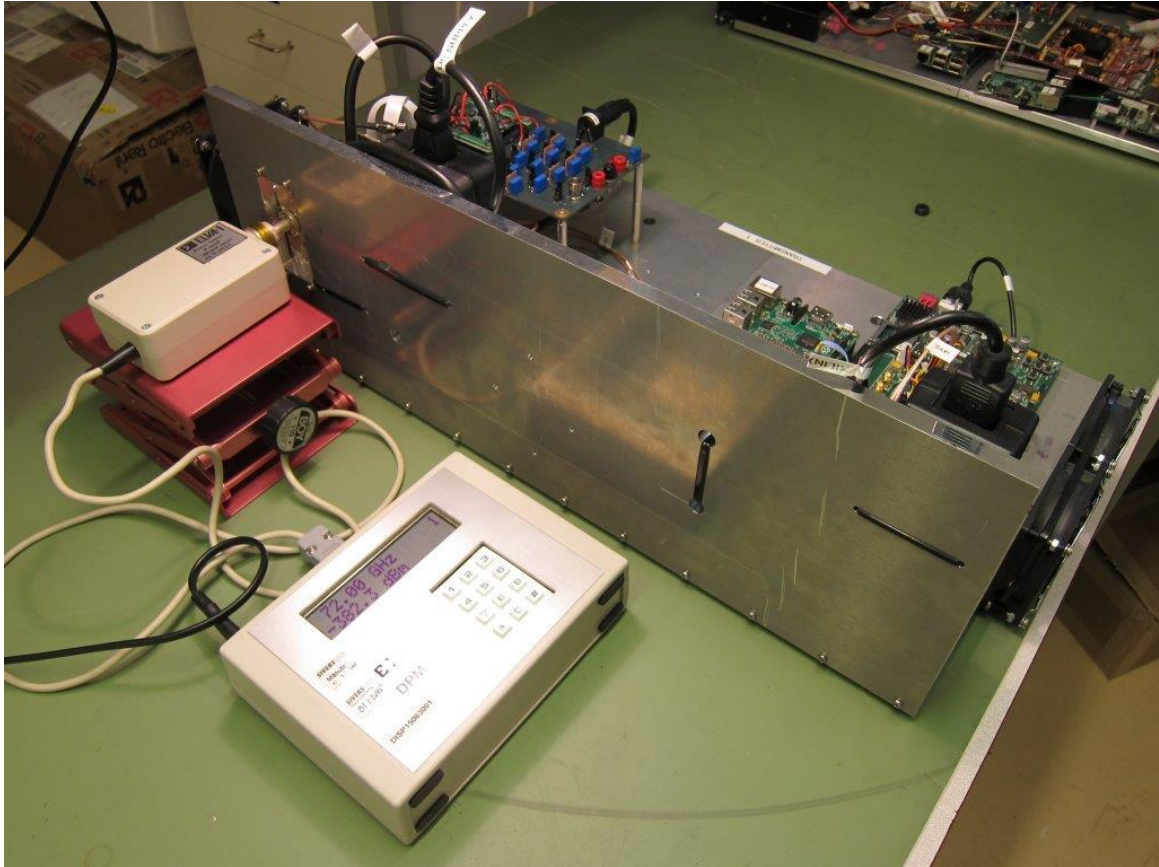


Figure 5. Transmitter RF output power at TX PCB and Duplexer output – photo of test setup

Test procedure:

With the transmitter power level set to the maximum useable level for 64 QAM transmissions, the average power output of the transmitter is measured using a WR12 RF power sensor connected to the duplexer antenna port. Table 2 and Table 3 give the detailed results as well as the specified value from D1.2.3.

Table 2. RF output power from diplexer – Transmitter #1

TX #1 - ANTENNA PORT						
Req. ID	Parameter	F0	Typ	Unit	TX unit	Spec.
[ReqDup_010]&[ReqRFT_001]& [ReqRFT_004]	TX power	CH 1	-4.4	dBm	TX #1	6 +/-1
[ReqDup_010]&[ReqRFT_001]& [ReqRFT_004]	TX power	CH 2	-7.3	dBm	TX #1	6 +/-1
[ReqDup_010]&[ReqRFT_001]& [ReqRFT_004]	TX power	CH 3	-9.1	dBm	TX #1	6 +/-1
[ReqDup_010]&[ReqRFT_001]& [ReqRFT_004]	TX power	CH 4	-13.4	dBm	TX #1	6 +/-1

Table 3. RF output power from diplexer – Transmitter #2

TX #2 - ANTENNA PORT						
Req. ID	Parameter	F0	Typ	Unit	TX unit	Spec.
[ReqDup_010]&[ReqRFT_001]& [ReqRFT_004]	TX power	CH 1	-0.8	dBm	TX #2	6 +/-1
[ReqDup_010]&[ReqRFT_001]& [ReqRFT_004]	TX power	CH 2	0	dBm	TX #2	6 +/-1
[ReqDup_010]&[ReqRFT_001]& [ReqRFT_004]	TX power	CH 3	-6.6	dBm	TX #2	6 +/-1
[ReqDup_010]&[ReqRFT_001]& [ReqRFT_004]	TX power	CH 4	-9.5	dBm	TX #2	6 +/-1

Discussion:

It is observed that the transmitter RF output power, measured at the diplexer antenna port, is lower compared to the specification in D1.2.3. The reasons for this mismatch have been identified:

- Higher die-PCB interconnection loss
- Lower P1dB at PA, which makes it necessary to operate at a lower output power to maintain the backoff.
- Using different dies for the I/Q up-converter and the mm-wave TX, which means higher interconnection losses and thus less TX gain.
- Inclusion of a 3dB splitter between the I/Q up-converter in order to sense the IF output signal and calibrate the I/Q imbalance.

Nonetheless, the measured power levels for usable transmitter RF output power when using 64-QAM modulated signals aligns well with the evaluation of a standalone TX up-converter PCB in D2.5 (figure 2-16, p. 17). The stand-alone TX up-converter demonstrates a typical P1dB figure of [+6, -2, +2, +1 dBm] for CH 1 to 4, respectively. Given the 10 dB back-off required when using 64QAM, the theoretical value of the useable RF output power would be of [-4, -12, -8, -9 dBm] for CH 1 to 4 at the TX PCB, respectively. Comparing these figures, it is seen that the measured output power is typically higher in D4.2 compared to what is presented in D2.5. This is due to the fact that the measurements of the output power performed in D4.2 are done on the combined IQ/TX PCB rather than on the stand-alone TX board (both described in section 4.3.1 in D4.1). One difference between these boards is the bondwire compensation structure for the RF output of the TX die. The combined IQ/TX PCB possess therefore better output match for the TX die compared to the stand-alone TX PCB, resulting in higher output RF power on CH 1 to CH 3, but most prominent on CH 2. From these measurements it can be assumed that the optimum frequency of the bondwire compensation circuit has been shifted somewhat down in frequency (ideally it was designed for an optimum at 78.5 GHz), most likely due to longer bondwires than anticipated in simulations.

Figure 6 shows the RF output power from the TX PCB (with the diplexer and WG loss de-embedded) vs. channel number for the two transmitters, as well as the theoretical value derived from D2.5 (=P1dB from D2.5 minus 10 dB back-off required for 64-QAM modulation).

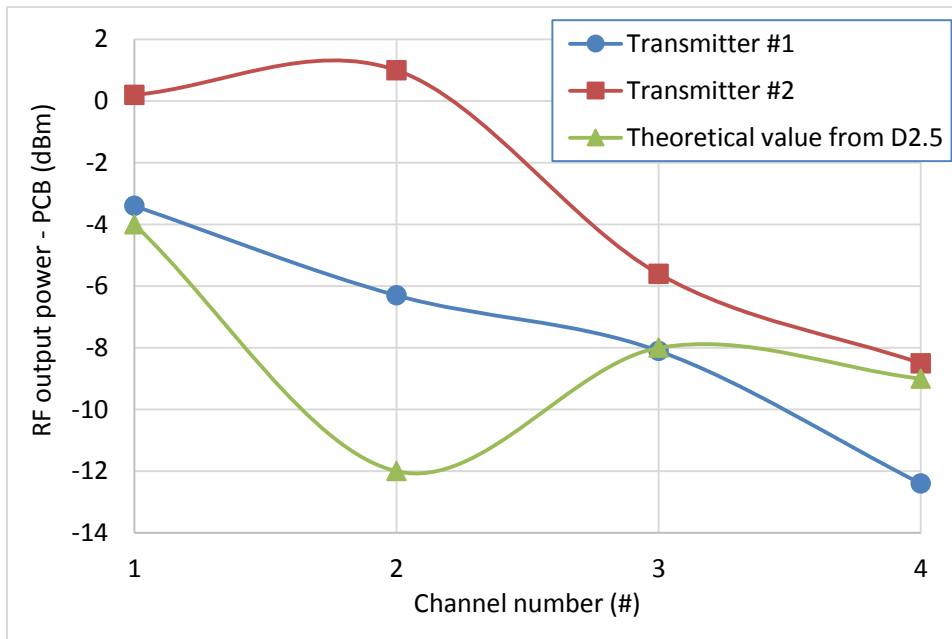


Figure 6. RF output power from TX PCB vs. channel number

Conclusion:

Based on the presented results and considering the maximum possible tolerance according to the ETSI HS EN 302 217-2-2 (+/- 3 dB), the transceiver demonstrator will be able to be used within WP5 in CH 1, CH 2 and CH 3 with a typical transmitter RF output power at the diplexer antenna port of -7 dBm.

2.2 Transmitter & Receiver RF stability and spectral purity

Introduction:

Measurements are performed at room temperature and in two different channels, CH1 and CH3, for transmitter #2. The same receiver is used for all the measurements. The channels are outlined in Table 1. As for transmitter #2, it is tested with CW signals only but it was found to be working as expected.

Objective:

Verify that no major unexplained discrete CW components or spurious originating from oscillations in the mmW TX or RX are present in the RF spectrum.

The spectrum mask will be investigated carefully within WP5. The test in this section is instead qualitative in nature, as the spectrum is manually searched for “odd” spurious that might indicate oscillations or unwanted signal leakage. Moreover, the spectrum is tested at the receiver IF output port and, thus, considers also the RX contribution. Additionally, due to the low received signal power, the spectrum analyzer noise floor is limiting the measurements and, thus, some amplification would be needed to test the “real” noise floor of the transmitted signal spectrum.

Test instruments:

- Spectrum Analyzer (HP 8564E)

Test configuration:

A 10 Gbps, 64-QAM and 2 GHz wide modulated signal is created in baseband in the TX FPGA, converted to analogue using the DAC board and then up-converted to the E-Band. The RF signal at the mmW TX output is down-converted to a suitable intermediate frequency by the mmW RX in the receiver unit and the spectrum is displayed on a spectrum analyzer as shown in Figure 7 and Figure 8. This way, both the mmW TX and mmW RX are tested for stability and spectral purity simultaneously.

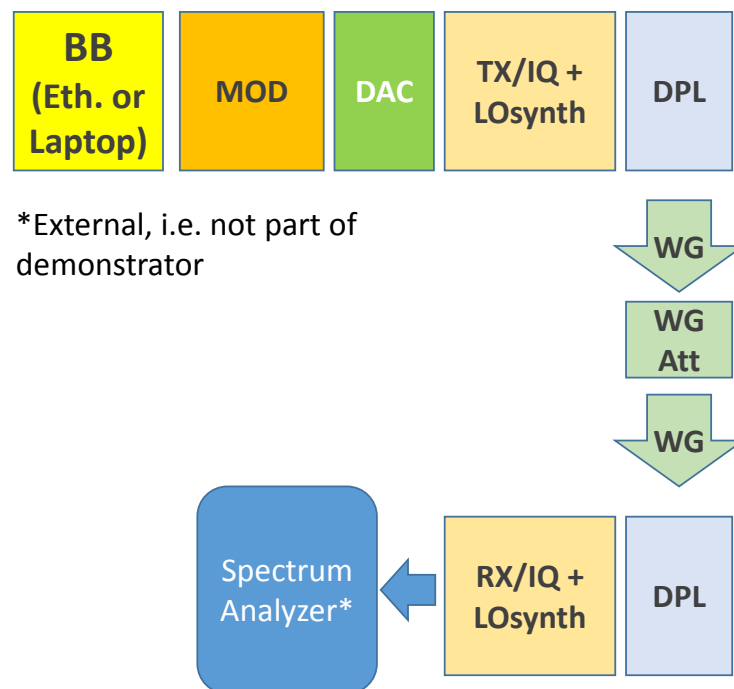


Figure 7. Transmitter & Receiver RF stability and spectral purity – test setup

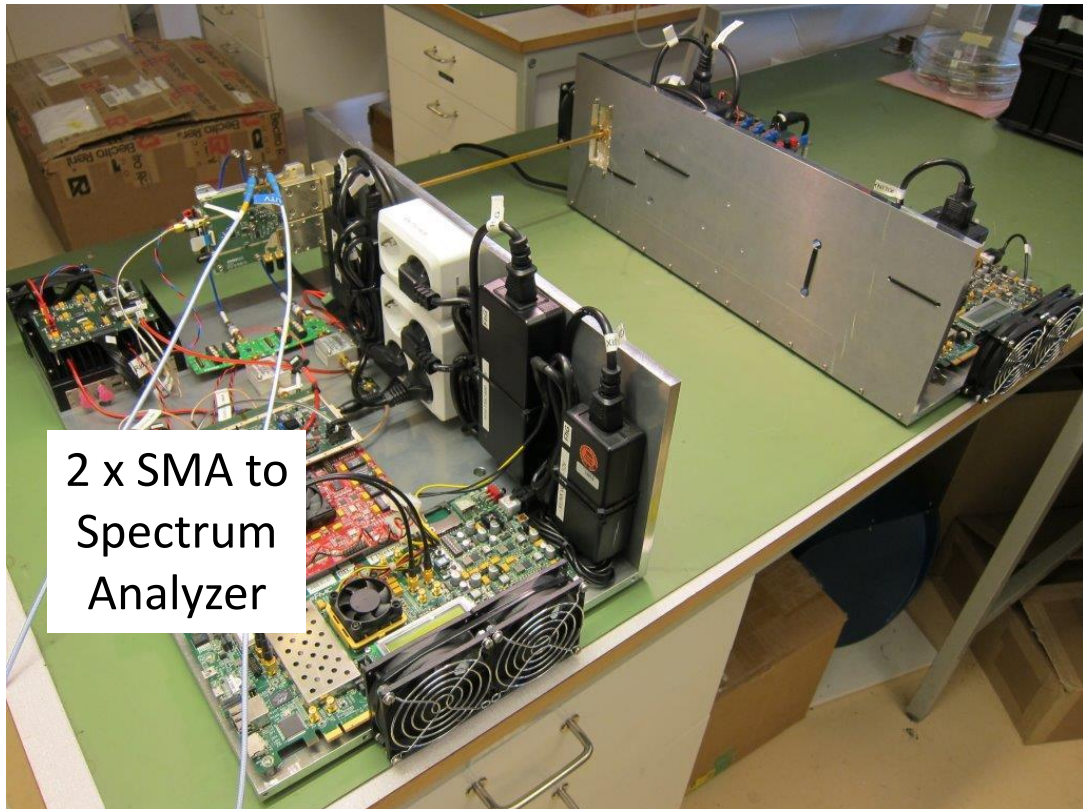


Figure 8. Transmitter & Receiver RF stability and spectral purity – photo of test setup

Test procedure:

The mmW TX output is connected to the mmW RX input over the WR12 waveguide and attenuator, which have the losses shown in Figure 3. The 30 dB waveguide attenuator is placed to ensure that the mmW RX works within its linear region. The IF output from the mmW RX is fed directly to the spectrum analyzer as seen in Figure 7. Both IF-I and IF-Q signals are examined manually with the spectrum analyzer but only one signal at a time. The unused IF output is terminated in a 50 Ohm load. For all measurements, there were no significant differences between the I and Q signal and only one plot per channel is therefore presented.

The centre frequency of the IF is chosen to 3.5 GHz for all measurements in order to allow for a broadband examination of the spectrum. As seen in Figure 9, this centre frequency makes it possible to simultaneously display the wanted (2 GHz wide) channel as well as an upper and a lower channel with the same width. With an even higher centre frequency, even more channels would be possible to display but the mmW RX has an upper frequency limit of around 6 GHz.

Photos of the wideband frequency spectrums captured are found in Figure 10 and Figure 11 for channel 1 and 3, respectively.

RX LO frequency @ CH 1: 12.604 GHz (corresponding to 75.625 GHz at Eband)

RX LO frequency @ CH 3: 13.104 GHz (corresponding to 78.625 GHz at Eband)

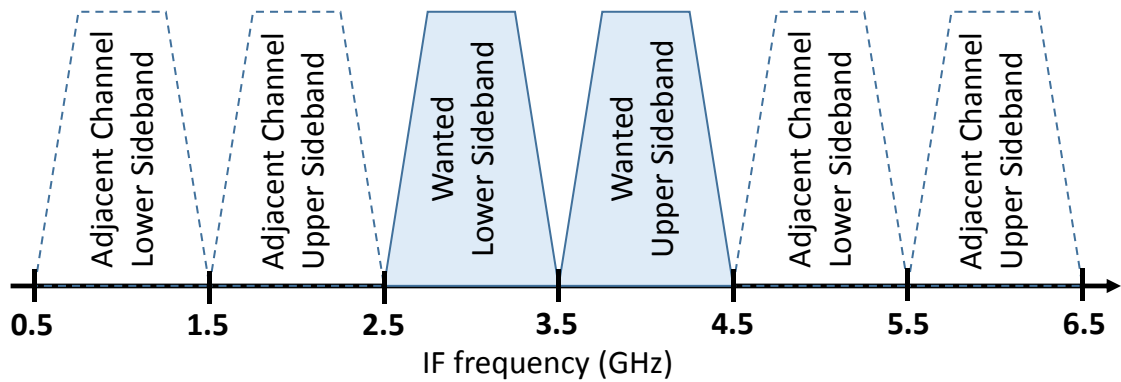


Figure 9. IF spectrum and frequency plan

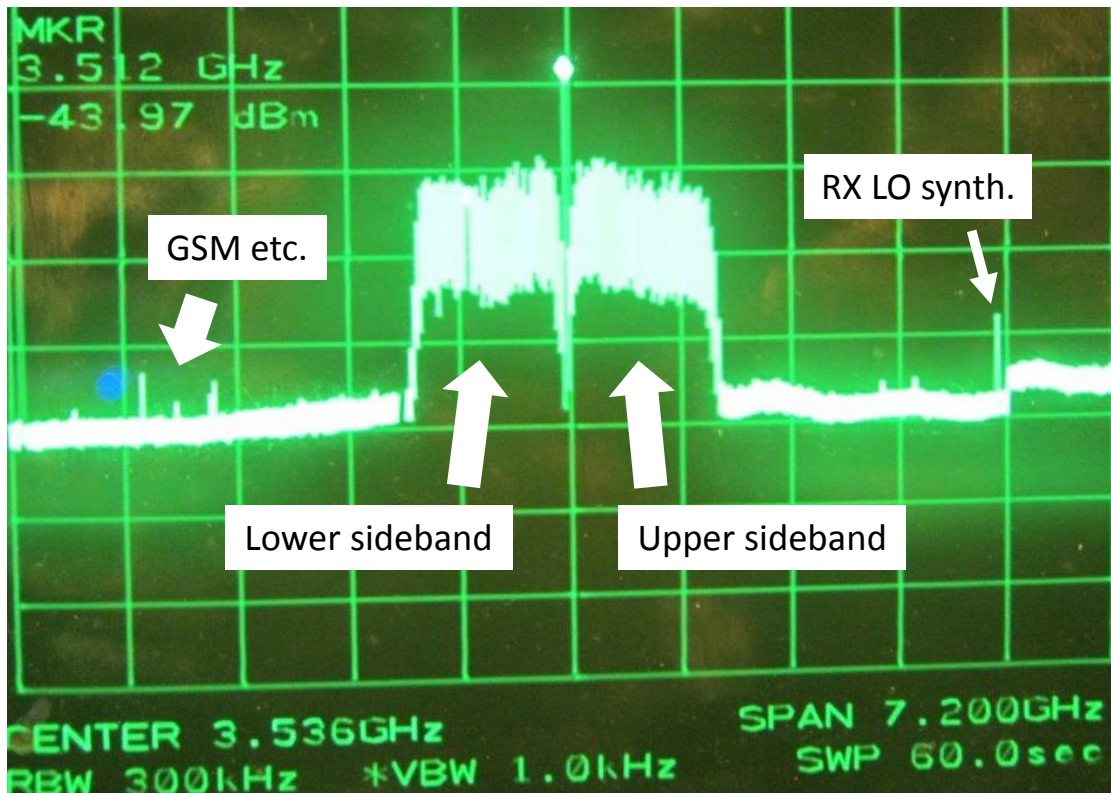


Figure 10. Transmitter & Receiver RF stability, spectral purity, and spurious emissions
- Transmitter #1 @ Channel 1

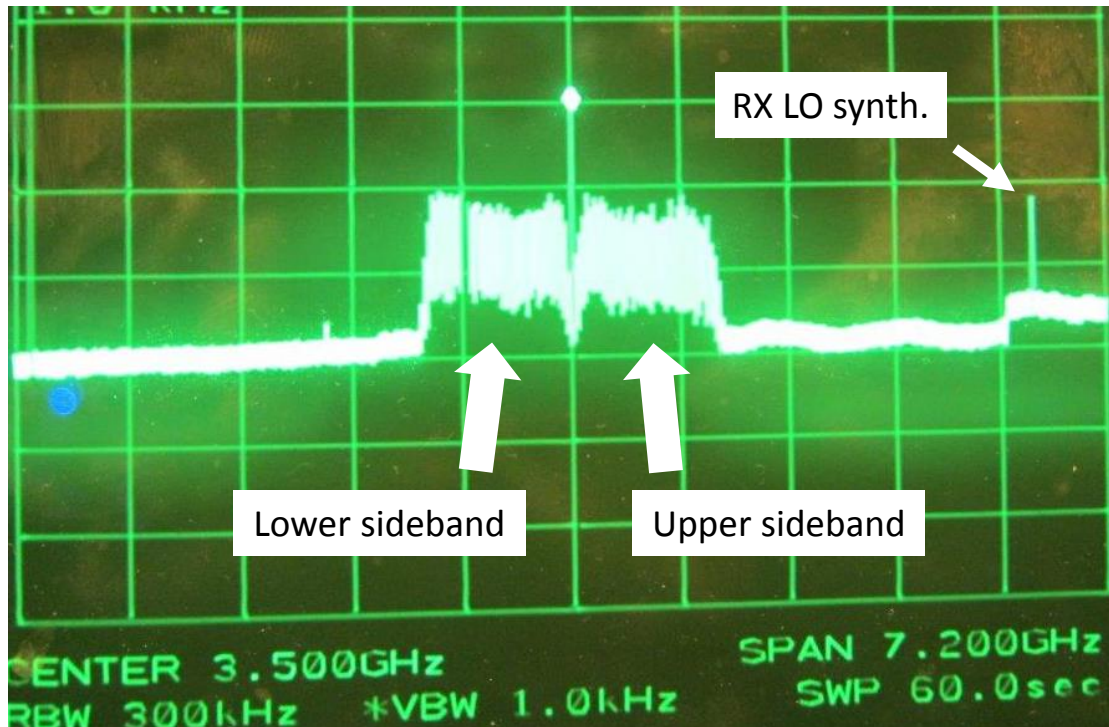


Figure 11. Transmitter & Receiver RF stability, spectral purity, and spurious emissions
– Transmitter #1 @ Channel 3

Conclusion:

The spectrum at the antenna port has been observed and presented. Given the limitations in the test bench regarding dynamic range it was only possible to perform a qualitative investigation.

However, according to the results of these measurements, it can be said that the system can work properly from the emissions and oscillation point of view. No evident limitations, apart from the PTx level, or issues are found.

2.3 Transmit & Receive modulated data in baseband

Introduction:

Measurements are performed at room temperature.

Objective:

Verify the functionality of the digital baseband TX and RX when working online, as well as the DAC and ADC converters.

Test instruments:

- No external equipment rather than the demonstrator itself is required for this test

Test configuration:

For this test the signal is generated in the FPGA with the DBB TX and then converted to analogue using the DAC board. The signal goes through low-pass filters and VGAs which adjust the signal levels. The signal is then converted back to the digital domain using the ADC and then processed in the DBB RX FPGA. Figure 12 and Figure 13 show a simplified and detailed test setup, respectively.

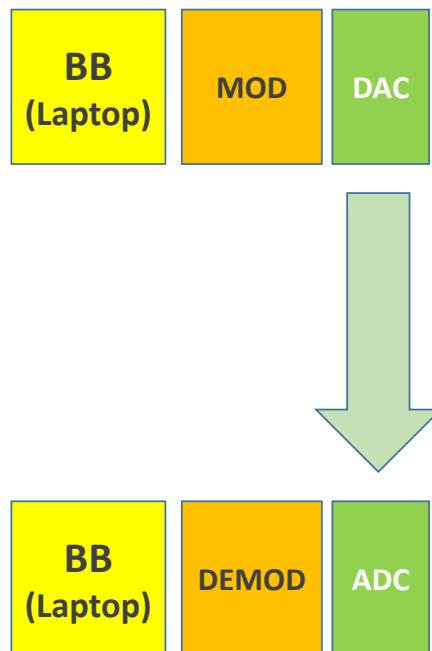


Figure 12. Transmit & Receive modulated data in baseband – simplified test setup

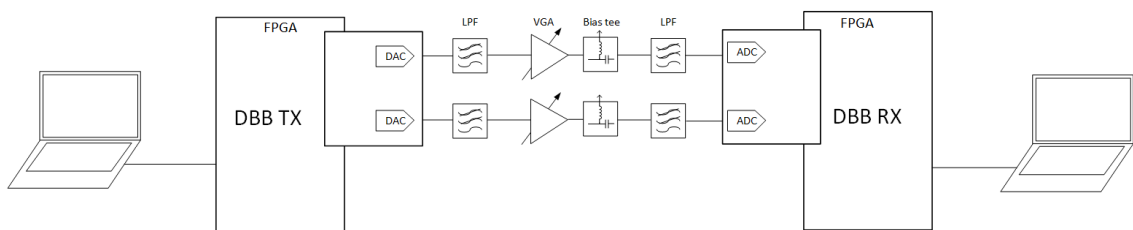


Figure 13. Transmit & Receive modulated data in baseband – detailed test setup

Test procedure:

IDLE and Ethernet frames are generated at 10 Gbps, encoded and modulated in the DBB TX. The signal is captured by the DBB Rx FPGA at the ADC's digital output and offline analyzed to calculate the RX equalizer coefficients. They are then applied to the DBB RX to operate the system online. Error-free decodification is obtained.

Conclusion:

This test has shown the functionality of the DBB TX, DBB RX, ADCs and DACs, as well as their successful integration.

2.4 Transmit & Receive modulated data in E-Band**Introduction:**

Measurements are performed at room temperature and in the best channel (CH1).

Objective:

Verify that it is possible to transmit 10 Gbps 64-QAM modulated signal, using the complete TX (including baseband signal generation) and the receiver front-end.

Test instruments:

- Oscilloscope (Agilent infiniium DSO9404A, 4 GHz, 20 GSa/s)

Test configuration:

A 10 Gbps, 64-QAM, and 2 GHz wide modulated signal is created in the TX modulator and up-converted to E-Band. The RF spectrum at the mmW TX output is down-converted to a suitable 1.25 GHz intermediate frequency by the mmW RX module and the signal is sampled by an oscilloscope as seen in Figure 14. The captured data is then processed off-line using Matlab.

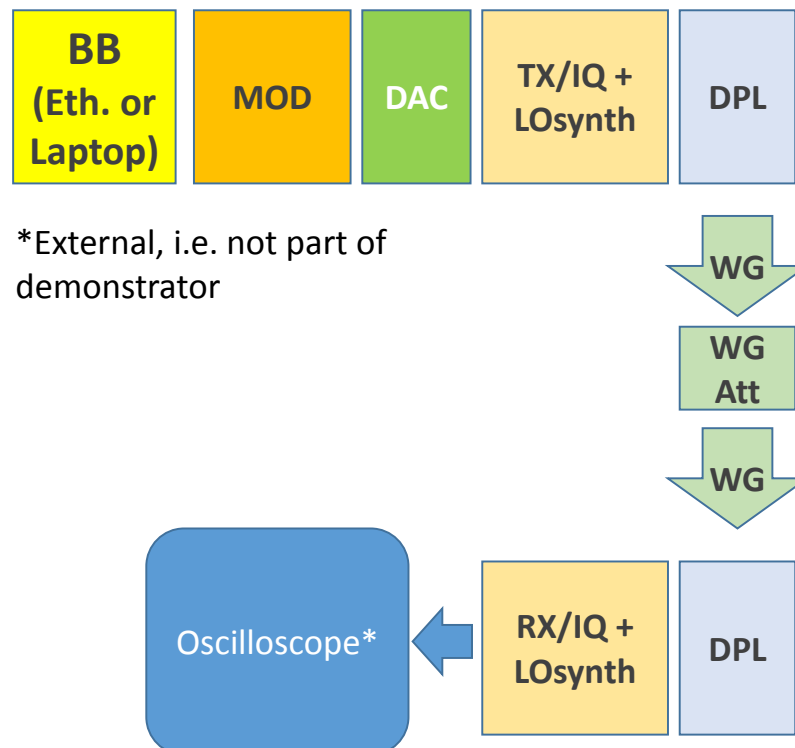


Figure 14. Transmit & Receive modulated data with offline demodulation – test setup

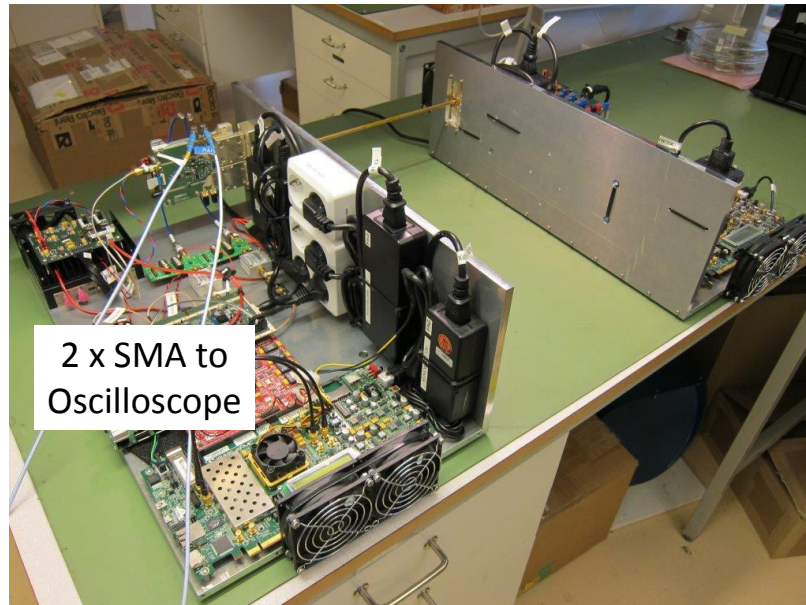


Figure 15. Transmit & Receive modulated data with off-line demodulation – photo of test setup

Test procedure:

The test procedure is very similar to the one described in section 2.2. The received signal is down-converted to an IF frequency of 1.25 GHz and then fed into the oscilloscope. This way, the 2 GHz wide signal covers 0.25 to 2.25 GHz which matches the 4 GHz bandwidth of the oscilloscope. The sampled captured IF signals are then post-processed in a laptop using Matlab. The signal is demodulated and its quality is assessed by means of the I/Q plots and EVM metrics. Figure 16 shows the received constellations of both digital sub-bands. The measured EVM is 3.5 % at each sub-band.

The same procedure is repeated but down-converting the signal to baseband and implementing an algorithm to correct the receiver I/Q imbalance in Matlab. Very similar results to the ones shown are obtained.

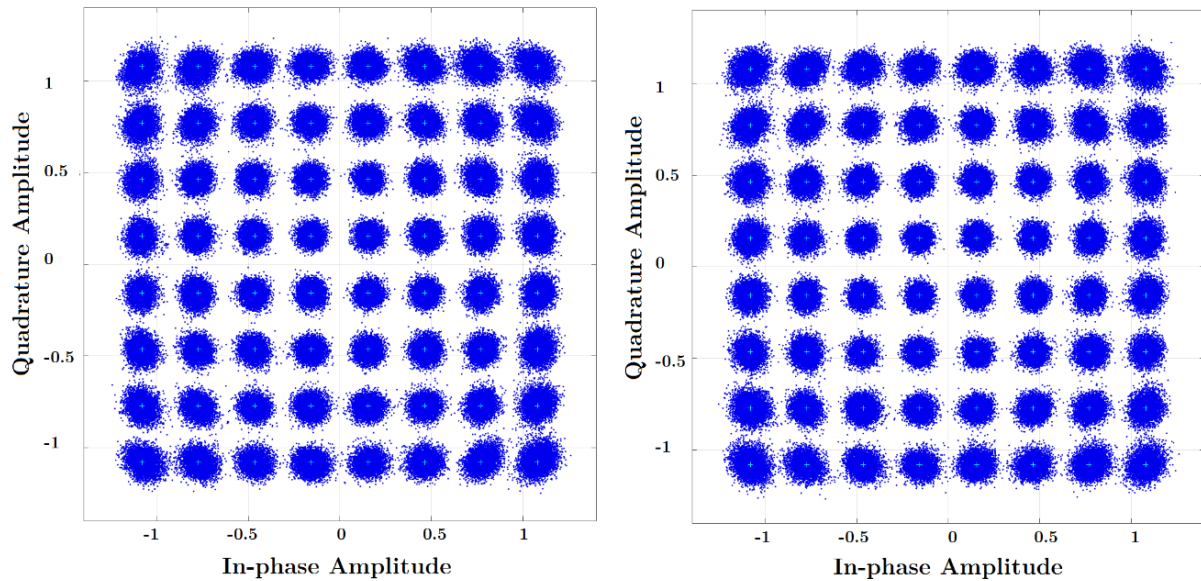


Figure 16. Received 64-QAM constellation when transmitted 10 Gbps.

Left: Lower digital sub-band. Right: Upper digital sub-band.

Conclusion:

Figure 16 demonstrates the feasibility of creating, transmitting, and receiving a 10 Gbps 64-QAM signal including the full demonstrator except for the ADC and the RX BB. During these measurements the set-up was optimized for signal in CH1. The results provide a good confidence that the parts tested can support a transmission of a 10 Gbps 64-QAM signal.

3. COMPARISON WITH PROJECT OBJECTIVES O1-O4

As was mentioned in section 1, project objectives O1-O4 shall also be fulfilled and described in D4.2.

3.1 Project Objective 1

“O1. Modern digital multi-level modulation and demodulation methods and novel digital processing methods will be applied. These modern modulation techniques will increase the spectral efficiency of the E-band link providing an augmented backhaul capacity. The project targets a capacity for the wireless link of at least 10 Gbps.”

Digital multi-level modulation, demodulation and novel digital processing methods have been applied and implemented in the TX and RX baseband circuitry. These methods have also increased the spectral efficiency and are in detail described in D3.4 (“Report on the E-band digital base-band subsystems design”).

10 Gbps transmission capability over the E-Band using the overall transceiver demonstrator has been demonstrated in two steps. Firstly, the DBB TX and DBB RX have been verified together by closing the loop in baseband. Secondly, the functionality of the E-Band loop has been proven with the DBB TX, RF TX and RX front-ends and off-line demodulation.

3.2 Project Objective 2

“O2. The developed transceiver will be able to meet the timing requirements of both IP backhauling and CPRI interconnect. Therefore, the latency of the E3Network transceiver will be well below one millisecond.”

This test has not been specifically performed within WP4, but preliminary results reported in D3.5 suggest that this requirement can be met. This requirement will be tested in WP5.

3.3 Project Objective 3

“O3. New mixed analogue-digital techniques will be devised that will automatically compensate for process, ageing, temperature variations, etc in the RF front-end. These techniques will make it possible the design of a more energy and area efficient, low-power transceiver. The expected reduction in power consumption of the RF / analogue front-end transceiver by applying the proposed techniques will be higher than 25%.”

This objective concerns the mmW sub-blocks, i.e. the BiCMOS transmitter, receiver, and LO synthesizer dies and not the overall transceiver demonstrator. This objective refers therefore to D2.5, “Integrated RF/Analogue front-end transceiver”. As shown in D2.5, a significant improvement in efficiency has been achieved by innovative RF mmW designs and by using the chosen advanced 55 nm BiCMOS technology.

Table 4 shows the measured DC consumption of the developed TX SiGe blocks, while Table 5 summarizes the DC consumption of some representative commercial blocks available in the market. As observed, by using a modern SiGe technology and implementing efficiency-enhancing design techniques, a reduction in the power consumption of the modules of the RF/analogue front-end of more than 50% is obtained when compared to available commercial solutions.

Table 4 DC power consumption of the blocks designed within E3Network

Block	Technology	Power consumption
E3Network IF I/Q up-converter	SiGe	89.5 mW
E3Network mmW transmitter	SiGe	600 mW

Table 5 DC power consumption of different blocks available in the market

Block	Model number	Technology	Power consumption
IF I/Q up-converter	Hittite HMC710LC5	GaAs	1.2 W
BB to E-Band I/Q up-converter, with LO	SIV FC1003E/02	GaAs	5.5 W
BB to E-Band I/Q up-converter, with LO	SIV FC2121E/01	SiGe	3.3 W
IF to E-Band up-converter	Millitech MB1-12	N/A	2.4 W
E-Band PA	Hittite HMC-AUH320	GaAs	520 mW
E-Band PA	SaGe SBP-8138632018-1212-S1	GaAs	5.2W

3.4 Project Objective 4

“O4. A “pencil beam” transmission in the E-Band will be employed. This will result in low EMF radio exposure, as people must be in direct line of sight of the microwave link to be subject to EMF exposure. The E3Network transceiver will be compliant with the relevant European standards such as [10] to ensure reduced EMF radio exposure of European citizens.”

The E3Network transceiver will be in compliance with exposure limits specified in the European directive 2004/40/CE of 29 April 2004 for limiting exposure to electromagnetic fields. This directive is based on ICNIRP reference level. In particular, the E3Network transceiver fulfill the requirements to be considered suitable for an installation/deployment that respects the EMF European rules.

Furthermore, thanks to the decision of using the relatively unexploited E-Band within the project, a better exploitation of the overall frequency spectrum is made possible and consequently, a wider range of different choices in implementing a radio link is feasible. This will in turn make it easier to find an overall PtP backhaul solution that will fulfill the technical requirements and simultaneously lower the overall EMF radio exposure of European citizens.

4. CONCLUSIONS

D4.2 describes the initial testing of the transceiver demonstrator designed and assembled within T4.2 in the project E3Network. T4.2 describes all the tests that have been considered mandatory to pass, in order to demonstrate the demonstrator is working as intended. A more comprehensive testing and comparison with the specification was initially planned to be done in WP5. The goal of the work within T4.2 is that the demonstrator will be proven useful for the work within WP5.

Section 2.1 analyzes the RF output power of the demonstrator. The RF output power of the transmitter is lower than specified in D1.2.3. Impact of this aspect will be evaluated in the next phase of the project. As formal input for WP5, considering the maximum possible tolerance according to the ETSI HS EN 302 217-2-2 (+/- 3 dB), the transceiver demonstrator will be able to be used within WP5 in CH 1, CH 2 and CH 3 with a typical transmitter RF output power at the diplexer antenna port of -7 dBm.

Section 2.2 studies both the mmW Tx and the mmW Rx for spurious and oscillations. It can be said that the system can work properly from the RF emissions and oscillation point of view. No evident limitations or issues are found with regard to its use for WP5.

Section 2.3 checks the performance of the base-band loop (DBB-Tx, DAC, ADC and DBB-Rx). Error free reception of a 2GHz bandwidth signal following the E3Network waveform is achieved. Therefore, the base-band portion of the prototype can be used in WP5.

Section 2.4 demonstrates the feasibility of creating, transmitting, and receiving the E3Network 10 Gbps 64-QAM signal including the demonstrator's full transmitter path and the receiver's RF front-end. A continuous error free operation of the full demonstrator has not been achieved. However, by applying data that have been captured at the output of the receiver's analogue section, the E3Network signal can be successfully processed by means of HW simulation. As the captured data cover only a very short time period, dynamic effects that might affect the E-Band loop cannot be observed. A similar setup to the one described in Section 2.4 can be used in WP5 to validate the performance of the receiver prototype.