PHASTFlex

Photonic Hybrid ASsembly
Through FLEXible waveguides

Newsletter #2 | September 2016

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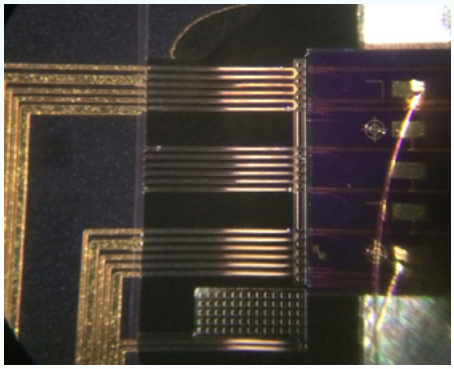
Introduction

Welcome to the second newsletter of the PHASTFlex consortium. In this issue we present recent PHASTFlex achievements in the field of PIC packaging, but first a brief introduction to the PHASTFlex project.



About PHASTFlex

Photonic Integrated Circuits (PICs) are chips which work with light signals instead of electronic signals. They are in increasing demand, for example to help process ever-growing internet traffic flows. In telecoms photonic chips are beginning to penetrate market sectors other than long haul; having application in metro and even fibre to the home. What is less well known is that they also have great potential in many other application areas, in datacomms, in remote sensing, in structural health monitoring and in metrology for example.

► read more...

General facts and figures

PHASTFlex (Photonic Hybrid ASsembly Through Flexible Waveguides) is funded through EU FP7 (Project Number: 619267).
PHASTFlex proposes the development of a fully automated, high precision, cost-effective assembly technology for next generations of hybrid photonic packages.

Project Start Date:
January 1st 2014. The project duration will be of three years, and the cost will be close to 4M€.

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EU funded project

Ref: FP7-ICT 619267
PHASTFlex

The consortium, which is coordinated by TU Eindhoven supported by LioniX bv in the Netherlands and Willow Photonics Ltd in the UK, consists of nine partners in total; seven industrial (LioniX bv, Oclaro Technology Ltd, IMST GmbH, Telnet-Redes Intelligentes SA, Willow Photonics Ltd, Aifotec GmbH and Ficontec Service GmbH) of which two provide applications (Oclaro, Telnet), and two are universities (TU Delft and TU Eindhoven). All are recognized to be leading industrial and research entities in the photonics components and systems industry.

1. About PHASTFlex (continued from page 1)

A long standing problem in the deployment of optical circuits based on Indium Phosphide has been the small size of the optical waveguides compared to the standard transmission medium – glass optical fibre. High-precision, sub-micron alignments are needed, which makes packaging, achieving the coupling of the light from the PIC to the optical fibre and hence the outside world, expensive. The Photonics21 Strategic Research Agenda (http://www.photonics21.org/download/sra_april.pdf) refers to photonics packaging technology as a short term research priority for Europe. The PHASTFLex project focuses specifically on finding a solution to this technical problem.

In PHASTFlex, InP PICs with active functions are combined with passive TriPleX™ PICs on a ceramic carrier as shown in Figure 1. The most demanding assembly task for multi-port PICs is the high-precision (±0.1µm) alignment and fixing of the optical waveguides. The PHASTFlex consortium proposes an innovative concept, in which the waveguides in the passive dielectric TriPleX (http://www.lionixbv.nl/triplex-mpw) PIC are released during fabrication to create an electrically controllable MEMS structure. A two stage assembly process is then envisaged in which a passive flip-chip placement and bonding stage is followed by an active fine alignment stage using the integrated MEMS functions on the TriPleX chip after which the waveguides can be locked in position. MEMS actuators and fixing functions integrated in the same PIC, place and fix the flexible waveguides in the optimal position (peak out-coupled optical power) with the accuracy required.

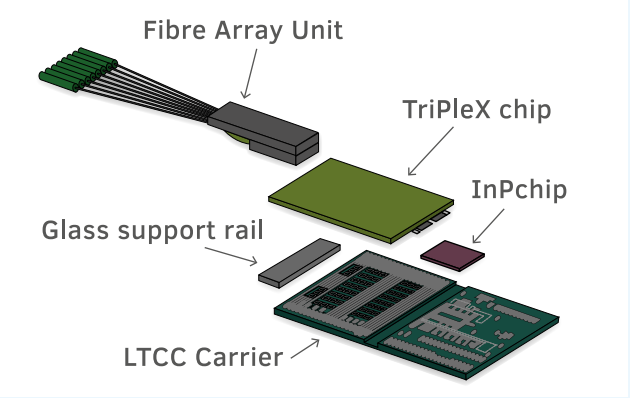
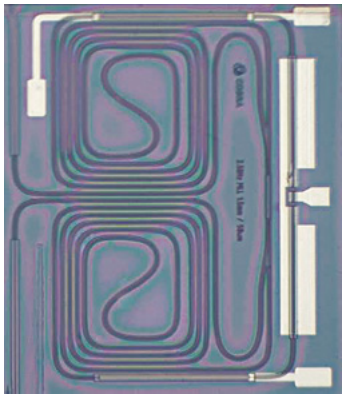


Figure 1 Exploded drawing of the assembly showing the piece parts required (from left to right): Fibre array unit, TriPleX chip with MEMS (back side view), glass rail, InP chip (back side view), LTCC carrier (top view)

PHASTFlex partners Telnet and Oclaro are working on developing leading edge PIC applications which can take advantage of, and test, this new technology. InP PICs are ideally suited for transmitter applications offering high performance integrated laser sources and high speed detectors. TriPleX PICs offer ultra-low loss waveguides and optical multiplexing and de-multiplexing functions.

InP-based photonic integrated circuits



ASPIC: An Application Specific Photonic Integrated Circuit fabricated in InP; the photonic equivalent of micro-electronic ASIC allowing integration of multiple passive and active photonic components within a single chip, enabling the manipulation of light intensity, wavelength, phase and polarisation in photonics integrated circuits.

Applications: telecommunication, datacomm, sensor systems and fibre sensors, microwave systems, medical, bio-imaging and diagnostics, metrology, and many more...

Advantages: compact, highly integrated, multifunctional, high-speed, energy-efficient, lower cost of fabrication and packaging.

2. Flexible Waveguides and Actuators (TU Delft and LioniX)

Since the first project newsletter was published in early 2015 PHASTFlex has made significant progress in the development of the required MEMS functions. Our first chips with actuator functions have been realised based on newly developed fabrication processes. Also, a novel actuator design has been proposed and demonstrated: the short-loop bimorph actuator.

The fine-alignment of the waveguides uses MEMS functionality, which is integrated into the TriPleX chip. For this purpose, the TriPleX chip needs flexible waveguide structures, actuators to bring the waveguide structures in the optimal position, and, finally, locking functions to maintain the optimal position after alignment. Currently we have demonstrated the feasibility of flexible waveguide structures and out-of-plane actuation.
For the out-of-plane actuation, thermal bimorph actuators are used. The TriPleX material is essentially a stack of SiO_2 cladding material with Si_3N_4 waveguide cores. The thickness of this material stack is about 16µm. A typical bimorph actuator beam consists of the SiO_2 (without the nitride cores) with a layer of deposited poly-Si (typically 2-5µm thickness). Upon heating, for which purpose conductors and heaters are added, the beam will have an out-of-plane displacement due to the difference in thermal expansion of the two materials involved.

The real situation in the PHASTFlex hybrid package is slightly more complex. The waveguide layers in the two chips (InP and TriPleX) are defined in different ways, which leads to a height mismatch if the chips are flip-chip bonded to a flat substrate. Hence the challenge is to design a structure which both compensates for the height mismatch and offers sufficient motion range for the fine-alignment.

To achieve this goal a short-loop bimorph actuator is proposed, where the post-fabrication deformation the structures can be exploited. The phrase “short-loop” refers to the fact that only a short section of the SiO_2 beam is covered with poly-Si. This section will have a constant curvature after fabrication. The remaining section of the beam consists of SiO_2 only, and this will have a very small curvature, is almost straight. Hence, by playing with design parameters including the total length of the beam and the length and thickness of the poly-Si section, the out-of-plane position of the wave-

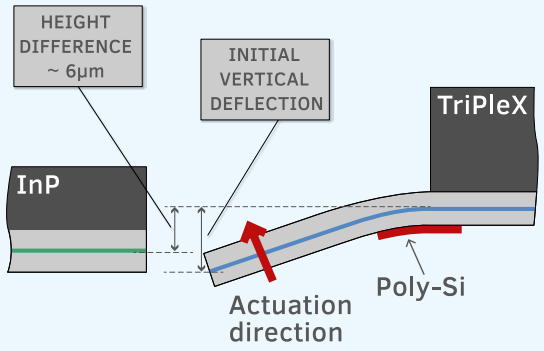


Figure 2 Waveguide alignment in the vertical plane

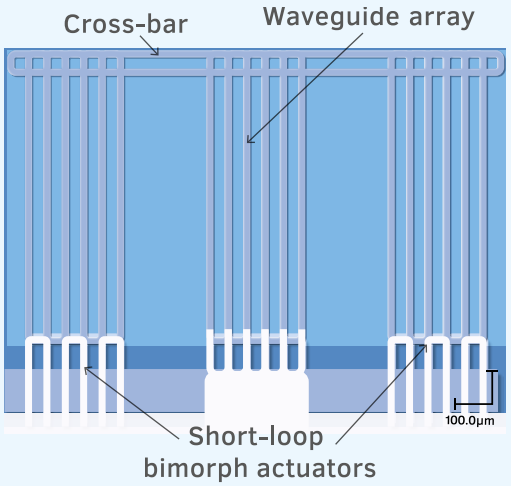


Figure 3 Short, loop actuator based design realised in TriPleX. The actuator groups to left and right are either side of the 6 fold waveguide array, and all are connected by the cross-bar at the top of the picture.

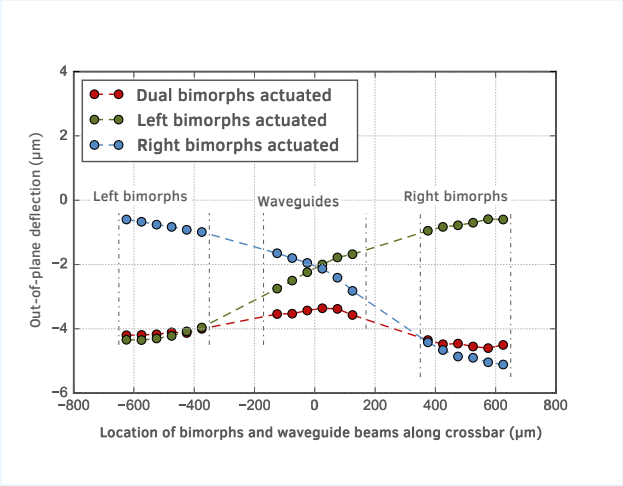


Figure 4 Measurement of the movement range available. The two actuator groups can be independently addressed adjusting the both the height and the angle of the cross-bar.

guide end-facet after fabrication can be tuned by design. Upon operation, the bimorph actuator changes the curvature of the poly-Si section of the actuator beam, and the final waveguide end-position can be fine-tuned electrically.
The movement available from these MEMS structures has been characterised using laser interferometry and an example data set is shown in Figure 4.

These novel short loop actuators have been shown to provide both height compensation, and actuation range, and are clearly compatible with the overall package design. Many of the basic principles of the PHASTFlex assembly concept have been established and the consortium is currently working hard to integrate the remaining MEMS functions which will achieve the lateral movement of the cross-bar and locking after alignment.

3. Automated assembly machine (Ficontec and Aifotec)

An industrial prototype of an assembly machine has been built by partner Ficontec in the first half of the project, and is now installed at Aifotec. The main motion system of the machine which is shown in Figure 5 consists of a 4-axis manipulator, with nozzles for chip handling and sensor systems for process control. A separate high accuracy vision system allows an in-situ monitoring of the chip placement and is used to support the alignment. For performing a vision analysis, which can be done independently of the chip placement, the vision system is mounted on a separate 3-axis motion system. The machine is built to allow oven bonding of the InP and the TriPleX chips to the LTCC carrier, as well as to allow active alignment of the MEMS structures of the TriPleX chip through probe cards and contact pads designed into the LTCC. Targeting passive alignments of better than ±0.5µm requires this machine to better the current state-of-the-art.

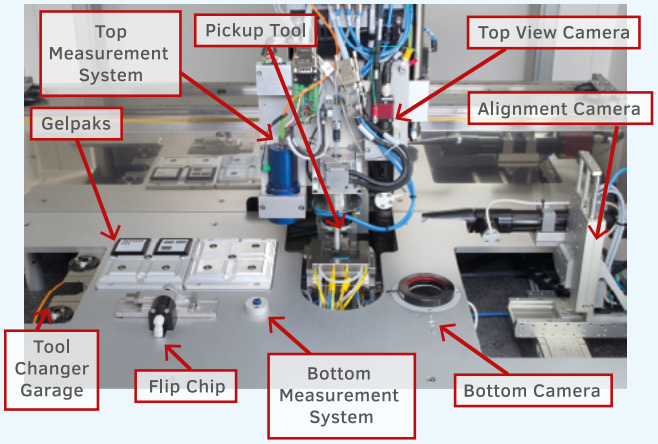


Figure 5 PHASTFlex assembly machine, detail of interior structure

Alignment principles utilizing a novel top-bottom viewing system have been chosen to enable the placement of the second chip with respect to the first-bonded chip, targeting a 1.5 ± 0.5µm gap between the optical interfaces. The typical lateral placement accuracy requirement for the chips is in the range of 2-5µm. The assembly process, based on eutectic AuSn bonding, is carried out in an integrated bonding oven on the machine, with the chips held in position and under pressure during the soldering cycle.

Examples of InP and TriPleX chips bonded to the carrier are shown in Figure 6.

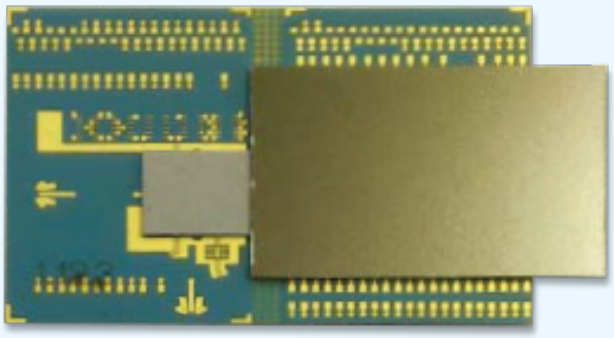


Figure 6 First assembly of InP (to left) and TriPleX (to the right) chips on an LTCC carrier. In this photograph the assembly is without the MEMS alignment structures.

4. LTCC carriers and RF performance (IMST)

Potential for high speed operation up to 40Gb is an important aspect of the overall design of the subassembly. RF striplines included in the LTCC (low temperature co-fired ceramic) carrier give the subassembly a capability for high speed operation, with RF access using the multi-layer LTCC for tracking. Assemblies have been independently tested and Figure 7 shows the measurement set-up using two, 200µm, pitch ground-signal-ground (GSG) probes.
S-parameters up to 30GHz have been measured. With both lines present a return loss (S_{11}) lower than -10dB over the complete frequency bandwidth has been measured. As expected, transmission losses increase with frequency and with line length, but they remain lower than -2dB across the bandwidth. Initial assemblies of the active InP chip on the LTCC carrier (Figure 8) have allowed the project to extend the RF characterisation to include the coplanar waveguides included on the chip.

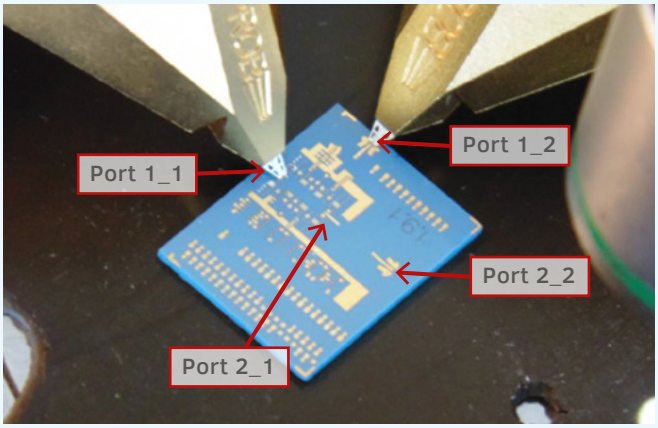


Figure 7 LTCC stripline measurement set-up

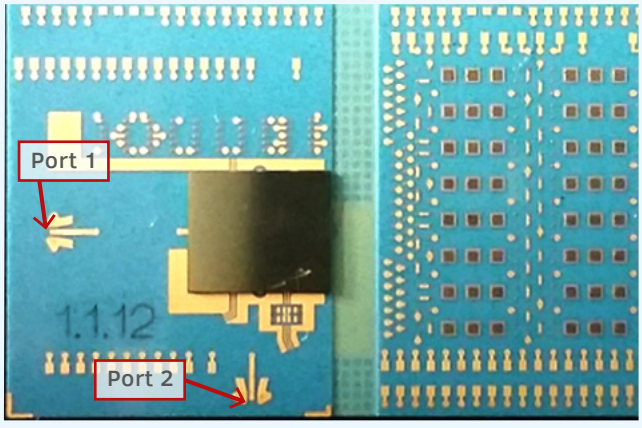


Figure 8 InP chip assembled on LTCC carrier

Figure 9 shows S-parameters for the combined carrier and InP chip measured at the LTCC GSG pads. These measurements include the two LTCC striplines together with the coplanar waveguide (CPW) on InP. It can be seen that the assembled chip presents a return loss lower than -6dB up to 8GHz and the transmission losses are high all along the frequency bandwidth. These measurements agree with simulations carried out using the EMPIRE[1] software, and also with the standalone InP chip measurements (not shown here).

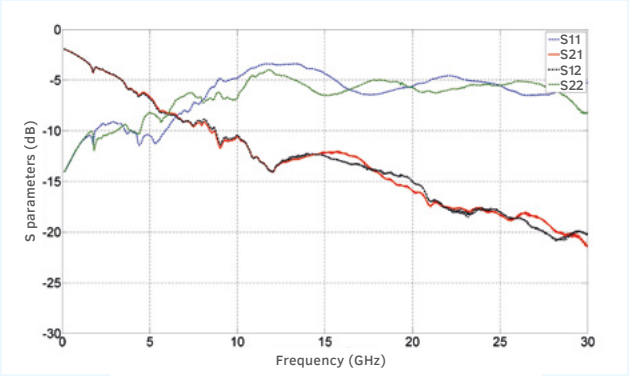


Figure 9 S-parameters of the CPW on InP chip bonded to the LTCC striplines

1 EMPIRE software suite http://www.empire.de/

JePPIX

Joint European Platform for Photonic Integration of InP-based Components and Circuits

JePPIX is a brokering organisation for InP-based Photonic Integrated Circuits (PICs), and is based at TU Eindhoven.

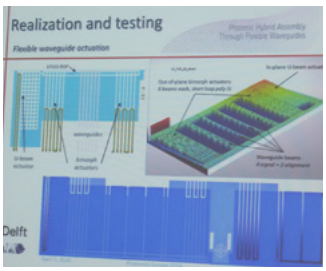
JePPIX (www.jeppix.eu) helps organizations around the world gain access to advanced fabrication facilities for Photonic Integrated Circuits. It aims for low-cost development of application specific InP and TriPleX PICs using the generic foundry model, and organises rapid prototyping via Multi-Project Wafer runs.

JePPIX collaborates closely with Europe's key players in the field of photonic integration and acts as a focal point for the whole eco system, including manufacturing and packaging partners, photonic CAD software partners, R&D labs and photonic IC design houses.

The JePPIX Roadmap, last published in 2015, can be downloaded from: www.jeppix.eu

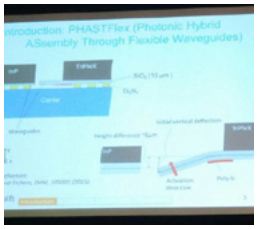
A video describing JePPIX can be found at www.jeppix.eu/video

Dissemination



PHASTFlex has sought to publicise is work through a variety of workshops, symposia and meetings, in Europe and in the US. PHASTFlex work was presented at the SPIE Photonics Europe meeting in the spring of 2016.

Published in: *Photonic hybrid assembly through flexible waveguides*, Wörhoff K. et. al. in the SPIE Digital Library as part of the proceedings of the Silicon Photonics and Photonic Integrated Circuits V conference. The DOI for the paper is: http://dx.doi.org/10.1117/12.2227814



More details can be found in SPIE Photonics West *Bimorph actuators in thick SiO_2 for photonic alignment*, Kai Wu et al. The DOI for the paper is: http://dx.doi.org/10.1117/12.2209499

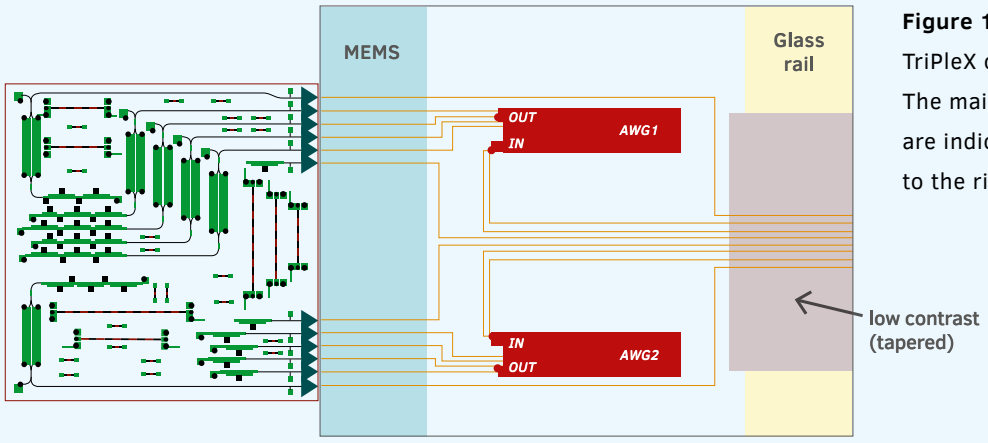


Figure 10 Layout schematic for the InP – TriPleX chip combination on LTCC.
The main functional areas of the assembly are indicated, including the fibre array attach to the right hand side.

5. Where next? Applications (Telnet, Oclaro)

PHASTFlex still has much to do. Our focus for the remainder of the project is the realization of an applications-orientated chip set and co-designed LTCC carrier which can exercise all of the main aspects of the assembly concept. Preparations are already well advanced.

The chosen application is for next generation passive optical network (PON). PON technology is currently migrating to support 10Gbps per user traffic. The massive implied aggregation of high bit rate modules and related discrete components over the Optical Line Termination (OLT) chassis and rack equipment has to respond to important cost and energy constraints, as well as simply to the large-size of the network equipment. PIC technology is well placed to make a significant impact here.

PHASTFlex is working on a multi-channel WDM-PON transceiver chip for next-generation access systems as an exemplar for its assembly technology.
To achieve bidirectional transmission on a single fibre, a WDM filter combines/separates the upstream and downstream wavelengths, and can also be implemented in TriPleX.
Figure 10 shows the proposed layout of a 4-channel OLT transceiver module. For the transmitter, there are four Distributed Bragg Reflector (DBR) lasers with a tuning range of ~5nm, each modulated by a 10Gbs data stream, channel separation is 50GHz, and the signal is amplified using a Semiconductor Optical Amplifier (SOA), all implemented in the InP PIC. The outputs of the single-channel transmitters at different wavelengths are then multiplexed by a 50GHz AWG implemented in the low loss TriPleX PIC. On the receive side, optical signals from the optical network units (ONUs) using four different wavelength channels are separated by a demux, a 50GHz AWG also implemented in the TriPleX, before being detected by photo-detectors on the InP PIC. To achieve bidirectional transmission on a single fibre, a WDM filter combines/separates the upstream.

Both chips and carriers are currently being fabricated, and will be available for assembly trials in the last quarter of 2016.

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